2SK2373

Silicon N Channel MOS FET

REJ03G1009-0300
Rev.3.00
Dec 27, 2006

Application

High speed power switching

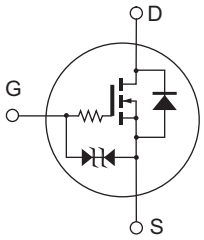
Features

- Low on-resistance
- Small package
- Low drive current
- 4 V gate drive device can be driven from 5 V source.
- Suitable for low signal load switch

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)





1. Source
2. Gate
3. Drain

Note: Marking is “ZE–”.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}$*[1]	0.4	A
Body to drain diode reverse drain current	I_{DR}	0.2	A
Channel dissipation	Pch*[2]	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤100 µs, duty cycle ≤ 10 %

Electrical Characteristics

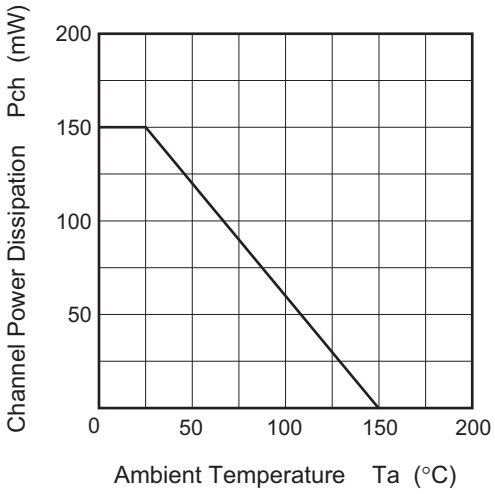
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±2	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 10 µA, V_{DS} = 5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.4	7.5	Ω	I_D = 20 mA, V_{GS} = 4 V*[2]
		—	1.0	7.0	Ω	I_D = 10 mA, V_{GS} = 10 V*[2]
Input capacitance	Ciss	—	17.8	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	25.4	—	pF	
Reverse transfer capacitance	Crss	—	3.7	—	pF	
Turn-on delay time	$t_{d(on)}$	—	50	—	ns	I_D = 0.1 A, V_{GS} = 10 V, R_L = 100 Ω, PW = 2 µs
Rise time	t_r	—	125	—	ns	
Turn-off delay time	$t_{d(off)}$	—	660	—	ns	
Fall time	t_f	—	400	—	ns	

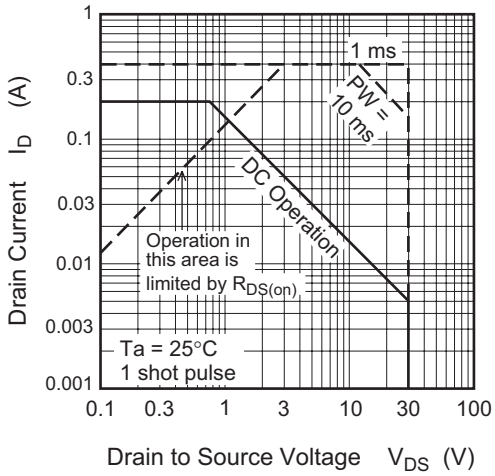
Note: 2. Pulse Test

Main Characteristics

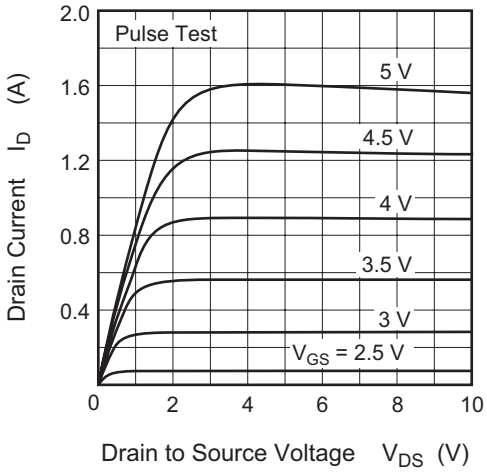
Maximum Channel Dissipation Curve



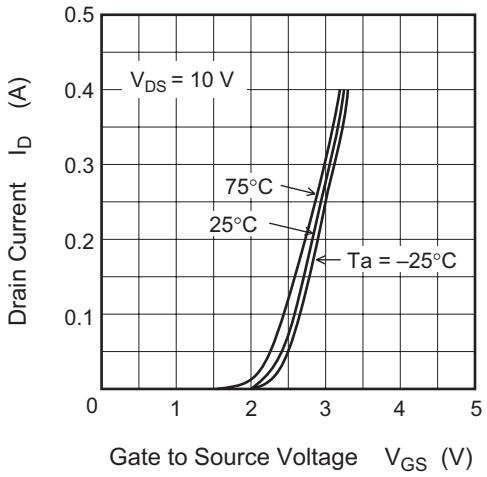
Maximum Safe Operation Area



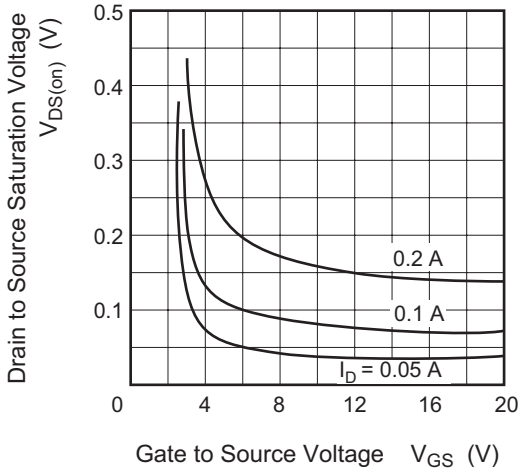
Typical Output Characteristics



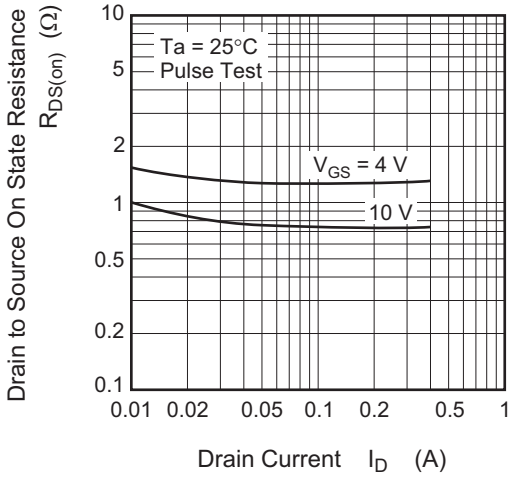
Typical Transfer Characteristics



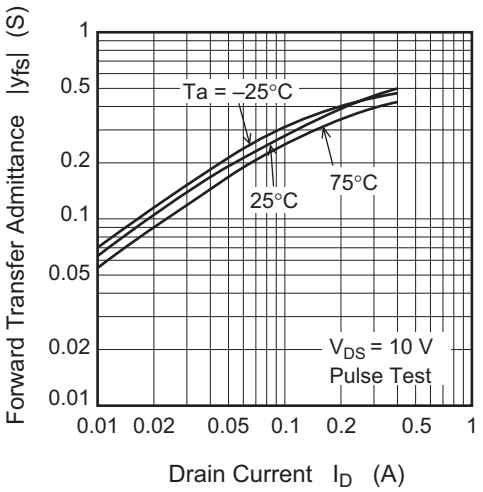
Drain to Source Saturation Voltage vs. Gate to Source Voltage



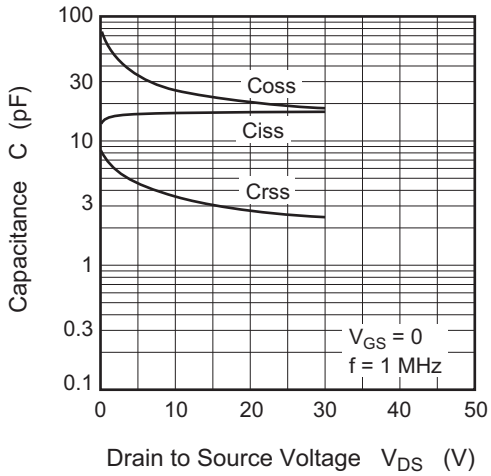
Static Drain to Source on State Resistance vs. Drain Current



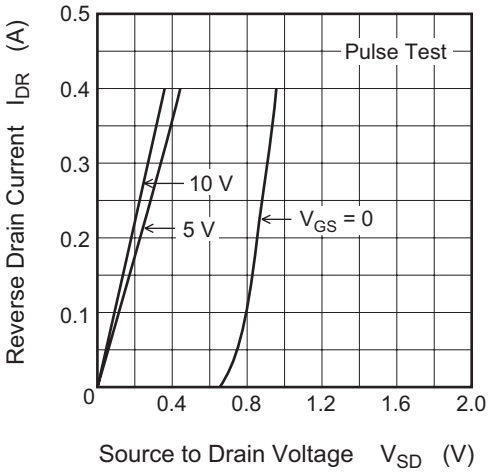
Forward Transfer Admittance vs. Drain Current



Typical Capacitance vs. Drain to Source Voltage

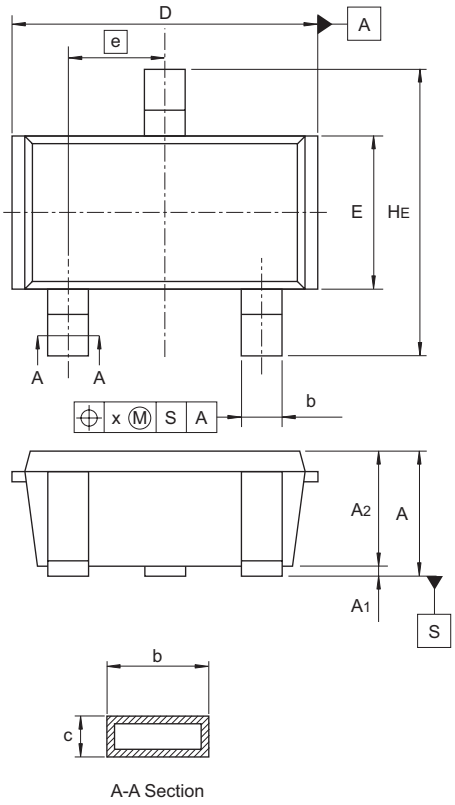


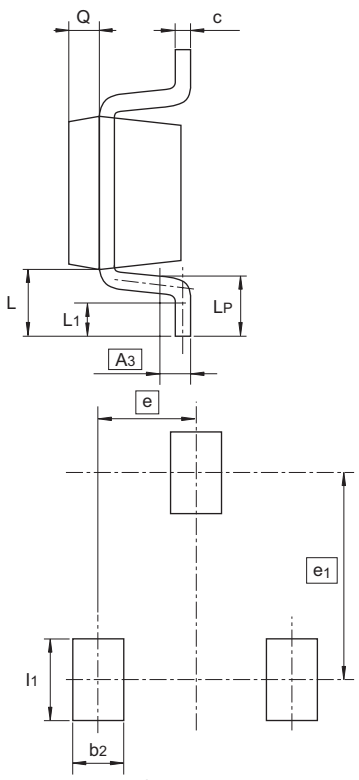
Reverse Drain Current vs. Source to Drain Voltage



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MPAK	SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.0	–	1.3
A_1	0	–	0.1
A_2	1.0	1.1	1.2
A_3	–	0.25	–
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	–	3.1
E	1.35	1.5	1.65
e	–	0.95	–
H_E	2.2	2.8	3.0
L	0.35	–	0.75
L_1	0.15	–	0.55
L_P	0.25	–	0.65
x	–	–	0.05
b_2	–	–	0.55
e_1	–	1.95	–
l_1	–	–	1.05
Q	–	0.3	–

Ordering Information

Part Name	Quantity	Shipping Container
2SK2373ZE-TL-E	3000 pcs	Taping
2SK2373ZE-TR-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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