

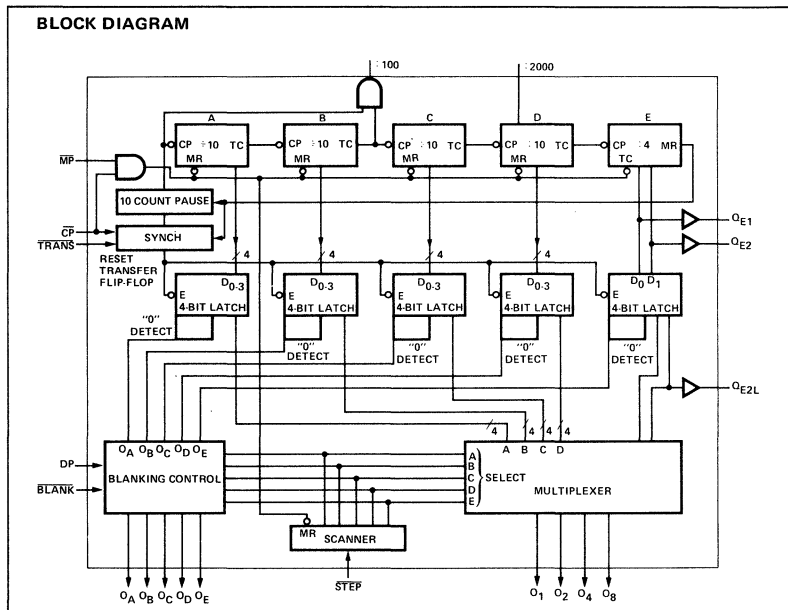
3814

DIGITAL VOLTMETER LOGIC ARRAY

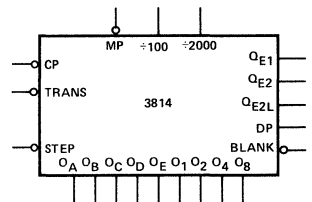
GENERAL DESCRIPTION — The 3814 provides the logic required to implement a four and one-half decade Digital Voltmeter. In addition to four full decade counters and two overflow latches, the device provides a Binary Coded Decimal output (to drive a BCD converter) and five decoded outputs to strobe a multiplexed display.

Automatic leading-zero blanking is simply accomplished, and a separate input is provided to blank the entire display. Other outputs provide counter overflow information and auto-ranging control signals. The 3814 is manufactured using silicon gate p-channel enhancement mode technology.

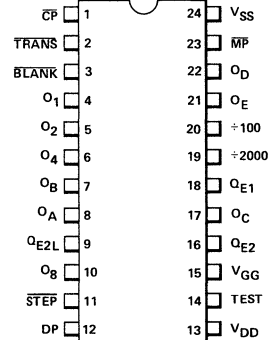
- DIRECT TTL/DTL COMPATIBILITY — NO EXTERNAL COMPONENTS
- DC TO 600 kHz OPERATION
- BCD OUTPUT — COMPATIBLE WITH DISPLAY DECODERS
- EXTERNAL CONTROL MULTIPLEX FREQUENCY — ACCOMMODATES LED DISPLAYS
- UNDERRANGE AND OVERRANGE OUTPUTS
- 10-COUNT DELAY TO MASK ANALOG SWITCHING NOISE



LOGIC SYMBOL



CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

CP	Clock Pulse Input
MP	Master Preset
TRANS	Transfer Count Control
BLANK	Display Blank Control
O ₁ , O ₂ , O ₄ , O ₈	Display Count Outputs
O _A , O _B , O _C , O _D , O _E	Selected Digit Outputs
DP	Decimal Point Control Input
STEP	Digit Scanner Step Control
O _{E2L}	Overrange Output
O _{E2N}	Count Control Outputs
+100	Count-divided-by-100 Output
+2000	Underrange Output
TEST	Test Input (Tie to V _{SS})

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to 70°C
V _{GG}	+0.3 to -24 V
All Other Inputs	+0.3 to -16 V
Outputs	+0.3 to -8 V ($I_L < 10$ mA)

FUNCTIONAL DESCRIPTION — The 3814 is intended for use as the digital logic portion of digital voltmeter systems. An input clock ($\overline{CP}$) drives 4-1/2 decades of BCD counters, with the counters changing state on the LOW to HIGH clock transition. The output of the second decade is gated with the input clock ($\overline{CP}$) and brought off chip ($\div 100$) for use as an additional clock. This clock may be used to drive the multiplexer input (Step).

A clock input synchronized with a LOW state on Master Preset ($\overline{MP}$) will set the counters to 30,000. The 3814 will then count the next 10,000 clock pulses, and be in the 00,000 state. At this count the device will ignore the next 10 clock inputs. This feature is useful when the device is used in systems where the current switching associated with analog to digital conversion generates transients which might cause false triggering. This 10 count correction requires a small current (equal to the integral of 10 counts of the standard current) be added to the unknown current. Thus, even if the current to be measured is zero, the integrator output voltage is moved off zero, eliminating comparator transient triggering. Following this 10 count pause, the 3814 continues to count; in normal operation the A/D circuitry will provide a transfer input, causing the count to be loaded into the latches. The count stored (and present at the output multiplexer) will be proportional to the ratio of the unknown current to the standard current. The counter will continue to accept clock pulses, and at 20,000 the QE_1 output will go LOW and the QE_2 output will go HIGH. This state may be decoded and used to reset the analog circuitry. Since current switching associated with this reset may again cause false triggering, only one transfer command is accepted during the interval from 00,000 to 39,000.

In typical operation, the states of the two overflow flip-flops (QE_1 and QE_2) may be used to control system operation.

Table 1.

COUNT	QE_1	QE_2
30,000 to 00,000	1	1
00,000 to 10,000	0	0
10,000 to 20,000	1	0
20,000 to 30,000	0	1

Table 2.

DIGIT FED BACK TO DP	EXAMPLE COUNT	DISPLAY*
A, or DP = V_{SS}	00000	0
A, or DP = V_{SS}	00120	120
B	00120	12.0
C	00120	1.20
D	00120	0.120
E, or DP = V_{DD}	00120	0.0120
		E DCBA

*The decimal point itself in the display is not controlled by the 3814.

COUNT CONTROL OUTPUTS

In addition, the QE_2 output is latched and brought out as QE_{2L} . If a system utilizing a full scale count of 19,999 is implemented with the 3814, the HIGH state of QE_{2L} will indicate an overrange condition. The divide by 2,000 output ($\div 2,000$) is intended for use as an underrange indicator. If this output has not gone HIGH when a transfer command is received, the total count is less than 10% of full scale.

A power-on reset should be provided externally to insure proper counter initialization.

DATA OUTPUTS — The state of one of the 4-1/2 decade counters is presented as a BCD multiplexed output (O_1, O_2, O_4, O_8). One of the five decoded outputs (O_A, O_B, O_C, O_D, O_E) will be HIGH, indicating which decade's count is present at the BCD outputs. The multiplexer is clocked by a separate input ($\overline{Step}$) which may be driven at 1/100 of the clock frequency by directly connecting the $\div 100$ output to the Step input.

BLANKING — Automatic leading zero blanking is simply accomplished by directly wiring two pins of the 3814. One of the decade outputs (O_A through O_E) when wired to the decimal point (DP) input will cause all leading zeros to the left of the feedback decade to be automatically blanked. For example if the count is 00120 and decade "A" (O_A) is connected to DP, the display will be "120". With the same count, and decade "D" (O_D) connected to DP, the display will be 0120. When the Blank input is LOW all outputs (O_A thru O_E) go LOW (see Table 2).

TEST INPUT — This pin is used during the testing of the 3814 and must be wired to V_{SS} for operation.

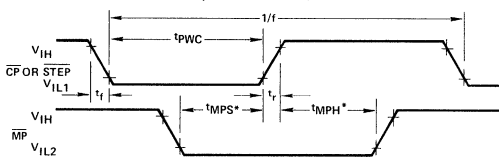
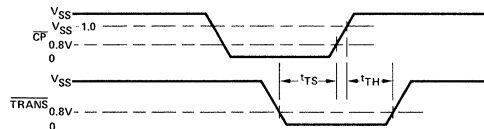
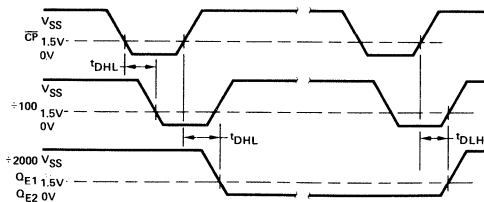
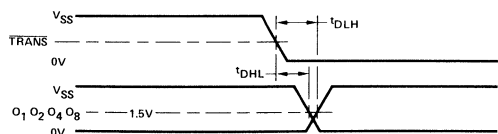
LEADING-ZERO BLANKING

DC CHARACTERISTICS: $V_{SS} = +5.0 \text{ V} \pm 5\%$, $V_{DD} = 0 \text{ V}$, $V_{GG} = -12 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	$V_{SS}-1.0$		$V_{SS}+0.3$	V	All Inputs Including $\overline{CP}$
V_{IL1}	Input LOW Voltage	-2		0.5	V	$\overline{CP}$ and $\overline{STEP}$
V_{IL2}	Input LOW Voltage	-2		+0.8	V	All Inputs Except $\overline{CP}$ and $\overline{STEP}$ a) Sourcing 200 μA for Outputs; Q_{E1} , Q_{E2} , Q_{E2L} , $\div 2000$, $C_L < 20 \text{ pF}$.
V_{OH1}	Output HIGH Voltage	2.4		V_{SS}	V	b) Sourcing 400 μA for Outputs; O_1 , O_2 , O_4 , O_8 ; $C_L < 30 \text{ pF}$.
V_{OH2}	Output HIGH Voltage	$V_{SS}-1.0$		V_{SS}	V	Sourcing 200 μA for Outputs O_A , O_B , O_C , O_D , O_E , $\div 100$; $C_L < 20 \text{ pF}$ a) Sink 1.6 mA on Outputs Q_{E1} , Q_{E2} , Q_{E2L} , O_A , O_B , O_C , O_D , O_E , $\div 100$, $\div 2000$; $C_L < 20 \text{ pF}$.
V_{OL}	Output LOW Voltage			0.4	V	b) Sink 2.0 mA on Outputs O_1 , O_2 , O_4 , O_8 , $C_L < 30 \text{ pF}$.
R_{IN1}	Input Resistor Returned to V_{SS}	1	2.5	5	k Ω	Inputs: $\overline{CP}$, Blank, MP, Trans.
R_{IN2}	Input Resistor Returned to V_{SS}	10	25	50	k Ω	Inputs: $\overline{STEP}$, DP
I_{GG}	V_{GG} Supply Current	3	5	15	mA	
I_{SS}	V_{SS} Supply Current	20	30	50	mA	

AC CHARACTERISTICS: $V_{SS} = +5.0 \text{ V} \pm 5\%$, $V_{DD} = 0 \text{ V}$, $V_{GG} = -12 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
f	Operating Frequency	DC		600	kHz	Fig. 1
t_{PWC}	Clock Pulse Width	300	220		ns	Fig. 1
t_{TS}	$\overline{TRANS}$ Set Up Time	250			ns	Fig. 2
t_{TH}	$\overline{TRANS}$ Hold Time	50			ns	Fig. 2
t_{DHL}	HIGH to LOW Transition for Outputs $\div 100$		320	1000	ns	Fig. 3
	$\div 2000$		375	1000	ns	Fig. 3
	Q_{E1} , Q_{E2}		400	800	ns	Fig. 3
	O_1 , O_2 , O_4 , O_8		450	1000	ns	Fig. 4
t_{DLH}	LOW to HIGH Transition for Outputs $\div 100$		350	1000	ns	Fig. 3
	$\div 2000$		450	1000	ns	Fig. 3
	Q_{E1} , Q_{E2}		425	800	ns	Fig. 3
	O_1 , O_2 , O_4 , O_8		550	1000	ns	Fig. 4
t_r , t_f	Clock Rise and Fall Times			200	ns	Fig. 1
t_{MPS}	Master Preset Set-up Time	300			ns	Fig. 1
t_{MPH}	Master Preset Hold Time	200			ns	Fig. 1

INPUT CLOCK ($\overline{STEP}$ OR $\overline{CP}$) WAVEFORM**Fig. 1.** *APPLIES ONLY TO $\overline{CP}$ INPUT**TIMING DIAGRAMS****TRANSFER SETUP AND HOLD TIMES****Fig. 2.****PROPAGATION DELAY-OUTPUTS****Fig. 3.****PROPAGATION DELAY - BCD OUTPUTS****Fig. 4.**

Ideally, SW₁ and SW₂ have zero resistance when on, infinite resistance when off and no offset voltage. For an accurate system then, bipolar transistors cannot be used because of offset. P-Channel or N-Channel FETs ably satisfy all three of the switch criteria. To avoid gate-to-source debiasing, P-Channel devices should be used for negative input voltages and N-Channel devices for positive inputs. The versatile μ A776 is used again as the integrator amplifier; the μ A734 comparator receives the integrator signal and upon a null crossing, generates the transfer command to the 3814. All gating for mode control to SW₁, SW₂ and SW₃ is obtained from the QE₁ and QE₂ output. The FND21 LED Display Module and the associated decoder and drivers are also shown. For flexibility of decimal point location and zero suppression, a five position SPST switch has been added to appropriately gate the DIGIT SELECT outputs to the DP inputs.

This DVM (exclusive of display circuitry) can be built with a total of *only six integrated circuits* — *seven* if input buffering is required.

