FAIRCHILD SEMICONDUCTOR®

January 2008

74AC541, 74ACT541
Octal Buffer/Line Driver with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- 3-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24mA
- 74AC541 is a non-inverting option of the 74AC540
- 74ACT541 has TTL-compatible inputs

General Description

The 74AC541 and 74ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 74AC244 and 74ACTC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

Ordering Information

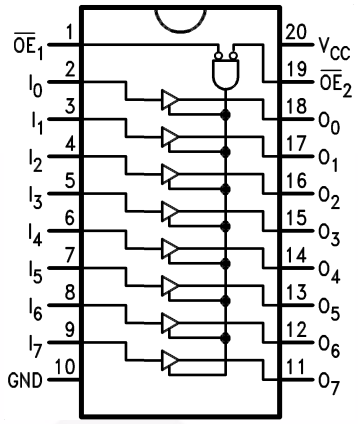
Order Number	Package Number	Package Description
74AC541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC541PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

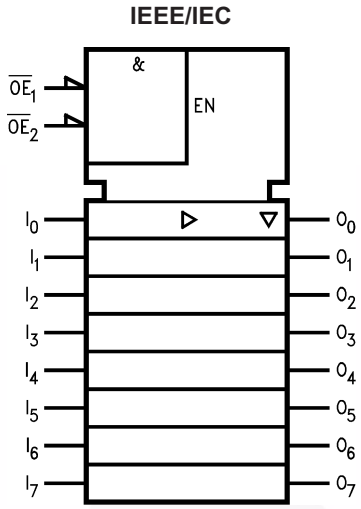
All packages are lead free per JEDEC: J-STD-020B standard.

©1988 Fairchild Semiconductor Corporation

Connection Diagram



Logic Symbol



Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

Z = High Impedance

©1988 Fairchild Semiconductor Corporation

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 0.5$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns
	V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

©1988 Fairchild Semiconductor Corporation

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = –50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –12mA		2.56	2.46	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –24mA		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –24mA(1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 12mA		0.36	0.44	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 24mA		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 24mA(1)		0.36	0.44	
I_{IN}(2)	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Leakage Current	5.5	V_I (OE) = V_{IL}, V_{IH}; $V_I = V_{CC}$, GND; $V_O = V_{CC}$, GND		±0.25	±2.5	µA
I_{OLD}	Minimum Dynamic Output Current(3)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}(2)	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
3. Maximum test duration 2.0ms, one output loaded at a time.

©1988 Fairchild Semiconductor Corporation

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = –50µA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –24mA		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –24mA(4)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 24mA		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 24mA(4)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Leakage Current	5.5	$V_I = V_{IL}$, V_{IH}; $V_O = V_{CC}$, GND		±0.25	±2.5	µA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC}$ – 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current(5)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

©1988 Fairchild Semiconductor Corporation

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	$T_A = +25°C$, $C_L = 50pF$			$T_A = -40°C$ to $+85°C$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Output	3.3	2.0	5.5	8.0	1.5	9.0	ns
		5.0	1.5	4.0	6.0	1.0	6.5	
t_{PHL}	Propagation Delay, Data to Output	3.3	2.0	5.5	8.0	1.5	8.5	ns
		5.0	1.5	4.0	6.0	1.0	6.5	
t_{PZH}	Output Enable Time	3.3	3.0	8.0	11.5	3.0	12.5	ns
		5.0	2.0	6.0	8.5	1.5	9.5	
t_{PZL}	Output Enable Time	3.3	2.5	7.0	10.0	2.5	11.5	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t_{PHZ}	Output Disable Time	3.3	3.5	9.0	12.5	2.5	14.0	ns
		5.0	2.0	7.0	9.5	1.0	10.5	
t_{PLZ}	Output Disable Time	3.3	2.5	6.5	9.5	2.0	10.5	ns
		5.0	2.0	5.5	7.5	1.0	8.5	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[7]	$T_A = +25°C$, $C_L = 50pF$			$T_A = -40°C$ to $+85°C$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min	Max	
t_{PLH}	Propagation Delay, Data to Output	5.0	2.0	4.5	7.0	2.0	7.5	ns
t_{PHL}			2.0	5.5	7.0	2.0	7.5	
t_{PZH}	Output Enable Time	5.0	2.0	5.0	9.0	2.0	9.5	ns
t_{PZL}			2.0	6.5	9.0	2.0	9.5	
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	7.5	1.5	8.0	ns
t_{PLZ}			1.5	5.5	7.5	1.5	8.0	

Note:

7. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance for AC	V_{CC} = 5.0V	30.0	pF
	Power Dissipation Capacitance for ACT		70.0	

©1988 Fairchild Semiconductor Corporation

Physical Dimensions

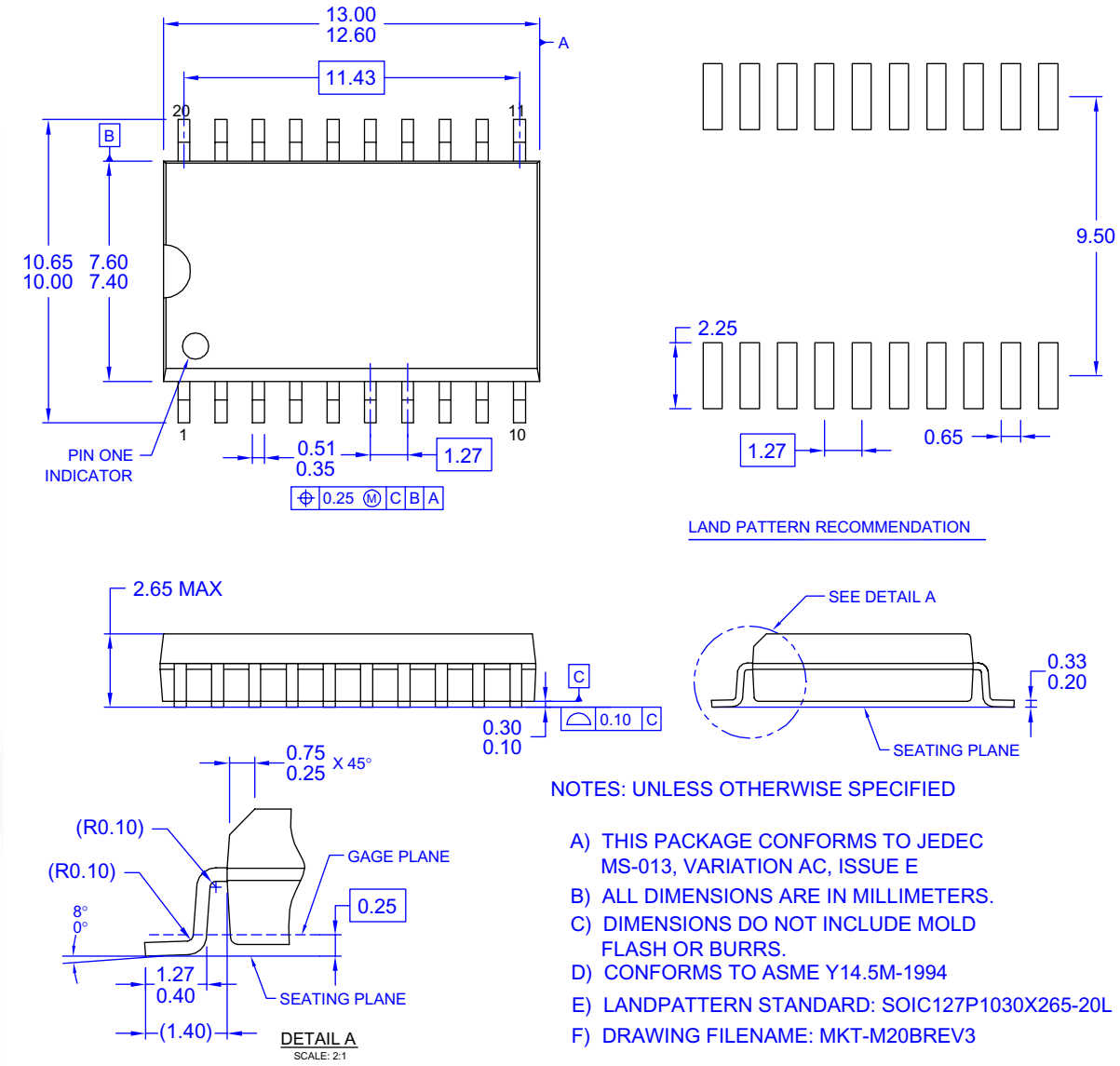


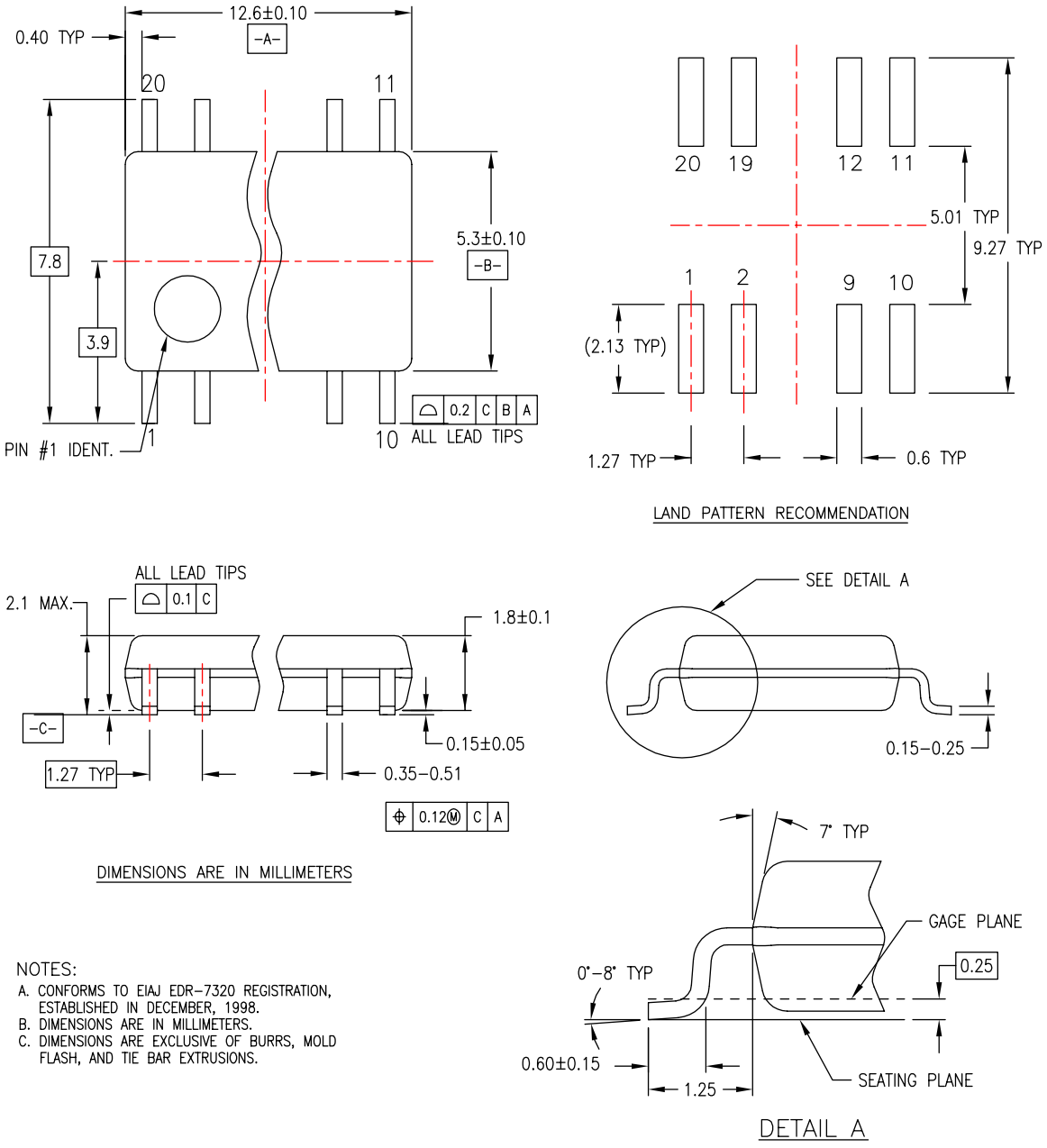
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

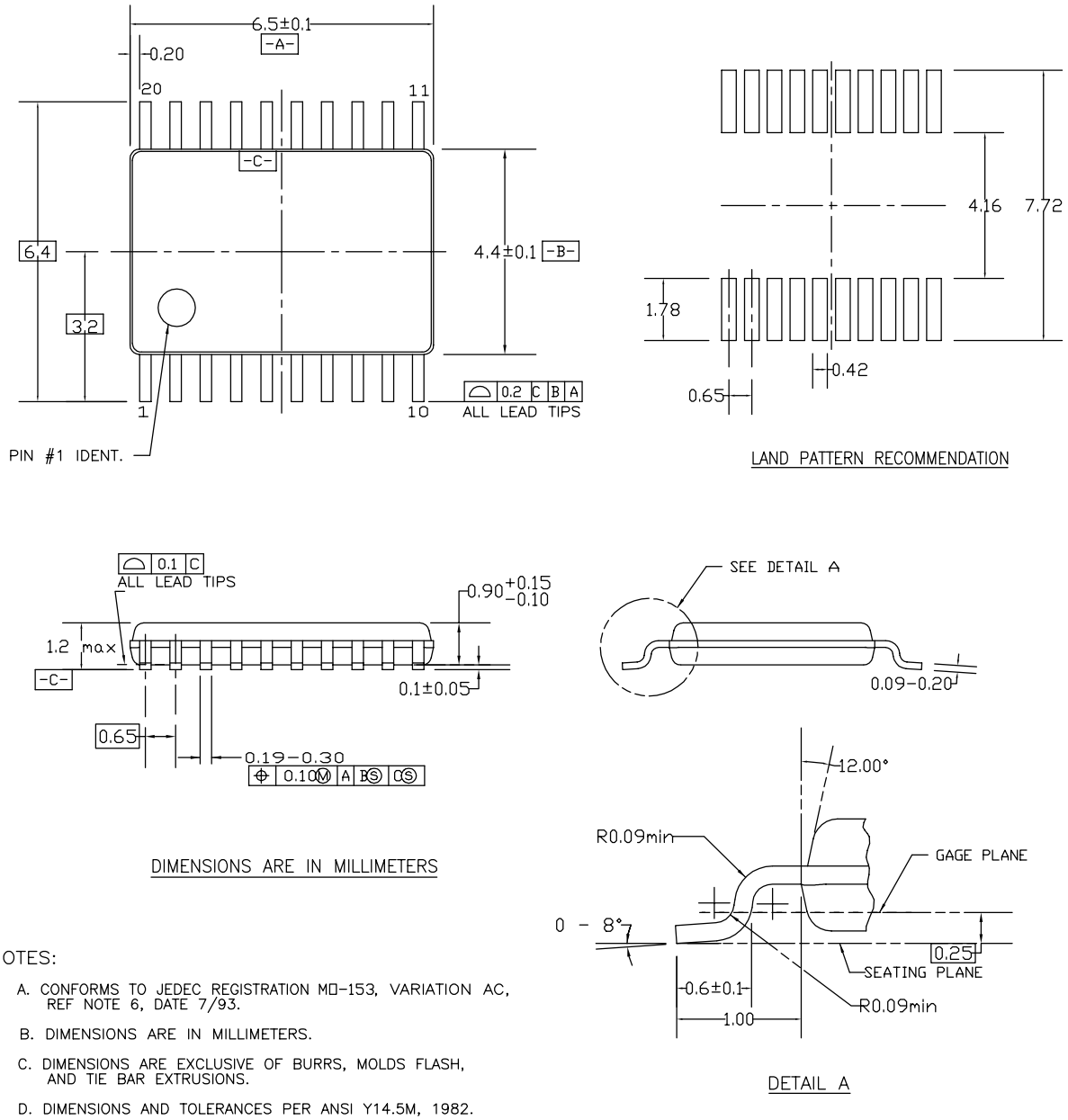
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

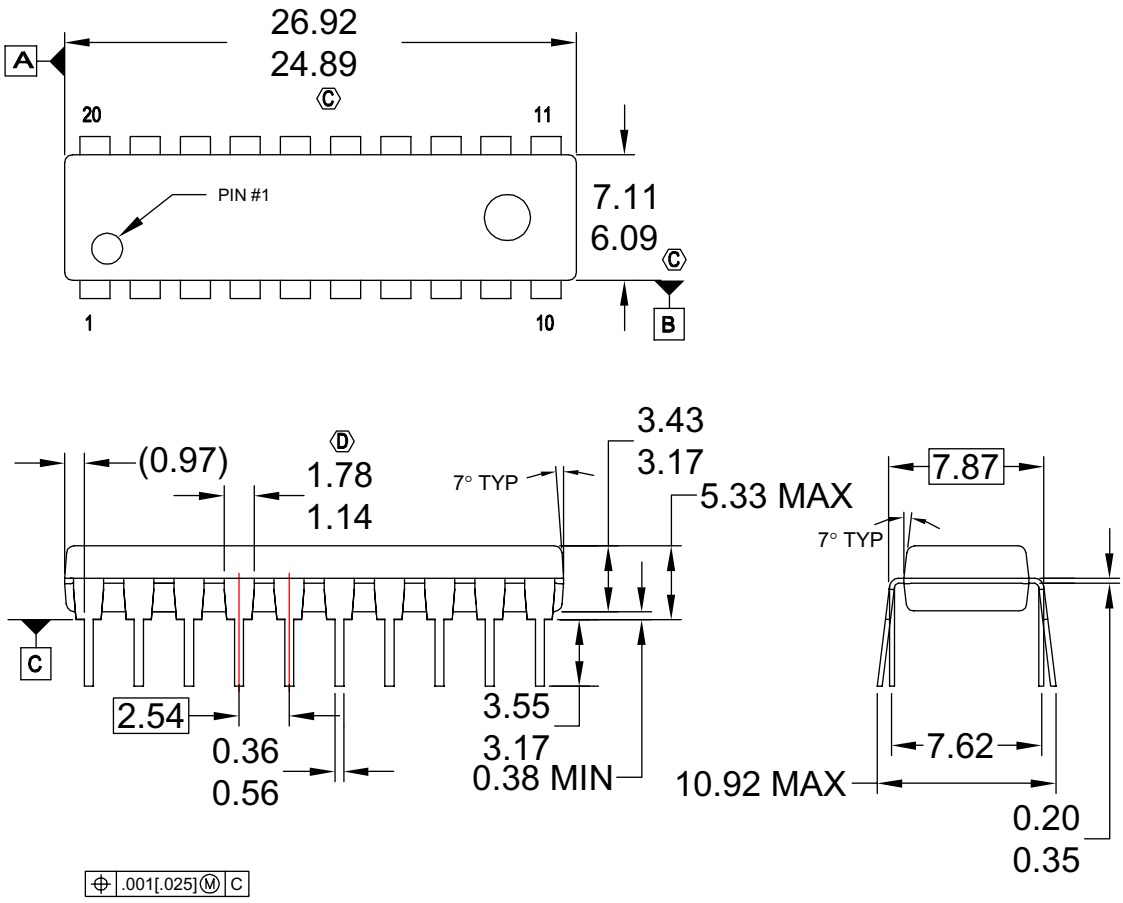
Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.

B. ALL DIMENSIONS ARE IN MILLIMETERS

C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.

D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.

E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter® *
FPS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32

©1988 Fairchild Semiconductor Corporation