FAIRCHILD SEMICONDUCTOR™

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74ALVC16501
Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The ALVC16501 is an 18-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in a high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active HIGH and $\overline{\text{OEBA}}$ is active LOW).

The ALVC16501 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The ALVC16501 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
  - 3.4 ns max for 3.0V to 3.6V V_{CC}
  - 4.0 ns max for 2.3V to 2.7V V_{CC}
  - 7.0 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistors is determined by the current-sourcing capability of the driver.

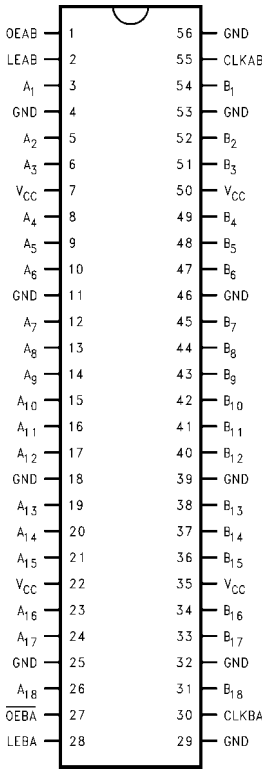
Ordering Code:

Order Number	Package Number	Package Description
74ALVC16501MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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Connection Diagram



Pin Descriptions

Pin Names	Description
OEAB	Output Enable Input for A to B Direction (Active HIGH)
$\overline{OEBA}$	Output Enable Input for B to A Direction (Active LOW)
LEAB, LEBA	Latch Enable Inputs
CLKAB, CLKBA	Clock Inputs
A_1–A_{18}	Side A Inputs or 3-STATE Outputs
B_1–B_{18}	Side B Inputs or 3-STATE Outputs

Function Table (Note 2)

Inputs				Outputs
OEAB	**LEAB**	**CLKAB**	**A_n**	**B_n**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0 (Note 3)
H	L	L	X	B_0 (Note 4)

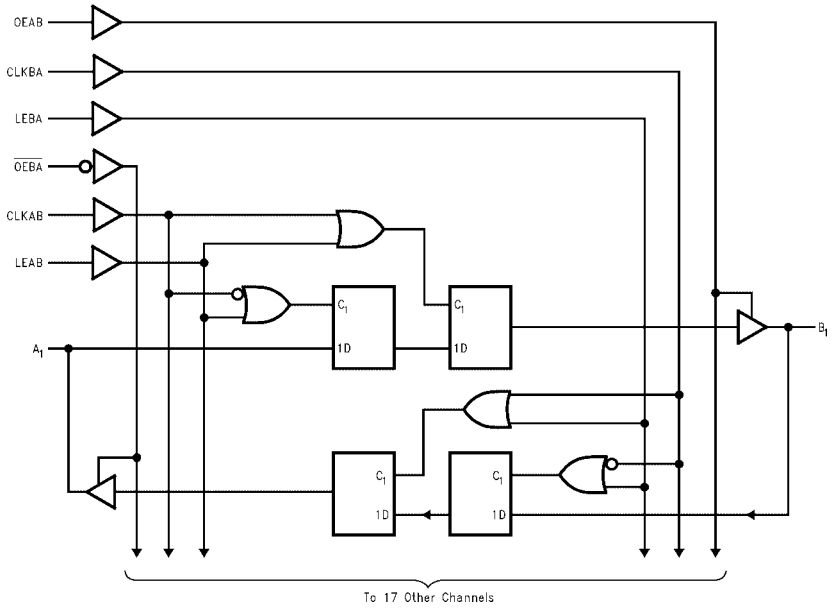
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Note 2: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA and CLKBA. $\overline{OEBA}$ is active LOW.

Note 3: Output level before the indicated steady-state input conditions were established.

Note 4: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



Absolute Maximum Ratings (Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 6)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 -1.95	0.65 x V_{CC}		V
			2.3 - 2.7	1.7		
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 -1.95		0.35 x V_{CC}	V
			2.3 - 2.7		0.7	
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −4 mA	1.65	1.2		
		I_{OH} = −6 mA	2.3	2		
		I_{OH} = −12 mA	2.3	1.7		
			2.7	2.2		
			3.0	2.4		
		I_{OH} = −24 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	V
		I_{OL} = 4 mA	1.65		0.45	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 12mA	2.3		0.7	
			2.7		0.4	
		I_{OL} = 24 mA	3		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V	3.6		±10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6		40	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	3 -3.6		750	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
		$C_L = 50$ pF				$C_L = 30$ pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	250		200		200		100		ns
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus	1.1	3.4	1.3	4.0	0.8	3.5	1.5	7.0	ns
t_{PHL}, t_{PLH}	Propagation Delay CLK to Bus	1.1	4.0	1.3	4.9	0.8	4.4	1.5	8.8	ns
t_{PHL}, t_{PLH}	Propagation Delay LE to Bus	1.1	4.3	1.3	5.4	0.8	4.9	1.5	9.8	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.1	4.3	1.3	5.4	0.8	4.9	1.5	9.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.3	4.2	1.3	4.7	0.8	4.2	0.8	7.6	ns
t_W	Pulse Width	1.5		1.5		1.5		4.0		ns
t_S	Setup Time	1.5		1.5		1.5		2.5		ns
t_H	Hold Time	1.0		1.0		1.0		1.0		ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		$V_I = 0V$ or V_{CC}	3.3	6	pF
C_{OUT}	Output Capacitance		$V_I = 0V$ or V_{CC}	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, $C_L = 50$ pF	3.3	20	pF
				2.5	20	

AC Loading and Waveforms

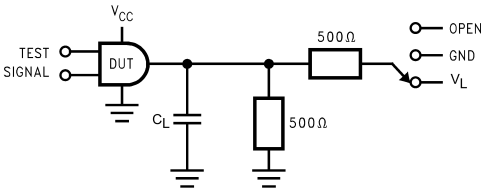


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; Z_0 = 50Ω)

Symbol	V_{CC}			
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V
V_L	6V	6V	V_{CC}*2	V_{CC}*2

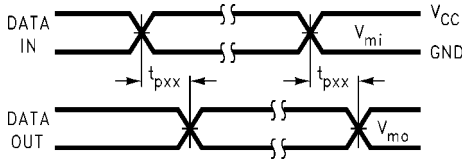


FIGURE 2. Waveform for Inverting and Non-inverting Functions

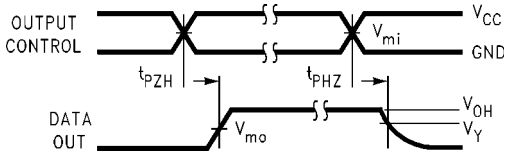


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

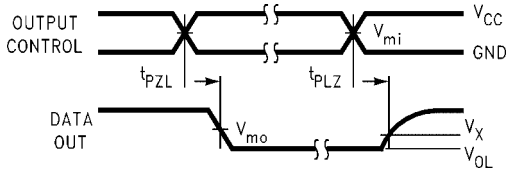


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

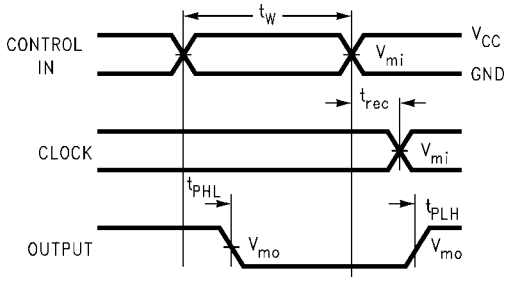


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

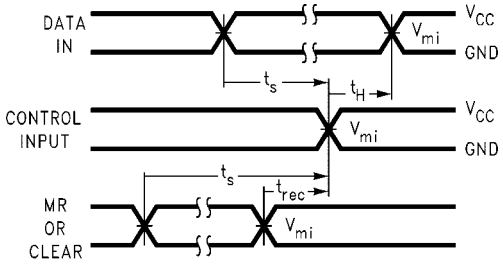
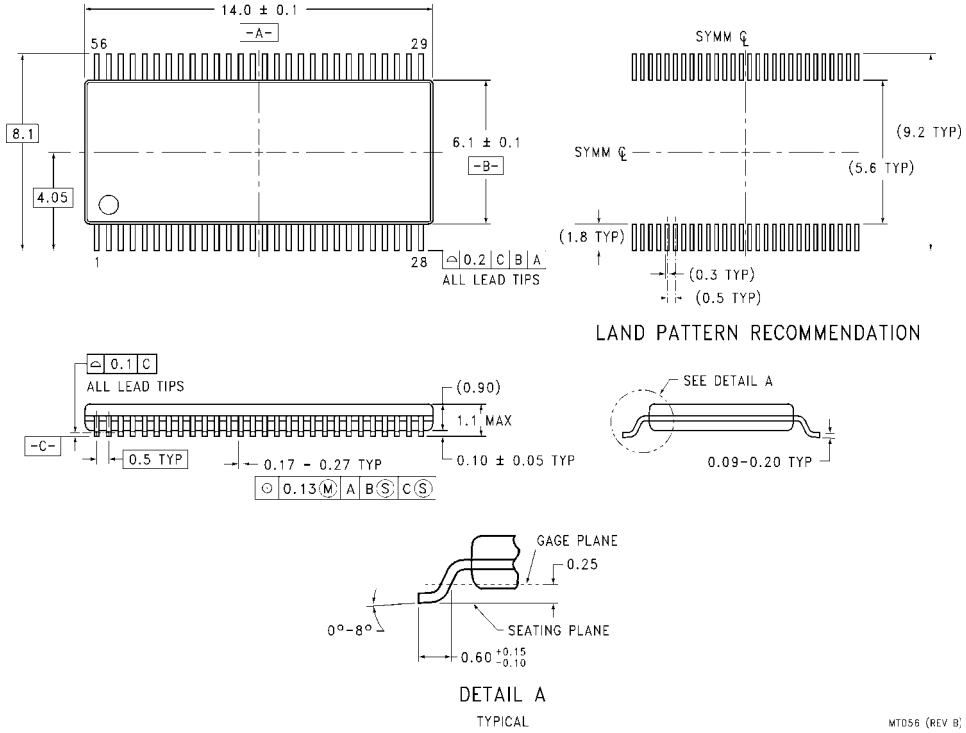


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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