

## SNx4HCT138 3-Line to 8-Line Decoders/Demultiplexers

### 1 Features

- Operating voltage range of 4.5 V to 5.5 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 80- $\mu$ A max  $I_{CC}$
- Typical  $t_{pd} = 17$  ns
- $\pm 4$ -mA output drive at 5 V
- Low input current of 1  $\mu$ A max
- Inputs are TTL-Voltage compatible
- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporate three enable inputs to simplify cascading and/or data reception

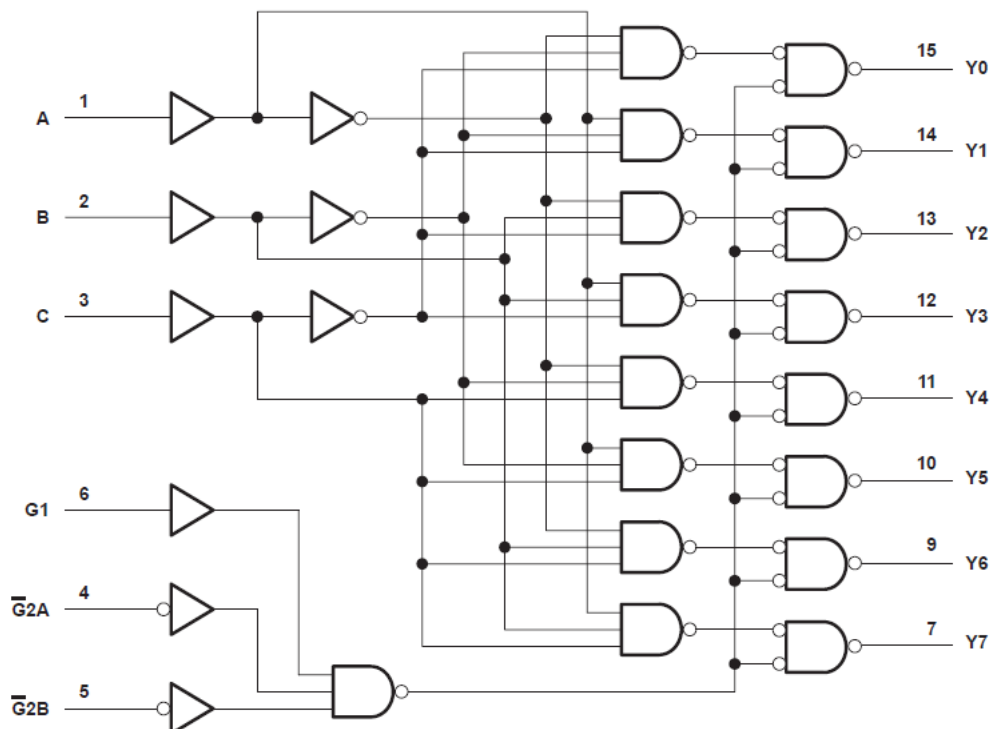
### 2 Description

The 'HCT138 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

#### Device Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)    |
|---------------|------------------------|--------------------|
| SN74HCT138D   | SOIC (16)              | 9.90 mm × 3.90 mm  |
| SN74HCT138N   | PDIP (16)              | 19.31 mm × 6.35 mm |
| SN74HCT138NS  | SO (16)                | 6.20 mm × 5.30 mm  |
| SN74HCT138PW  | TSSOP (16)             | 5.00 mm × 4.40 mm  |
| SN54HCT138J   | CDIP (16)              | 24.38 mm × 6.92 mm |
| SNJ54HCT138FK | LCCC (20)              | 8.89 mm × 8.45 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

### Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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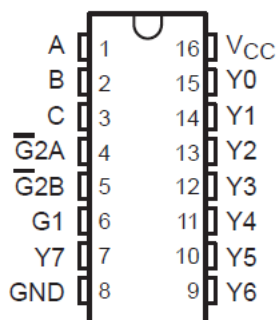
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## 3 Revision History

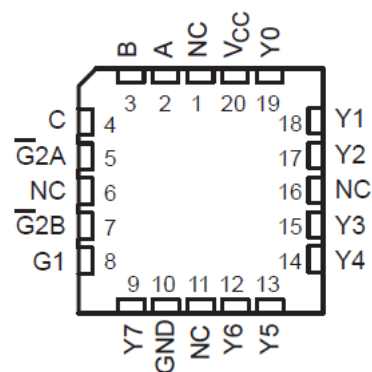
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision E (September 2003) to Revision F (March 2022)</b>                                                                                                                     | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <ul style="list-style-type: none"> <li>Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....</li> </ul> | <b>1</b>    |

## 4 Pin Configuration and Functions



**J, W, D, N, NS, or PW Package**  
**16-Pin CDIP, CFP, SOIC, PDIP, SO, TSSOP**  
**Top View**



NC – No internal connection

**FK Package**  
**20-Pin LCCC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                            | MIN                                  | MAX | UNIT        |
|-----------|--------------------------------------------|--------------------------------------|-----|-------------|
| $V_{CC}$  | Supply voltage range                       | -0.5                                 | 7   | V           |
| $I_{IK}$  | Input clamp current <sup>(2)</sup>         | $(V_I < 0 \text{ or } V_I > V_{CC})$ |     | $\pm 20$ mA |
| $I_{OK}$  | Output clamp current <sup>(2)</sup>        | $(V_O < 0 \text{ or } V_O > V_{CC})$ |     | $\pm 20$ mA |
| $I_O$     | Continuous output current                  | $(V_O = 0 \text{ to } V_{CC})$       |     | $\pm 25$ mA |
|           | Continuous current through $V_{CC}$ or GND |                                      |     | $\pm 50$ mA |
| $T_J$     | Junction temperature                       |                                      |     | 150 °C      |
| $T_{stg}$ | Storage temperature                        |                                      |     | -65 150 °C  |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

|          |                                 |                                            | SN54HCT138 |     |          | SN74HCT138 |     |          | UNIT |
|----------|---------------------------------|--------------------------------------------|------------|-----|----------|------------|-----|----------|------|
|          |                                 |                                            | MIN        | NOM | MAX      | MIN        | NOM | MAX      |      |
| $V_{CC}$ | Supply voltage                  |                                            | 4.5        | 5   | 5.5      | 4.5        | 5   | 5.5      | V    |
| $V_{IH}$ | High-level input voltage        | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2          |     |          | 2          |     |          | V    |
| $V_{IL}$ | Low-level input voltage         | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ |            |     | 0.8      |            |     | 0.8      | V    |
| $V_I$    | Input voltage                   |                                            | 0          |     | $V_{CC}$ | 0          |     | $V_{CC}$ | V    |
| $V_O$    | Output voltage                  |                                            | 0          |     | $V_{CC}$ | 0          |     | $V_{CC}$ | V    |
| $t_t$    | Input transition rise/fall time |                                            |            |     | 500      |            |     | 500      | ns   |
| $T_A$    | Operating free-air temperature  |                                            | -55        |     | 125      | -40        |     | 85       | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating CMOS Inputs, literature number [SCBA004](#).

### 5.3 Thermal Information

| THERMAL METRIC  |                                                       | D (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|-----------------|-------------------------------------------------------|----------|----------|---------|------------|------|
|                 |                                                       | 16 PINS  | 16 PINS  | 16 PINS | 16 PINS    |      |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance <sup>(1)</sup> | 73       | 67       | 64      | 108        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

| PARAMETER                       |                           | TEST CONDITIONS <sup>(1)</sup>                                    | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |       |      | SN54HCT138 |       | SN74HCT138 |       | UNIT |
|---------------------------------|---------------------------|-------------------------------------------------------------------|------------------------|-----------------------|-------|------|------------|-------|------------|-------|------|
|                                 |                           |                                                                   |                        | MIN                   | TYP   | MAX  | MIN        | MAX   | MIN        | MAX   |      |
| V <sub>OH</sub>                 | High-level output voltage | I <sub>OH</sub> = –20 µA                                          | 4.5                    | 4.4                   | 4.499 |      | 4.4        |       | 4.4        |       | V    |
|                                 |                           | I <sub>OH</sub> = –4 mA                                           |                        | 3.98                  | 4.3   |      | 3.7        |       | 3.84       |       |      |
| V <sub>OL</sub>                 | Low-level output voltage  | I <sub>OL</sub> = 20 µA                                           | 4.5                    |                       | 0.001 | 0.1  |            | 0.1   |            | 0.1   | V    |
|                                 |                           | I <sub>OL</sub> = 4 mA                                            |                        |                       | 0.17  | 0.26 |            | 0.4   |            | 0.33  |      |
| I <sub>I</sub>                  | Input hold current        | V <sub>I</sub> = V <sub>CC</sub> or 0                             | 5.5                    |                       | ±0.1  | ±100 |            | ±1000 |            | ±1000 | nA   |
| I <sub>CC</sub>                 | Supply current            | V <sub>I</sub> = V <sub>CC</sub> or 0. I <sub>O</sub> = 0         | 5.5                    |                       |       | 8    |            | 160   |            | 80    | µA   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | Supply-current change     | One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub> | 5.5                    |                       | 1.4   | 2.4  |            | 3     |            | 2.9   | mA   |
| C <sub>i</sub>                  | Input capacitance         |                                                                   | 4.5 to 5.5             |                       | 3     | 10   |            | 10    |            | 10    | pF   |

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.5 Switching Characteristics

C<sub>L</sub> = 50 pF. See [Parameter Measurement Information](#)

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> (V) | T <sub>A</sub> = 25°C |     |     | SN54HCT138 |     | SN74HCT138 |     | UNIT |
|-----------------|-----------------|----------------|---------------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                 |                 |                |                     | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub> | A, B or C       | Any Y          | 4.5                 |                       | 23  | 36  |            | 54  |            | 45  | ns   |
|                 |                 |                | 5.5                 |                       | 17  | 32  |            | 49  |            | 34  |      |
|                 | Enable          | Any Y          | 4.5                 |                       | 22  | 33  |            | 50  |            | 42  |      |
|                 |                 |                | 5.5                 |                       | 18  | 30  |            | 45  |            | 38  |      |
| t <sub>t</sub>  |                 | Y              | 4.5                 |                       | 12  | 15  |            | 22  |            | 19  | ns   |
|                 |                 |                | 5.5                 |                       | 11  | 14  |            | 20  |            | 17  |      |

## 5.6 Operating Characteristics

T<sub>A</sub> = 25°C

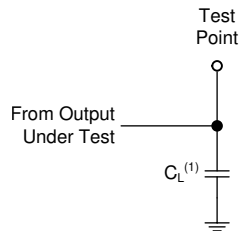
| PARAMETER       |                               | TEST CONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|-----------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance | No load         | 85  | pF   |

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

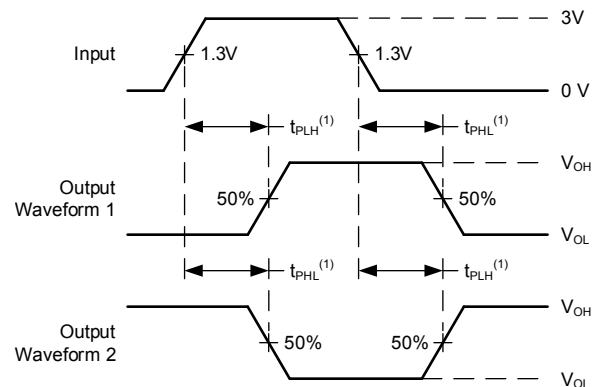
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}$ .

**Figure 6-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**

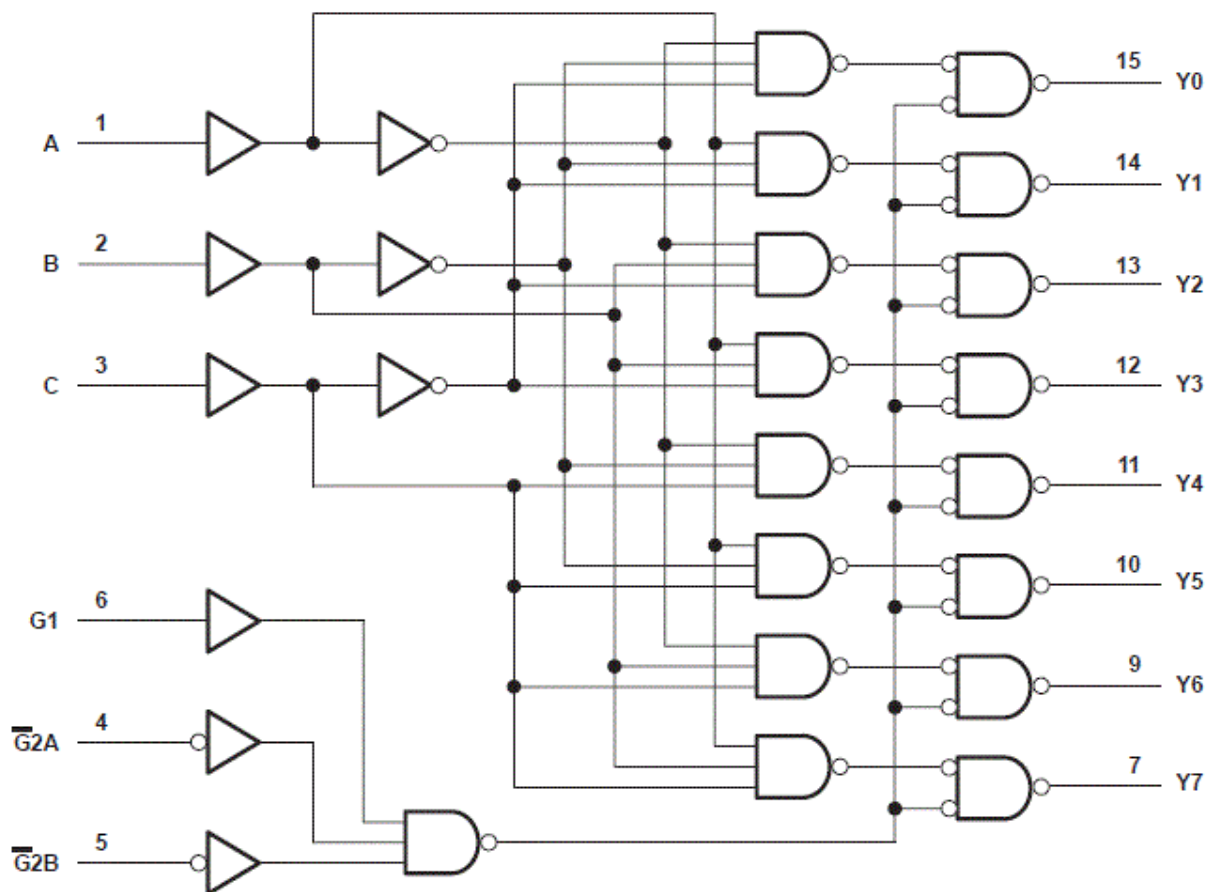
## 7 Detailed Description

### 7.1 Overview

The 'HCT138 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low ( $\overline{G}$ ) and one active-high (G) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

### 7.2 Functional Block Diagram



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

## 7.3 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS |                  |                  |        |   |   | OUTPUTS |    |    |    |    |    |    |    |
|--------|------------------|------------------|--------|---|---|---------|----|----|----|----|----|----|----|
| ENABLE |                  |                  | SELECT |   |   |         |    |    |    |    |    |    |    |
| G1     | $\overline{G2A}$ | $\overline{G2B}$ | C      | B | A | Y0      | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X      | H                | X                | X      | X | X | H       | H  | H  | H  | H  | H  | H  | H  |
| X      | X                | H                | X      | X | X | H       | H  | H  | H  | H  | H  | H  | H  |
| L      | X                | X                | X      | X | X | H       | H  | H  | H  | H  | H  | H  | H  |
| H      | L                | L                | L      | L | L | L       | H  | H  | H  | H  | H  | H  | H  |
| H      | L                | L                | L      | L | H | H       | L  | H  | H  | H  | H  | H  | H  |
| H      | L                | L                | L      | H | L | H       | H  | L  | H  | H  | H  | H  | H  |
| H      | L                | L                | L      | H | H | H       | H  | L  | H  | H  | H  | H  | H  |
| H      | L                | L                | H      | L | L | H       | H  | H  | H  | L  | H  | H  | H  |
| H      | L                | L                | H      | L | H | H       | H  | H  | H  | H  | L  | H  | H  |
| H      | L                | L                | H      | H | L | H       | H  | H  | H  | H  | H  | L  | H  |
| H      | L                | L                | H      | H | H | H       | H  | H  | H  | H  | H  | H  | L  |

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.4 Trademarks

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### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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