

**SN54LS189A, SN54LS219A, SN54LS289A, SN54LS319A  
SN74LS189A, SN74LS219A, SN74LS289A, SN74LS319A  
64-BIT RANDOM-ACCESS MEMORIES**

D2417, SEPTEMBER 1980—REVISED FEBRUARY 1985

- Organized as 16 Words of Four Bits Each
- Choice of Buffered 3-State or Open-Collector outputs
- Choice of Noninverted or Inverted Outputs
- Typical Access Time . . . 50 ns

**description**

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state output version and an open-collector-output version are offered for both of the logic choices. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

**write cycle**

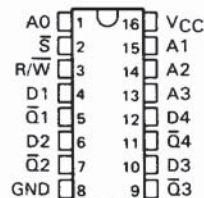
Information to be stored in the memory is written into the selected address location when the chip-select ( $\bar{S}$ ) and the write-enable (R/W) inputs are low. While the write-enable input is low, the memory outputs are off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

**read cycle**

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

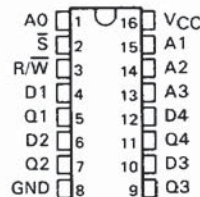
SN54LS189A, SN54LS289A . . . J PACKAGE  
SN74LS189A, SN74LS289A . . . J OR N PACKAGE

(TOP VIEW)



SN54LS219A, SN54LS319A . . . J PACKAGE  
SN74LS219A, SN74LS319A . . . J OR N PACKAGE

(TOP VIEW)



FUNCTION TABLE

| FUNCTION | INPUTS      |              | OUTPUTS                    |                            |              |              |
|----------|-------------|--------------|----------------------------|----------------------------|--------------|--------------|
|          | CHIP SELECT | WRITE ENABLE | 'LS189A                    | 'LS289A                    | 'LS219A      | 'LS319A      |
| Write    | L           | L            | Z                          | Off                        | Z            | Off          |
| Read     | L           | H            | Complement of Data Entered | Complement of Data Entered | Data Entered | Data Entered |
| Inhibit  | H           | X            | Z                          | Off                        | Z            | Off          |

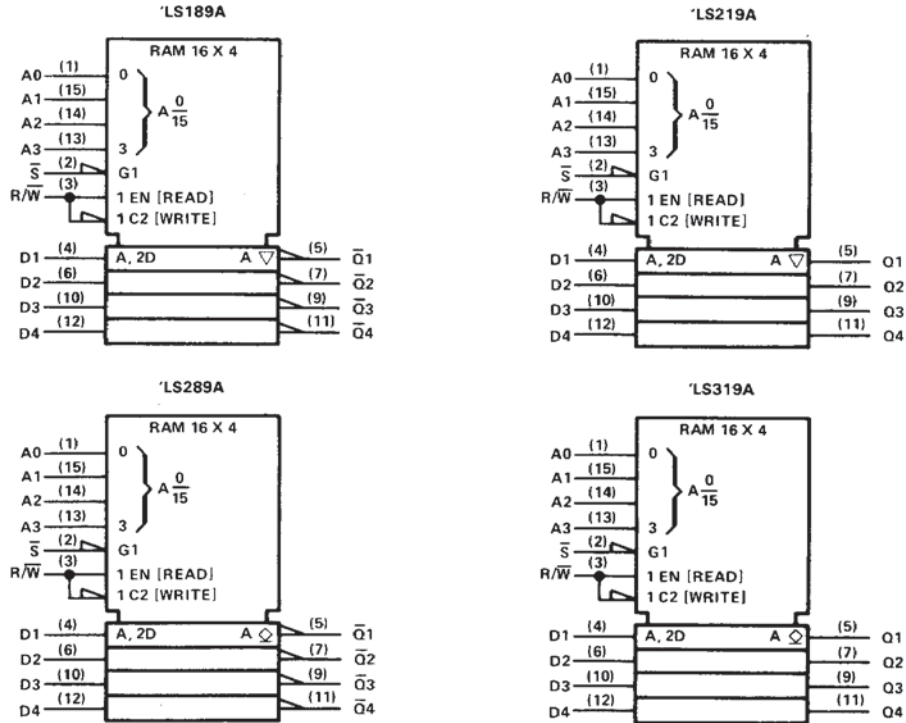
H = high level, L = low level, X = irrelevant, Z = high impedance

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**SN54LS189A, SN54LS219A, SN54LS289A, SN54LS319A  
SN74LS189A, SN74LS219A, SN74LS289A, SN74LS319A  
64-BIT RANDOM-ACCESS MEMORIES**

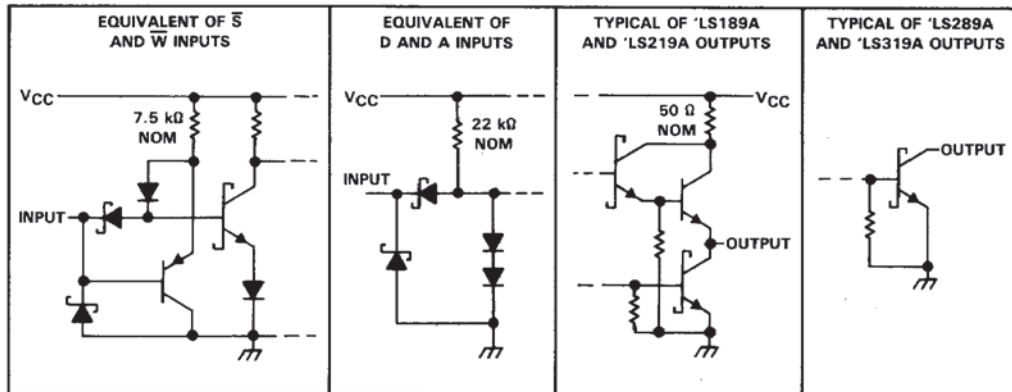
logic symbols



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schematics of inputs and outputs



**SN54LS189A, SN54LS219A, SN54LS289A, SN54LS319A  
SN74LS189A, SN74LS219A, SN74LS289A, SN74LS319A  
64-BIT RANDOM-ACCESS MEMORIES**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|                                                        |                |
|--------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)                  | 7 V            |
| Input voltage                                          | 7 V            |
| Off-state output voltage: 'LS189A, 'LS219A             | 5.5 V          |
| 'LS289A, 'LS319A                                       | 7 V            |
| Operating free-air temperature range: SN54LS' Circuits | -55°C to 125°C |
| SN74LS' Circuits                                       | 0°C to 70°C    |
| Storage temperature range                              | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

|                                                      |                                                    | SN54LS189A,<br>SN54LS219A |     |     | SN74LS189A,<br>SN74LS219A |     |      | UNIT |    |    |
|------------------------------------------------------|----------------------------------------------------|---------------------------|-----|-----|---------------------------|-----|------|------|----|----|
|                                                      |                                                    | MIN                       | NOM | MAX | MIN                       | NOM | MAX  |      |    |    |
| Supply voltage, $V_{CC}$                             |                                                    | 4.5                       | 5   | 5.5 | 4.75                      | 5   | 5.25 | V    |    |    |
| High-level output current, $I_{OH}$                  |                                                    |                           |     | -1  |                           |     | -2.6 | mA   |    |    |
| Low-level output current, $I_{OL}$                   |                                                    |                           |     | 12  |                           |     | 24   | mA   |    |    |
| Width of write pulse (write enable low), $t_{W(wr)}$ |                                                    | 100                       |     |     | 70                        |     |      |      |    |    |
| Setup time                                           | Address before write pulse, $t_{su(ad)}$           | 0†                        |     |     | 0†                        |     |      | ns   |    |    |
|                                                      | Data before end of write pulse, $t_{su(da)}$       | 100†                      |     |     | 60†                       |     |      |      |    |    |
|                                                      | Chip-select before end of write pulse, $t_{su(S)}$ | 100†                      |     |     | 60†                       |     |      |      |    |    |
| Hold time                                            | Address after write pulse, $t_h(ad)$               | 0†                        |     |     | 0†                        |     |      | ns   |    |    |
|                                                      | Data after write pulse, $t_h(da)$                  | 0†                        |     |     | 0†                        |     |      |      |    |    |
|                                                      | Chip-select after write pulse, $t_h(S)$            | 0†                        |     |     | 0†                        |     |      |      |    |    |
| Operating free-air temperature, $T_A$                |                                                    | -55                       |     |     | 125                       |     |      | 0    | 70 | °C |

††The arrow indicates the transition of the write-enable input used for reference: † for the low-to-high transition, ‡ for the high-to-low transition.

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**SN54LS189A, SN54LS219A, SN74LS189A, SN74LS219A**  
**64-BIT RANDOM-ACCESS MEMORIES**  
**WITH 3-STATE OUTPUTS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                               | TEST CONDITIONS <sup>†</sup>                                                                                                               | SN54LS189A<br>SN54LS219A |                  |      | SN74LS189A<br>SN74LS219A |                  |      | UNIT |
|-------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------------------|------|--------------------------|------------------|------|------|
|                                                                         |                                                                                                                                            | MIN                      | TYP <sup>‡</sup> | MAX  | MIN                      | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IH</sub> High-level input voltage                                |                                                                                                                                            | 2                        |                  |      | 2                        |                  |      | V    |
| V <sub>IL</sub> Low-level input voltage                                 |                                                                                                                                            |                          | 0.7              |      |                          | 0.8              |      | V    |
| V <sub>IK</sub> Input clamp voltage                                     | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA                                                                                             |                          | -1.5             |      |                          | -1.5             |      | V    |
| V <sub>OH</sub> High-level output voltage                               | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OH</sub> = MAX                              | 2.4                      | 3.1              |      | 2.4                      | 3.1              |      | V    |
| V <sub>OL</sub> Low-level output voltage                                | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OL</sub> = 12 mA<br>I <sub>OL</sub> = 24 mA |                          | 0.25             | 0.4  |                          | 0.25             | 0.4  | V    |
| I <sub>OZH</sub> Off-state output current<br>high-level voltage applied | V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>ILmax</sub> , V <sub>O</sub> = 2.7 V                             |                          | 20               |      |                          | 20               |      | μA   |
| I <sub>OZL</sub> Off-state output current,<br>low-level voltage applied | V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>ILmax</sub> , V <sub>O</sub> = 0.4 V                             |                          | -20              |      |                          | -20              |      | μA   |
| I <sub>I</sub> Input current at<br>maximum input voltage                | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V                                                                                                |                          | 100              |      |                          | 100              |      | μA   |
| I <sub>IH</sub> High-level input current                                | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                                                                                              |                          | 20               |      |                          | 20               |      | μA   |
| I <sub>IL</sub> Low-level input current                                 | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                                                                                              |                          | -0.4             |      |                          | -0.4             |      | mA   |
| I <sub>OS</sub> Short-circuit output<br>current <sup>§</sup>            | V <sub>CC</sub> = MAX                                                                                                                      | -30                      |                  | -130 | -30                      |                  | -130 | mA   |
| I <sub>CC</sub> Supply current                                          | V <sub>CC</sub> = MAX, See Note 2                                                                                                          |                          | 35               | 60   |                          | 35               | 60   | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I<sub>CC</sub> is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T<sub>A</sub> and V<sub>CC</sub> (unless otherwise noted)

| PARAMETER                                                    | TEST CONDITIONS                       | SN54LS189A<br>SN54LS219A |                  |     | SN74LS189A<br>SN74LS219A |                  |     | UNIT |
|--------------------------------------------------------------|---------------------------------------|--------------------------|------------------|-----|--------------------------|------------------|-----|------|
|                                                              |                                       | MIN                      | TYP <sup>‡</sup> | MAX | MIN                      | TYP <sup>‡</sup> | MAX |      |
| t <sub>a(ad)</sub> Access time from address                  | C <sub>L</sub> = 45 pF,<br>See Note 3 |                          | 50               | 90  |                          | 50               | 80  | ns   |
| t <sub>a(S)</sub> Access time from chip select (enable time) |                                       |                          | 35               | 70  |                          | 35               | 60  | ns   |
| t <sub>SR</sub> Sense recovery time                          |                                       |                          | 55               | 100 |                          | 55               | 90  | ns   |
| t <sub>PXZ</sub> Disable time from high or low level         | from $\overline{S}$                   |                          | 30               | 60  |                          | 30               | 50  | ns   |
|                                                              | from R/W                              |                          | 40               | 70  |                          | 40               | 60  |      |

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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**SN54LS289A, SN54LS319A, SN74LS289A, SN74LS319A**  
**64-BIT RANDOM-ACCESS MEMORIES**  
**WITH OPEN-COLLECTOR OUTPUTS**

**recommended operating conditions**

|                                                    |                                                    | SN54LS289A,<br>SN54LS319A |     |     | SN74LS289A,<br>SN74LS319A |     |      | UNIT |
|----------------------------------------------------|----------------------------------------------------|---------------------------|-----|-----|---------------------------|-----|------|------|
|                                                    |                                                    | MIN                       | NOM | MAX | MIN                       | NOM | MAX  |      |
| Supply voltage, $V_{CC}$                           |                                                    | 4.5                       | 5   | 5.5 | 4.75                      | 5   | 5.25 | V    |
| High-level output voltage, $V_{OH}$                |                                                    |                           |     | 5.5 |                           |     | 5.5  | V    |
| Low-level output current, $I_{OL}$                 |                                                    |                           |     | 12  |                           |     | 24   | mA   |
| Width of write pulse (write enable low), $t_W(wr)$ |                                                    | 100                       |     |     | 70                        |     |      |      |
| Setup time                                         | Address before write pulse, $t_{su}(ad)$           | 01                        |     |     | 01                        |     |      | ns   |
|                                                    | Data before end of write pulse, $t_{su}(da)$       | 1001                      |     |     | 601                       |     |      |      |
|                                                    | Chip-select before end of write pulse, $t_{su}(S)$ | 1001                      |     |     | 601                       |     |      |      |
| Hold time                                          | Address after write pulse, $t_h(ad)$               | 01                        |     |     | 01                        |     |      | ns   |
|                                                    | Data after write pulse, $t_h(da)$                  | 01                        |     |     | 01                        |     |      |      |
|                                                    | Chip-select after write pulse, $t_h(S)$            | 01                        |     |     | 01                        |     |      |      |
| Operating free-air temperature, $T_A$              |                                                    | -55                       |     | 125 | 0                         |     | 70   | °C   |

11The arrow indicates the transition of the write-enable input used for reference: 1 for the low-to-high transition, 1 for the high-to-low transition.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                                    | TEST CONDITIONS <sup>†</sup>                                                                                        | SN54LS289A<br>SN54LS319A |                  |     | SN74LS289A<br>SN74LS319A |                  |     | UNIT |
|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------|--------------------------|------------------|-----|--------------------------|------------------|-----|------|
|                                              |                                                                                                                     | MIN                      | TYP <sup>‡</sup> | MAX | MIN                      | TYP <sup>‡</sup> | MAX |      |
| $V_{IH}$ High-level input voltage            |                                                                                                                     | 2                        |                  |     | 2                        |                  |     | V    |
| $V_{IL}$ Low-level input voltage             |                                                                                                                     |                          | 0.7              |     |                          | 0.8              |     | V    |
| $V_{IK}$ Input clamp voltage                 | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                                                         |                          | -1.5             |     |                          | -1.5             |     | V    |
| $I_{OH}$ High-level output current           | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_O = 2.4 \text{ V}$<br>$V_{IL} = V_{ILmax}, V_O = 5.5 \text{ V}$       |                          | 20               |     |                          | 20               |     | μA   |
| $V_{OL}$ Low-level output voltage            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$<br>$V_{IL} = V_{ILmax}, I_{OL} = 24 \text{ mA}$ | 0.25                     | 0.4              |     | 0.25                     | 0.4              |     | V    |
| $I_I$ Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$                                                                            |                          | 100              |     |                          | 100              |     | μA   |
| $I_{IH}$ High-level input current            | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$                                                                          |                          | 20               |     |                          | 20               |     | μA   |
| $I_{IL}$ Low-level input current             | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                                          |                          | -0.4             |     |                          | -0.4             |     | mA   |
| $I_{CC}$ Supply current                      | $V_{CC} = \text{MAX}, \text{ See Note 2}$                                                                           | 35                       | 60               |     | 35                       | 60               |     | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

**switching characteristics over recommended operating ranges of  $T_A$  and  $V_{CC}$  (unless otherwise noted)**

| PARAMETER                                                                 | TEST CONDITIONS                                        | SN54LS289A<br>SN54LS319A |                  |     | SN74LS289A<br>SN74LS319A |                  |     | UNIT |
|---------------------------------------------------------------------------|--------------------------------------------------------|--------------------------|------------------|-----|--------------------------|------------------|-----|------|
|                                                                           |                                                        | MIN                      | TYP <sup>‡</sup> | MAX | MIN                      | TYP <sup>‡</sup> | MAX |      |
| $t_a(ad)$ Access time from address                                        | $C_L = 45 \text{ pF}, R_L = 667\Omega$ ,<br>See Note 3 | 50                       | 90               |     | 50                       | 80               |     | ns   |
| $t_a(S)$ Access time from chip select (enable time)                       |                                                        | 35                       | 70               |     | 35                       | 60               |     | ns   |
| $t_{SR}$ Sense recovery time                                              |                                                        | 55                       | 100              |     | 55                       | 90               |     | ns   |
| $t_{PLH}$ Propagation delay time, low-to-high-level output (disable time) |                                                        | 30                       | 60               |     | 30                       | 50               |     | ns   |
|                                                                           |                                                        | 40                       | 70               |     | 40                       | 60               |     |      |

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.