64Mb Synchronous DRAM Specification

A2V64S40CTP

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General Description

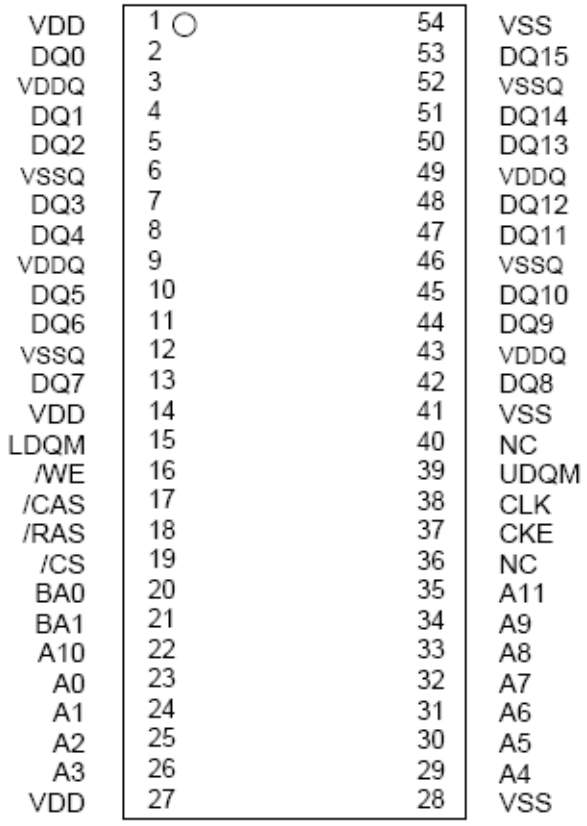
The A2V64S40CTP is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS latency (2 & 3)
  - Burst length (1, 2, 4, 8 & Full page)
  - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Auto & self refresh
- 64ms refresh period (4K cycle)
- Burst read single write operation
- LDQM & UDQM for masking

Pin Configurations

54-pin Plastic TSOP (II)



(Top view)

Ordering Information

54Pin TSOPII (400mil x 875mil)

Part No.	Max. Frequency	Supply Voltage
A2V64S40CTP-G5	200MHz (CL=3)	3.3V
A2V64S40CTP-G6	166MHz (CL=3)	3.3V
A2V64S40CTP-G7	143MHz (CL=3)	3.3V

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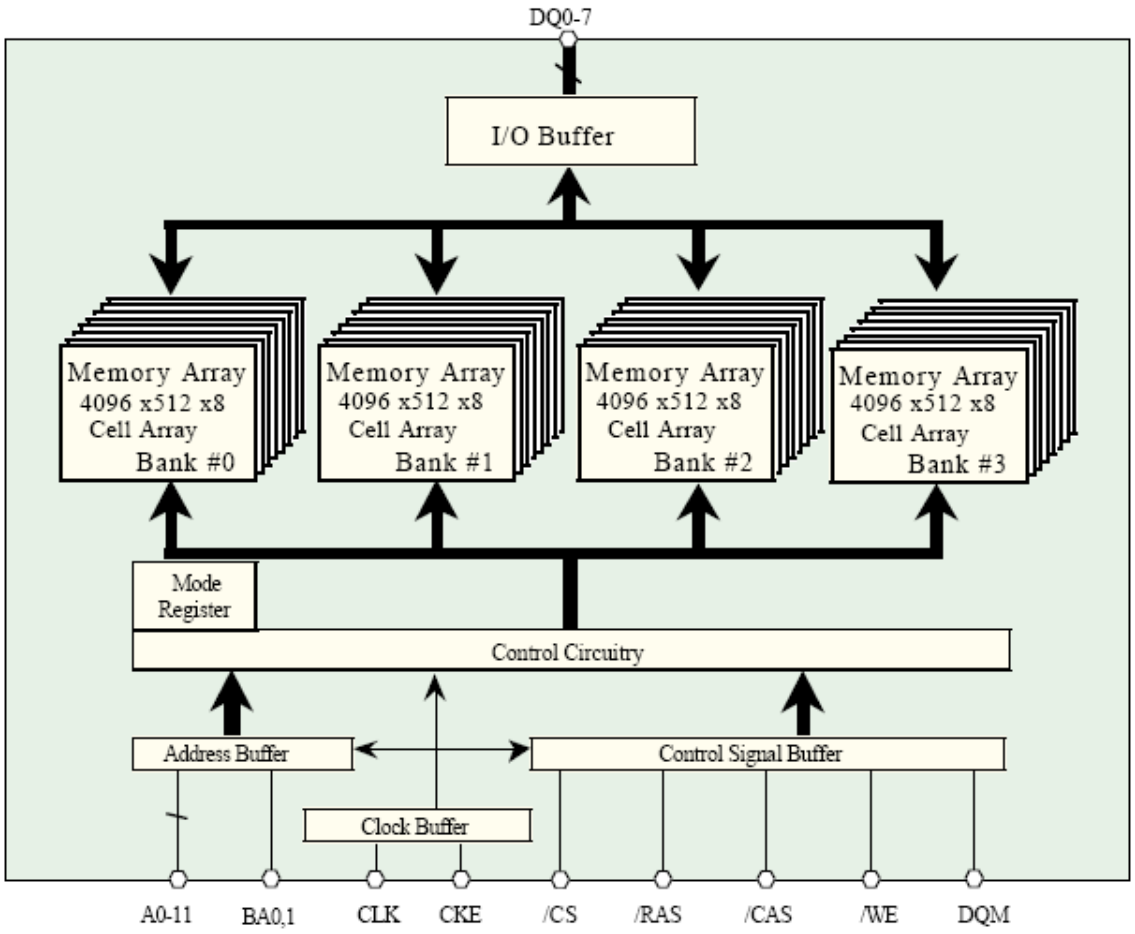
BLOCK DIAGRAM



Note:This figure shows the A2V64S30CTP
The A2V64S20CTP configuration is 4096x1024x4 of cell array and DQ0-3
The A2V64S40CTP configuration is 4069x256x16 of cell array and DQ0-15

Type Designation Code

A 2 V 6 4 S 4 0 C T P – G 5

- Speed Grade 7： 143MHz@CL=3, 6： 166MHz@CL=3, 5： 200MHz@CL=3
- Package Type TP：TSOP (II)
- Process Generation
- Function Reserved for Future Use
- Organization 2^n 3：x8, 4：x16
- SDR Synchronous DRAM
- Density 64：64M bits
- Interface V：LVTTL
- Memory Style (DRAM)
- Zentel DRAM

Pin Descriptions

SYMBOL	TYPE	DESCRIPTION
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank), DEEP POWER DOWN (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
/CS	Input	Chip Select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/CAS, /RAS, /WE	Input	Command Inputs: /CAS, /RAS, and /WE (along with /CS) define the command being entered.
LDQM, UDQM,	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.
BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. These pins also select between the mode register and the extended mode register.
A0–A11	Input	Address Inputs: A0–A11 are sampled during the ACTIVE command (row address A0–A11) and READ/WRITE command (column-address A0–A7; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0–DQ15	I/O	Data Input/Output: Data bus.
NC	–	Internally Not Connected: These could be left unconnected, but it is recommended they be connected or V_{SS}.
$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V_{DD}	Supply	Core Power Supply.
V_{SS}	Supply	Ground.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	° C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTES:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, **T_A = 0 to 70° C**)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
	V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0		V_{DDQ} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 0.1mA
Input leakage current	I_{LI}	-5	-	5	uA	3
Output leakage current	I_{oL}	-5	-	5	uA	3

Note:
1. VIH(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. VIL(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ VIN ≤ VDD + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled , 0V ≤ VOUT ≤ VDD.

CAPACITANCE (Vdd =3.3V, **T_A = 25°C**, f = 1MHz)

Parameter	Symbol	Min	Max	Unit	Note
Clock	Cclk	2.0	4.0	pF	
/CAS,/RAS,/WE,/CS,CKE,L/UDQM	Cin	2.0	4.0	pF	
Address	C_{ADD}	2.0	4.0	pF	
DQ0~DQ15	C_{OUT}	3.0	6.0	pF	

DC CHARACTERISTICS

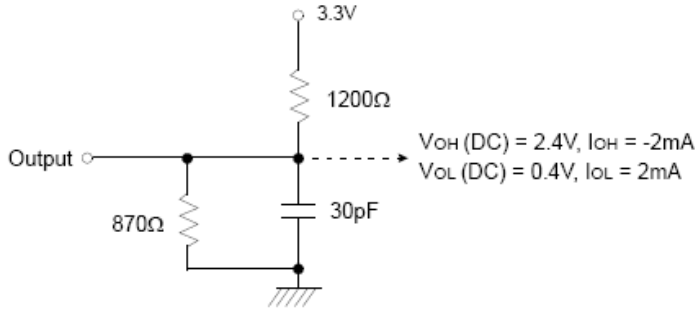
Recommended operating conditions (Voltage referenced to V_{SS} = 0V, **T_A = 0 to 70° C**)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-5	-6	-7		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	80	70	60	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≦ V_{IL}(max), t_{CC} = 10ns	2	2	2	mA	
	I_{CC2PS}	CKE & CLK ≦ V_{IL}(max), t_{CC} = ∞	1	1	1		
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≧ V_{IH}(min), CS ≧ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	20	20	20	mA	
	I_{CC2NS}	CKE ≧ V_{IH}(min), CLK ≦ V_{IL}(max), t_{CC} = ∞ Input signals are stable	15	15	15		
Active Standby Current in power-down mode	I_{CC3P}	CKE ≦ V_{IL}(max), t_{CC} = 10ns	10	10	10	mA	
	I_{CC3PS}	CKE & CLK ≦ V_{IL}(max), t_{CC} = ∞	10	10	10		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≧ V_{IH}(min), CS ≧ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	30	25	20	mA	
	I_{CC3NS}	CKE ≧ V_{IH}(min), CLK ≦ V_{IL}(max), t_{CC} = ∞ Input signals are stable	10	10	10		
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	100	90	80	mA	1
Refresh Current	I_{CC5}	$t_{ARFC} \geq t_{ARFC}$(min)	150	130	110	mA	2
Self Refresh Current	I_{CC6}	CKE ≦ 0.2V	1.5	1.5	1.5	mA	

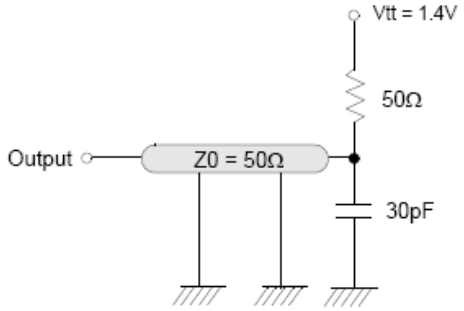
NOTES:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V, T_A = 0 to 70° C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	Ns
Output timing measurement reference level	1.4	V
Output load condition	See Figure 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-5	-6	-7		
Row active to row active delay	t_{RRD}(min)	10	12	14	ns	1
RAS to CAS delay	t_{RCD}(min)	15	18	21	ns	1
Row precharge time	t_{RP}(min)	15	18	21	ns	1
Row active time	t_{RAS}(min)	40	40	42	ns	1
	t_{RAS}(max)	100	100	100	us	
Row cycle time	t_{RC}(min)	50	58	63	ns	1
Last data in to row precharge	t_{RDL}(min)	2	2	2	CLK	2
Last data in to Active delay	t_{DAL}(min)	6	5	5	CLK-	
Last data in to new col. address delay	t_{CDL}(min)	1	1	1	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	1	1	CLK	2
Auto refresh cycle time	t_{ARFC}(min)	50	60	70	ns	

NOTES:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-6		-7		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	$t_{CC(3)}$	5		6		7		ns	1
	CAS latency=2	$t_{CC(2)}$	10		10		10			
CLK to valid output delay	CAS latency=3	$t_{SAC(3)}$		4.5		4.5		4.5	ns	1,2
	CAS latency=2	$t_{SAC(2)}$				4.5		4.5		
Output data hold time	CAS latency=3	$t_{OH(3)}$	2		2		2		ns	2
	CAS latency=2	$t_{OH(2)}$			2		2			
CLK high pulse width		t_{CH}	2		2.5		2.5		ns	3
CLK low pulse width		t_{CL}	2		2.5		2.5		ns	3
Input setup time		t_{SS}			1.5		1.5		ns	3
Input hold time		t_{SH}			1		1		ns	3
CLK to output in Low-Z		t_{SLZ}			1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		4.5		4.5		4.5	ns	
	CAS latency=2					4.5		4.5		

NOTES :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

TRUTH TABLE

Command Truth Table

COMMAND	Symbol	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	BA1	BA0	A10/ AP	A11, A9 ~ A0
Device deselect	DSL	H	X	H	X	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X	X
Burst stop	BST	H	X	L	H	H	L	X	X	X	X
Read	RD	H	X	L	H	L	H	V	V	L	V
Read with auto precharge	RDA	H	X	L	H	L	H	V	V	H	V
Write	WR	H	X	L	H	L	L	V	V	L	V
Write with auto precharge	WRA	H	X	L	H	L	L	V	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	L	X
Extended mode register set	EMRS	H	X	L	L	L	L	H	L	L	V

(V=Valid, X=Don´ t Care, H=Logic High, L=Logic Low)

CKE Truth Table

Current state	Function	Symbol	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	/Address
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend mode		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	Auto refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SREF	H	L	L	L	L	H	X
Idle	Power down entry	PD	H	L	L	H	H	H	X
			H	L	H	X	X	X	X
Idle	Deep power down entry	DPD	H	L	L	H	H	L	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Power down	Power down exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Deep power down	Deep power down exit		L	H	X	X	X	X	X

(V=Valid, X=Don´ t Care, H=Logic High, L=Logic Low)

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	/Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	Row activating	
	L	L	H	L	BA,A10	PRE/PALL	NOP	
	L	L	L	H	X	REF	Auto refresh	
	L	L	L	L	OC,BA1=L	MRS	Mode register set	
	L	L	L	L	OC,BA1=H	EMRS	Extended mode register set	
Row active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA,CA,A10	RD/RDA	Begin read	2
	L	H	L	L	BA,CA,A10	WR/WRA	Begin write	2
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Precharge / Precharge all banks	3
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA	MRS / EMRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	RD/RDA	Terminate burst,begin new read	4
	L	H	L	L	BA,CA,A10	WR/WRA	Terminate burst,begin write	4,5
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Terminate burst → Precharging	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	RD/RDA	Terminate burst, start read : Determine AP	4,5
	L	H	L	L	BA,CA,A10	WR/WRA	Terminate burst,new write : Determine AP	4
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Terminate burst → Precharging	6
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Write recovering	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	/Address	Command	Action	Notes
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after tRP	
	L	H	H	H	X	NOP	Nop → Enter idle after tRP	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA	MRS/EMRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	X	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1,7
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA	MRS / EMRS	ILLEGAL	
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	X	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	X	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA,CA,A10	RD/RDA	Begin read	5
	L	H	L	L	BA,CA,A10	WR/WRA	Begin new write	
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DESL	Nop → Enter precharge after tDPL	
	L	H	H	H	X	NOP	Nop → Enter precharge after tDPL	
	L	H	H	L	X	BST	Nop → Enter precharge after tDPL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1,5
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Refresh	H	X	X	X	X	DESL	Nop → Enter idle after tRC1	
	L	H	H	H	X	NOP	Nop → Enter idle after tRC1	
	L	H	H	L	X	BST	Nop → Enter idle after tRC1	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Mode register accessing	H	X	X	X	X	DESL	Nop → Enter idle after tRSC	
	L	H	H	H	X	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	X	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	MODE	MRS	ILLEGAL	

Notes: 1. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Illegal if tRCD is not satisfied.
3. Illegal if tRAS is not satisfied.
4. Must satisfy burst interrupt condition.
5. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
6. Must mask preceding data which don't satisfy tDPL.
7. Illegal if tRRD is not satisfied

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1	A11 ~ A10/AP	A9*2	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU*1	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

B. POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
- Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

C. BURST SEQUENCE

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE=SEQUENTIAL	TYPE=INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	N=A0 – A8 (location 0 – y)	Cn, Cn+1, Cn+2, Cn+3, Cn+4..., …Cn-1, Cn…	Not Supported

NOTE:
1. For full-page accesses: y = 512.
2. For a burst length of two, A1–A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A8 select the block-of-four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A8 select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0–A8 select the unique column to be accessed, and mode register bit M3 is ignored.

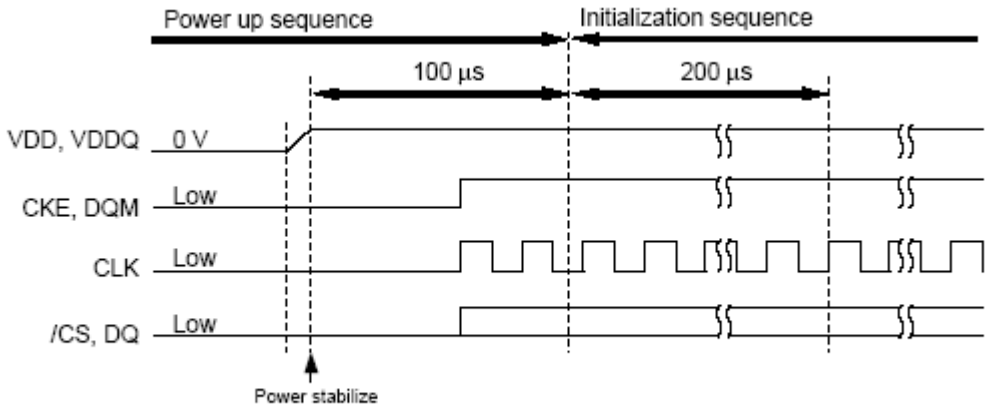
Power-up sequence

Power-up sequence

The SDRAM should be goes on the following sequence with power up.
The CLK, CKE, /CS, DQM and DQ pins keep low till power stabilizes.
The CLK pin is stabilized within 100 µs after power stabilizes before the following initialization sequence.
The CKE and DQM is driven to high between power stabilizes and the initialization sequence.
This SDRAM has VDD clamp diodes for CLK, CKE, address, /RAS, /CAS, /WE, /CS, DQM and DQ pins. If the sepins go high before power up, the large current flows from these pins to VDD through the diodes.

Initialization sequence

When 200 µs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After tRP delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQM and CKE to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.



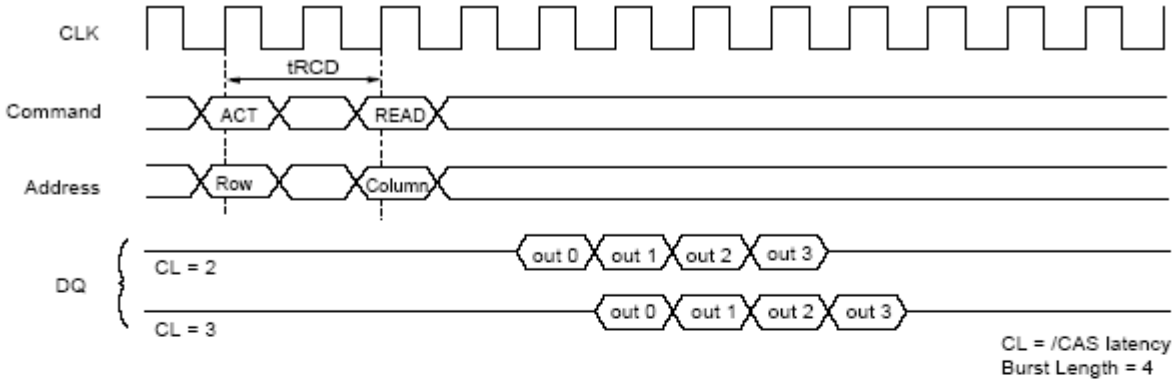
Power-up sequence and Initialization sequence

Operation of the SDRAM

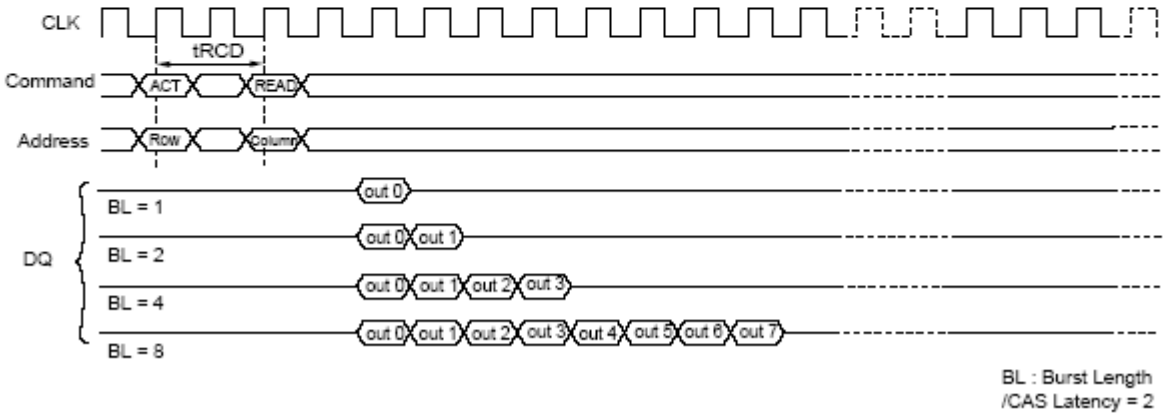
Read/Write Operations

Bank active
Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

Read operation
A read operation starts when a read command is input. Output buffer becomes Low-Z in the (/CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the /CAS Latency. The /CAS Latency can be set to 2 or 3.
When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.
The /CAS latency and burst length must be specified at the mode register.



/CAS Latency



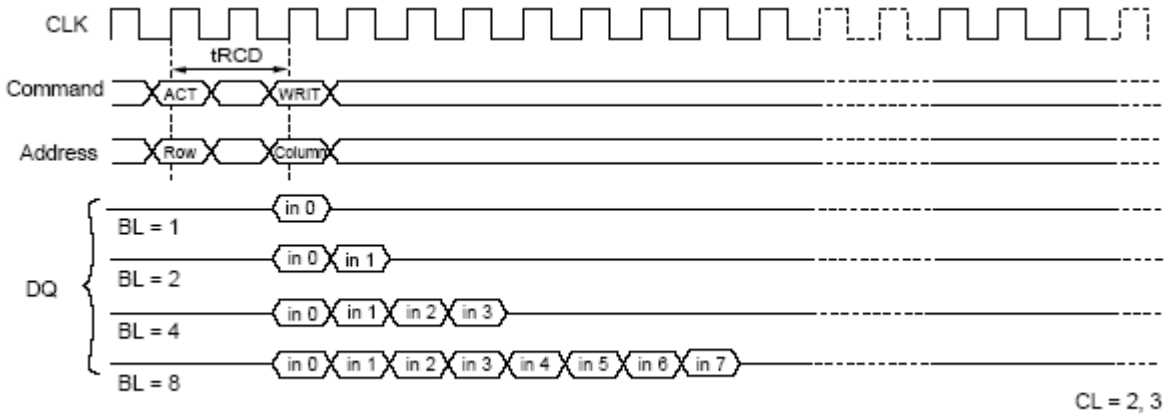
Burst Length

Write operation

Burst write or single write mode is selected

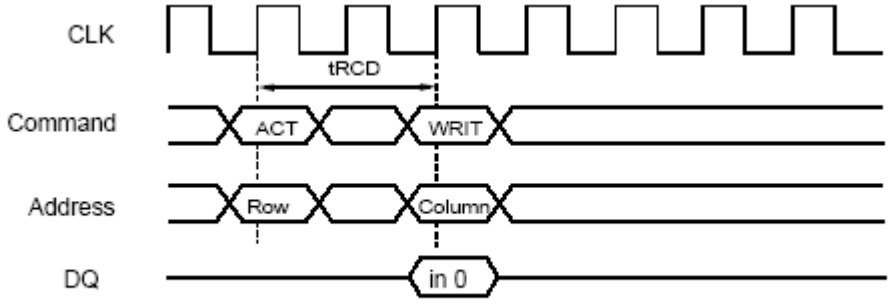
1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4 and 8, like burst read operations. The write start address is specified by the column address and the bank select address at the write command set cycle.

.



Burst write

2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock).



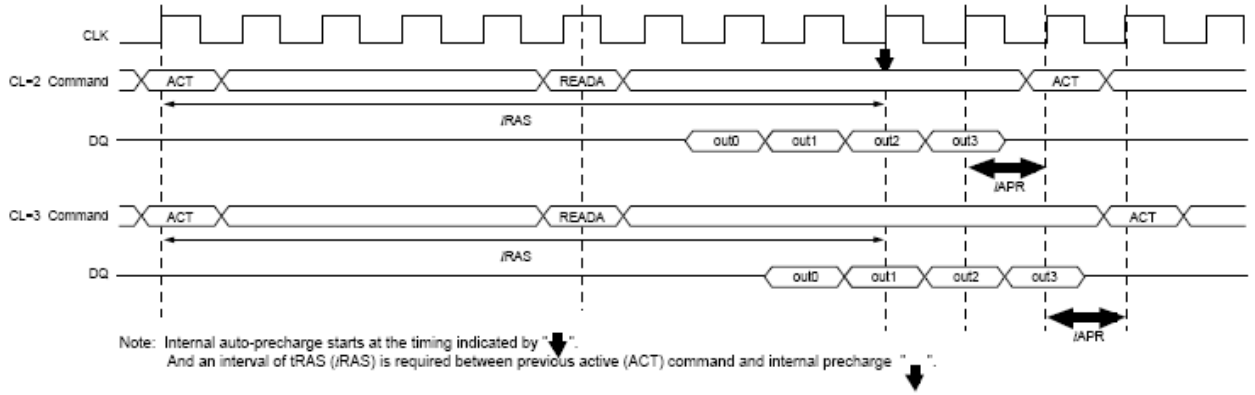
Single write

Auto Precharge

Read with auto-precharge
In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval defined by *l*APR is required before execution of the next command.

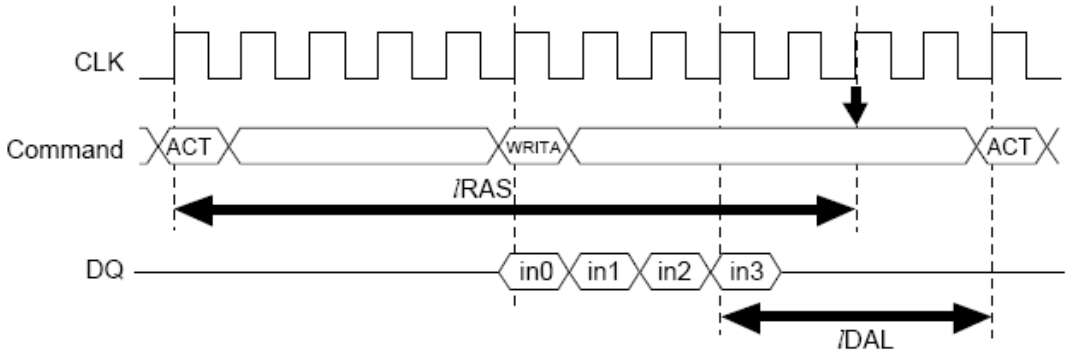
[Clock cycle time]

/CAS latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output



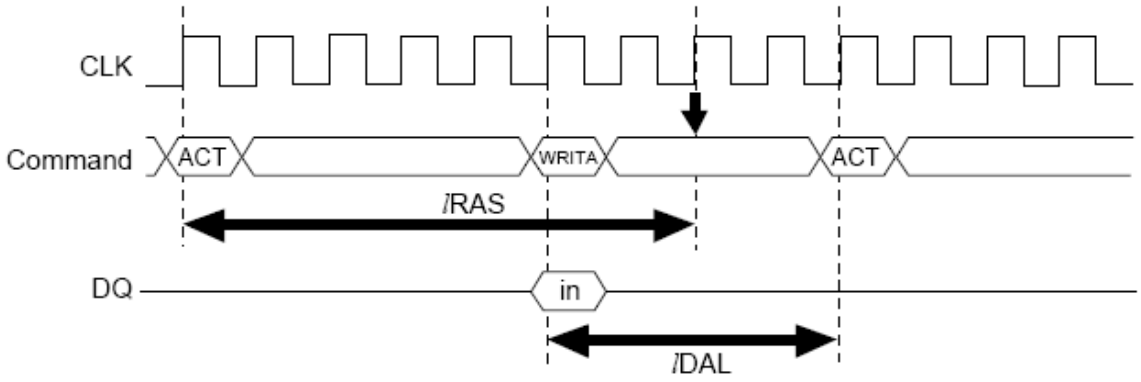
Burst Read (BL = 4)

Write with auto-precharge
In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval of *l*DAL is required between the final valid data input and input of next command.



Note: Internal auto-precharge starts at the timing indicated by "▼".
and an interval of tRAS (*l*RAS) is required between previous active (ACT) command and internal precharge "▼".

Burst Write (BL = 4)

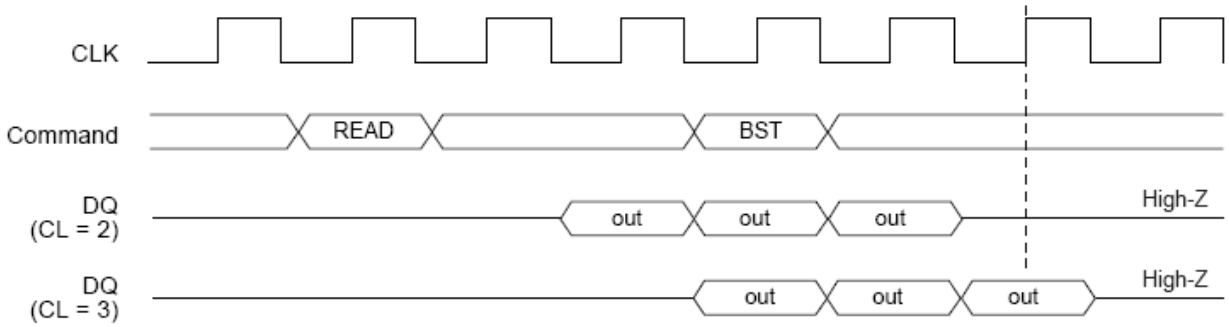


Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (tRAS) is required between previous active (ACT) command
and internal precharge "↓".

Single Write

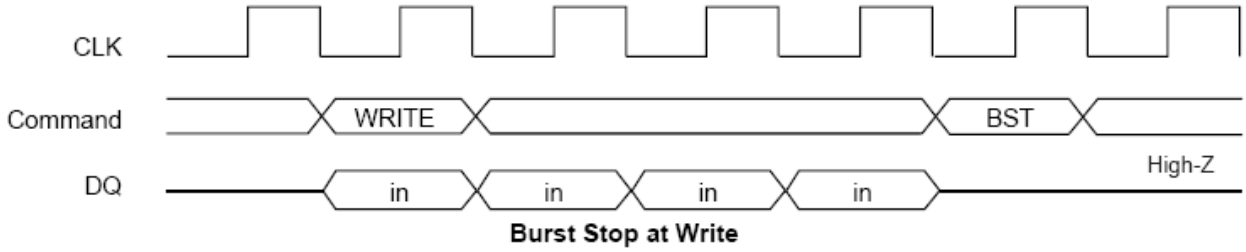
Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.



Burst Stop at Read

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.

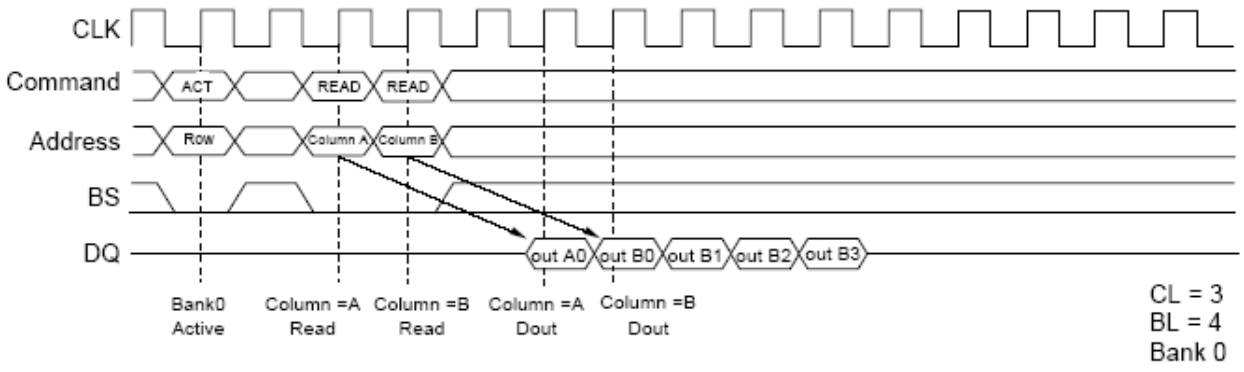


Burst Stop at Write

Command Intervals

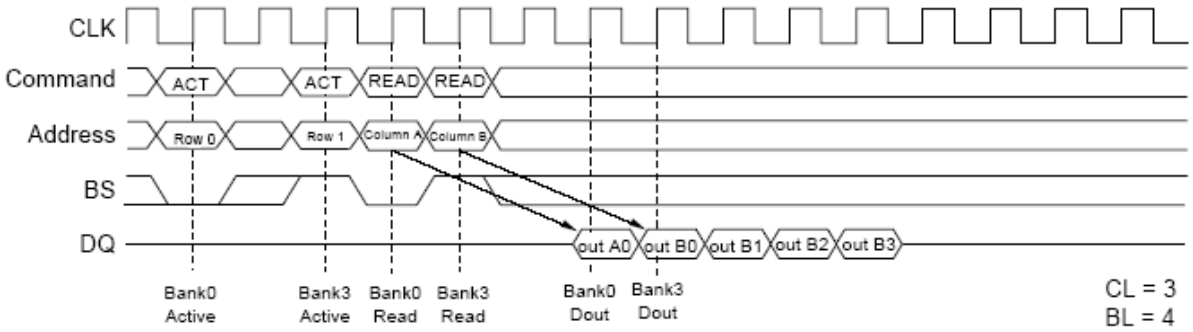
Read command to Read command interval

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (same ROW address in same bank)

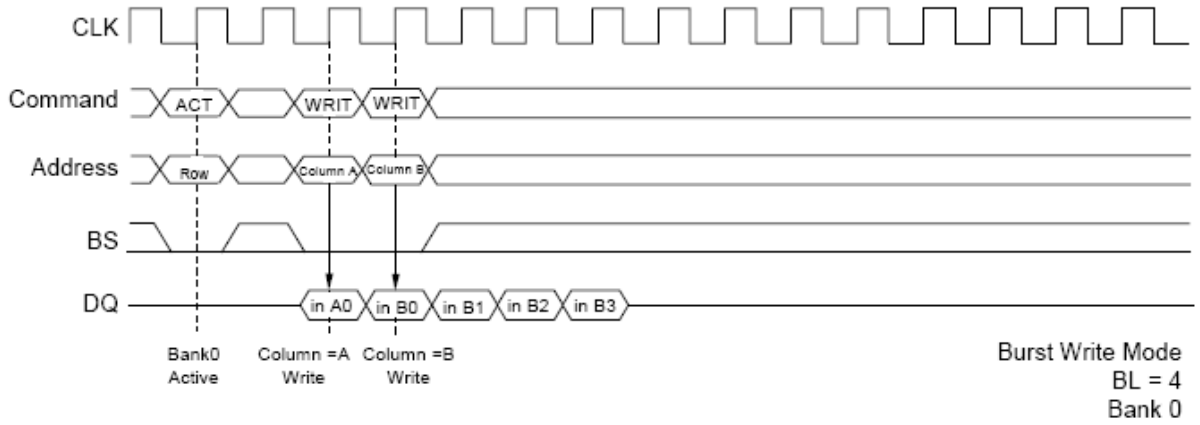
2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (different bank)

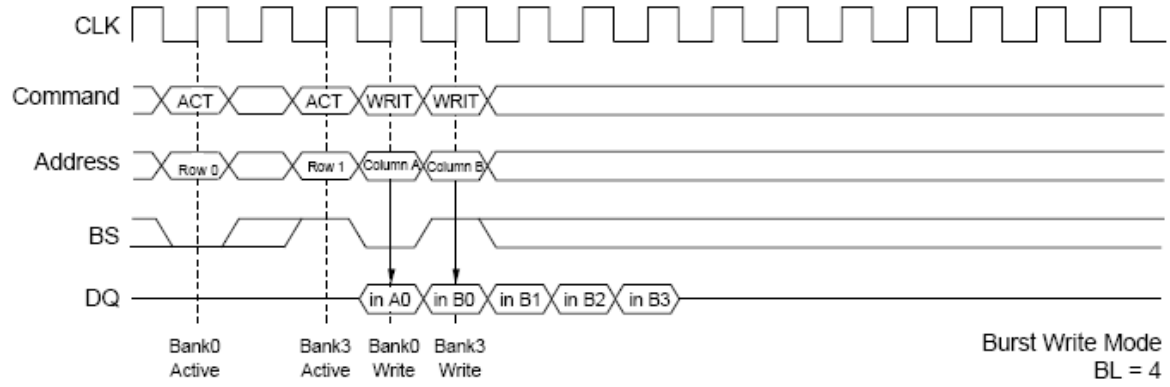
Write command to Write command interval

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.



WRITE to WRITE Command Interval (same ROW address in same bank)

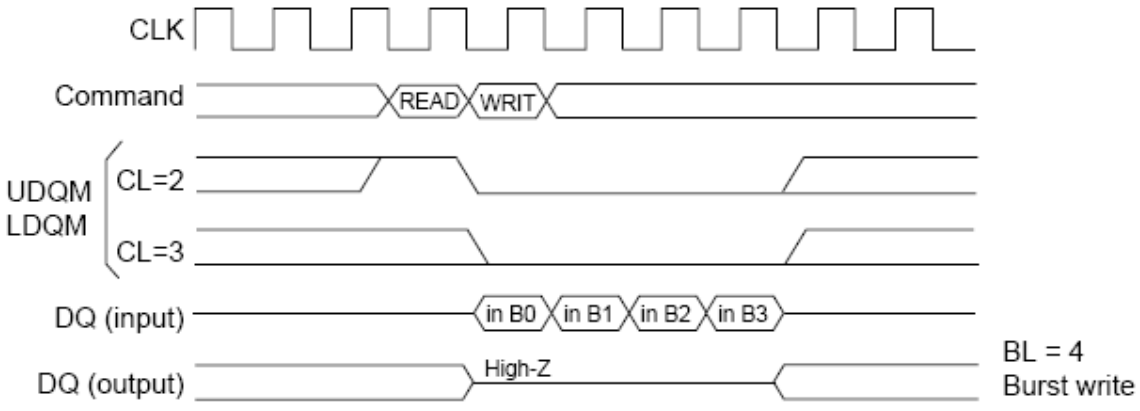
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.



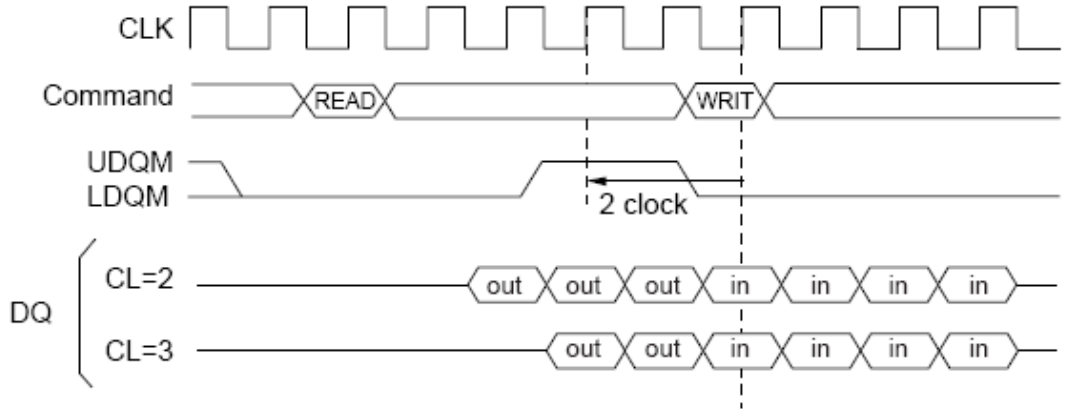
WRITE to WRITE Command Interval (different bank)

Read command to Write command interval

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input.



READ to WRITE Command Interval (1)

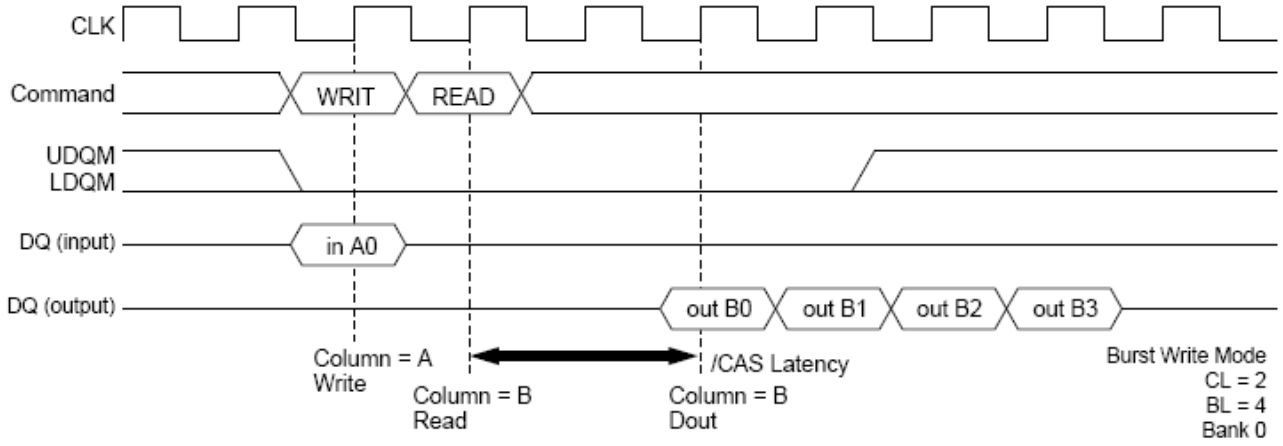


READ to WRITE Command Interval (2)

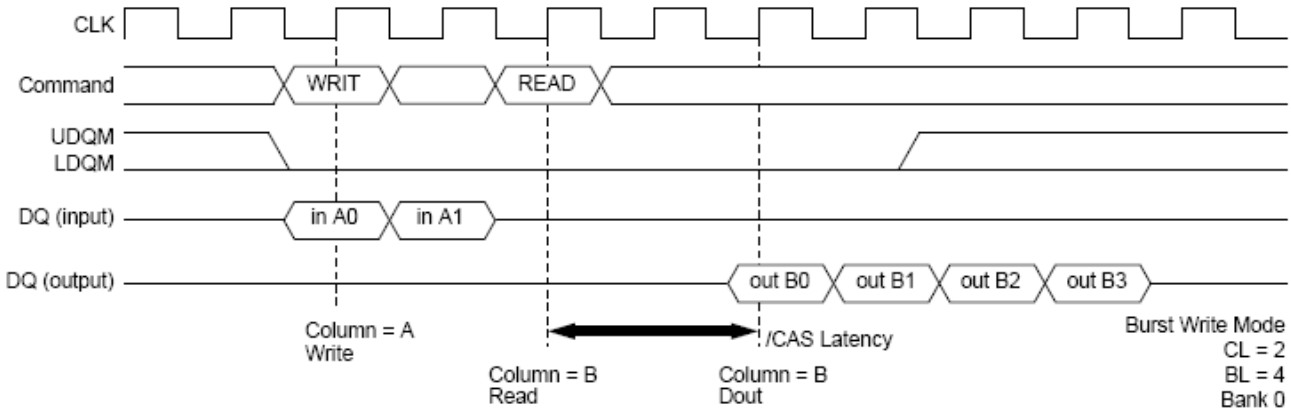
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input.

Write command to Read command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.



WRITE to READ Command Interval (1)

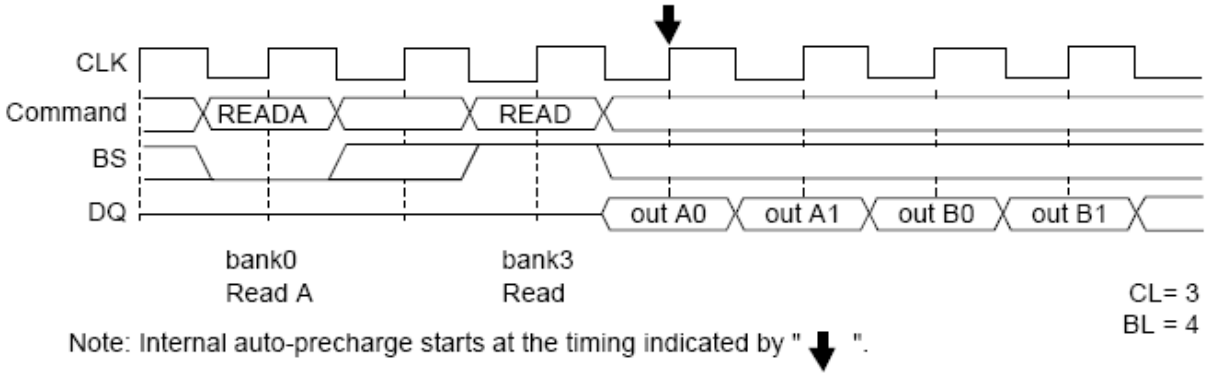


WRITE to READ Command Interval (2)

2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

Read with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the next clock of the second command.

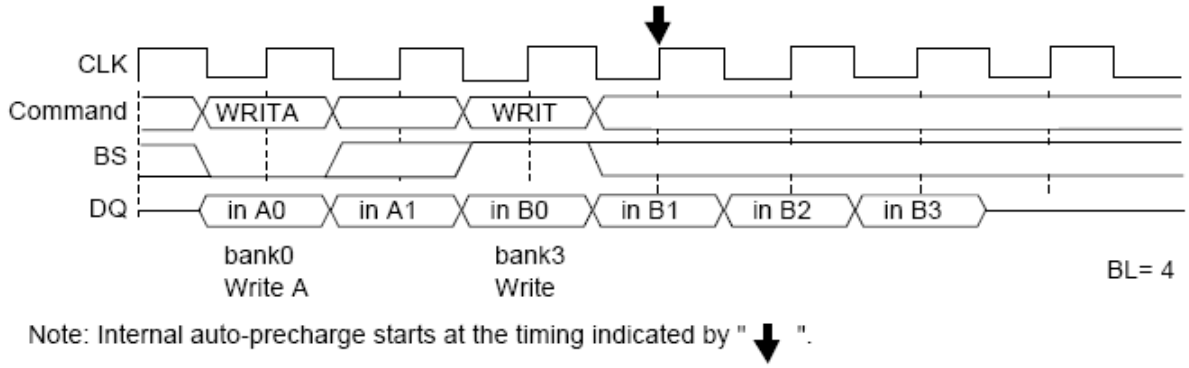


Read with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command (the same bank) is illegal.

Write with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts 2 clocks later from the second command.

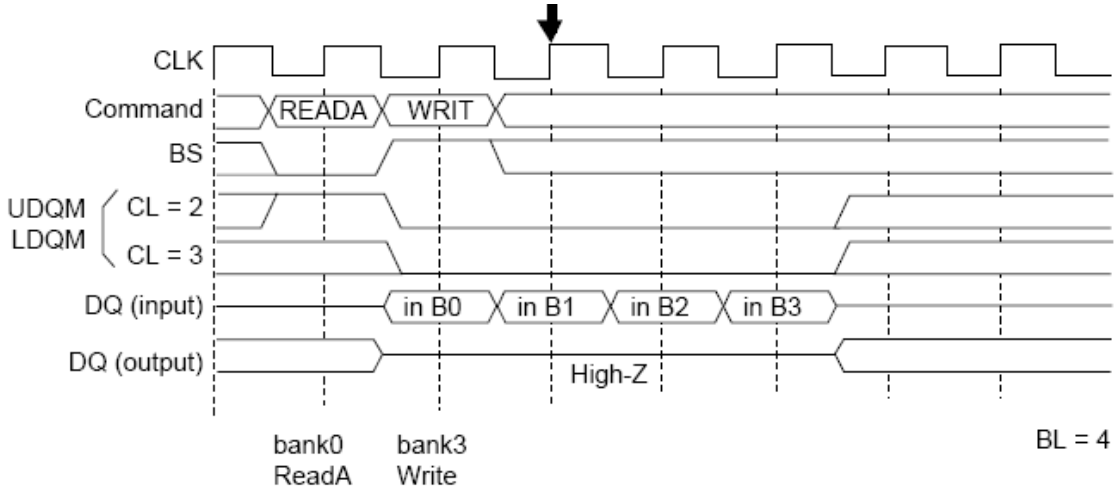


Write with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command (the same bank) is illegal.

Read with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.



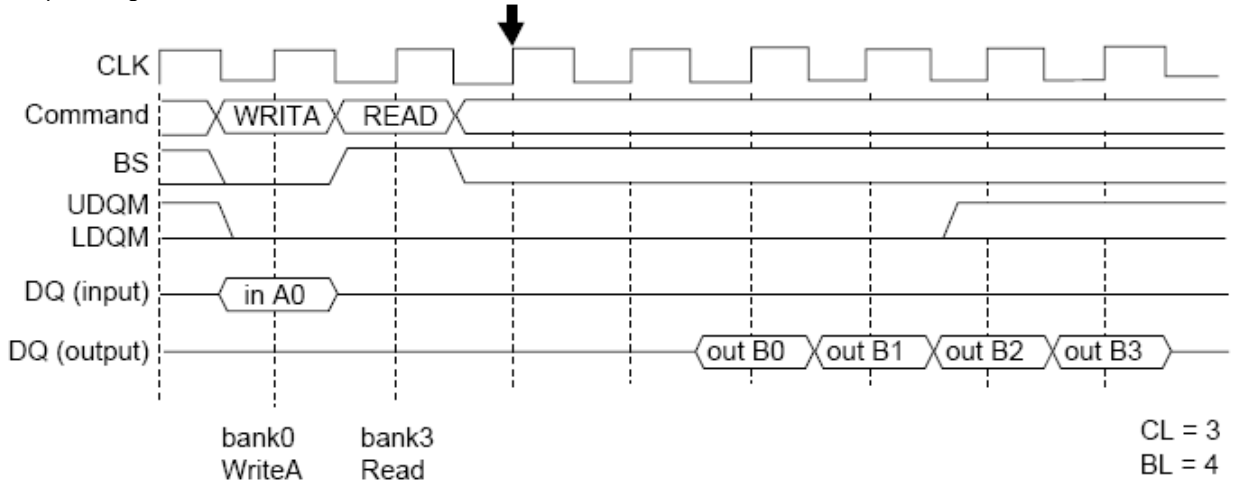
Note: Internal auto-precharge starts at the timing indicated by " ".

Read with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Write with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at 2 clocks later from the second command.

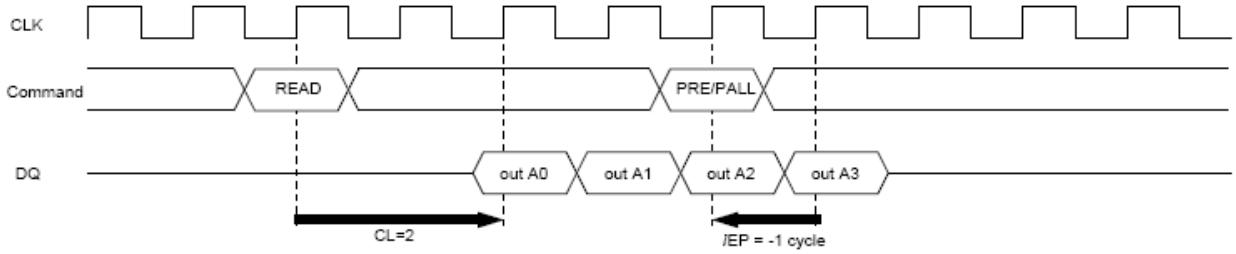


Note: Internal auto-precharge starts at the timing indicated by " ".

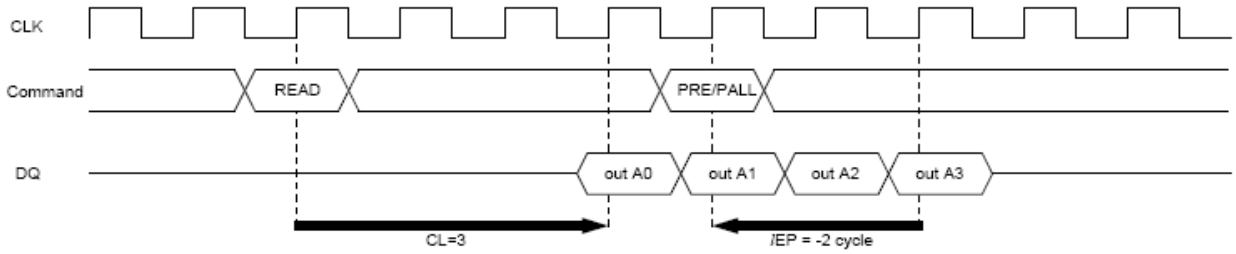
Write with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

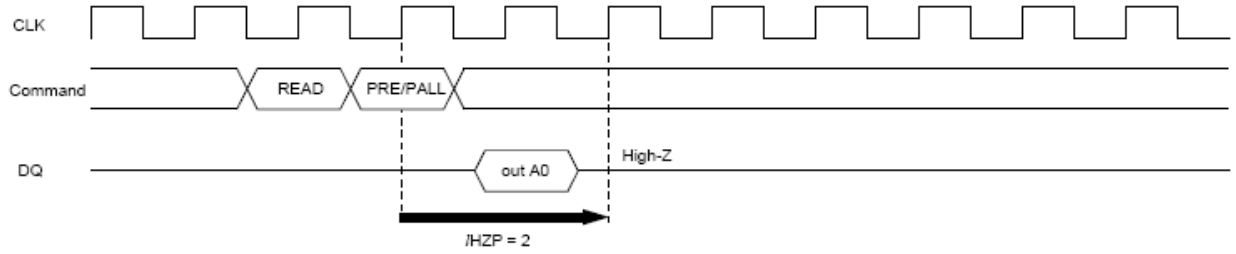
Read command to Precharge command interval (same bank)
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by *I*HZP, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by *I*EP must be assured as an interval from the final data output to precharge command execution.



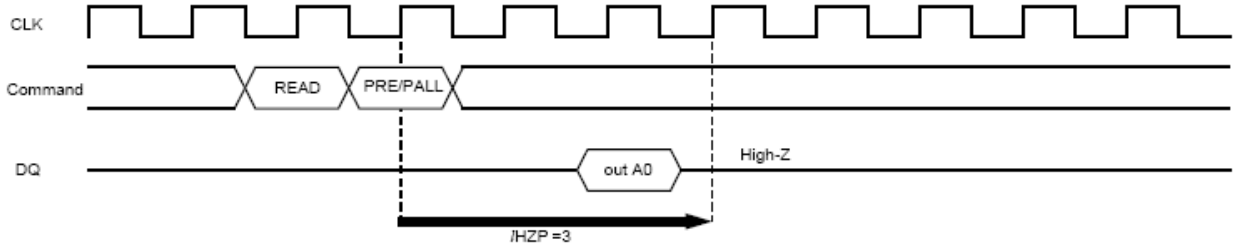
READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2, BL = 4)



READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)

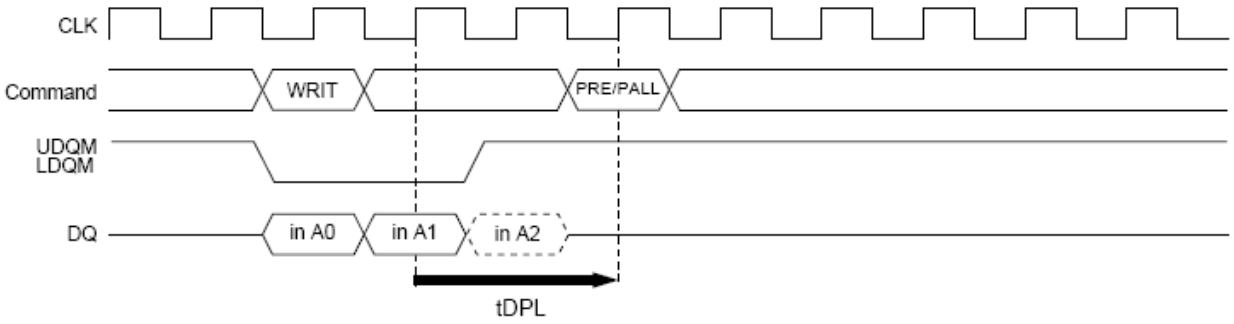


READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2, BL = 1, 2, 4, 8)

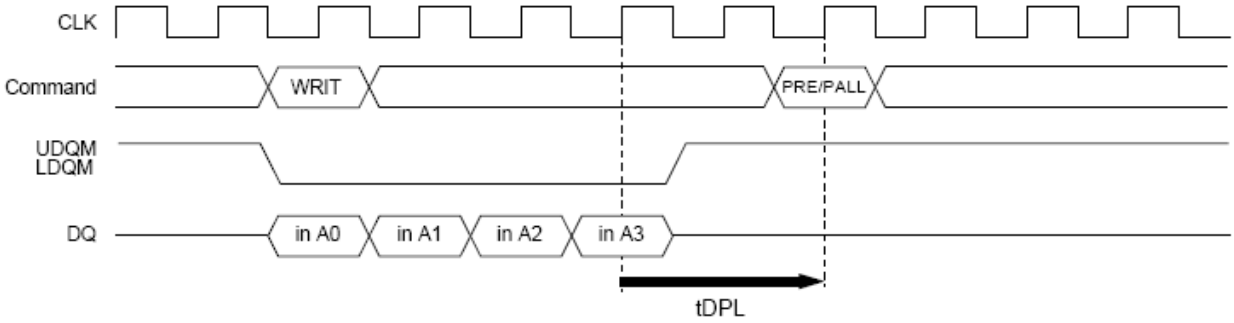


READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 1, 2, 4, 8)

Write command to Precharge command interval (same bank)
When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of UDQM and LDQM for assurance of the clock defined by tDPL.



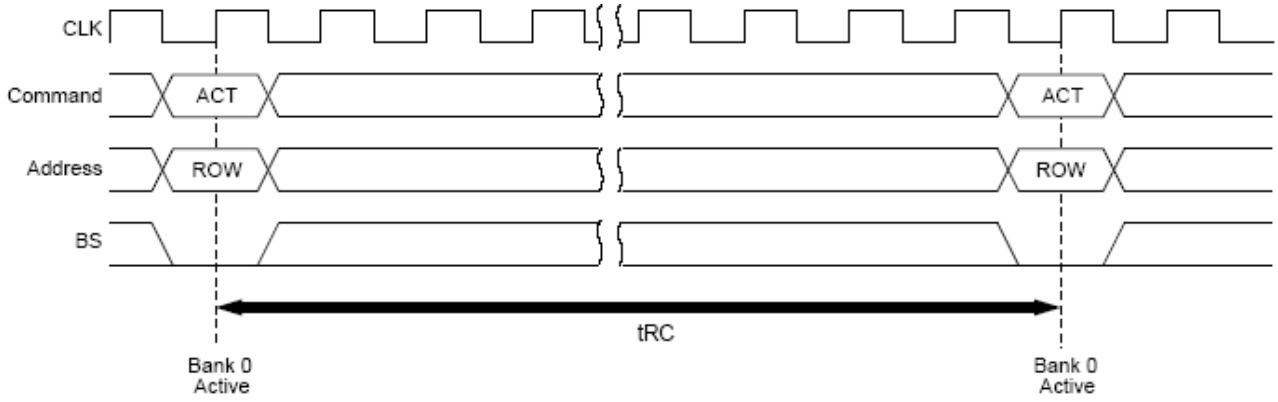
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To stop write operation))



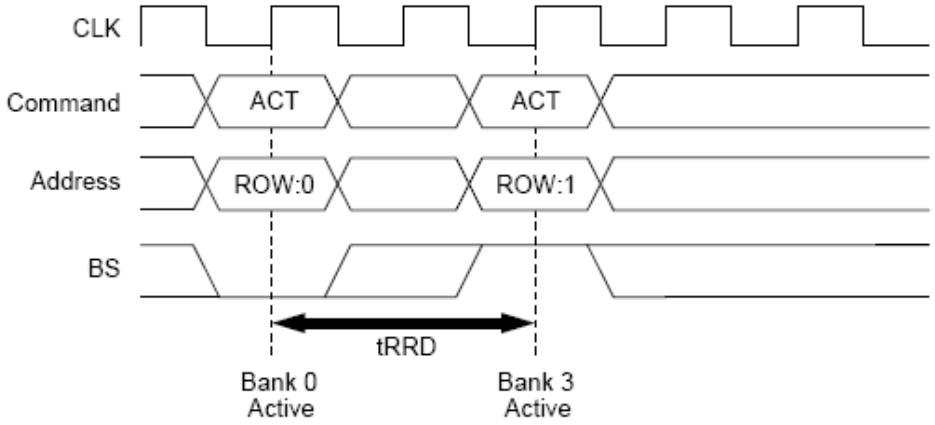
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To write all data))

Bank active command interval

1. Same bank: The interval between the two bank active commands must be no less than tRC.
2. In the case of different bank active commands: The interval between the two bank active commands must be no less than tRRD.



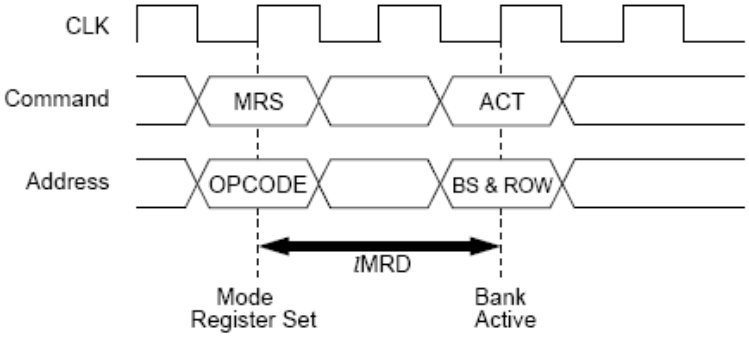
Bank Active to Bank Active for Same Bank



Bank Active to Bank Active for Different Bank

Mode register set to Bank active command interval

The interval between setting the mode register and executing a bank active command must be no less than *l*MRD.

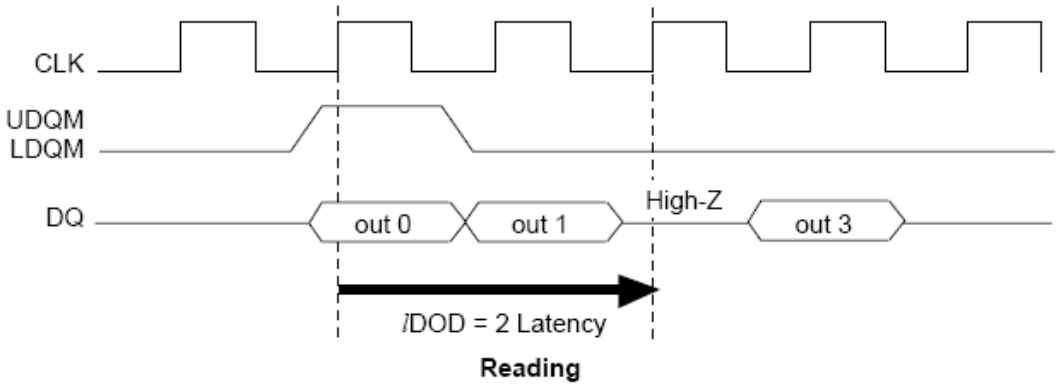


Mode register set to Bank active command interval

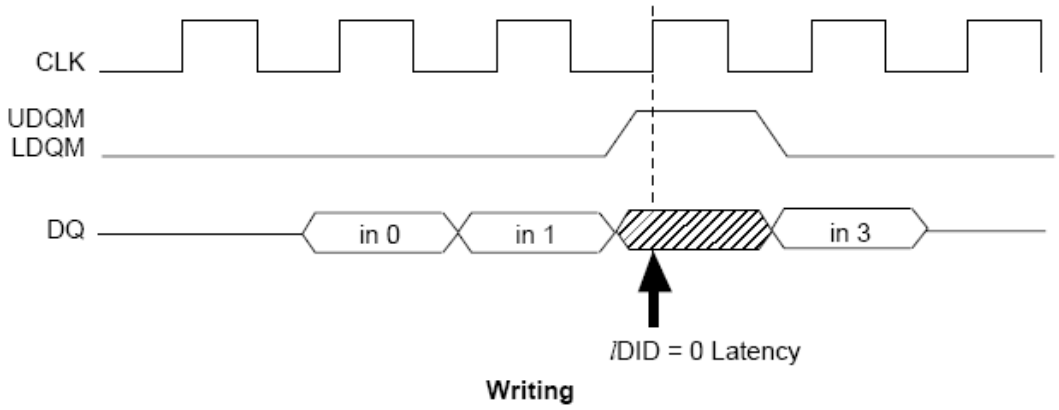
DQM Control
The UDQM and LDQM mask the upper and lower bytes of the DQ data, respectively. The timing of UDQM and LDQM is different during reading and writing.

Reading
When data is read, the output buffer can be controlled by UDQM and LDQM. By setting UDQM and LDQM to Low, the output buffer becomes Low-Z, enabling data output. By setting UDQM and LDQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of UDQM and LDQM during reading is 2 clocks.

Writing
Input data can be masked by UDQM and LDQM. By setting DQM to Low, data can be written. In addition, when UDQM and LDQM are set to High, the corresponding data is not written, and the previous data is held. The latency of UDQM and LDQM during writing is 0 clock.



Reading



Writing

Refresh

Auto-refresh
All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycles are required to refresh all the ROW addresses within tREF (max.). The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh
After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During selfrefresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF (max.) period on the condition 1 and 2 below.
1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below*after exiting from self-refresh mode.

Note: tREF (max.) / refresh cycles.

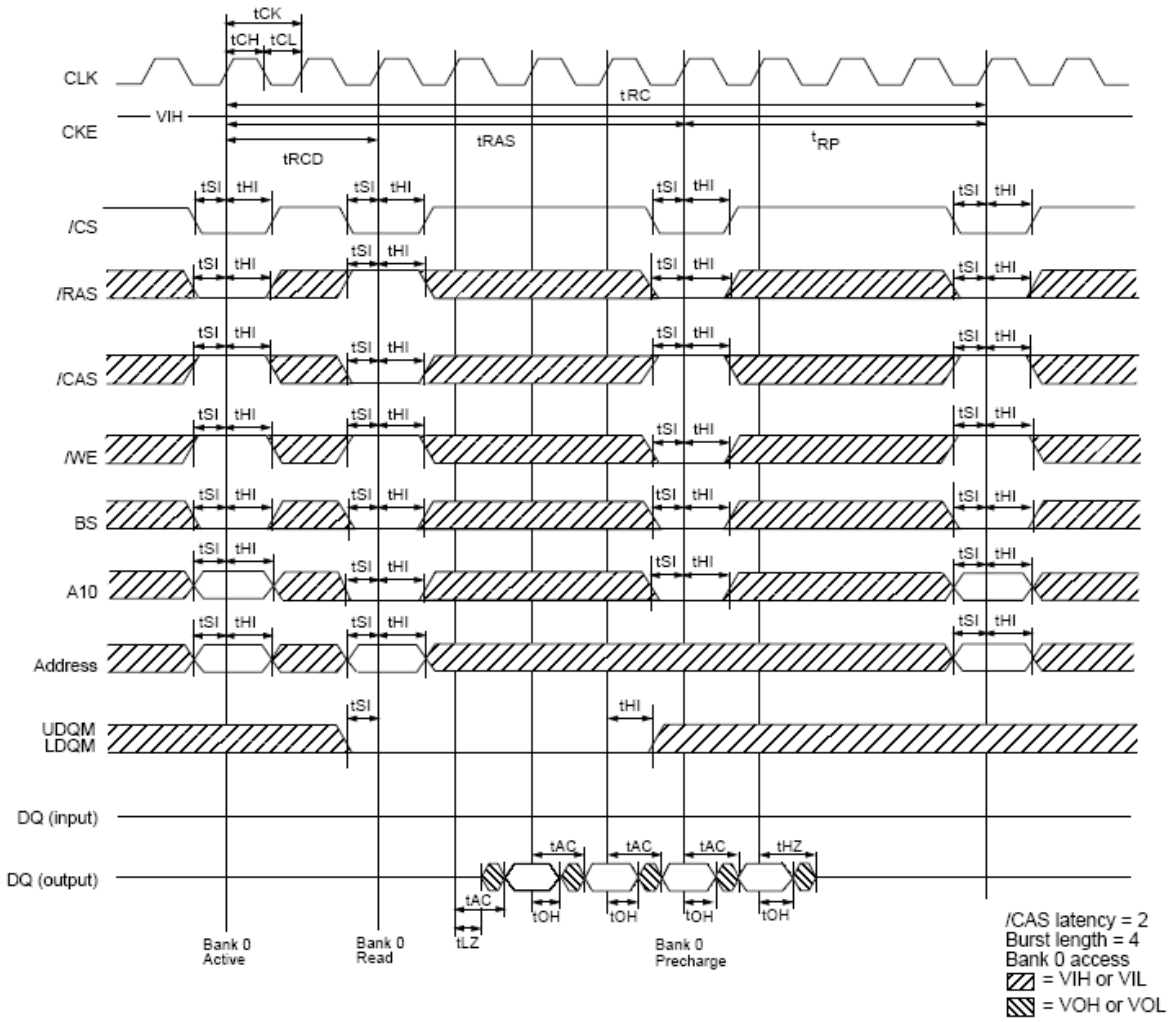
Others

Power-down mode
The SDRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

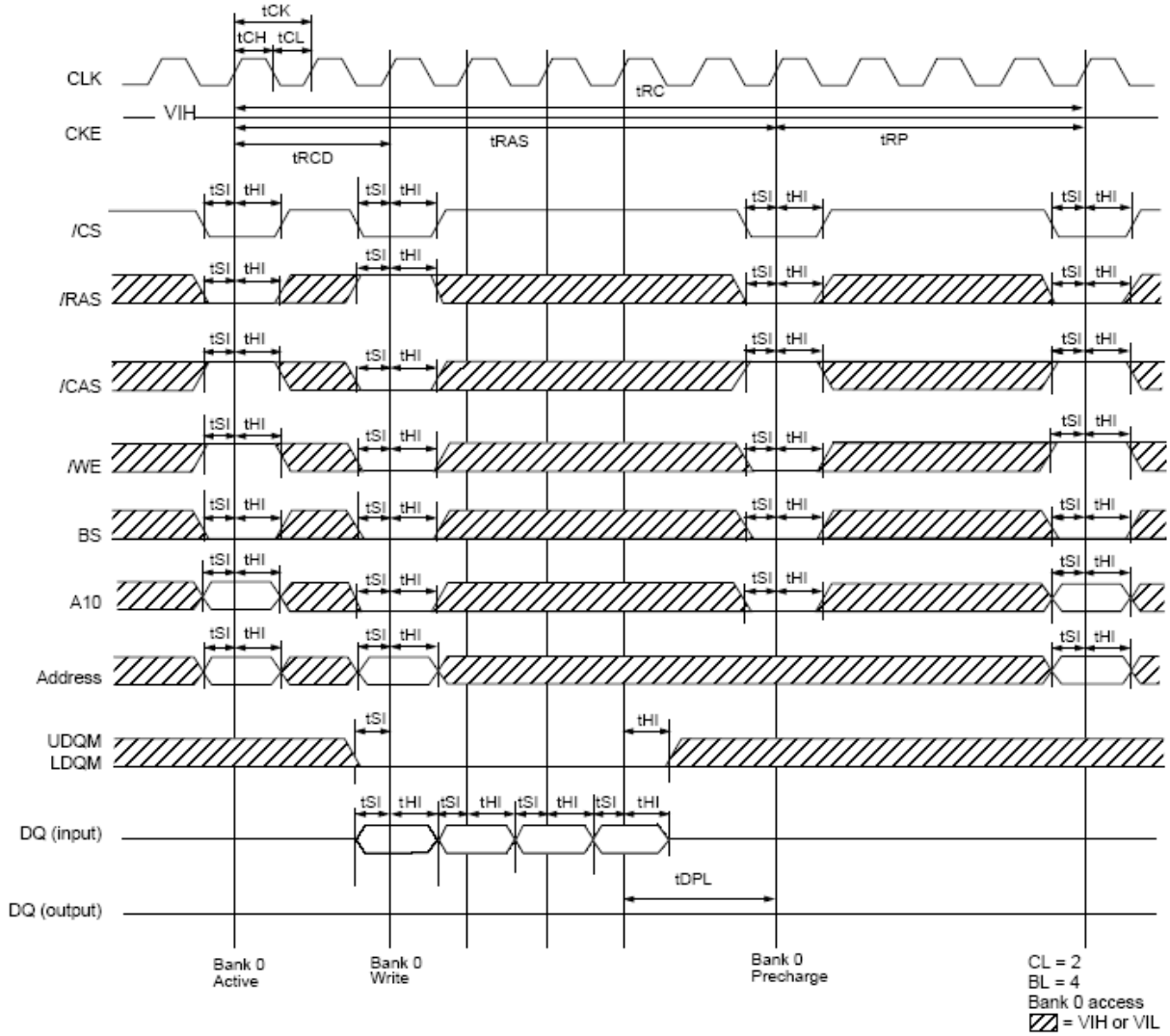
Clock suspend mode
By driving CKE to Low during a bank active or read/write operation, the SDRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

Timing Waveforms

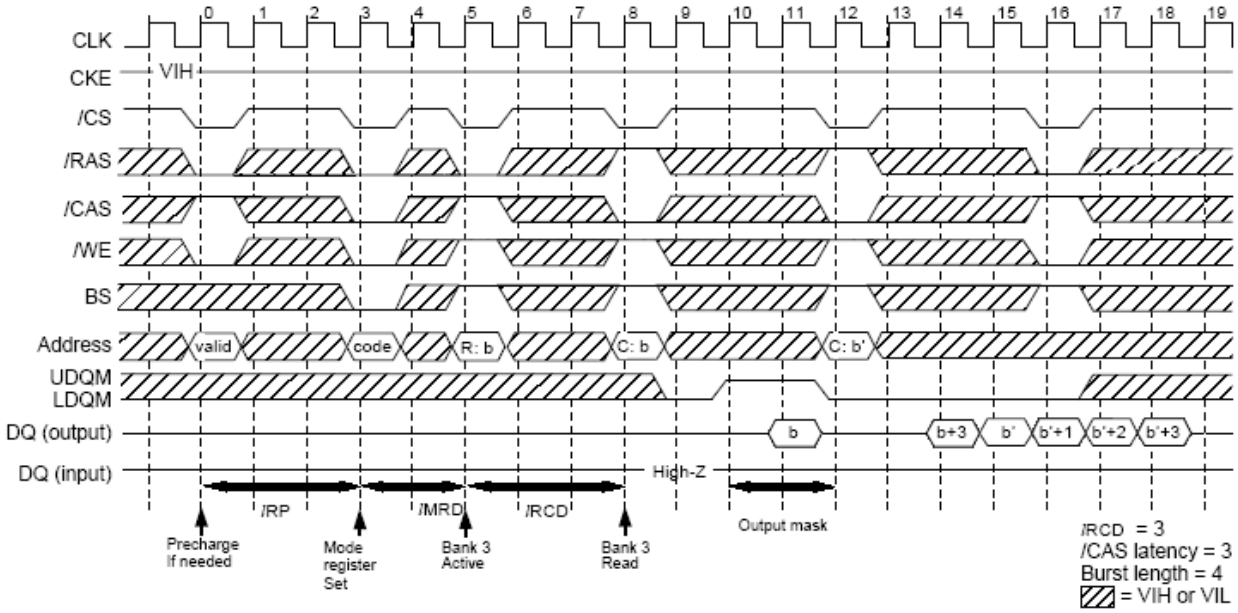
Read Cycle



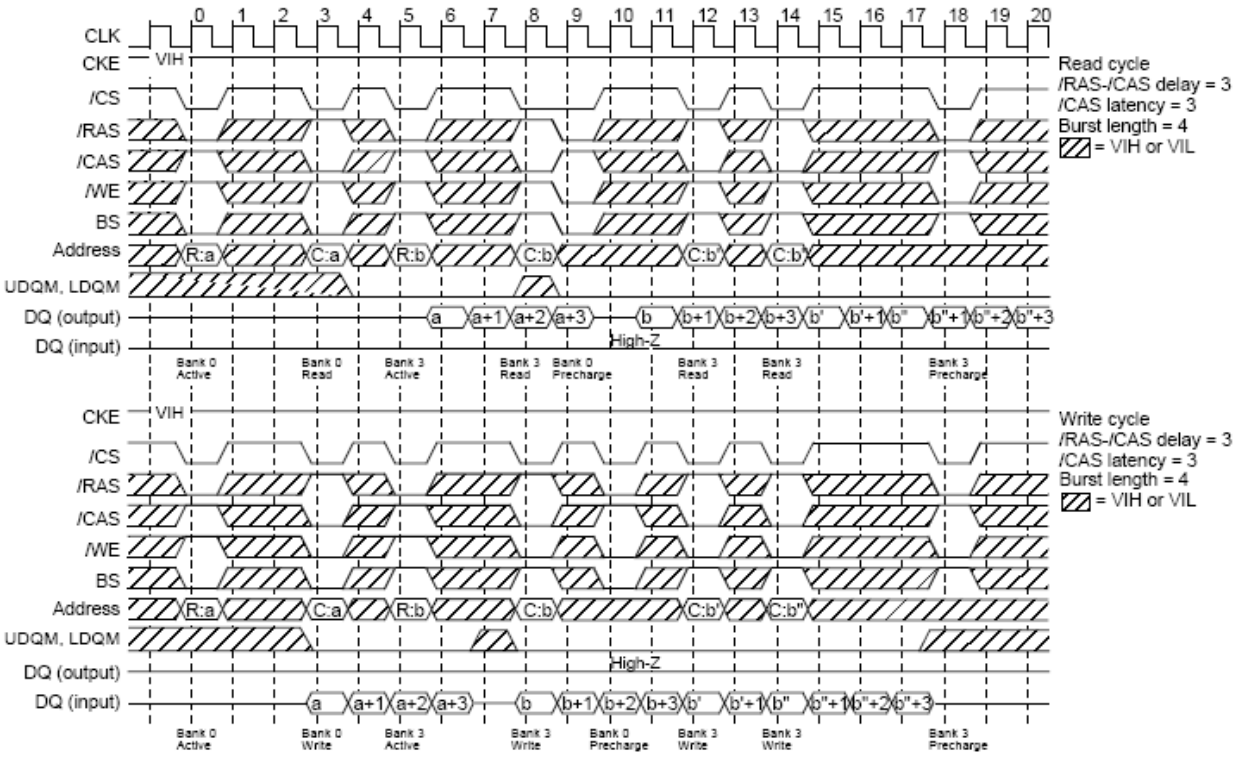
Write Cycle


tCK
tCH
tCL
CLK
VIH
CKE
tRC
tRAS
tRP
tRCD
tSI
tHI
/CS
/RAS
/CAS
/WE
BS
A10
Address
UDQM
LDQM
DQ (input)
DQ (output)
tDPL
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CL = 2
BL = 4
Bank 0 access
= VIH or VIL

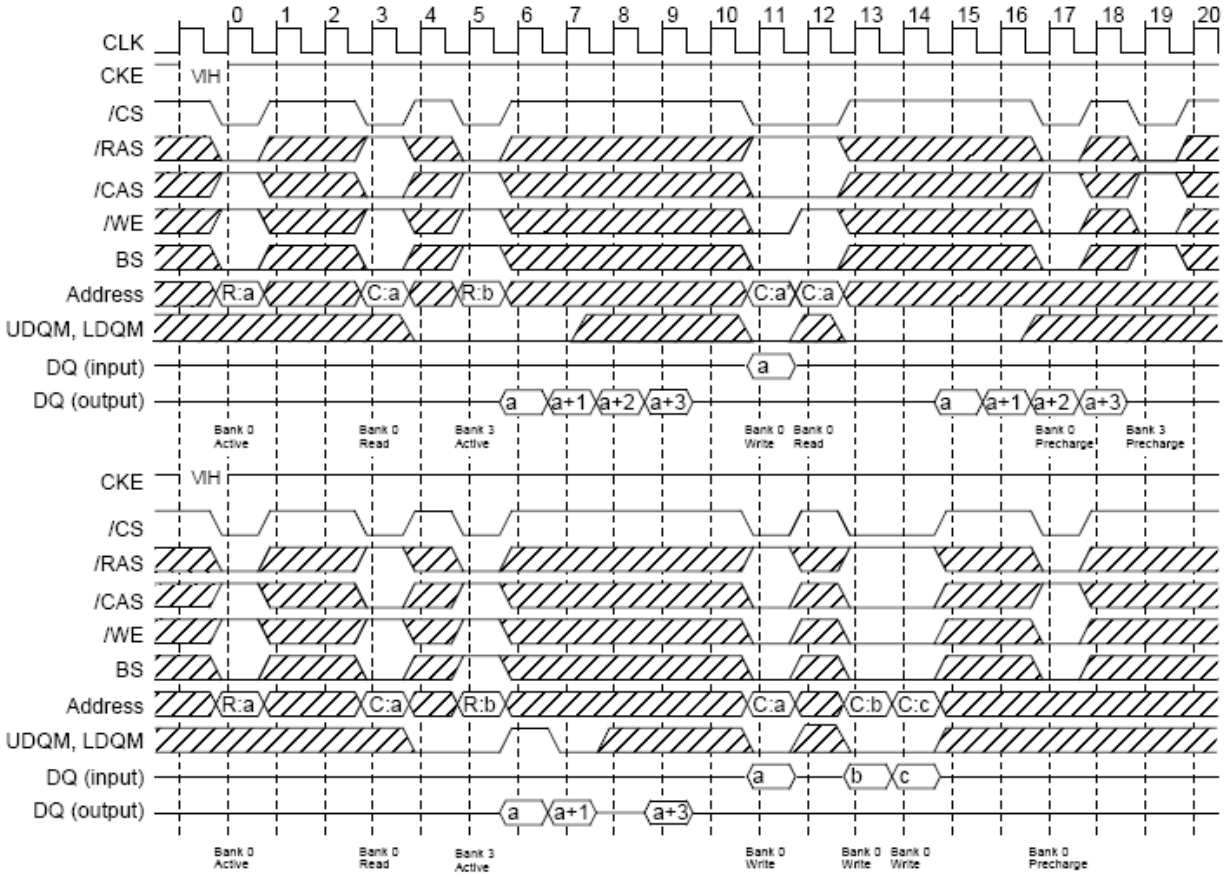
Mode Register Set Cycle



Read Cycle/Write Cycle

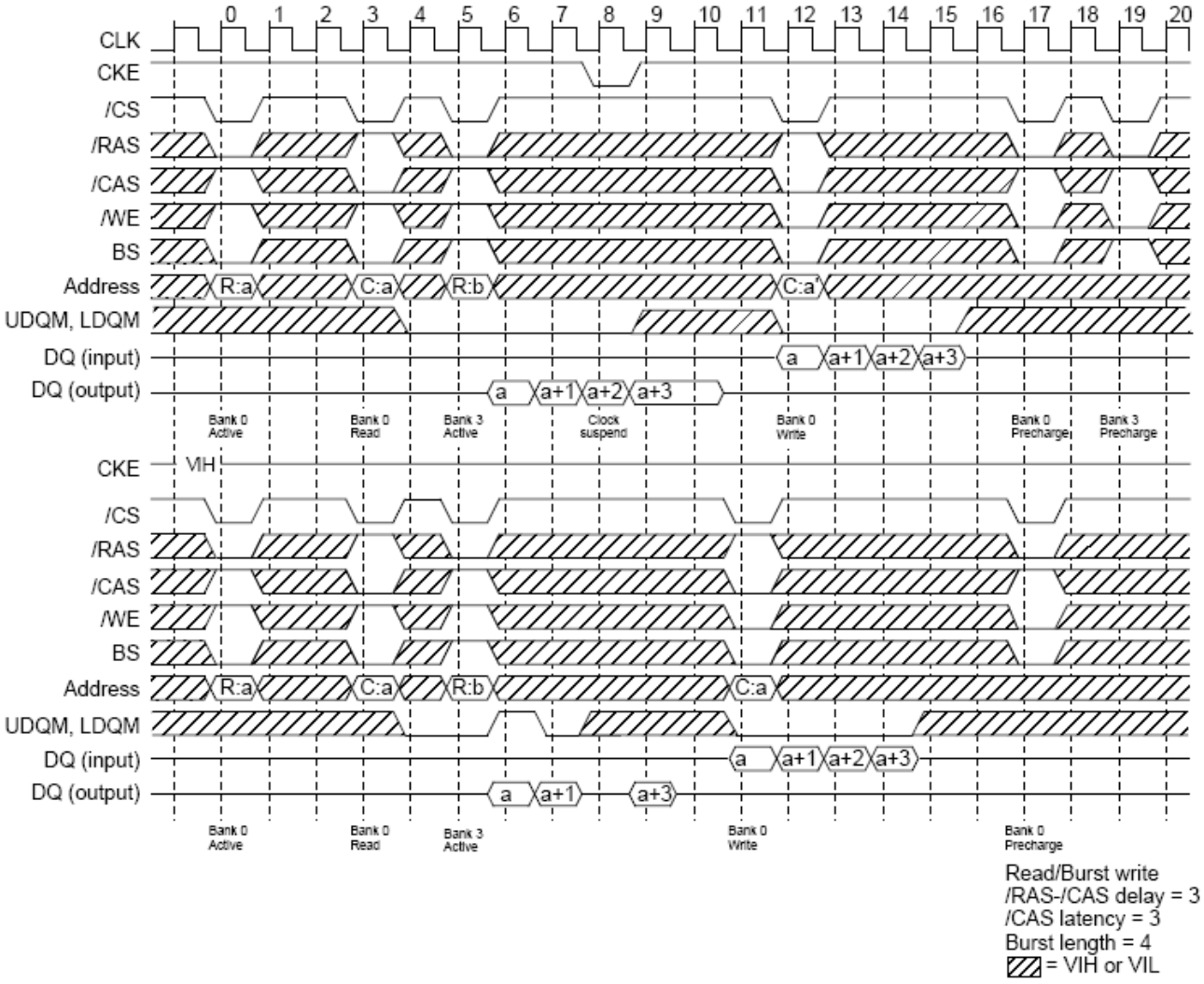


Read/Single Write Cycle

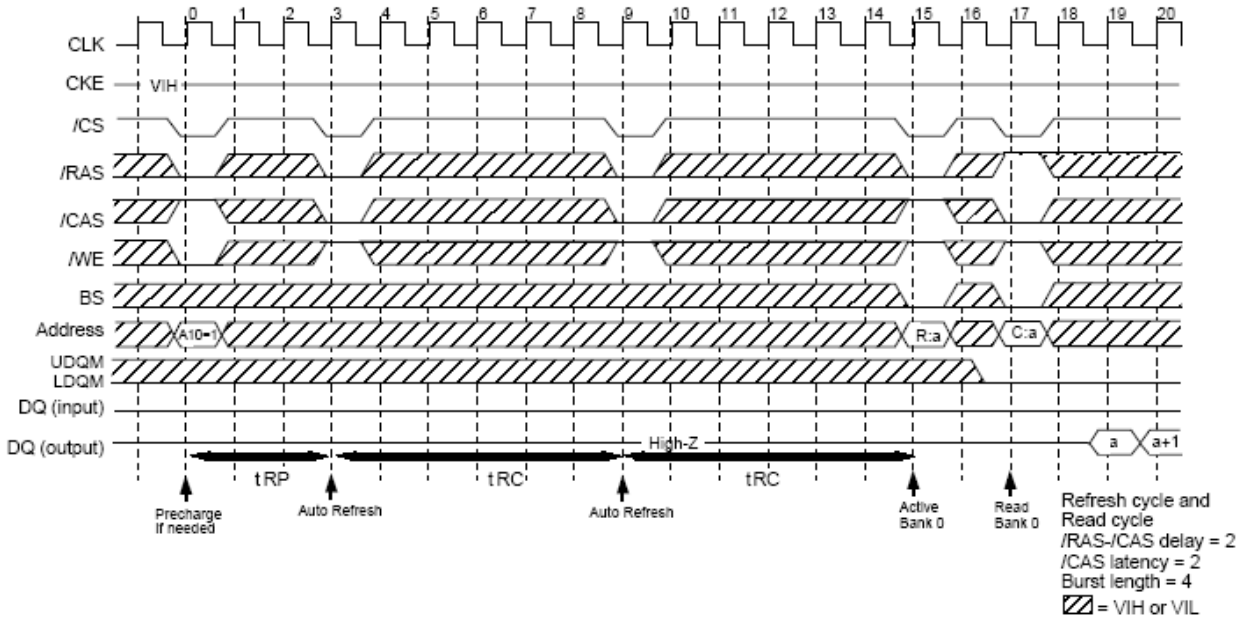


Read/Single write
/RAS-/CAS delay = 3
/CAS latency = 3
Burst length = 4
▨ = VIH or VIL

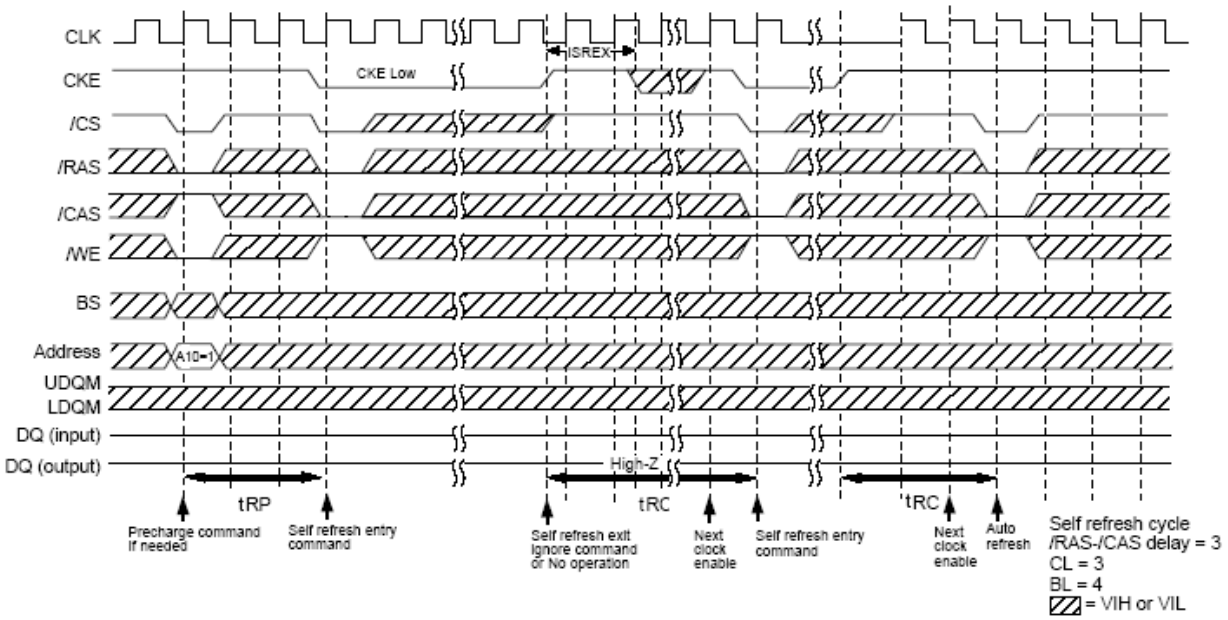
Read/Burst Write Cycle



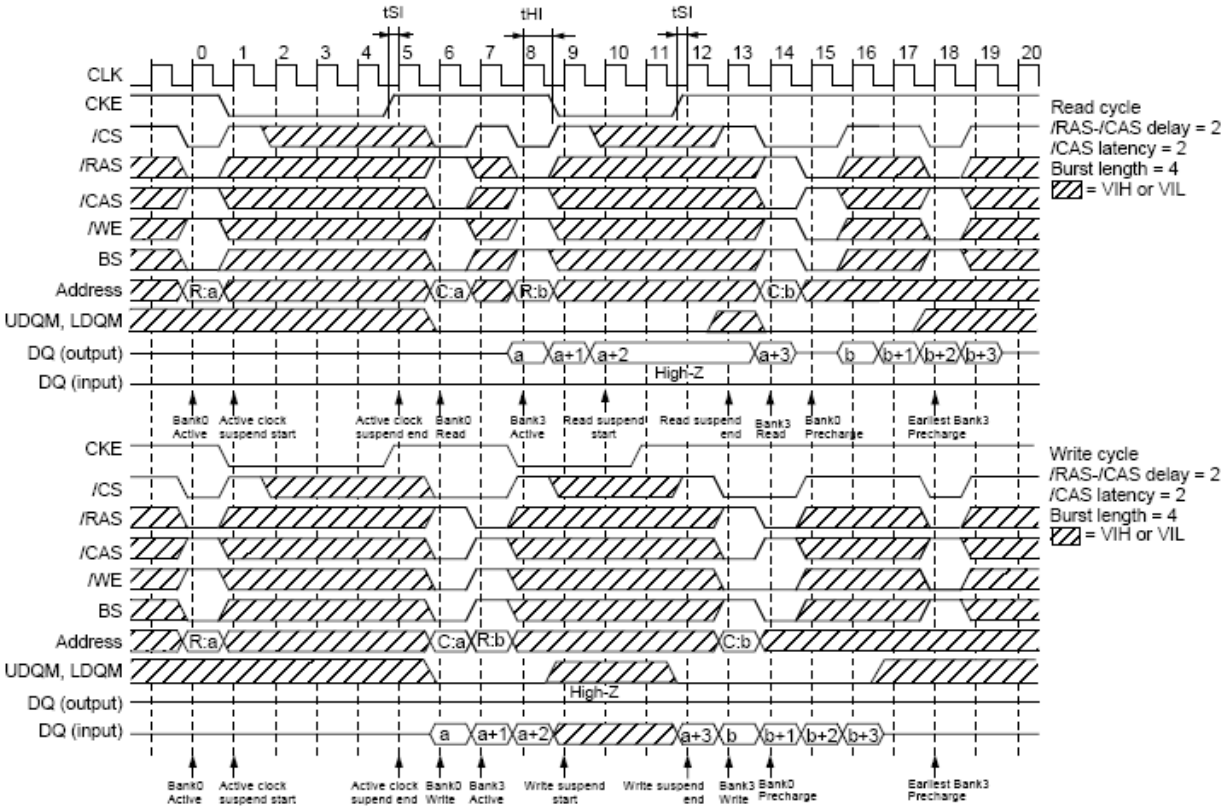
Auto Refresh Cycle



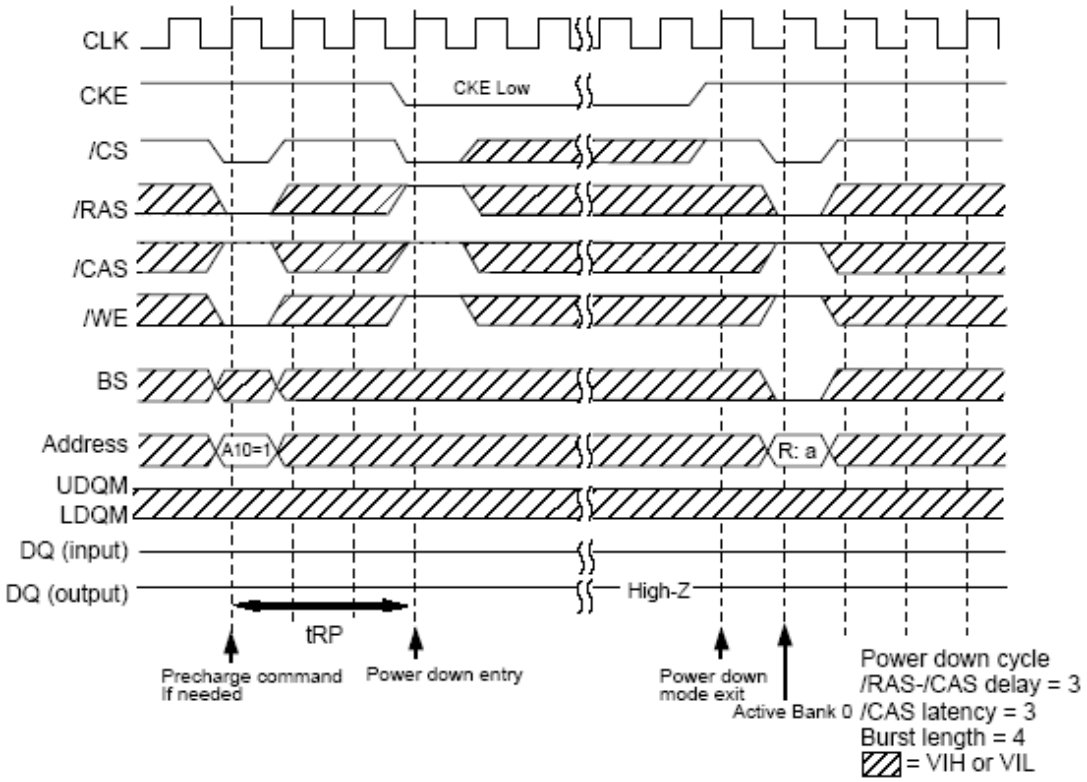
Self Refresh Cycle



Clock Suspend Mode



Power Down Mode



Initialization Sequence