LED Drivers for LCD Backlights

6ch boost LED driver which constant setting can be shared by I2C control

BD9423EFV

1.1 General Description

BD9423EFV is a high efficiency driver for white LEDs and designed for large LCD panel. This IC is built-in high current drive and high responsibility type 6ch LED drivers and 1ch boost DCDC converter. BD9423EFV has some protect function against fault conditions, such as the over-voltage protection (OVP), LED OPEN and SHORT protection, the over current limit protection of DCDC (OCP). Therefore BD9423EFV is available for the fail-safe design over a wide range output voltage.
Moreover the functions and the detection voltage can be controlled by the I2C. This enables for the constant setting of external parts to be shared by I2C control, nevertheless the different usage condition.

Features

- Operating power supply voltage range:9.0V to 35.0V
- Oscillator frequency: 200kHz (RT=100kΩ)
- Operating Current: 9mA (typ.)
- Operating temperature range: -40°C to +85°C

Applications

- TV, Computer Display, Notebook, LCD Backlighting

Key Specifications

- LED drivers Max curret 400mA per channel
- Constant current accuracy ±1.8% (IC only)
- Current analog (linear) dimming by ADIM pin
- Several protection functions
  DCDC part : OCP/OVP/UVLO
  LED driver part :OPEN,SHORT detection
- SHORT detection voltage is set by LSP pin
- Error detection output by FAIL pin
- Master/Slave mode inside

1.2 Package

	W(Typ) x D(Typ) x H(Max)
HTSSOP-B40:	13.60mm x 7.80mm x 1.00mm
Pin Pitch:	0.65mm

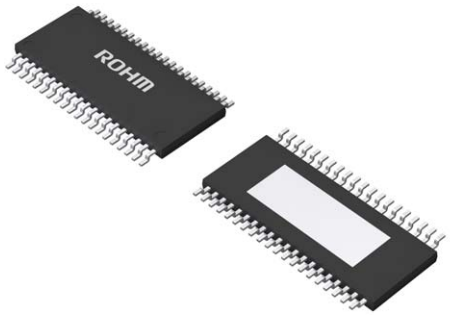


Figure 1. HTSSOP-B40

Typical Application Circuit

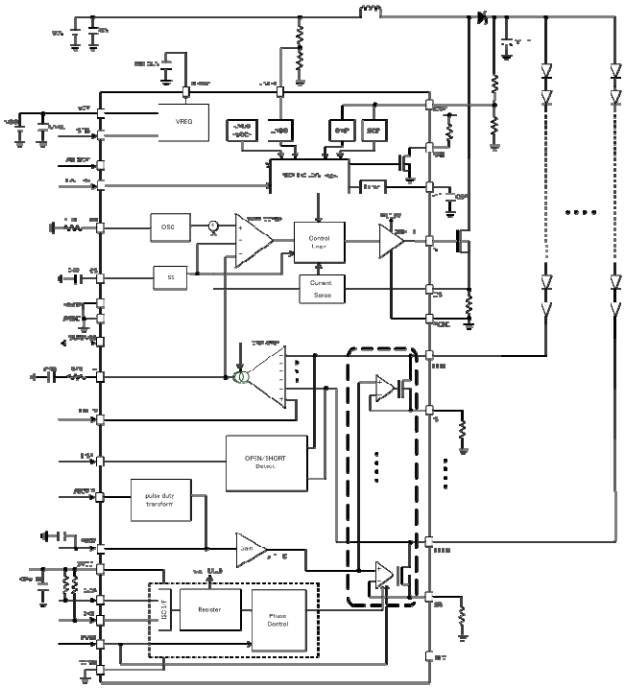


Figure 2. Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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1.3 Pin Configuration

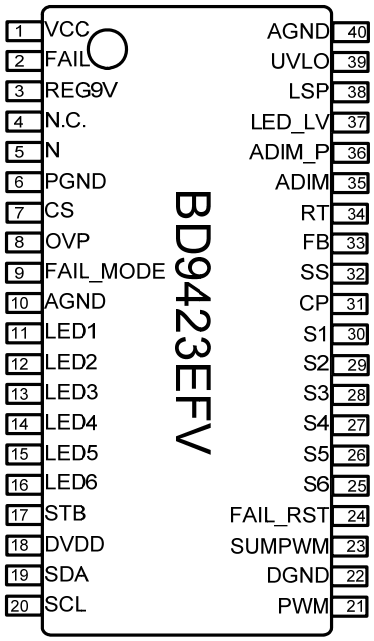


Figure 3. Pin Configuration

1.4 Pin Descriptions

No.	Name	Function	No.	Name	Function
1	VCC	Power supply pin	40	AGND	GND pin for analog part
2	FAIL	Abnormality detection output pin	39	UVLO	Low voltage malfunction detection pin
3	REG9V	9.0V regulator output pin	38	LSP	LED SHORT detection voltage setting pin
4	N.C.	-	37	LED_LV	LED feedback voltage setting pin
5	N	DC/DC switching output pin	36	ADIM_P	Pulse analog dimming signal input pin
6	PGND	Power GND pin	35	ADIM	Analog dimming DC voltage I/O pin
7	CS	DC/DC FET current detection pin	34	RT	Connecting pin for DC/DC frequency setting resistor
8	OVP	OVP detection pin	33	FB	Error AMP output pin
9	FAIL_MODE	FAIL function selection pin	32	SS	Connecting pin for soft start
10	AGND	GND pin for analog part	31	CP	setting capacitor
11	LED1	LED output 1	30	S1	Connecting pin for abnormality
12	LED2	LED output 2	29	S2	detection setting capacitor
13	LED3	LED output 3	28	S3	Connecting pin for LED1 constant current setting resistor
14	LED4	LED output 4	27	S4	Connecting pin for LED2 constant current setting resistor
15	LED5	LED output 5	26	S5	Connecting pin for LED3 constant current setting resistor
16	LED6	LED output 6	25	S6	Connecting pin for LED4 constant current setting resistor
17	STB	ON/OFF pin	24	FAIL_RST	Connecting pin for LED5 constant current setting resistor
18	DVDD	Power supply pin for I2C part and register	23	SUMPWM	Connecting pin for LED6 constant current setting resistor
19	SDA	I2C data pin	22	DGND	FAIL output reset pin
20	SCL	I2C Clock pin	21	PWM	Master/Slave setting input/output pin

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1.5 Block Diagram

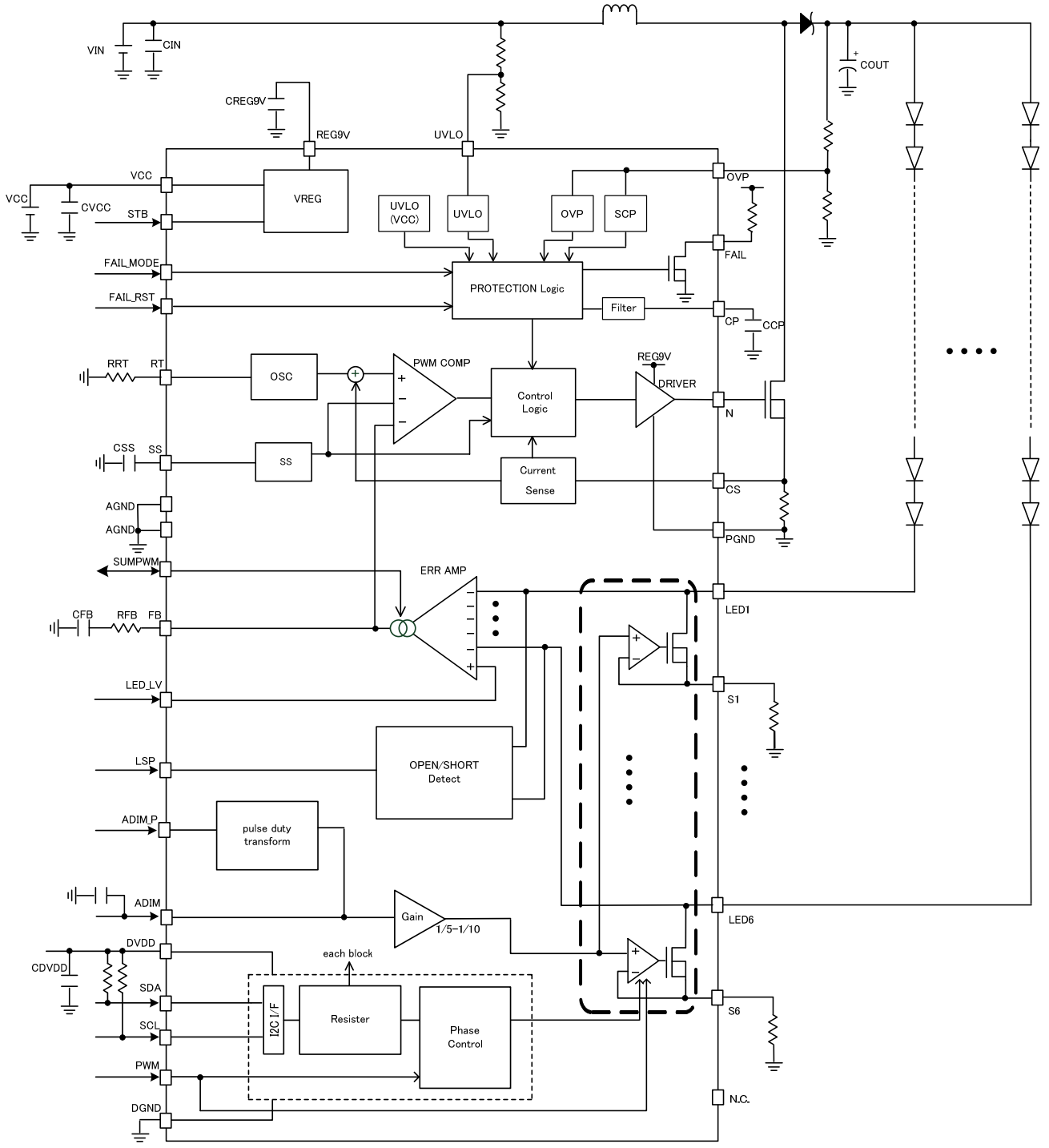


Figure 4. Block Diagram

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1.6 Absolute maximum ratings(Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power supply voltage	VCC	-0.3～36	V
Power dissipation	Pd	4.7(Note1)	W
Junction temperature range	Tjmax	-40 ～+150	°C
Operation temperature range	Topr	-40～+85	°C
Storage temperature range	Tstg	-55～+150	°C
Maximum LED output current	ILED	400(Note2)(Note3)	mA

No.	Pin	Rating [V]	No.	Pin	Rating [V]
1	VCC	-0.3~36	40	AGND	-
2	FAIL	-0.3~36	39	UVLO	-0.3~10.5
3	REG9V	-0.3~13	38	LSP	-0.3~7
4	N.C.	-	37	LED_LV	-0.3~7
5	N	-0.3~13	36	ADIM_P	-0.3~20
6	PGND	-	35	ADIM	-0.3~20
7	CS	-0.3~7	34	RT	-0.3~7
8	OVP	-0.3~7	33	FB	-0.3~7
9	FAIL_MODE	-0.3~7	32	SS	-0.3~7
10	AGND	-	31	CP	-0.3~7
11	LED1	-0.3~60	30	S1	-0.3~7
12	LED2	-0.3~60	29	S2	-0.3~7
13	LED3	-0.3~60	28	S3	-0.3~7
14	LED4	-0.3~60	27	S4	-0.3~7
15	LED5	-0.3~60	26	S5	-0.3~7
16	LED6	-0.3~60	25	S6	-0.3~7
17	STB	-0.3~36	24	FAIL_RST	-0.3~22
18	DVDD	-0.3~4.0	23	SUMPWM	-0.3~7
19	SDA	-0.3~4.0	22	DGND	-
20	SCL	-0.3~4.0	21	PWM	-0.3~22

(Note1) In the case of mounting 4 layer glass epoxy base-plate of 70mm × 70mm × 1.6mm, 37.6mW is reduced at 1°C above Ta=25°C.
(Note2) Wide VF variation of LED increases loss at the driver, which results in rise in package temperature. Therefore, the board needs to be designed with attention paid to heat radiation.
(Note3) This current value is per 1ch. It needs be used within a range not exceeding Pd.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

1.7 Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1層基板*(Note 3)*	4層基板*(Note 4)*	
HTSSOP-B40				
Junction to Ambient	θ_{JA}	99.8	26.0	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	5	2	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.
(Note 4)Using a PCB board based on JESD51-5, 7.

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1.8 Electrical Characteristics 1/3 (unless otherwise specified, V_{IN}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【Whole device】						
Operating circuit current	ICC	-	9	16	mA	STB=3.0V, LED1-6=ON, RT=100kΩ
Standby circuit current	ISTB	-	15	25	μA	STB=0V
DVDD circuit current	IDVDD	-	1.8	-	mA	DVDD=3.3V
【UVLO block】						
VCC operating supply voltage	VUVLO_VCC	7.0	7.5	8.0	V	VCC=SWEEP UP
VCC hysteresis voltage	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO release voltage	VUVLO_UVLO	2.40	2.50	2.60	V	VUVLO=SWEEP UP
UVLO HYS width	VUHYS_UVLO	100	200	400	mV	VUVLO=SWEP DOWN
UVLO pin input current	IUVLO	-2	0	2	μA	VUVLO=3.0V
DVDD release voltage	VUVLO_DVDD	2.10	2.35	2.60	V	VDVDD=SWEEP UP
DVDD HYS width	VUHYS_DVDD	100	200	400	mV	VDVDD=SWEP DOWN
【REG9V block】						
REG9V output voltage	REG9V	8.91	9.0	9.09	V	IO=0mA, VCC>11.0V
REG9V max. output current	IREG9V	20	-	-	mA	
【DCDC block】						
Error AMP reference voltage	VEAMP	0.97	1.00	1.03	V	LED_LV=1.0V, LEDLV[3:0]=0000
		0.578	0.60	0.622	V	LEDLV[3:0]=1001
		0.278	0.300	0.322	V	LEDLV[3:0]=1111
FB sink current	IFBSINK	85	100	115	μA	LED_LV=1.0V, LEDx=2.0V, VFB=1.0V
FB source current (Master)	IFBSOURCEM	-115	-100	-85	μA	LED_LV=1.0V, LEDx=0.0V, VFB=1.0V,CS=0.0V
FB source current (Slave)	IFBSWRCKS	-230	-200	-170	μA	LEDx=0V,VFB=1.0V,CS=5.0V
LED_LV pin input current	ILED_LV	-2	0	2	μA	VLED_LV=3.0V
Oscillation frequency	FCT	190	200	210	kHz	RT=100kΩ, FOSC[4:0]=00000
MAX DUTY	DMAX	83	89	96	%	
SS pin source current	ISS	-3.75	-3.0	-2.25	μA	SS=0V
SS pin release voltage	VSS	3.8	4.0	4.2	V	SS=SWEEP UP
N pin source resistor	RONH	-	2.5	3.5	Ω	ION=-10mA
N pin sink resistor	RONL	-	3.0	4.2	Ω	ION=10mA

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1.8 Electrical Characteristics 2/3 (unless otherwise specified, V_{IN}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【DCDC protection block】						
OCP detection voltage	VOCP	0.405	0.45	0.495	V	VCS=SWEEP UP
OVP detection voltage	VOVP	2.91	3.00	3.09	V	VOVP=SWEEP UP, OVPSET[3:0]=0000
OVP hysteresis voltage	VOVPHYS	10	50	100	mV	VOVP=SWEEP DOWN, OVPSET[3:0]=0000
OVP pin input current	IOVP	-2	0	2	µA	VOVP=3.0V
SCP detection voltage	VSCP	0.12	0.20	0.28	V	VOVP=SWEEP DOWN
【LED driver block】						
S pin voltage 1	VSLED1	196	200	204	mV	ADIM=1.0V, ADIMGAIN[3:0]=0000
		294.6	300	305.4	mV	ADIM=1.5V, ADIMGAIN[3:0]=0000
		392.8	400	407.2	mV	ADIM=2.0V, ADIMGAIN[3:0]=0000
		491	500	509	mV	ADIM=2.5V, ADIMGAIN[3:0]=0000
S pin voltage 2	VSLED2	101.7	106	110.3	mV	ADIM=1.0V, ADIMGAIN[3:0]=1111
		153.2	159	164.8	mV	ADIM=1.5V, ADIMGAIN[3:0]=1111
		204.3	212	219.7	mV	ADIM=2.0V, ADIMGAIN[3:0]=1111
		254.4	265	275.6	mV	ADIM=2.5V, ADIMGAIN[3:0]=1111
LED current rise time	ILEDtr	-	400	760	ns	ADIM=0.3V,RS=2Ω, DVDD=0V
LED current fall time	ILEDtf	-	100	280	ns	ADIM=0.3V,RS=2Ω, DVDD=0V
OPEN detection voltage	VOPEN	0.12	0.20	0.28	V	VLED=SWEEP DOWN
SHORT detection voltage	VSHORT	5.7	6.0	6.3	V	VLED=SWEEPUP, VLSP=1.2V, LSPSET[3:0]=0000
SHORT MASK voltage	VSHTMASK	2.85	3.0	3.15	V	
LSP pin input current	ILSP	-2	0	2	µA	VLSP=3.0V
【Analog dimming block】						
ADIM_P pin HIGH voltage	ADIM_PH	2.0	-	5.5	V	
ADIM_P pin LOW voltage	ADIM_PL	-0.3	-	0.8	V	
ADIM_P Pin input MASK voltage	ADIM_PPU	6.5	-	18	V	
ADIM_P pin pull-down R	RADIM_P	2.4	4.0	5.6	MΩ	VADIM_P=3.0V
ADIM pin output voltage H (During output)	ADIMH	2.462	2.500	2.538	V	VADIM_P=3.3V
ADIM pin output voltage L (During output)	ADIML	-	0.0	0.05	V	VADIM_P=0.0V
ADIM pin output R (During output)	ADIMR	6.6	10	15	kΩ	VADIM_P=0.0V
ADIM pin input current (During input)	IADIM	-2	0	2	µA	VADIM_P=9.0V, VADIM=2.5V

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1.8 Electrical Characteristics 3/3 (unless otherwise specified, V_{IN}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【STB block】						
STB pin HIGH voltage	VSTBH	2.0	-	18	V	
STB pin LOW voltage	VSTBL	-0.3	-	0.8	V	
STB pin pull-down Resistor	RSTB	0.6	1.0	1.4	MΩ	STB=3.0V
【PWM block】						
PWM pin HIGH voltage	VPWMH	1.5	-	20	V	
PWM pin LOW voltage	VPWML	-0.3	-	0.8	V	
PWM pin pull-down Resistor	RPWM	180	300	420	kΩ	PWM=3.0V
【Abnormality detection block】						
FAIL pin LOW output voltage	VFAILL	0.0	0.15	0.3	V	IOL=500μA
FAIL_RST pin Input HIGH voltage	VFAIL_INH	2.0	-	20	V	
FAIL_MODE pin Input HIGH voltage	VFAIL_INH	2.0	-	5.5	V	
FAIL_MODE, FAIL_RST pin Input LOW voltage	VFAIL_INL	-0.3	-	0.8	V	
FAIL_MODE, FAIL_RST pin Input pull-down Resistor	RFAIL	60	100	140	kΩ	VIN=3.0V
CP detection voltage	VCP	2.91	3.0	3.09	V	CP=SWEEP UP
CP source current	ICP	-3.3	-3.0	-2.7	μA	CP=0V
【I2C block】						
SCL, SDA input HIGH voltage	VI2C_INH	0.8*DVDD	-	3.6	V	
SCL, SDA input LOW voltage	VI2C_INL	-0.3	-	0.2*DVDD	V	
SCL, SDA input HIGH current	II2C_INH	-	-	10	μA	DVDD=3.3V, VIN=3.3V
SCL, SDA input LOW current	II2C_INL	-10	-	-	μA	DVDD=3.3V, VIN=0V
L level SDA output	VSDA_OL	-	-	0.4	V	
【Master/Slave selection block】						
SUMPWM pin input HIGH voltage	VSUM_INH	2.0	-	5.5	V	
SUMPWM pin input LOW voltage	VSUM_INL	-0.3	-	0.8	V	
SUMPWM pin pull-down Resistor	RSUM	60	100	140	kΩ	VIN=3.0V

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1.9 Typical Performance Curves
(reference data)

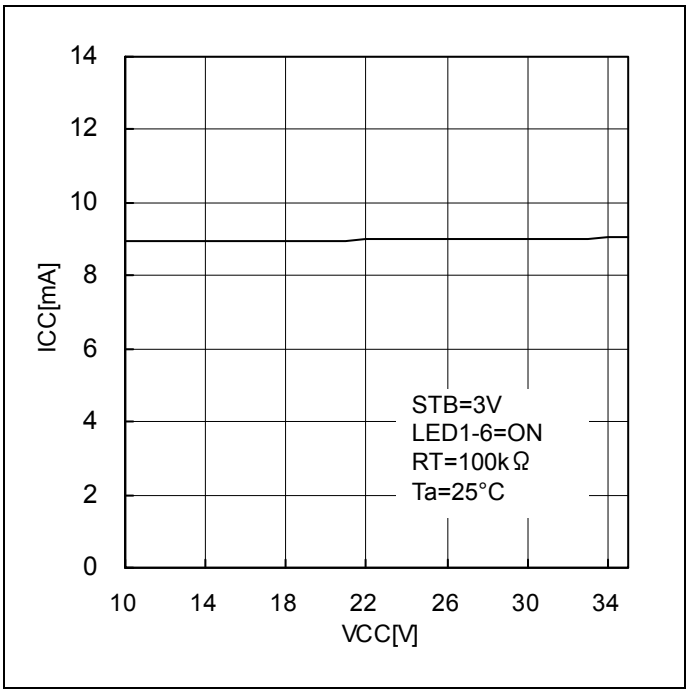


Figure 5. Operating circuit current

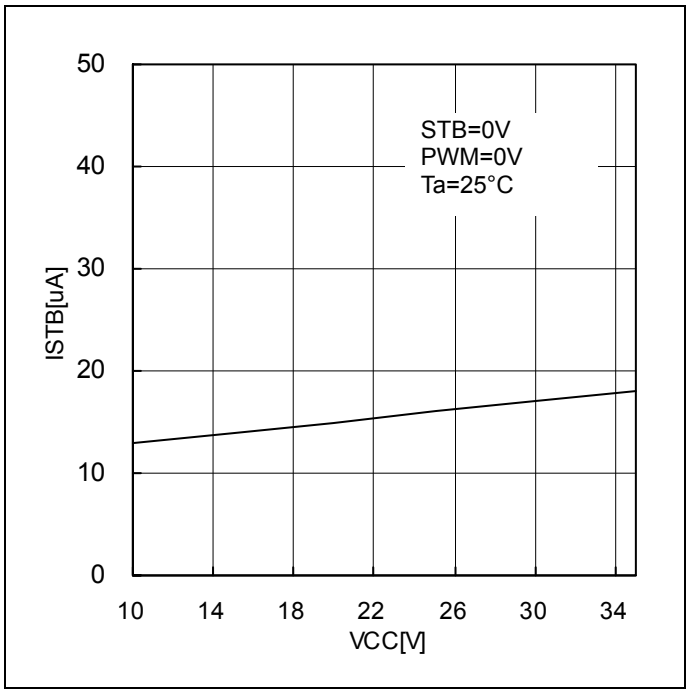


Figure 6. Standby circuit current

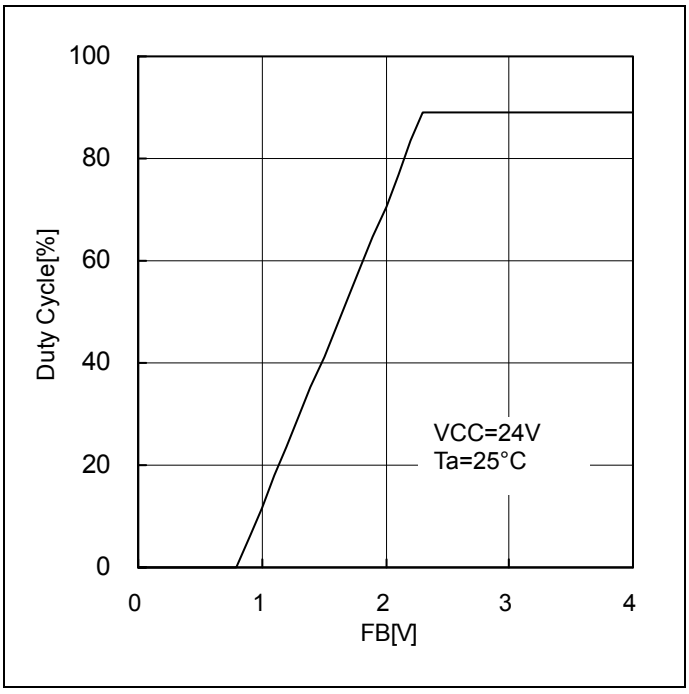


Figure 7. Duty Cycle vs FB character

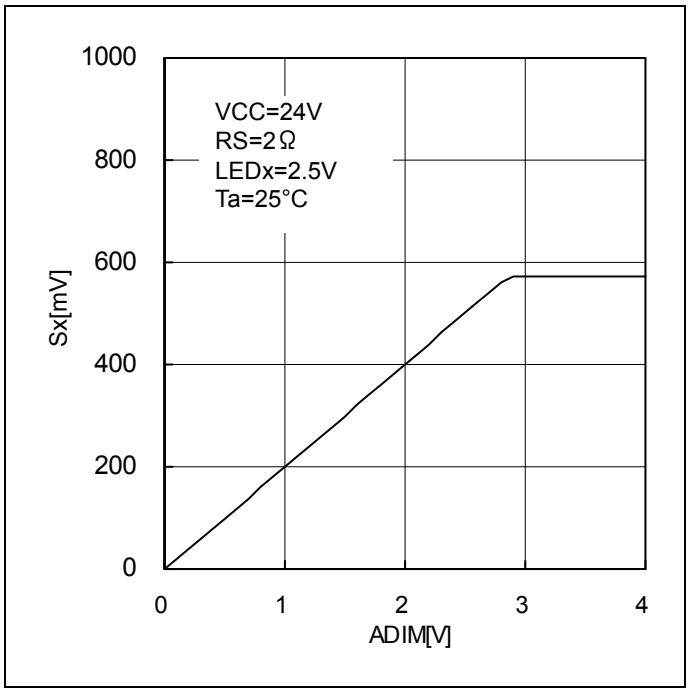


Figure 8. Sx vs ADIM character

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1.10 Operating range

Parameter	Symbol	Range	Unit
VCC power supply voltage	VCC	9 to 35	V
DVDD power supply voltage	VDD	2.7 to 3.6	V
Boost-up oscillation frequency	FCT	50 to 1250(Note1)	kHz
ADIM input voltage	VADIM	0.2 to 2.5	V
ADIM_P input frequency	FADIM_P	to 20k	Hz
LSP pin input voltage	VLSP	0.8 to 3	V
LED_LV pin input voltage	VLED_LV	0.3 to 1.8	V
FB pin output voltage	VFB	0 to 5.0	V
PWM pin input frequency (With DVDD)	FPWM	0, 100 to 25k	Hz
PWM pin input Low width (With DVDD)	TLPWM	from 157ns	ns
SCL Clock frequency	FSCL	to 400	kHz

(Note1) When driving the external FET with high frequency, it may increase FET heat generation, therefore please do the setting carefully.

1.11 Recommendation range of external parts

Parameter	Symbol	Range	Unit
VCC pin connection capacitance	CVCC	1.0 to 10	μF
DVDD pin connection capacitance	CDVDD	0.047 to 1.0	μF
Soft start setting capacitance	CSS	0.001 to 1.0	μF
Timer latch setting capacitance	CCP	0.001 to 2.7	μF
Boost-up frequency setting resistor	RRT	12 to 150(Note2)	kΩ
REG9V pin connection capacitance	CREG9V	1.0 to 10	μF

(Note2) It depends on FOSC[4:0] register value, but please do the setting that make the oscillation frequency within the specification written in section 1.10.
The operating condition described above is for single IC constants. Adequate attention must be paid when setting the constants at actual set.

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1.12 I2C command interface

1.12.1 Overview and condition

BD9423EF are using host CPU and Command Interface by I2C bus system. BD9423EFV register setting from 00h to 08h range is possible not only Write but also can Read. Besides, other than slave address, this IC also can perform to design 1bit Select Address and then do the Write and Read.
I2C bus slave mode format is shown as below.

	MSB LSB		MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	Data	A	P

S: Start Condition
Slave Address: After the set Slave Address (7bit) by ADDR, there is one more bit of Read Mode (H") or Write Mode (L") and the data will be sent in total of 8bit. (MSB format)
BD9423EFV slave address is 46h.
A: The acknowledge send and receive data is added by Acknowledge Bit as byte per byte.
When the send and receive data is correctly done, "L" will be sent and received.
When it is "H", acknowledge will be gone.
Select Address: BD9423EFV will use 1 byte of select address. (MSB format)
Data: Data Byte, send and receive data. (MSB format)
P: Stop Condition

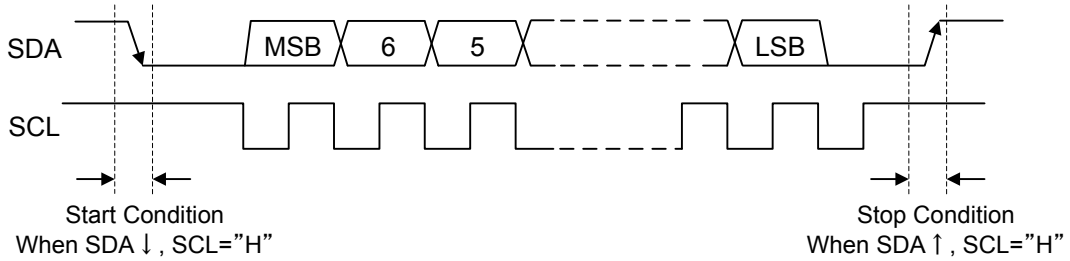


Figure 9. Command Interface

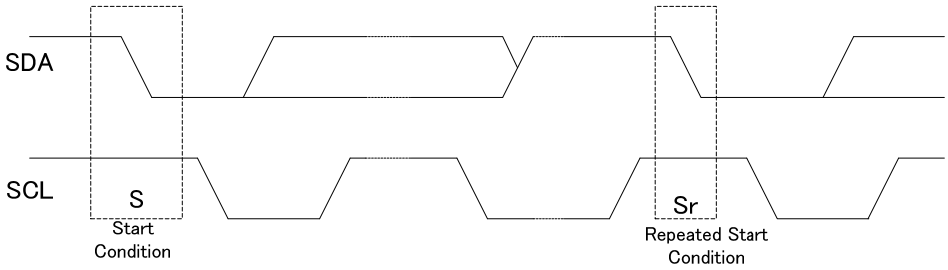


Figure 10. Repeated Start Condition

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1.12.2 Data format

1byte Write format

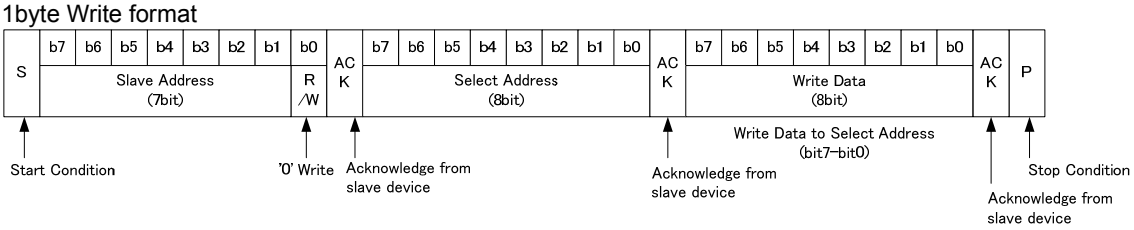


Figure 11. 1byte Write Data Format

1byte Read format (Read from select address=00h)

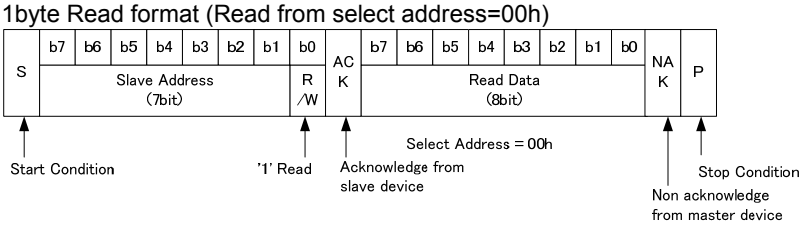


Figure 12. 1byte Read Data Format (Select Address=00h)

1byte Read format (Read from specific Select Address)

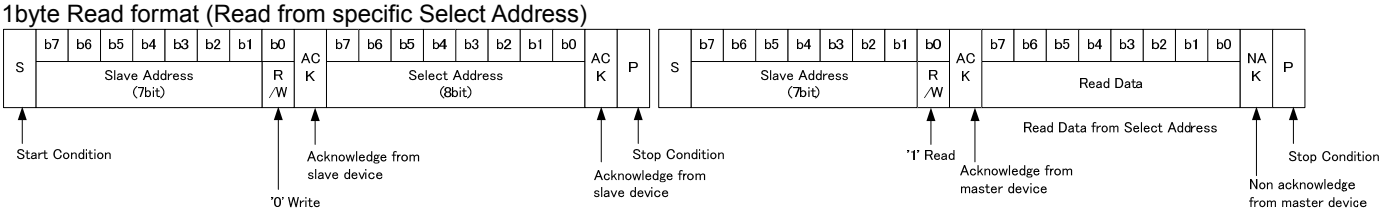


Figure 13. 1byte Read Data Format (specified select address)

Consecutive Write format

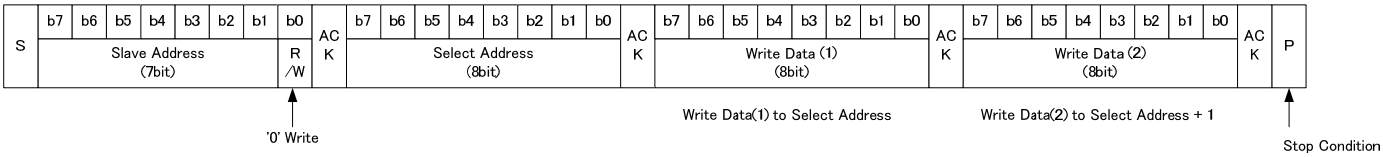


Figure 14. Consecutive Write Data Format

Consecutive Read format (Read from specific Select Address)

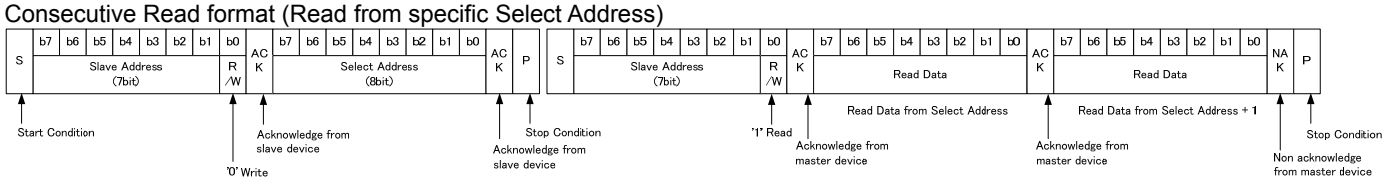


Figure 15. Consecutive Read Data Format

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1.12.3 Signal control specification

Bus Line and I/O stage electrical specification and timing

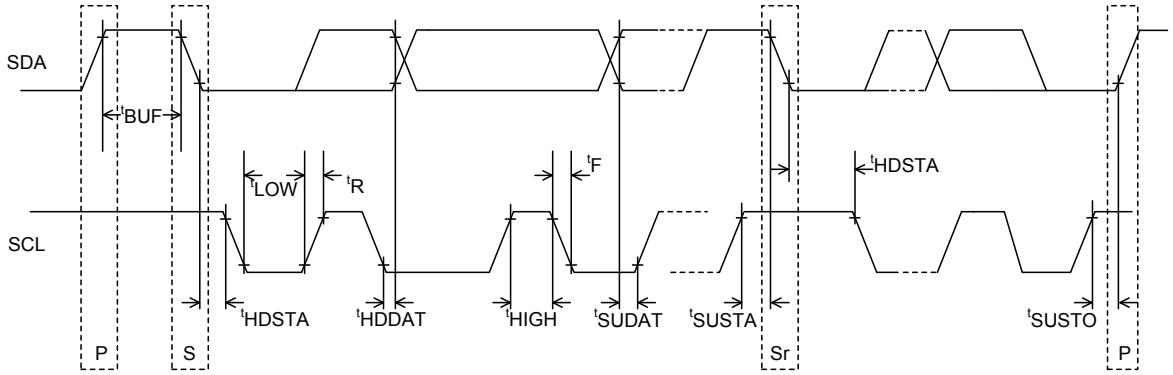


Figure 16. Timing chart

Table 1. SDA and SCL Bus Line characteristic (Unless otherwise stated Ta=25°C, DVDD=3.0V)

Parameter		Symbol	High speed mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus Free Time between “Stop” Condition and “Start” Condition.	tBUF	1.3	—	μs
3	Hold Time (Resend) “Start” Condition. After this period, the first Clock Pulse will be generated.	tHDSTA	0.6	—	μs
4	SCL clock LOW state Hold Time	tLOW	1.3	—	μs
5	SCL clock HIGH state Hold Time	tHIGH	0.6	—	μs
6	Resend “Start” Condition set-up time	tSUSTA	0.6	—	μs
7	Data Hold Time	tHDDAT	0(Note1)	—	μs
8	Data Set-up Time	tSUDAT	100	—	ns
9	SDA and SCL signal rising time	tR	20+0.1Cb	300	ns
10	SDA and SCL signal falling time	tF	20+0.1Cb	300	ns
11	“Stop” Condition set-up time	tSUSTO	0.6	—	μs
12	Each Bus Line capacitive load	Cb	—	400	pF

Above values are all $V_{IH\,min}$ and $V_{IL\,max}$ level supported.

(Note1) Please note that the master device has uncertain interval maximum 300ns for the negative edge of SLC, therefore SDA is necessary at least 300ns hold time.

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1.13 Register map and description

Slave address (Device address) for BD9423EFV is 46h. Please refer to section 1.12 I2C command interface for I2C details.

Update timing for each register is as follows.
(1) Data will reflect immediately after register is written.
(2) Data will reflect at next PWM rise after register is written (Refer to Section 1.14 PWM Phase shift setting)
(3) Data will reflect as PWM=Low after register is written.

Sequence that is assumed for each register will be as follow. (Please refer to 3.8.1 start up and shut down sequences). Writing is possible at any timing, however it is classified by the consideration of register function.
(A) Initial command: Please input the command before input the STB pin. It is assumed to set a condition for the application.
(B) Dimming command: It is possible to input the command before or after STB pin.

Address	R/W	Initial value	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	R/W	00h	SOFTRST	-	-	-	-	-		FAILSORST	PHASERST
			Update timing	-	-	-	-	-	-	(1)	(1)
			Write sequence	-	-	-	-	-	-	(B)	(B)
01h	R/W	00h	LEDDIS	-	-	LED6DIS	LED5DIS	LED4DIS	LED3DIS	LED2DIS	LED1DIS
			Update timing	-	-	(3)	(3)	(3)	(3)	(3)	(3)
			Write sequence	-	-	(A)	(A)	(A)	(A)	(A)	(A)
02h	R/W	00h	LEDPHASE	FOSC4	FOSC3	FOSC2	FOSC1	FOSC0	LEDPHASE2	LEDPHASE1	LEDPHASE0
			Update timing	(1)	(1)	(1)	(1)	(1)	(2)	(2)	(2)
			Write sequence	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
03h	R/W	00h	ADIMGAIN	CPADJ1	CPADJ0	SSADJ1	SSADJ0	ADIM GAIN3	ADIM GAIN2	ADIM GAIN1	ADIM GAIN0
			Update timing	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
04h	R/W	00h	OVPSET	OVPSET3	OVPSET2	OVPSET1	OVPSET0	LSPSET3	LSPSET2	LSPSET1	LSPSET0
			Update timing	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
05h	R/W	00h	SFTONOFF	-	-	MSTSLVSFT	MSTSLVSEL	SFTONT1	SFTONT0	SFTOFFT1	SFTOFFT0
			Update timing	-	-	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	-	-	(A)	(A)	(B)	(B)	(B)	(B)
06h	R/W	00h	LOPMSK	SCPMSK	OVPMSK	LOPMSK6	LOPMSK5	LOPMSK4	LOPMSK3	LOPMSK2	LOPMSK1
			Update timing	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	(B)	(B)	(B)	(B)	(B)	(B)	(B)	(B)
07h	R/W	00h	LSPMSK	-	-	LSPMSK6	LSPMSK5	LSPMSK4	LSPMSK3	LSPMSK2	LSPMSK1
			Update timing	-	-	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	-	-	(B)	(B)	(B)	(B)	(B)	(B)
08h	R/W	00h	LEDLVSET	-	-	IFBSET1	IFBSET0	LEDLVSET3	LEDLVSET2	LEDLVSET1	LEDLVSET0
			Update timing	-	-	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	-	-	(A)	(A)	(A)	(A)	(A)	(A)

Note) "-" : Invalid during Write, "0" during Read
Please do not write register other than 00h-08h. Besides, Read value from register other than 00h-08h is disabled.

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●**ADDR=00h**

SOFTRST (SoftRESET control register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	-	-	-		FAILSO RST	PHASERST
Initial Value	-	-	-	-	-	-	0	0

FAILSORST	RESET setting
0	Normal
1	Latch OFF release, Protection operation mask

When FAILSORST is set as 1 (FAILSORST=1), protection circuit and FAIL are reset.
It is same with the operation when FAIL_RST pin=High.
During FAILSORST=1, latch OFF protection operation is masked.

PHASERST	RESET setting
0	Normal
1	Counter clear

When PHASERST=1, logics other than Phase shift part register are reset. Register values shown in the section 1.13 will not be reset. In order to release reset, please write PHASERST=0, it will return to normal condition.

●**ADDR=01h**

LEDDIS (LED driver disable setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	-	-	LED6DIS	LED5DIS	LED4DIS	LED3DIS	LED2DIS	LED1DIS
Initial Value	-	-	0	0	0	0	0	0

LEDDIS	Disable Control
0	Enable (LED driver operates when PWM=H)
1	Disable (LED driver is not used)

Unused channel will be set. The unused channel will not detect the abnormality (Short, Open).

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●**ADDR=02h**

LEDPHASE (Phase shift setting, FCT setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	FOSC4	FOSC3	FOSC2	FOSC1	FOSC0	LEDPHASE2	LEDPHASE1	LEDPHASE0
Initial Value	0	0	0	0	0	0	0	0

FOSC[4:0]	FOSC setting	FCT default=200kHz
00000	1.000 time	200kHz
00001	0.250 time	50 kHz
00010	0.375 time	75 kHz
00011	0.500 time	100 kHz
00100	0.625 time	125 kHz
00101	0.750 time	150 kHz
00110	0.875 time	175 kHz
00111	1.000 time	200 kHz
01000	1.125 times	225 kHz
01001	1.250 times	250 kHz
01010	1.375 times	275 kHz
01011	1.500 times	300 kHz
01100	1.625 times	325 kHz
01101	1.750 times	350 kHz
01110	1.875 times	375 kHz
01111	2.000 times	400 kHz
10000	2.125 times	425 kHz
10001	2.250 times	450 kHz
10010	2.375 times	475 kHz
10011	2.500 times	500 kHz
10100	2.625 times	525 kHz
10101	2.750 times	550 kHz
10110	2.875 times	575 kHz
10111	3.000 times	600 kHz
11000	3.125 times	625 kHz
11001	3.250 times	650 kHz
11010	3.375 times	675 kHz
11011	3.500 times	700 kHz
11100	3.625 times	725 kHz
11101	3.750 times	750 kHz
11110	3.875 times	775 kHz
11111	4.000 times	800 kHz

Oscillating frequency FCT will be set.
When RT=100kΩ, default frequency is 200kHz, frequency will be set as the values shown in above table.
Register is setting based on how many times of frequency base, therefore, please always connect a resistor at RT terminal.

LEDPHASE[2:0]	LEDPHASE control
000	Phase1 setting (0 shift)
001	
010	Phase2 setting (1/2T shift)
011	Phase3 setting (1/3T shift)
100	Phase4 setting (1/4T shift)
101	Phase5 setting (1/5T shift)
110	Phase6 setting (1/6T shift)
111	

Phase shift setting will be done. Please refer to section 1.14 "PWM phase shift setting" for each phase shift timing.

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●**ADDR=03h**

ADIMGAIN (ADIM GAIN Setting, CP and SS time setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	CPADJ1	CPADJ0	SSADJ1	SSADJ0	ADIMGAIN3	ADIMGAIN2	ADIMGAIN1	ADIMGAIN0
Initial value	0	0	0	0	0	0	0	0

CPADJ[1:0]	CP time setting
00	1time
01	2times
10	1/2time
11	1/4time

CP timer time, Tcp can be set.
CP timer time can be decided by, Tcp[s] = (Ccp[F]×3V×CPADJ) / 3μA.

SSADJ[1:0]	SS time setting
00	1time
01	2times
10	1/2time
11	1/4time

SS release time, Tss can be set.
SS release time can be decided by, Tss[s] = (Css[F]×4V×SSADJ) / 3μA.

ADIMGAIN[3:0]	ADIMGAIN setting
0000	0.200 time
0001	0.194 time
0010	0.188 time
0011	0.181 time
0100	0.175 time
0101	0.169 time
0110	0.163 time
0111	0.156 time
1000	0.150 time
1001	0.144 time
1010	0.138 time
1011	0.131 time
1100	0.125 time
1101	0.119 time
1110	0.113 time
1111	0.106 time

ADIM gain will be set. ADIM pin voltage × ADIMGAIN=Sx pin voltage.

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●**ADDR=04h**

OVPSET (OVP voltage, LSP voltage setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	OVPSET3	OVPSET2	OVPSET1	OVPSET0	LSPSET3	LSPSET2	LSPSET1	LSPSET0
Initial value	0	0	0	0	0	0	0	0

OVPSET[3:0]	OVP voltage setting	OVP default=90V
0000	3.00V	90V
0001	0.90V	27V
0010	1.05V	32V
0011	1.20V	36V
0100	1.35V	41V
0101	1.50V	45V
0110	1.65V	50V
0111	1.80V	54V
1000	1.95V	59V
1001	2.10V	63V
1010	2.25V	68V
1011	2.40V	72V
1100	2.55V	77V
1101	2.70V	81V
1110	2.85V	86V
1111	3.00V	90V

OVP voltage will be set. When setting the OVP detection resistor 30 times (OVP upper side resistor : OVP lower side resistor=29 : 1), the setting shown in above table can be done.

LSPSET[3:0]	LSP voltage setting	LSP detection voltage value
0000	LSP pin input	4V to 15V
0001	0.8V	4V
0010	0.8V	4V
0011	0.8V	4V
0100	0.8V	4V
0101	1.0V	5V
0110	1.2V	6V
0111	1.4V	7V
1000	1.6V	8V
1001	1.8V	9V
1010	2.0V	10V
1011	2.2V	11V
1100	2.4V	12V
1101	2.6V	13V
1110	2.8V	14V
1111	3.0V	15V

LSP voltage will be set. When LSPSET[3:0]=0000, LSP pin voltage will be used as LSP detection reference voltage.
Other than LSPSET[3:0]=0000, IC internal reference voltage will be used, therefore external bias setting can be removed.
If you set the LSP by this register, it will be the priority rather than LSP pin voltage.

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●**ADDR=05h**

SFTONOFF (SOFT ON, SOFT OFF setting register, Master/Slave setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	MSTSLV SFT	MSTSLV SEL	SFTONT1	SFTONT0	SFTOFFT1	SFTOFFT0
Initial Value	-	-	0	0	0	0	0	0

MSTSLVSFT	Master/Slave software setting
0	Master mode
1	Slave mode

(Note) Valid when MSTSLVSEL =1

MSTSLVSEL	Master/Slave selection setting
0	Hardware recognition (CSDET output detection)
1	MSTSLVSEL register control

Master/Slave setting is possible when MSTSLVSEL=1. This setting means for when CS pin is set to open. Please separately connect the SUMPWM pin between the IC.

SFTONT[1:0]	Soft ON time setting
00	Soft ON function stop
01	2time
10	1time (correspond to fsw 10CLK)
11	1/2time

Set Soft ON time when PWM＝L→H. CLK when N pin is operating in MAX duty.

SFTOFFT[1:0]	Soft OFF time setting
00	1time (correspond to fsw 15CLK) However, when Soft ON is 1/2time (SFTONT[1:0]=11), it will become 1/2time.
01	2times However, when Soft ON is 1time (SFTONT[1:0]=10), it will become 1time, when Soft On is 1/2time (SFTONT[1:0]=11), it will become 1/2time.
10	1/2time
11	-

Set Soft OFF time when PWM＝H→L. CLK when N pin is operating in MAX duty.

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●**ADDR=06h**

LOPMSK (SCP, OVP, LOP Mask register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	SCPMSK	OVPMSK	LOPMSK6	LOPMSK5	LOPMSK4	LOPMSK3	LOPMSK2	LOPMSK1
Initial Value	0	0	0	0	0	0	0	0

SCPMSK	Short circuit protection (SCP) Mask control
0	Normal
1	SCP Mask

OVPMSK	Over voltage protection (OVP) Mask control
0	Normal
1	OVP Mask

Mask the SCP and OVP detection.

LOPMSK	LED Open protection (LOP) Mask control
0	Normal
1	LOP Mask

Mask LED open detection for each channel.

Example 1: When masking the OVP, ADDR=06h, DATA=40h
Example 2: When masking the SCP and OVP, ADR=06h and DATA=C0h
Example 3: When masking the LED1 LOP, ADDR=06h, DATA=01h

●**ADDR=07h**

LSPMSK (LSP Mask register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	LSPMSK6	LSPMSK5	LSPMSK4	LSPMSK3	LSPMSK2	LSPMSK1
Initial Value	-	-	0	0	0	0	0	0

LSPMSK	LED Short protection (LSP) Mask control
0	Normal
1	LSP Mask

Example 1: When masking the LED6 LSP, ADDR=07h, DATA=20h

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●**ADDR=08h**

LEDLVSET (LED_LV voltage, FB current setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	IFBSET1	IFBSET0	LEDLVSET3	LEDLVSET2	LEDLVSET1	LEDLVSET0
Initial Value	-	-	0	0	0	0	0	0

IFBSET[1:0]	FB current setting
00	1time
01	2times
10	1/2time
11	1/4time

Set the FB current.

LEDLVSET[3:0]	LED_LV voltage setting
0000	LED_LV pin input
0001	1.00V
0010	0.95V
0011	0.90V
0100	0.85V
0101	0.80V
0110	0.75V
0111	0.70V
1000	0.65V
1001	0.60V
1010	0.55V
1011	0.50V
1100	0.45V
1101	0.40V
1110	0.35V
1111	0.30V

Set the LED_LV voltage.
When LEDLVSET[3:0]=0000, LED_LV pin voltage will be used as reference for feedback voltage.
Other than LEDLVSET[3:0]=0000, IC internal reference voltage will be used, thus external bias setting can be removed.
If you set the LED_LV by this register, it will be the priority rather than LED_LV pin voltage.

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1.14 PWM phase shift setting

Phase shifting for each channel is possible by setting the LEDPHASE register. In addition, by setting the LEDDIS register, unused channel also can be set. Therefore, various combinations of dimming can be performed.

1.14.1

(*1) When VCC and DVDD are supplied, STB becomes L→H, 15MHz oscillator for phase shift sampling will start operate.
(*2) Then, when PWM signal is supplied, counter will start at L→H edge as the starting point.
(*3) When PWM signal becomes H→L, PWM's ON width count-number N_{ON} will be decided.
(*4) PWM's period N_T will be decided at next PWM signal L→H edge when next PWM signal.

Period, duty and phase for each LED driver channel will be counted from ON width N_{ON}, period N_T and LEDPHASE register setting, then PWM signal will be reflected to each channel from next PWM signal.
Phase shift is possible for frequency within 100Hz to 20kHz.

This function operates during DVDD is being input and the cautions are as below. Please be noted that this function does not depend on phase shift amount.
(Caution 1) Possible phase shift frequency range is 100Hz to 25kHz.
(Caution 2) When input the signal around PWM=100%, please don't input the pulse lower than 157ns for Low interval. This is to correctly recognize the Low interval.

The following is the DUTY values which are not in the input range.
When PWM20kHz, above 99.68%, 100% and below (PWM=100% input is possible)
When PWM500Hz, above 99.992%, 100% and below (PWM=100% input is possible)

When there is no DVDD (during standalone), the PWM terminal will directly make the constant current driver goes ON/OFF, therefore above caution 1 and 2 are not applicable.

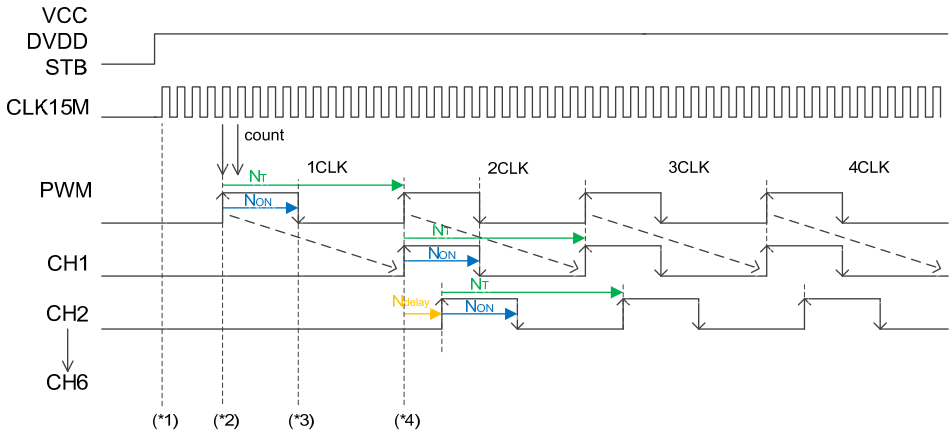


Figure 17. Timing chart for phase shift

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1.14.2 Case when PWM is below 100Hz, PWM=H during overflow

When PWM signal's ON width and counter (period counting) is above 2^{18}=262144clk (correspond to frequency below 57Hz), it becomes overflow. If PWM's L→H edge is not input by this time, PWM signal's period can be decided. The operation at this condition is shown below.

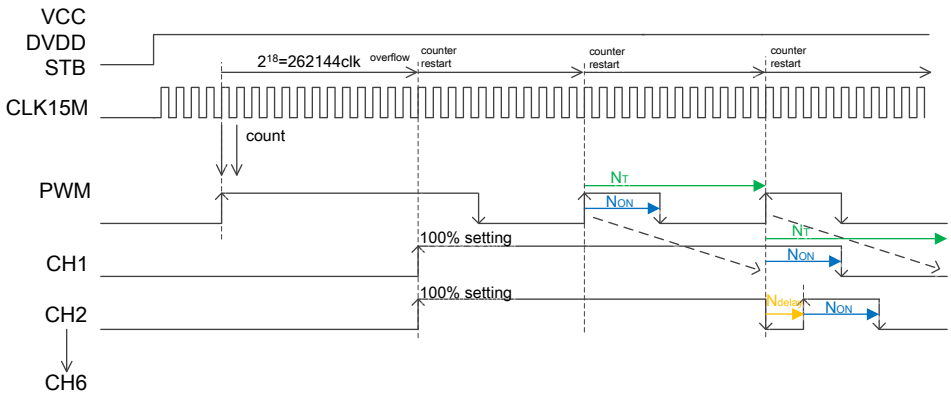


Figure 18. Timing chart for 100% duty overflow

PWM input is considered as High (Duty=100%), thus each LED driver channel will be set as Duty=100% same timing with counter restart.

1.14.3 Case when PWM is below 100Hz, PWM=L during overflow.

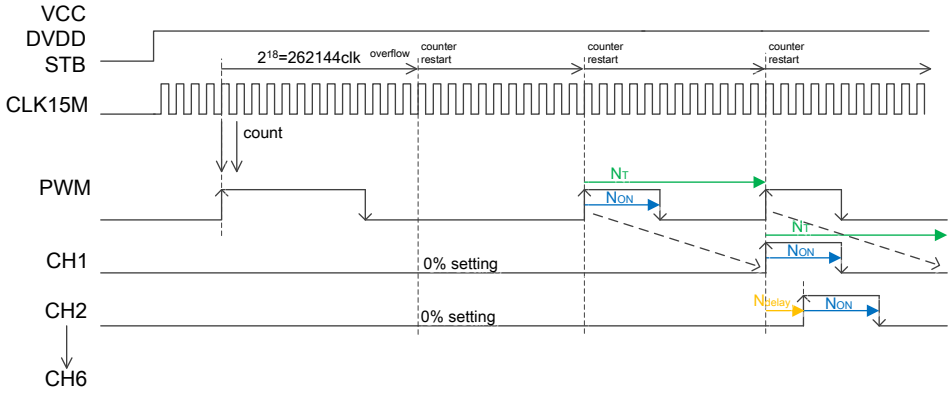


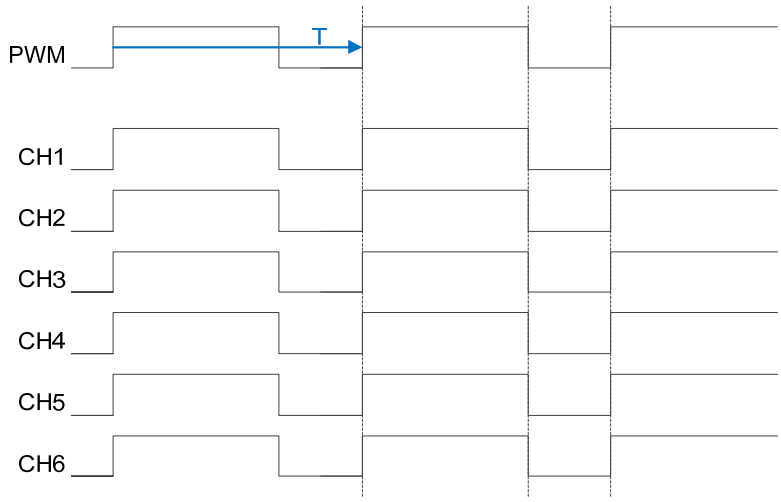
Figure 19. Timing chart for 0% duty overflow

PWM input is considered as Low (Duty=0%), thus each LED driver channel will be set as Duty=0% same timing with counter restart.

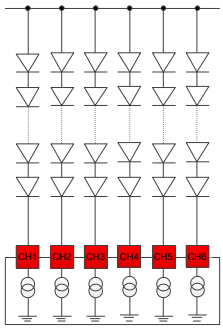
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1. Phase1 setting (0 shift)

□LEDDIS=00h[All ch ON], LEDPHASE=00h)

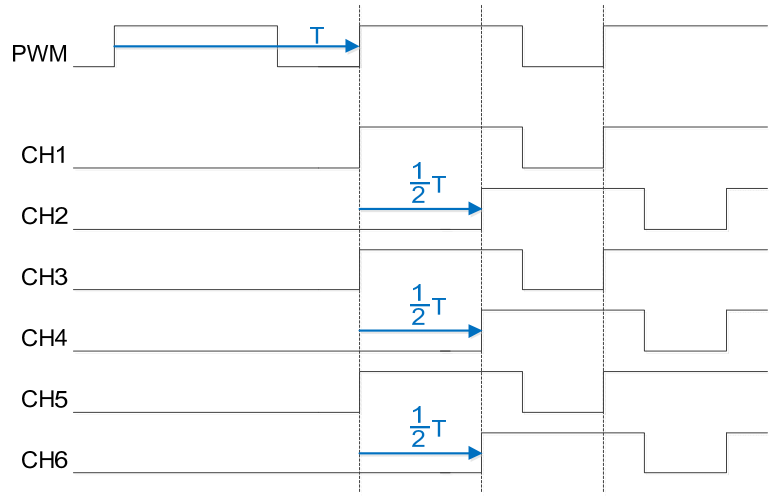


Signal from PWM pin is used as PWM signal for each channel. All channels will have same phase.

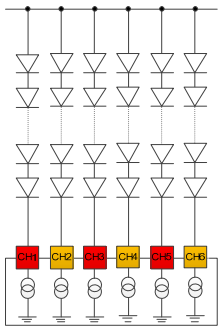


2.Phase2 setting (1/2T shift)

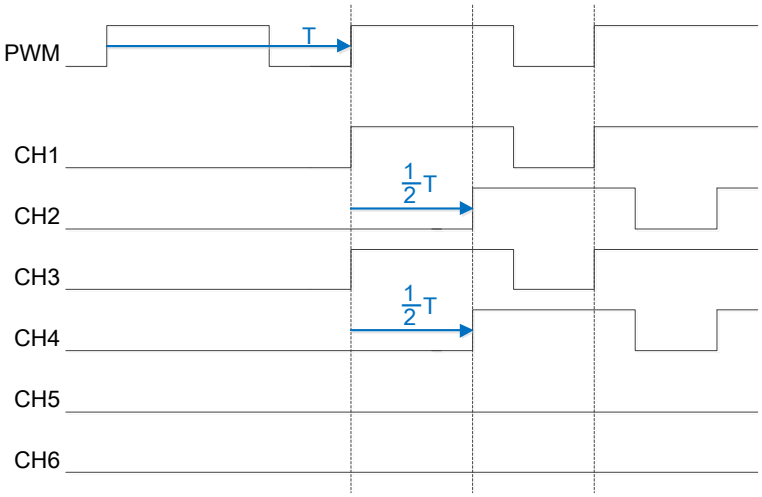
□LEDDIS=00h[All ch ON], LEDPHASE=02h



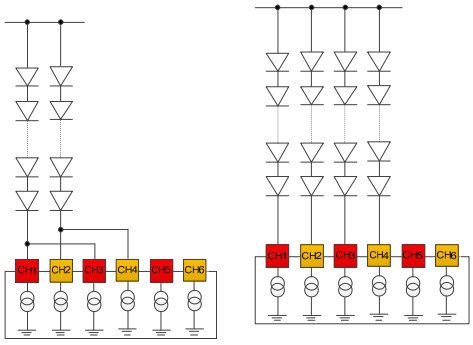
1/2T shift, mode which has 2 phases.



□LEDDIS=30h[CH5,6 OFF],LEDPHASE=02h

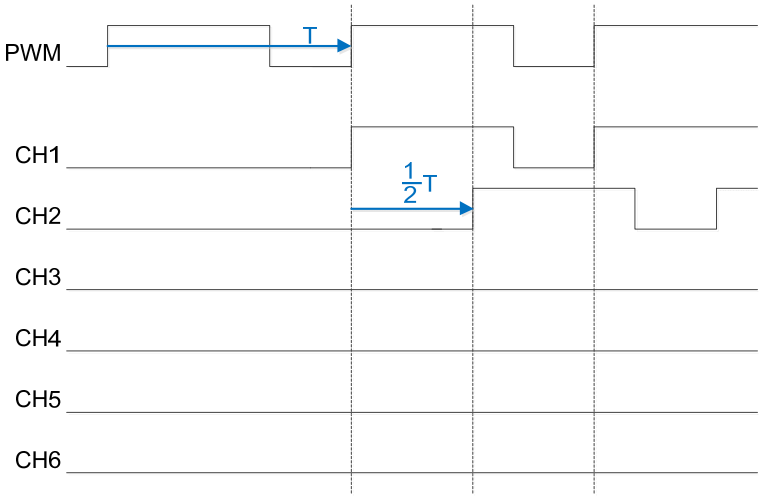


Case when CH5, CH6 are not in use.

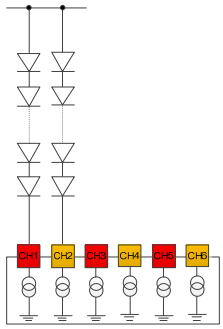


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・LEDDIS=3Ch[CH3-6 OFF], LEDPHASE=02h

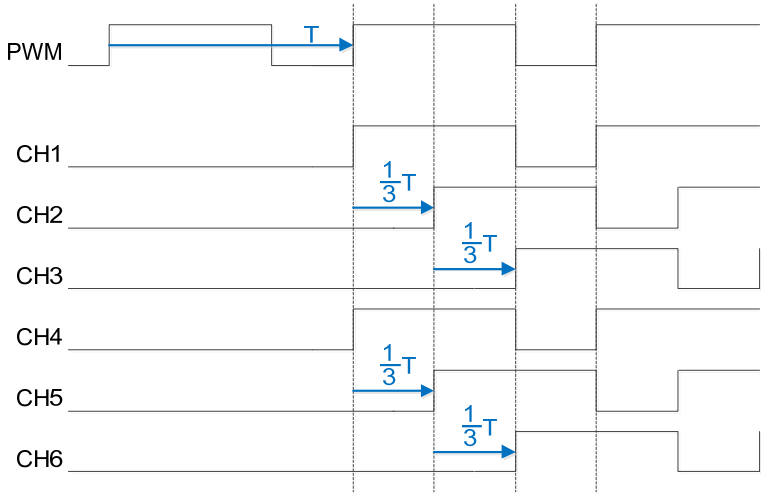


Case when CH3-6 are not in use.

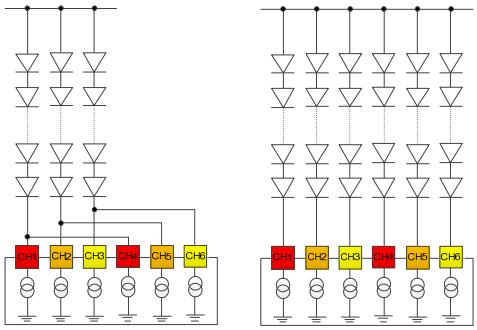


3. Phase3 setting (1/3T shift)

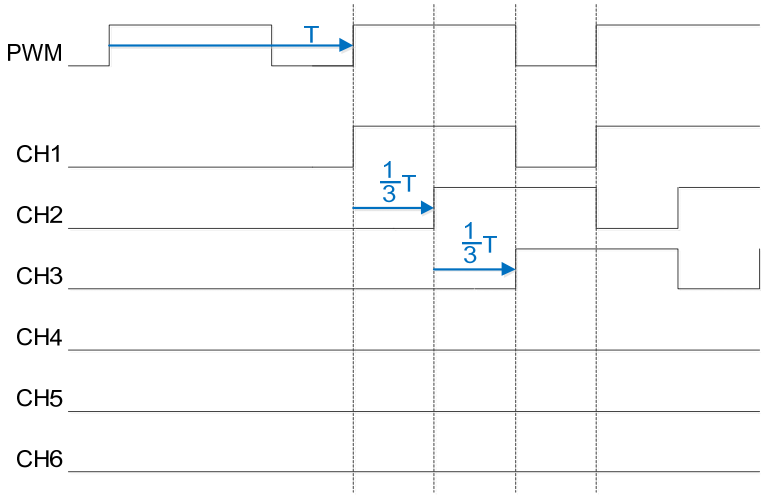
・LEDDIS=00h[All ch. ON]、LEDPHASE=03h



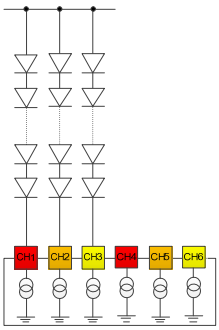
1/3T shift, mode which has 3 phases.



・LEDDIS=38h[CH4-6 OFF], LEDPHASE=03h



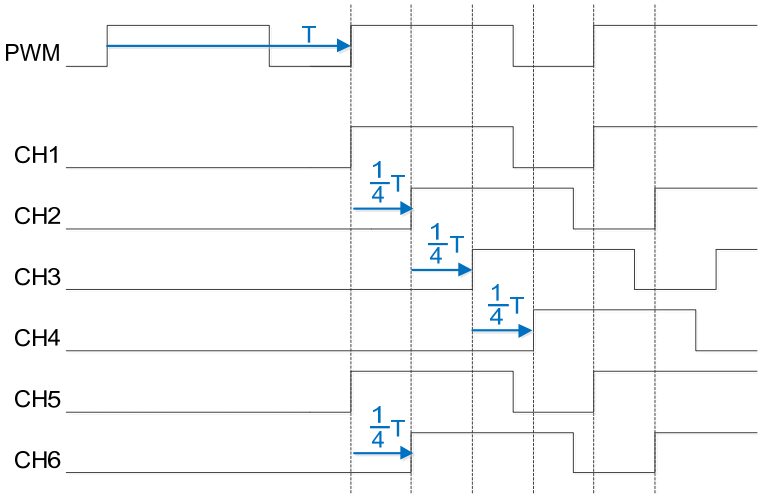
Case when CH4-6 are not in use.



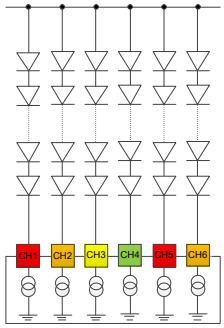
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4.Phase4 setting (1/4T shift)

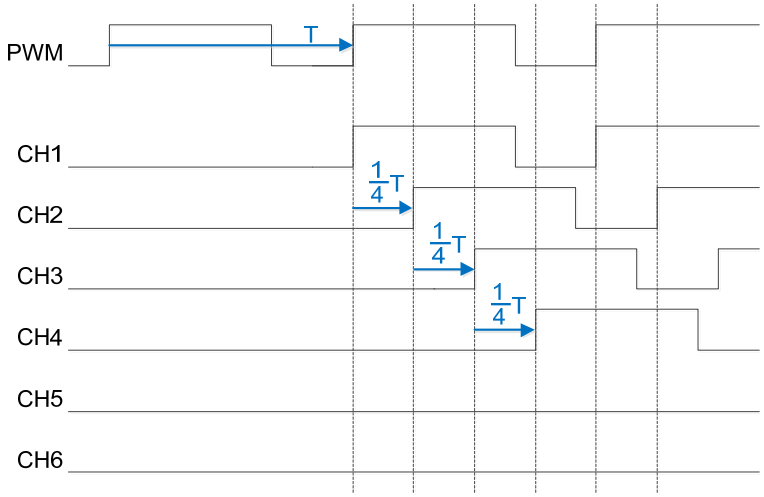
□LEDDIS=00h[All ch. ON], LEDPHASE=04h



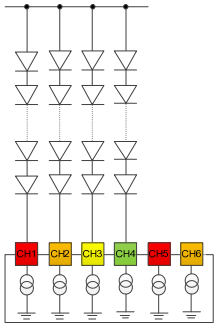
1/4T shift, mode which has 4 phases.



□LEDDIS=30h[LED5, 6 OFF], LEDPHASE=04h

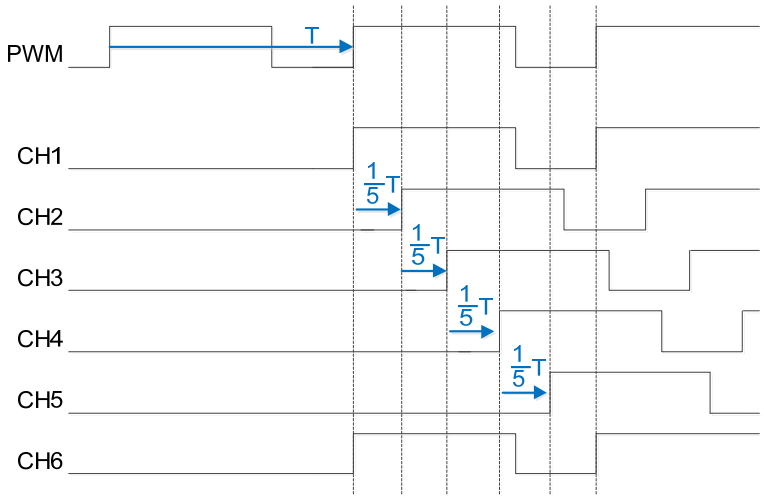


Case when CH5-6 are not in use.

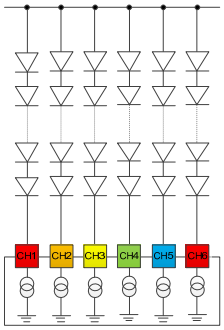


5. Phase5 setting (1/5T shift)

□LEDDIS=00h[All ch. ON], LEDPHASE=05h

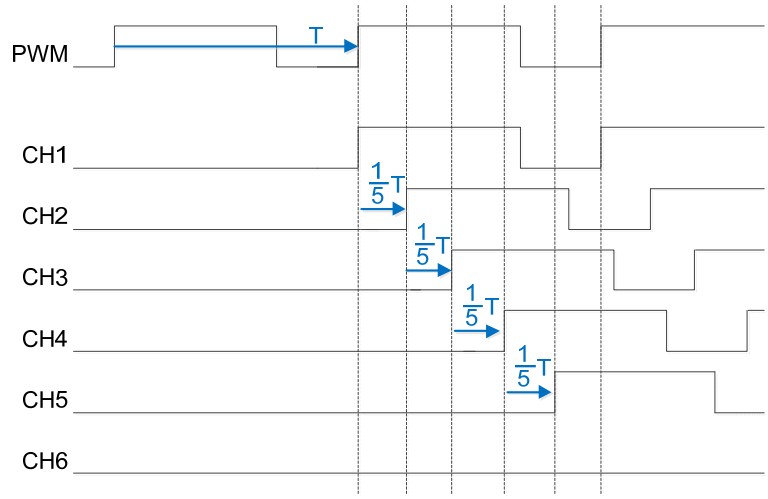


1/5T shift, mode which has 5 phases.

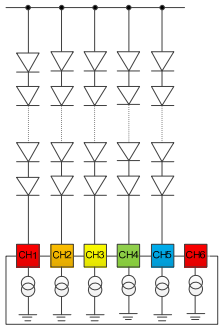


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□LEDDIS=20h[LED6 OFF], LEDPHASE=05h

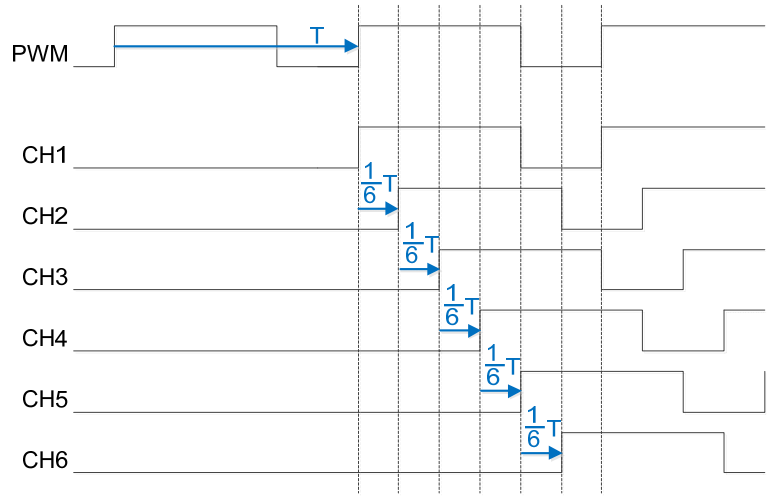


Case when CH6 is not in use.

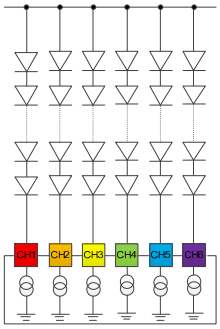


6. Phase6 setting (1/6T shift)

□LEDDIS=00h[All ch. ON], LEDPHASE=06h



1/6T shift, mode which has 6 phases.



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2 Understanding BD9423EFV

2.1 Pin description

1 pin. VCC

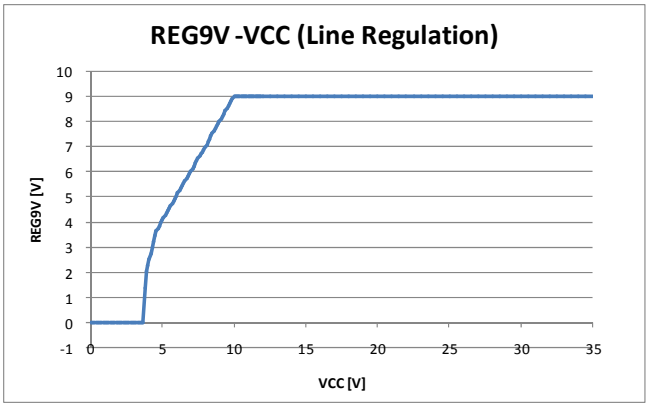
Power supply terminal of IC. The input range is 9 to 35V.
The operation starts over VCC＝7.5V (typ) and the system stops under VCC=7.2V (typ).

2 pin. FAIL

FAIL signal output terminal (OPEN DRAIN). NMOS is OPEN at the normal operation therefore FAIL pin is Hi-Z. It becomes FAIL=L at the abnormal detection. It is possible to select the FAIL type from latch type (FAIL_MODE=L) or one shot pulse (FAIL_MODE=H). Please refer to the detail explanation ＜FAIL_MODE terminal＞.

3 pin. REG9V

REG9V is a 9V output pin used delivering 20mA at maximum: Using at a current higher than 20mA may affect the reference voltage within IC.
The characteristic of VCC line regulation at REG9V is shown as figure. VCC must be used in more than 10.5V for stable 9V output.
Install an oscillation prevention ceramic capacitor (1.0μF to 10μF) nearest to VREG between VREG-AGND terminals.



4 pin. N.C

Non-connect pin. Please set it the open state or deal with connecting the GND.

5 pin. N

Gate driving output pin of external NMOS of DC/DC converter with 0 to 9V (REG9V) swing. Output resistance of source is 2.5Ω (typ), sink 3.0Ω (typ) in ON state. The oscillation frequency is set by a resistance connected to RT pin. For details, see the explanation of <RT terminal>.

6 pin. PGND

Power GND terminal of output terminal, N driver.

7 pin. CS

Inductor current detection resistor connecting terminal of DC/DC current mode. It transforms the current flowing through the inductor into voltage by sense resistor R_{CS} connected to CS terminal, and this voltage is compared with that set in the error amplifier by current detection comparator to control DC/DC output voltage. RCS also performs overcurrent protection (OCP) and stops switching action when the voltage of CS terminal is 0.45V (typ) or higher (Pulse by Pulse).
And this terminal switch the master mode and the slave mode. When the slave mode is set, please set OPEN as for CS pin. It can be set either with external pin or I2C setting by below setting.

State	Master/Slave setting method
Without DVDD or with DVDD (MSTSLVSEL=0)	CS pin
With DVDD (MSTSLVSEL=1)	I2C (05h, Bit4)

8 pin. OVP

OVP terminal is the detection terminal of overvoltage protection (OVP) and short circuit protection (SCP) for DC/DC output voltage.
OVP detection voltage can be adjusted the register OVPSET.
Depending on the setting of the FAIL_MODE terminal, FAIL and CP terminal behave differently when an abnormality is detected. For details, see the table for each protection operation is described in section 3.2 and 3.3.

9 pin. FAIL_MODE

Output mode of FAIL can be change by FAIL_MODE terminal.
When FAIL_MODE is in Low state, the output of FAIL terminal is the latch mode. FAIL terminal is latched if the CP charge time completed. Once IC is latched, even if the abnormal state is canceled, IC keeps stopping.
When FAIL_MODE is in Hi state, the output of FAIL terminal is one shot pulse mode. At detected abnormality, firstly FAIL is in Low state. FAIL returns to Hi-Z if abnormality through the reset active time is released after CP charge time. In this mode, there is no latch stop for protection operation in IC. Monitoring the FAIL with the Microcomputer, decide to stop working IC.
For FAIL_MODE=H when the detection sequence, see the explanation of section 3.8.4.
Changing FAIL_MODE during operating application is prohibited.

10 pin. AGND

GND for analog system inside IC.

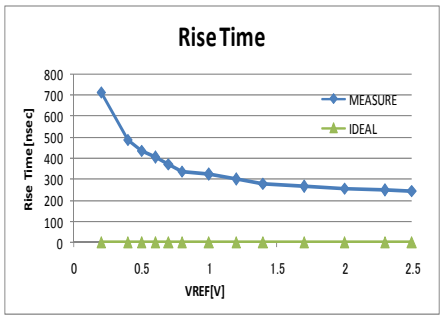
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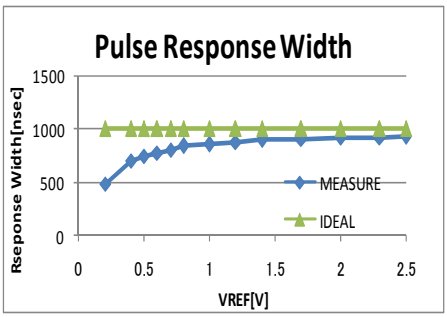
11 - 16pin. LED1 - LED6

LED constant current driver output terminal. Setting of LED current value is adjustable by setting the ADIM voltage and connecting a resistor to S terminal. For details, see the explanation of <PIN.25 to 30 S / PIN.35 ADIM>.
The PWM dimming frequency of LED current driver and upper/lower limit of the duty need to be set in a manner that necessary linearity of PWM dimming characteristics can be secured referring to the following figures:

Start/Stop time of constant current driver

Start-up time depends on the ADIM value; the response becomes quick, so that voltage is high.
In the way of reference, the current response upon application of current rise rate and pulse PWM1μs (current pulse) to describe the dependence of ADIM. It needs to be adequately verified with an actual device because the response rate may vary with application conditions.





17 pin. STB

ON/OFF setting terminal for IC, which can be used to perform a reset at shutdown.
(Caution) The voltage of STB input in the sequence of VCC→STB.
(Caution) Voltage input in STB terminal switches the state of IC (IC ON/OFF). Using the terminal between the 2 states (0.8V to 2.0V) needs to be avoided.

18 pin. DVDD

Standard oscillator power supply terminal for I2C interface and phase shift usage. Please input the voltage in range of 2.7V to 3.6V. Please set it to GND during standalone control without I2C setting.

19, 20 pin. SDA, SCL

I2C interface terminal. Please refer to “1.12 I2C Command Interface” for input signal regulation.
Please connect to GND during standalone mode when I2C setting is not using.

21 pin. PWM

ON/OFF terminal of LED driver: it inputs PWM dimming signal directly to PWM terminal and change of DUTY enables dimming. High/Low level of PWM terminal is shown as follows:

Status	PWM voltage
LED ON	PWM = 1.5V to 20V
LED OFF	PWM = -0.3V to 0.8V

There are standalone mode (without DVDD) which is the signal is directly input to PWM terminal and I2C mode (with DVDD) which is each CH set by phase difference.

Please refer to “1.14 PWM phase shift setting” for PWM terminal function of I2C mode.
This function operates during DVDD is being input and the cautions are as below. Please be noted that this function does not depend on phase shift amount.
(Caution 1) Possible phase shift frequency range is 100Hz to 25kHz.
(Caution 2) When input the signal around PWM=100%, please do not input the pulse lower than 157ns for Low interval. This is to correctly recognize the Low interval.
The following is the DUTY values which are not in the input range.
When PWM20kHz, above 99.68%, 100% and below (PWM=100% input is possible).
When PWM500Hz, above 99.992%, 100% and below (PWM=100% input is possible)
When there is no DVDD, the PWM terminal will directly make the constant current driver goes ON/OFF, therefore above caution 1 and 2 are not applicable.

22 pin. DGND

GND for DVDD power supply.

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23 pin. SUMPWM

The pin to judge whether there is High signal is input or not for PWM terminal. When using Master/Slave mode, connect the SUMPWM to each other, when any of PWM signal became High, SUMPWM will become high. Please refer to “3.4 operation during master slave connection” for more details.

Besides, switching Master/Slave mode can be done by register MSTSLVSEL using software control.

24 pin. FAIL_RST

Reset terminal of the protection circuit and FAIL terminal. Return the latch stopped protection block by setting the FAIL_RST to Hi. During Hi state, operation is masked by the latch system protection.

Moreover, it is possible to FAIL reset by register FAILSORST using software control. It can be set either with external pin or I2C setting by below setting.

Condition	FAIL_RST setting method
Without DVDD	FAIL_RST terminal
With DVDD	I2C (00h, Bit1)

When there is DVDD, please set by only I2C and set FAIL_RST to OPEN or GND.

Where there is DVDD and FAIL_RST=H, protection circuits will reset and LED will not light. The behaviors are slightly different compared to stated behaviors in above table.

25 – 30 pin. S1 - S6, 35 pin. ADIM

S terminal is a connecting terminal for LED constant current setting resistor, output current ILED is in an inverse relationship to the resistance value.

ADIM terminal is a terminal for analog dimming; output current ILED is in a proportional relationship to the voltage value to be input.

ADIM terminal is assumed that it is set by dividing the resistance with a high degree of accuracy, ADIM terminal inside the IC is in open state (High Impedance). It is necessary to input the external voltage by the divide resistance from the output of REG9V or use external voltage.

The relationship among output current ILED, ADIM input voltage, and RS resistance has the following equation. (during standalone)

$$I_{LED} = \frac{ADIM[V]}{RS[\Omega]} \times 0.2[A]$$

The voltage of S terminal is following equation:

$$VS = 0.2 \times ADIM[V]$$

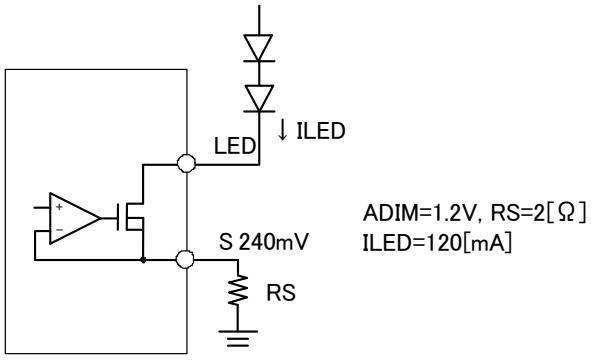


Figure 20. The relation of Sx pin and ADIM pin

(Caution) Rises LED current accelerate heat generation of IC. Adequate consideration needs to be taken to thermal design in use.

(Caution) When the ADIM voltage is changed rapidly, note that the necessary output voltage of the DC/DC converter largely changes because of LED VF change. In particularly, when the ADIM voltages become high to low, the LED terminal voltage can be higher transiently, so that may influence applications such as the LED short circuit protection. Adequate verification is necessary with an actual device as for analog dimming.

31 pin. CP

Terminal setting the timer latch for the abnormal detection. After the detection of LED short, LED open and SCP, it charges by the constant current 3.0μA to the external capacitor. When the CP terminal voltage reaches 3.0V (typ), the IC is latched and FAIL terminal operates (at FAIL_MODE=L).

The CP time can be adjusted by the register CPADJ.

32 pin. SS

Terminal setting the soft-start time of DC/DC converter. It performs constant current charge of 3.0μA (typ) to the external capacitor connected with SS terminal, which enables soft-start of DC/DC converter.

Since the LED protection function (OPEN/SHORT detection) works when the SS terminal voltage reaches 4.0V (typ) or higher, it must be set to bring stability to conditions such as DC/DC output voltage and LED constant current drive operation, etc.

The SS time can be adjusted by the register SSADJ.

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33 pin. FB

Output terminal of the error amplifier of current mode DC/DC converter.
The voltage of LED terminal which is the highest VF voltage among 6 LED strings and the voltage of LED_LV terminal become input of the error amplifier. The DC/DC output voltage is kept constant to control the duty of the output N terminal by adjusting the FB voltage.
The voltage of other LED terminals is, as a result, higher by the variation of Vf. Phase compensation setting is separately described in section 3.7.
The state in which all PWM signals are in LOW state brings high Impedance, keeping FB voltage. This action removes the time of charge to the specified voltage, which results in speed-up in DC/DC conversion.

34 pin. RT

RT sets frequency inside IC.
Only a resistor connected to RT determines the drive frequency inside IC, the relationship has the following equation: FCT is 200kHz at RT=100kΩ. (during standalone)
The oscillation frequency can be adjusted by the register FOSC. (during I2C control)

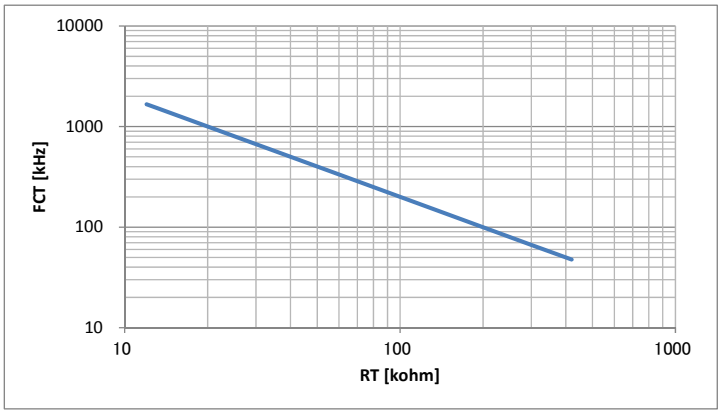


Figure 21. The relation of RRT and oscillation frequency

36 pin. ADIM_P

Analog dimming usage pulse signal terminal. When analog dimming signal is input by DC signal, please pull up above 6.5V (typ) and input DC signal at ADIM terminal. Please set the input voltage smaller than 18.0V during normal operation.
Based on ADIM_P input level, ADIM terminal function varies as below table. Pulse-DC conversion circuit is as shown in below figure.

ADIM_P input level	ADIM_P terminal function	ADIM terminal function	Needed signal from external
-0.3V<ADIM_P<5.5V	Analog dimming usage pulse signal input	Analog dimming usage DC signal output	Analog dimming usage DUTY signal
6.5V<ADIM_P<18V	ADIM_P terminal function mask	Analog diming usage DC signal input	Analog dimming usage DC signal output

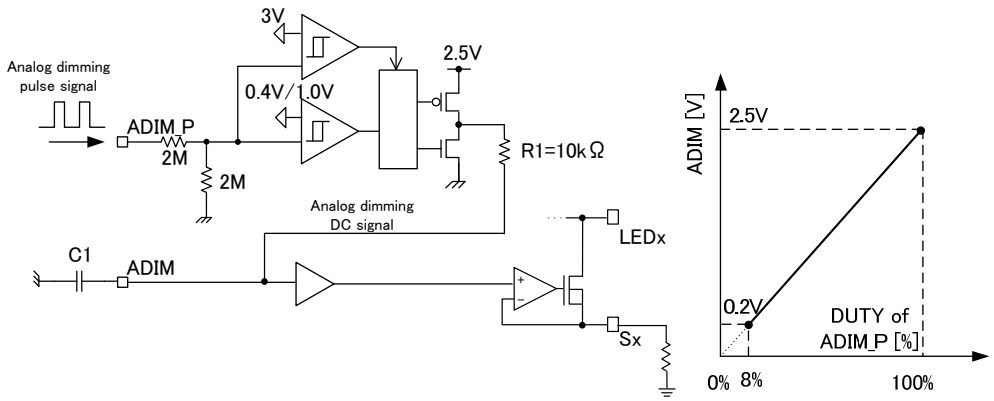


Figure 22. The relation of ADIM_P and ADIM

Based on this, it is possible to use both DUTY signal and DC signal for analog dimming usage signal input from external.

When using DUTY signal, input the DUTY signal at ADIM_P terminal around 3.0V amplitude. In order to keep the ADIM output not to become below 0.2V, the duty of 8% and above is needed to be input at ADIM_P.

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Input frequency is expected to be until 20kHz. When over 20khz is input, please be aware that the DC output error will become bigger over some percentage based on internal circuit delay effect. It also depends on input amplitude.
When the capacitance connected to ADIM terminal is too small, please be aware since it is possible that the ripple at ADIM terminal will become bigger and LED current different will get bigger.

When using DC signal, input the DC signal at ADIM terminal after ADIM_P terminal is pulled up by 6.5V and above.

By using two or more of this IC, when using DUTY signal for analog dimming, the configuration will be as shown in the right figure. Channel-to-channel error can be reduced since it uses a common circuit for pulse-DC conversion circuit.
Pulse-DC conversion circuit is defined by R1 and C1 constant values and output the DC at ADIM terminal. Increasing the C1 will make the generated ripple at ADIM becomes smaller, plus the response speed also will be slower.
Besides, when ADIM terminal is pulled down by a resistor, please be aware the voltage different since the resistor R1 is as shown in above figure.

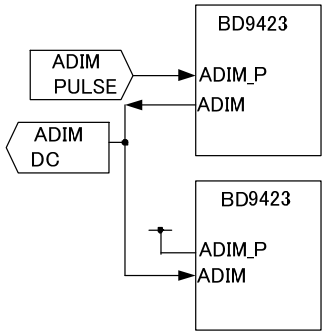
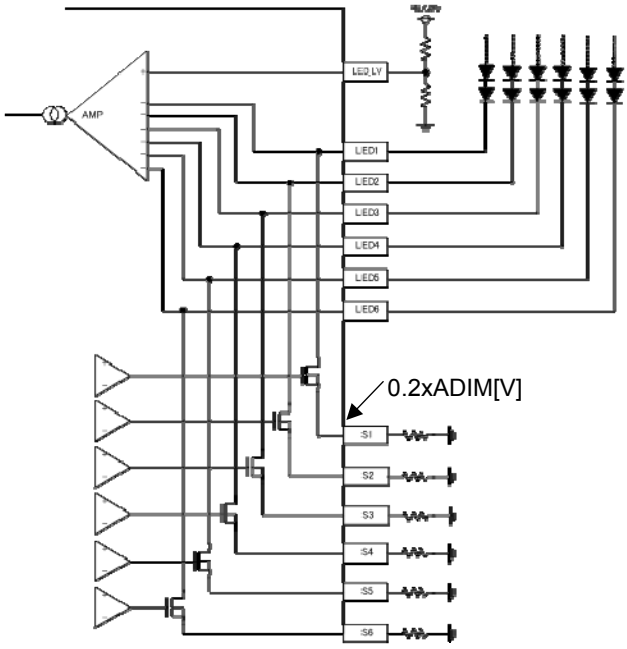


Figure 23. The example of analog dimming by duty signal with more than two IC

37 pin. LED_LV

LED_LV terminal sets the reference voltage error amplifier. LED_LV terminal is assumed that it is set by dividing the resistance with a high degree of accuracy, LED_LV terminal inside the IC is in open state (High Impedance). It is necessary to input voltage to divide the resistance from the output of REG9V or use external power source. Using the terminal in open state needs to be avoided.
According to output current, lowering LED_LV voltage can reduce the loss and heat generation inside IC. However, it is necessary to ensure the voltage between drain and source of FET inside IC, so LED_LV voltage has restriction on the following equation.
VLED_LV ≧ (LED-terminal voltage S) + 0.2 × ADIM [V]
For example, at ILED = 100mA setting by ADIM=1V, from figure the voltage between LED and S terminal is required 0.47V, so LED_LV voltage must be at least a minimum of 0.67V.



ILED	100mA	150mA	200mA	250mA
Needed LED-S terminal voltage (include temperature variety)	0.47V	0.71V	0.95V	1.19V

(Caution) Please make it linear interpolation for the middle of ILED.

(Caution) Rises in VLED_LV voltage and LED current accelerate heat generation of IC. Adequate consideration needs to be taken to thermal design in use.
(Caution) LED_LV voltage is not allowed setting below 0.3V.
(Caution) LED current by raising LED_LV voltage can flow to MAX 400mA, use with care in the dissipation of the package.

It is possible to set the LED_LV voltage setting by I2C. It can be set either with external pin or I2C setting by below setting.

Condition	LED_LV setting method
Without DVDD or without DVDD (LEDLVSET[3:0]=0000)	LED_LV terminal
With DVDD (except LEDLVSET[3:0]=0000 setting)	I2C (08h, Bit3-0)

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38 pin. LSP

Terminal which sets LED SHORT detection voltage: The input impedance of LSP pin is High Impedance, because it is assumed that the input of LSP terminal is set by dividing the resistance with a high degree of accuracy.
During standalone mode, it is necessary to input voltage to divide the resistance from the output of REG9V or use the external voltage. Using the terminal in open state needs to be avoided. Set LSP voltage in the range of 0.8V to 3.0V.
The relationship between LSP voltage and detect voltage of LED SHORT protection has the following equation.

$$LED_{SHORT} = 5 \times VLSP \quad [V]$$

LED_{SHORT} : LSP detection Voltage, VLSP : LSP terminal voltage

There are some restrictions for condition on short LED detection. For details, see the explanation of section 3.8.5
It can be set either with external pin or I2C setting by below setting.

Condition	LSP setting method
Without DVDD or with DVDD (LSPSET[3:0]=0000)	LSP terminal
With DVDD (except LSPSET[3:0]=0000 setting)	I2C (04h, Bit3-0)

39 pin. UVLO

UVLO terminal of the power of step-up DC/DC converter: at 2.5V (typ) or higher, IC starts step-up operation and stops at 2.3V or lower (typ). UVLO can be used to perform a reset after latch stop of the protections.
The power of step-up DC/DC converter needs to be set detection level by dividing the resistance.

40 pin. AGND

Analog GND for IC.

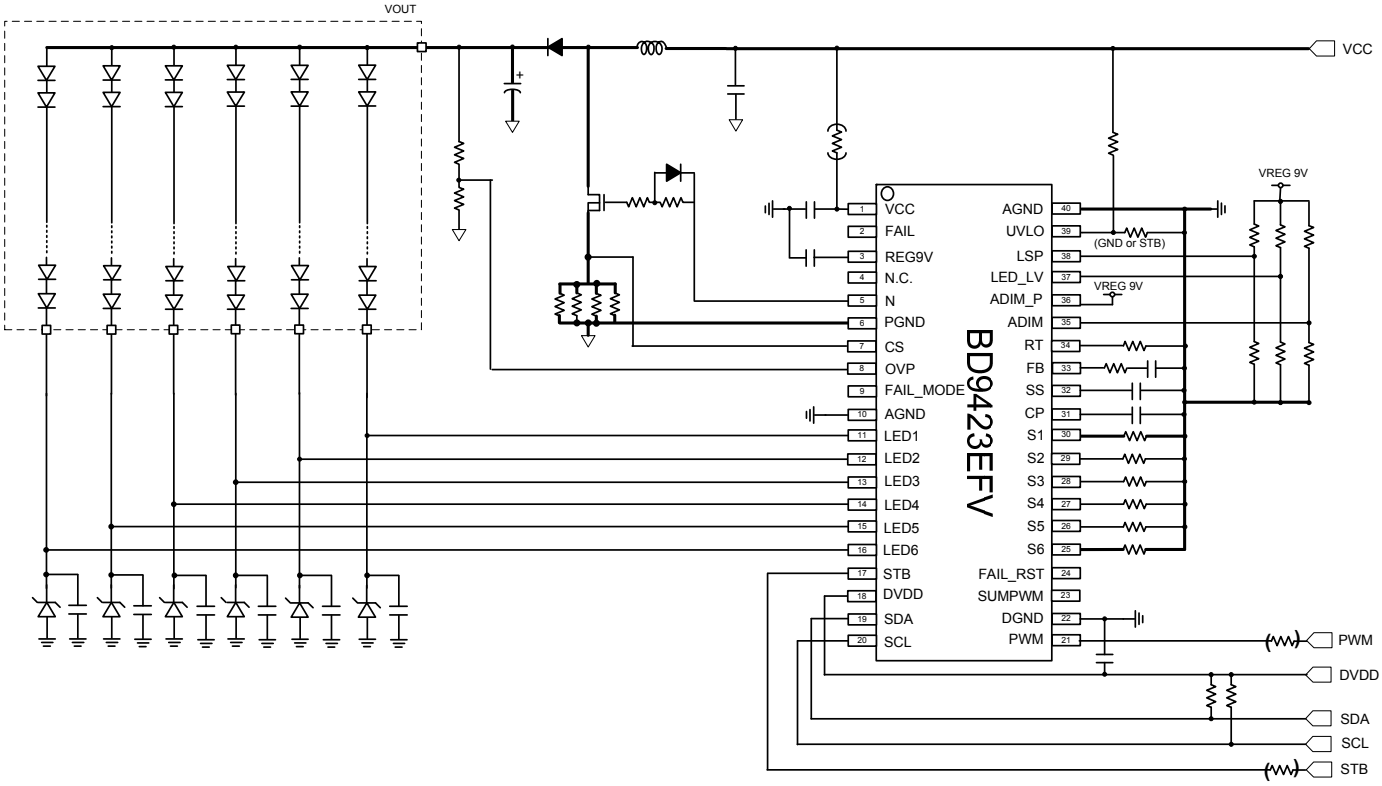
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3. Application Of BD9423EFV

3.1 Application circuit diagrams

Below are some examples using the basic application BD9423EFV.

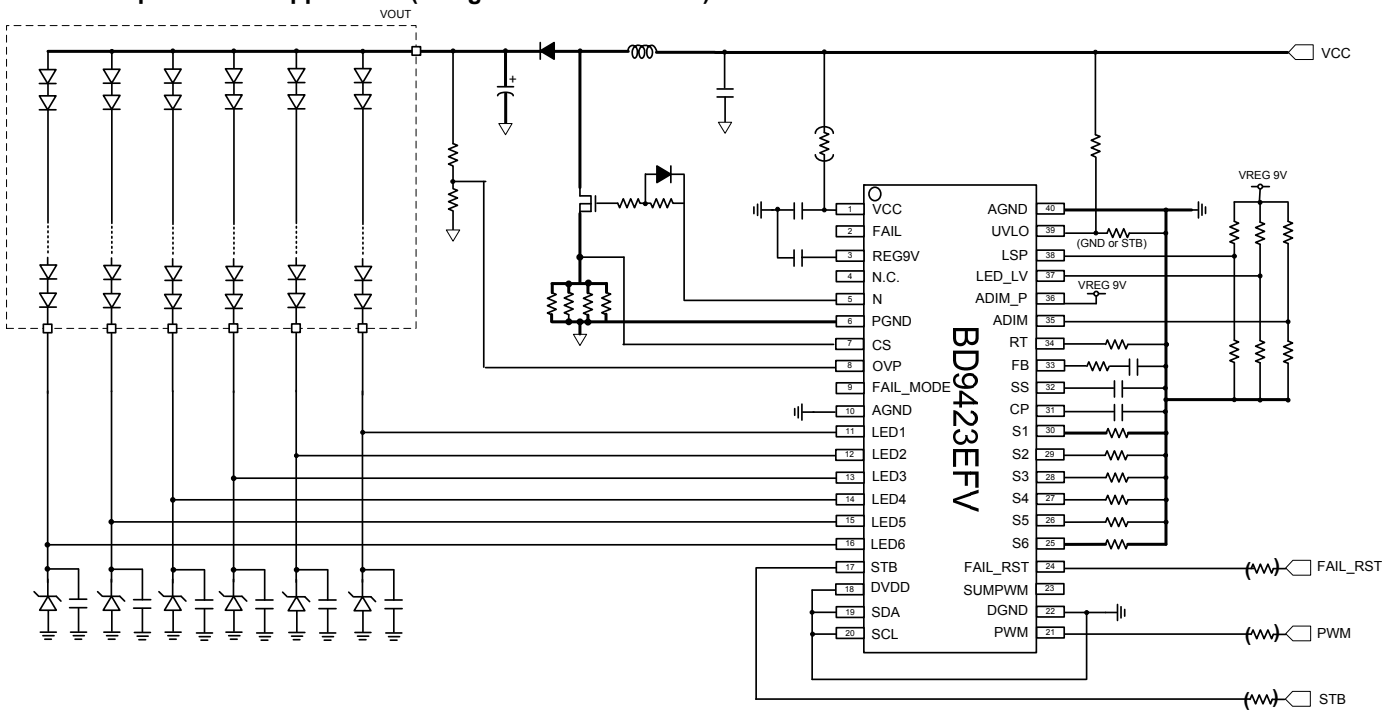
3.1.1 Example of basic application (using I2C control)



The basic configuration example of peripheral circuit using I2C interface control.

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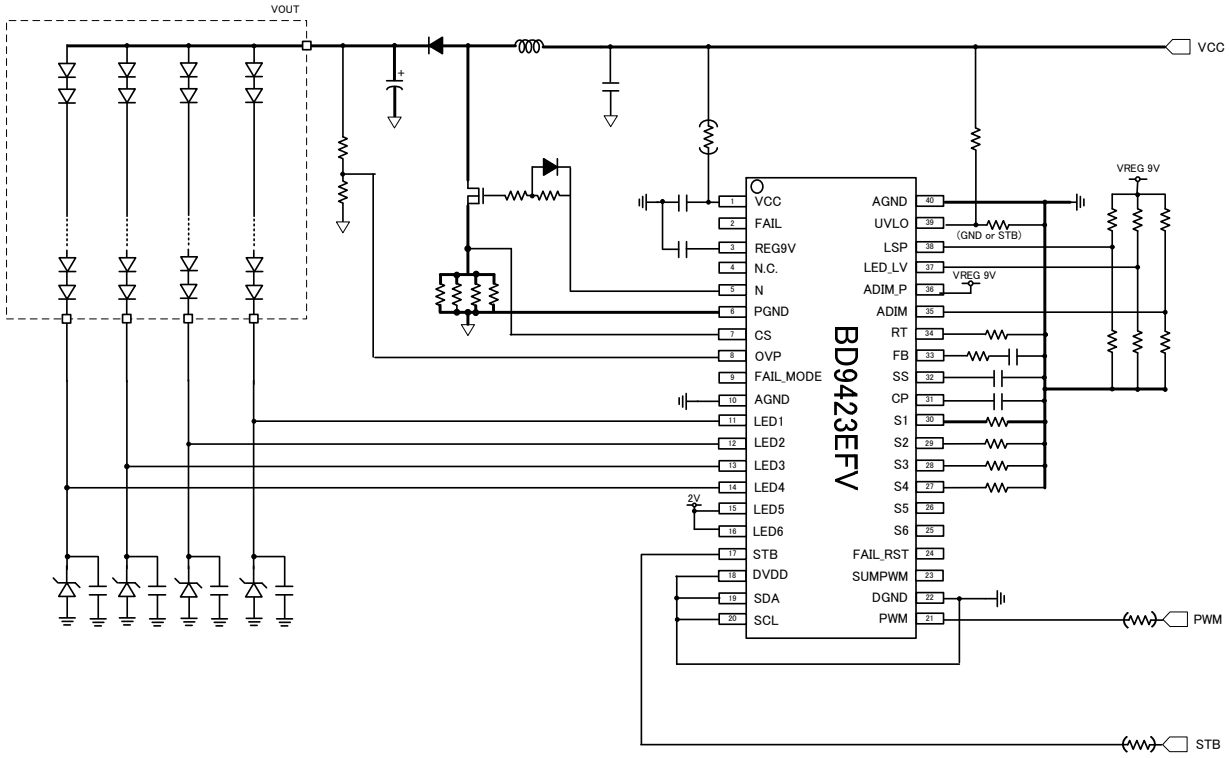
3.1.2 Example of basic application (using standalone control)



The basic configuration example of peripheral circuit without using I2C interface control but standalone control. Please connect the I2C related terminals (DVDD, SDA and SCL) to GND.

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3.1.3 Application example when there is unused LED channel during standalone (example: 5ch and 6ch are unused).

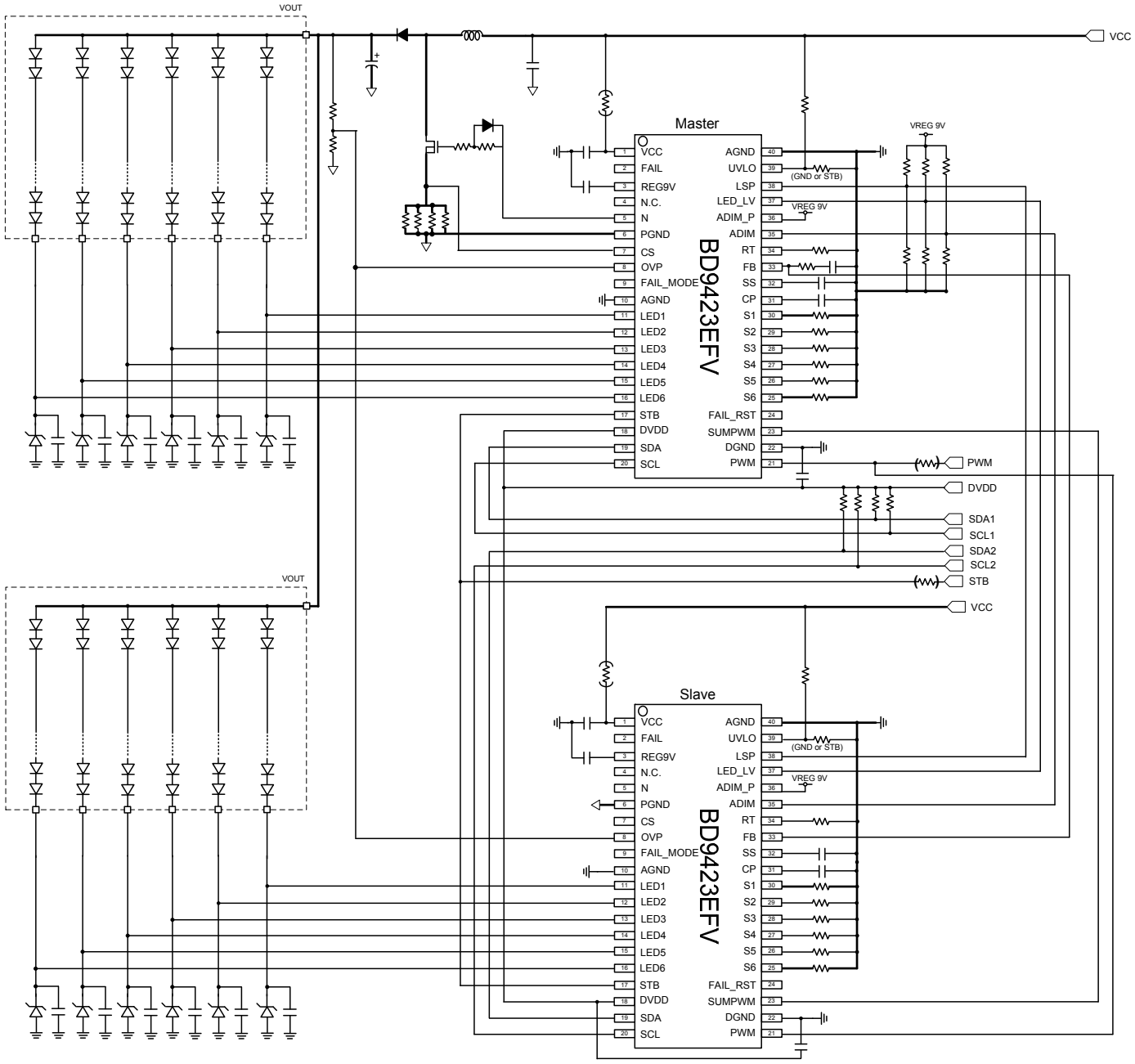


This is an example of the circuit when there is unused LED channel during standalone.
Please set Sx terminal to OPEN.
Pull up LEDx terminal with 2V to avoid abnormality.

I2C setting is done by the register.

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3.1.4 Example of Master/Slave connection



This is the example for Master/Slave connection.
SUMPWM terminal is connected between each IC,
CS terminal of slave side is set to OPEN for the slave recognition.
When the configuration is by I2C, SDA and SCL input are needed for both IC since the slave address is same.

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3.2 Protection operation during FAIL latch output (FAILMODE=L)
3.2.1 List of the protection function detection condition (typ condition)

Protection name	Detection pin name	Detection condition		Release condition	Protection type
			PWM		
LED Open	LEDx	LEDx < 0.2V(4clk) SS>4.0V	High	LEDx > 0.2V(3clk)	Stop the CH latch after the CP charge is completed
LED Short	LEDx	LEDx > 5×VLSP(4clk) SS>4.0V	High	LEDx < 5×VLSP(3clk)	Stop the CH latch after the CP charge is completed
UVLO	UVLO	UVLO < 2.3V	-	UVLO > 2.5V	Auto-feedback (System reset)
OVP	OVP	OVP > 3.00V	-	OVP < 2.95V	Auto-feedback
SCP	OVP	OVP < 0.2V	-	OVP > 0.2V	Stop all CH latch after the CP charge is completed.
OCP	CS	CS > 0.45V	-	CS < 0.25V	Pulse by Pulse

It is possible to reset with the FAIL_RST terminal to release the latch stop.

3.2.2 List of protection function operation

Protection function	Protection function operation			
	DC/DC converter	LED driver	SS terminal	FAIL terminal
STB	Stop	Stop	Discharge	Hi-Z
LED Open	Normal operation (Stop when all LED CH stop)	Stop after CP charge (Latch operation)	Normal operation (Discharge when all LED CH stop)	Low after CP charge is completed (Latch operation)
LED short	Normal operation(Note1)	Stop after CP charge (Latch operation)	Normal operation	Low after CP charge is completed (Latch operation)
UVLO	Stop	Stop	Discharge	Low
OVP	Stop N output	Normal operation	Normal operation	Hi-Z
SCP	Stop N output	Stop after CP charge (Latch operation)	Discharge after latch	Low after CP charge is completed (Latch operation)
OCP	Stop the N output (Pulse by Pulse)	Normal operation	Normal operation	Hi-Z

（Note1）Short protection doesn't hang when becoming remainder 1ch. DCDC output (LED anode voltage) will decrease along with LED SHORT.

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3.3 Protection operation during FAIL one shot output (FAILMODE=H)

3.3.1 List of the protection function detection condition (typ condition)

Protection name	Detection pin name	Detection condition		Release condition	Protection type
			PWM		
LED Open	LEDx	LEDx < 0.2V(4clk) SS>4.0V	High	LEDx > 0.2V(3clk)	Auto-feedback after CP charge and reset active time completed.
LED Short	LEDx	LEDx > 5×VLSP(4clk) SS>4.0V	High	LEDx < 5*VLSP(3clk)	Auto-feedback after CP charge and reset active time completed.
UVLO	UVLO	UVLO < 2.3V	—	UVLO > 2.5V	Auto-feedback (System reset)
OVP	OVP	OVP > 3.0V	—	OVP < 2.95V	Auto-feedback
SCP	OVP	OVP < 0.2V	—	OVP > 0.2V	Auto-feedback after CP charge and counter are completed
OCP	CS	CS > 0.45V	—	CS < 0.25V	Pulse by Pulse

3.3.2 List of the protection function operation

Protection function	Protection function operation			
	DC/DC converter	LED driver	SS terminal	FAIL terminal
STB	Stop	Stop	Discharge	Hi-Z
LED Open	Normal operation (Stop when all CH stop)	Normal operation	Normal operation	Low
LED Short	Normal operation	Normal operation	Normal operation	Low
UVLO	Stop	Stop	Discharge	Low
OVP	Stop the N output	Normal operation	Normal operation	Low
SCP	Stop the N output	Normal operation	Normal operation	Low
OCP	Stop the N output (Pulse by Pulse)	Normal operation	Normal operation	Hi-Z

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3.4 Operation during Master/Slave connection

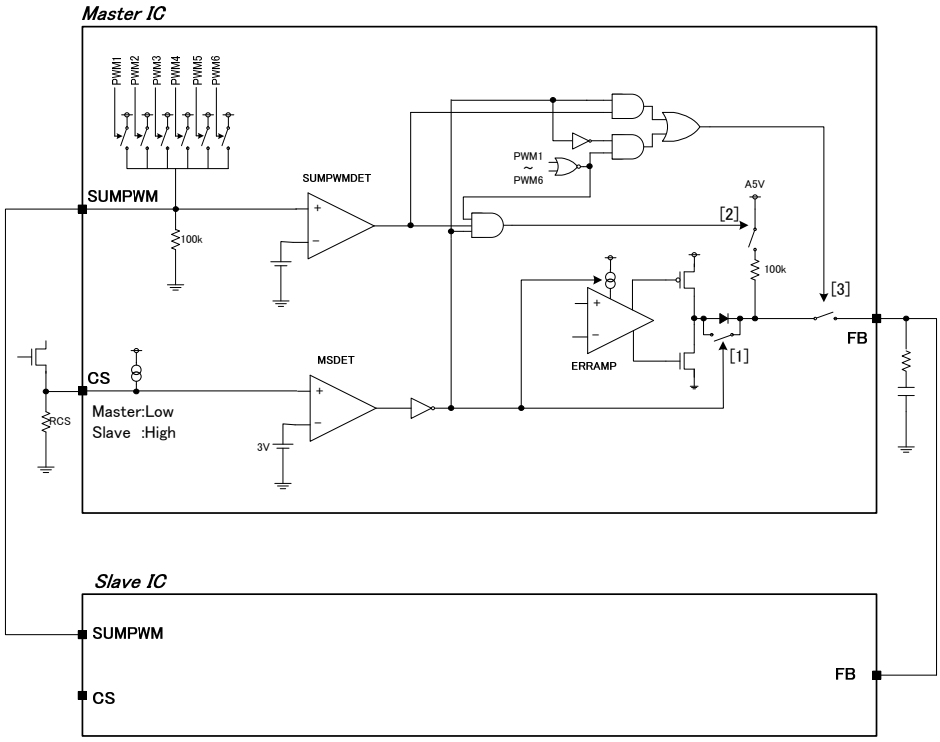


Figure 24. internal block for master slave function

BD9423EFV is built with a system that can drive multiple LED driver by one DCDC in Master from multiple connected BD9423EFV by using Master/Slave.
Herewith is the explanation on the operation of multiple connected IC using Master/Slave.

[MSDET] Master/Slave recognition usage comparator

Detect the CS terminal voltage, and judge by itself whether it is Master or Slave.
When using Master/Slave mode, Slave CS terminal is set to OPEN. Constant current is being supply to CS terminal by the internal IC, therefore CS terminal will be High.
A resistor is connected for DCDC switching current detection usage at Master CS terminal and swing in 0V to 0.45V range during operation.
The comparator will detect this voltage different and use it as Master/Slave recognition signal.

[SUMPWMDET] All PWM signals presence recognition usage comparator

At SUMPWM terminal, a switch and a pull down 100kΩ resistor which will ON when PWM signal is High and if over one PWM signal became High, SUMPWM terminal will become High.
Connecting the SUMPWM terminal in between of Master/Slave will make the judgment becomes possible if over one PWM signal from all PWM signal from Master/Slave became High or not.

Error amplifier is decided based on two signals of MSDET and SUMPWM.

[1] Error amplifier output part with or without diode

If Slave mode is detected by the IC, a diode will be added at the error amplifier output and the supply at error amplifier sink side will be cut.

[2] Error amplifier output part with or without pull up resistor

IC Master mode recognition and over one Slave PWM becomes ON, a pull up resistor will be added.

[3] Error amplifier output FB output cut

In case of Master recognition, when all Master/Slave PWM signals become OFF, error amplifier output will be cut.
In case of Slave recognition, when all Slave side PWM signals become OFF, error amplifier output will be cut.

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The summary for above contents is shown in below table.

Master / Slave mode usage

		Master			Slave		
		Error amplifier output			Error amplifier output		
Master	Slave	Source	Sink	Pull up	Source	Sink	Pull up
PWM ON	PWM ON	○	○	—	○	—	—
PWM ON	PWM OFF	○	○	—	—	—	—
PWM OFF	PWM ON	○	○	○	○	—	—
PWM OFF	PWM OFF	—	—	—	—	—	—

Only Master mode usage

		Master		
		Error amplifier output		
Master		Source	Sink	Pull up
PWM ON		○	○	—
PWM OFF		—	—	—

In addition, Master/Slave recognition is possible to set by register MSTSLVSEL using software control. Master/Slave recognition can be set by register MSTSLVSFT.
Please refer to section 3.1.4 for circuit example.

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3.5 Setting of the external components (typ Condition)

3.5.1 Setting the start-up operation and SS terminal capacitance

The explanation of start up sequence for this IC.

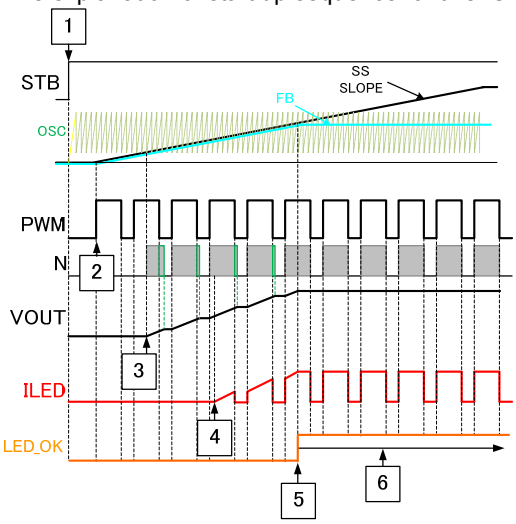


Figure 25. Waveform during start up

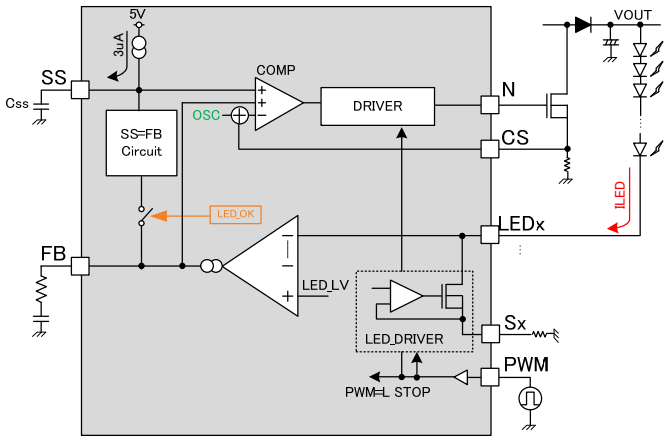


Figure 26. Circuit operation during start up

Start up sequence

1. Basic voltage REG9V will start up at STB=H.
2. At first timing of PWM=H, SS will start to charge. At this time, the equal circuit of slow start SS voltage and FB voltage will operate and without depending on PWM logic, it will become FB=SS.
3. Since FB=SS will achieve internal sawtooth-ish waveform lower limit, N pulse is generated and VOUT will start to increase.
4. VOUT is increased and LED current will achieve starting to flow voltage.
5. When LED current became over constant current, FB=SS circuit will be separated and start up operation is finished.
6. After that, based on feedback operation of ISENSE terminal, it will be normal operation. In addition, even there is no flow of LED current, when SS becomes over 4.0V, SS=FB circuit control will stop.

SS terminal capacitance setting method (during standalone)

In addition, Master/Slave recognition is possible to set by register MSTSLVSEL using software control. Master/Slave recognition can be set by register MSTSLVSFT.

Based on previous stated sequences, when start up is finished during FB=SS, it is possible to think that the startup time Tss is from STB=On to when FB voltage achieved the feedback point.

If SS terminal capacitance is Css and the FB terminal feedback voltage after the start up is VFB, the Tss time will be as below equation.

$$T_{ss} = \frac{C_{ss}[\mu F] \times VFB[V]}{3[\mu A]} \quad [sec]$$

Reducing too much of Css, inrush current will flow to inductor during start up. However, increasing too much of Css could make the LED lights step-by-step. The constants to set the Css vary based on required charateristics and also the factors such as boost ratio, output capacitance, DCDC frequency, LED current and etc. are different, therefore please perform actual evaluation.

3.5.2 Setting the LED current (ADIM pin, Sx pin) (during standalone)

Firstly, decide the ADIM terminal input voltage. When using analog dimming, please be aware of ADIM terminal possible input range (0.2V to 2.5V), and decide voltage at normal.

For this IC, Sx terminal is the standard point to control LED constant current. Sx terminal voltage should be controlled to become 1/5 of ADIM voltage. When ADIM=1V, Sx=0.2V. Therefore, if "*Rs*" is the resistance for Sx terminal to the GND, ADIM terminal load applied voltage is "V_{ADIM}", and the target LED current is "I_{LED}", the equation will be as below.

$$R_S\ [ohm] = \frac{V_{ADIM}[V]}{I_{LED}\ [A] \times 5}$$

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3.5.3 Setting the LED short detect voltage (LSP pin) (during standalone)

LED short detection voltage can be changed arbitrarily. It is possible by setting LSP pin within range (0.8V to 3.0V). The relationship between LED short detection voltage "VLEDshort" and LSP pin voltage "VLSP" is as follows.

$$V_{LSP}\,[V] = \frac{VLED_{short}\,[V]}{5}$$

Possible range setting for LSP pin setting range is 0.8V to 3.0V, and for VLEDshort is 4V to 15V.

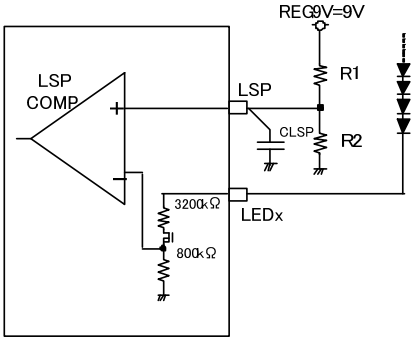


Figure 27. LSP setting circuit

Equation of setting LSP detect voltage

When the detection voltage VLSP of LSP is set up by resistance division of R1 and R2 using REG9V, it becomes like the following formula.

$$VLED_{short} = \left(REG9V \times \frac{R2}{R1+R2} \right) \times 5 \quad [V]$$

(Caution) Also including the variation in IC, please also take the part variation in a set into consideration for an actual constant setup, and inquire enough to it.

3.5.4 Timer latch time (CP pin) (during standalone)

When various abnormalities are detected, the source current of 3.0μA is first flowed from CP pin. BD93973EFV don't stop by latch, unless abnormal state continues and CP pin voltage reaches continuous 2V.

With the capacity linked to CP pin, the un-responded time from detection to a latch stop. The relationship between the un-responded time Tcp and CP pin connection capacitor Ccp is as follows.

$$C_{CP}\,[F] = \frac{T_{CP}\,[S] \times 3.0 \times 10^{-6}[A]}{3.0\,[V]}$$

3.5.5 DCDC operation frequency (RT pin) (during standalone)

The oscillation frequency of the DCDC output is decided by RT resistance.

BD9397EFV is designed to become a 200kHz setup at the time of 100kΩ.

RT resistance and frequency have a relation of an inverse proportion, and become settled as the following formula.

$$R_{RT} = \frac{2.0 \times 10^{10}}{f_{SW}} [\Omega]$$

Here, f_{sw} =DCDC comparator external oscillator [Hz]

Please connect RT resistance close as much as possible from RT pin and an AGND pin.

3.5.6 Maximum DCDC output voltage (Vout, max)

The DCDC output maximum voltage is restricted by Max Duty of N output. Moreover, the voltage needed in order that Vf may modulate by LED current also with the same number of LEDs. Vf becomes high, so that there is generally much current. When you have grasped the variation factor of everything, such as variation in a DCDC input voltage range, the variation and temperature characteristics of LED load, and external parts, please carry out a margin setup.

3.5.7 Setting the OVP (during standalone)

Please input the voltage divided by the divider resistors at DCDC output line. In BD9423EFV, when OVP is detected, the instant stop of the N pin output is carried out, and voltage rise operation is stopped. But the latch stop by CP charge is not performed. If VOUT drops by naturally discharge, it is less than the hysteresis voltage of OVP detection and the oscillation condition is fulfilled, N output will be resumed again.

Equation of setting OVP detect

$$VOVP = 3.0 \times \frac{R1+R2}{R2} \quad [V]$$

N pin output is suspended at the time of SCP detection, it stops step-up

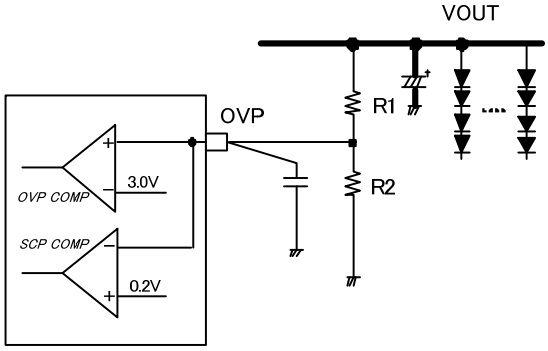


Figure 28. OVP setting circuit

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operation, and the latch protection by CP timer.

Equation of setting SCP detection

$$VSCP = 0.2 \times \frac{R1 + R2}{R2} \quad [V]$$

3.5.8 FAIL logic

FAIL signal output pin. The relation logic and the output state is shown below table. Refer the section 3.2, 3.3 for the relation between this pin logic and the kind of the detection of abnormalities, FAIL_MODE.

State	FAIL output
In Normal state, In STB=L	Hi-Z
When an abnormality	GND Level (300Ω typ)

3.5.9 Set the UVLO

UVLO terminal for step-up DCDC converter power supply. Operation starts more than 2.5V (typ) and operation stops less than 2.3V (typ).
Since UVLO terminal is high impedance terminal, there is no pull down at internal. Therefore, please set the voltage since the potential is not determined at open state.

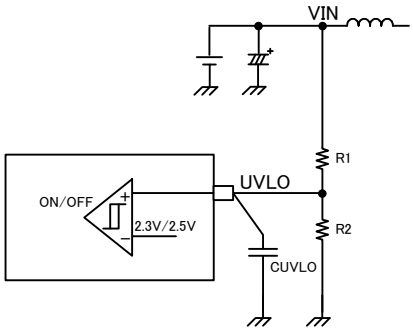


Figure 29. UVLO setting circuit

Equation of UVLO detection setting

VIN decreases, when UVLO detection voltage is VIN_{DET}, the R1 and R2 setting is as below.

$$R1 = R2[k\Omega] \times \frac{VIN_{DET}[V] - 2.3[V]}{2.3[V]} \quad [k\Omega]$$

Equation of UVLO release setting

Based on above equation, when R1 and R2 are decided, the UVLO release voltage will be as follow equation.

$$VIN_{CAN} = 2.5[V] \times \frac{R1[k\Omega] + R2[k\Omega]}{R2[k\Omega]} \quad [V]$$

3.5.10 Setting of the LED_LV voltage (LED_LV pin)(during standalone)

LED_LV pin is in the OPEN (High Impedance) state.
LED_LV terminal is in open state (High Impedance). It is necessary to input voltage to divide the resistance from the output of REG9V or use external power source.

Equation of Setting LED_LV voltage

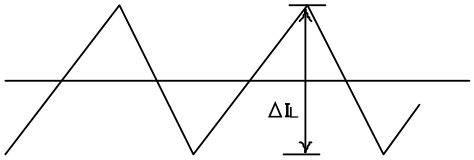
When LED_LV voltage is set up by resistance division of R1 and R2 using REG9V, the relation is following formula.

$$V_{LED_LV} = REG9V \times \frac{R2}{R1 + R2} [V]$$

(Caution) The setting constant should be adequately verified, considering IC tolerance and the components tolerance on application.

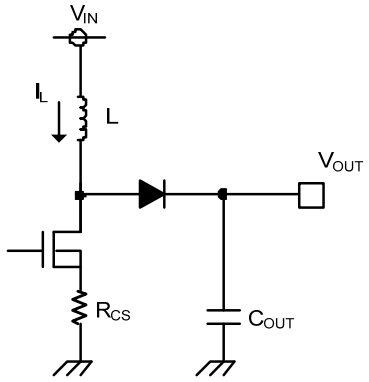
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3.6 Selecting of DCDC parts
3.6.1 Selecting inductor L



The value of inductor has a great influence on input ripple current. As shown in Equation (1), as the inductor becomes large and switching frequency becomes high, the ripple current of an inductor ⊿IL becomes low.

$$\Delta IL = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{L \times V_{OUT} \times f_{SW}} [A] \quad \cdots\cdots \quad (1)$$



When the efficiency is expressed by Equation (2), input peak current will be given by Equation (3).

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \quad \cdots\cdots \quad (2)$$

$$IL_{MAX} = I_{IN} + \frac{\Delta IL}{2} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{\Delta IL}{2} \quad \cdots\cdots \quad (3)$$

Here,
L: reactance value [H] V_{OUT}: DC/DC output voltage [V]
V_{IN}: input voltage [V]
L_{OUT}: output load current (total of LED current) [A]
I_{IN}: input current [A] F_{SW}: oscillation frequency [Hz]
Generally, ⊿IL is set at around 30 – 50 % of output load current.

Figure 30. Coil current and boost circit

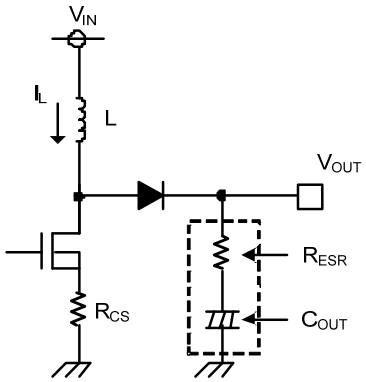
(Caution) Current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, resulting in decrease in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.
(Caution) To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected.

3.6.2 Selecting output capacitor C_{OUT}

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple voltage is high.
Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}} [V] \quad \cdots\cdots \quad (4)$$

R_{ESR}: equivalent series resistance of C_{OUT}



(Caution) Rating of capacitor needs to be selected to have adequate margin against output voltage.
(Caution) To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that current larger than set value flows transitionally in case that LED is provided with PWM dimming especially.

Figure 31. Output capacitance

3.6.3 Selecting switching MOSFET

Though there is no problem if the absolute maximum rating is the rated current of L or (withstand voltage of C_{OUT} + rectifying diode) VF or higher, one with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.
(Caution) One with over current protection setting or higher is recommended.
(Caution) Selection of one with small ON resistance results in high efficiency.

3.6.4 Selecting rectifying diode

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than withstand voltage of C_{OUT}, and low forward voltage VF especially needs to be selected.

3.6.5 Selecting MOSFET for load switch and its soft-start.

As a normal step-up DC/DC converter does not have a switch on the path from V_{IN} to V_{OUT}, output voltage is generated even though IC is OFF. To keep output voltage at 0 V until IC works, PMOSFET for load switch needs to be inserted between V_{IN} and the inductor. FAIL terminal needs to be used to drive the load switch. PMOSFET for the load switch of which gate-source withstand voltage and drain-source withstand voltage are both higher than V_{IN} needs to be selected.
To provide soft-start for the load switch, a capacitor must be inserted among gates and sources.

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3.7 How to set phase compensation

DC/DC converter application controlling current mode has each one pole (phase lag) f_p due to CR filter composed of output capacitor and output resistance (=LED current) and ZERO (phase lead) f_Z by output capacitor and ESR of the capacitor.
Moreover, step-up DC/DC converter has RHP ZERO f_{ZRHP} as another ZERO. The operation will be unstable when this ZERO point is applied. In order to prevent unstable operation of the RHP ZERO, here the phase compensation of control loop bandwidth fc is set to fc=f_{ZRHP} /5 (RHP ZERO frequency f_{ZRHP}).
Based on response speed consideration, since the constant is not applicable, please perform sufficient actual evaluation to confirm the characteristics.

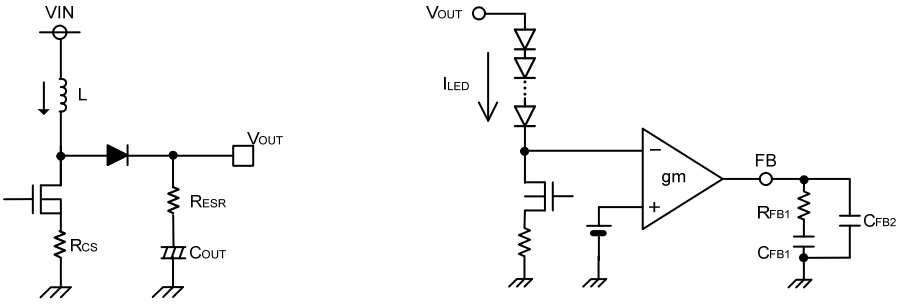


Figure 32. Output circuit and error amplifier circuit

i. Determine Pole f_p and RHP ZERO frequency f_{ZRHP} of DC/DC converter.

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Here, I_{LED} = Total LED current [A], $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous current mode)

ii. Determine Phase compensation to be inserted into error amplifier (with f_c set at 1/5 of f_{ZRHP})

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega]$$

$$C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_c} = \frac{5}{2\pi \times R_{FB1} \times f_{ZRHP}} [F]$$

Here, $gm = 1.036 \times 10^{-3} [S]$

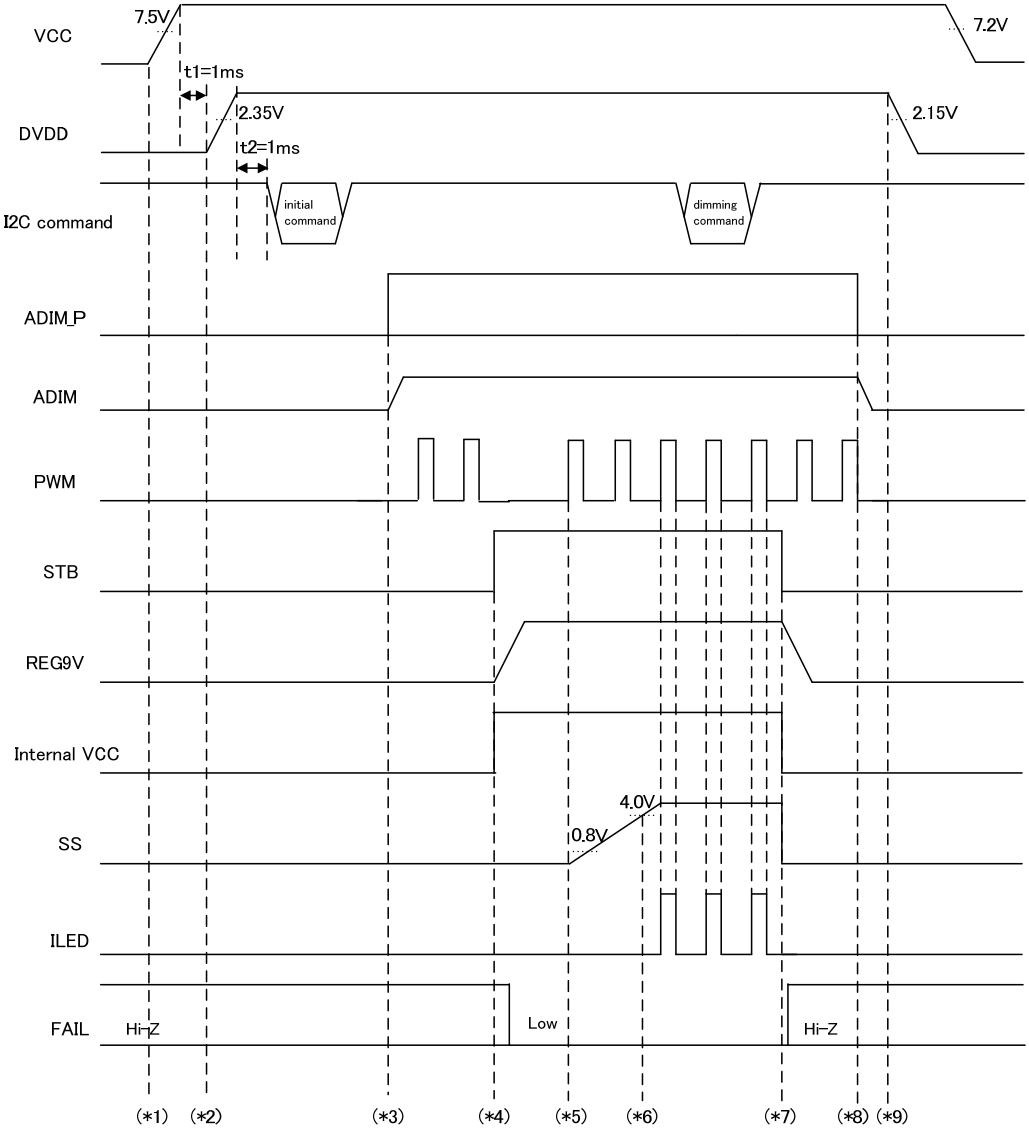
Above equations shows the LED lighting without the oscillation. In order to allow the response characteristic, even based on steep dimming signal, it is possible that the value might be different.
Though increase in R_{FB1} and decrease in C_{FB1} are necessary to improve transient response, it needs to be adequately verified with an actual device in consideration of variation between external parts since phase margin is decreased.

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3.8 Timing chart

3.8.1 Start up and shut down sequence 1 (PWM signal input before STB input)

Please refer to “1.13 register map” for figure initial command and dimming command differentiation.

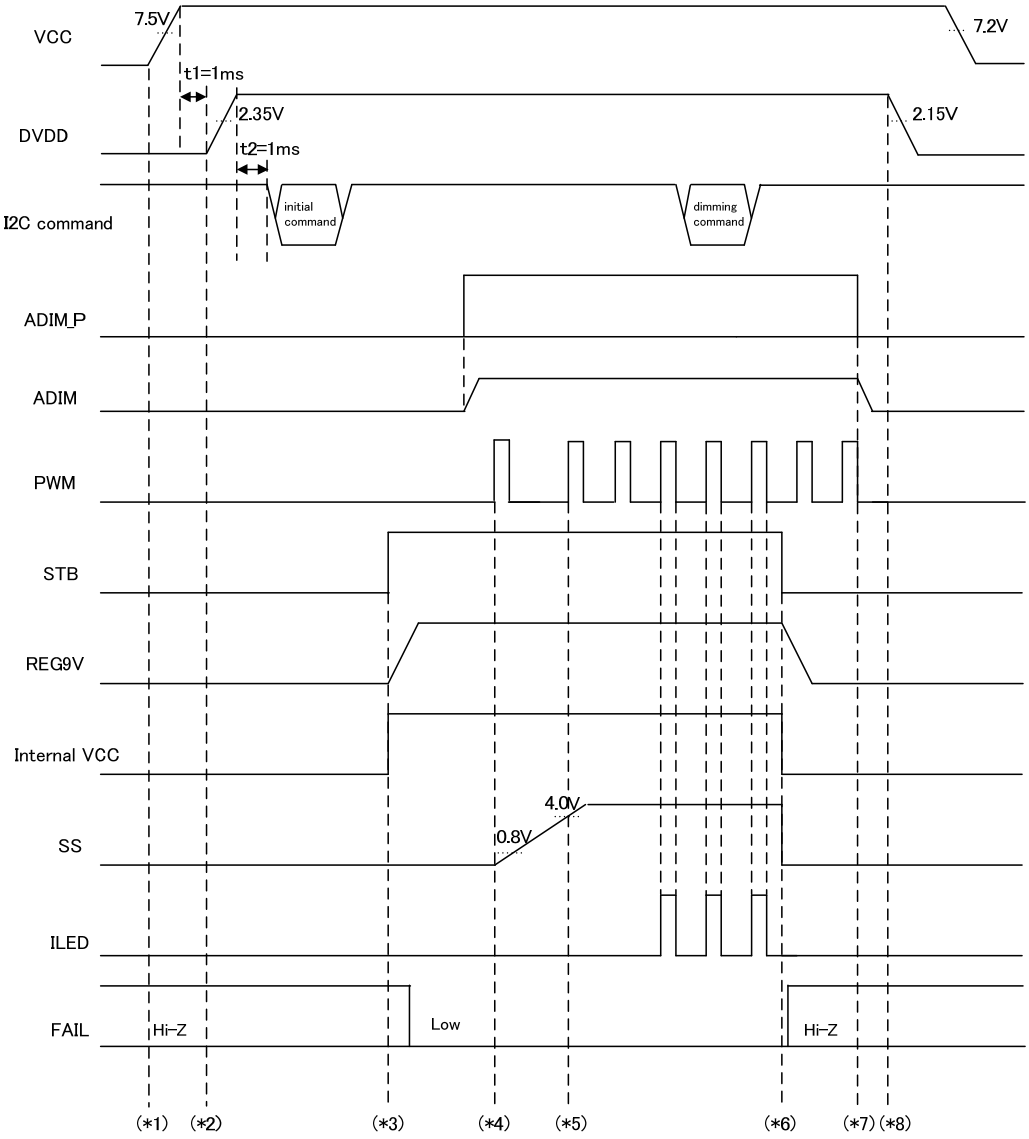


(*1)…When VCC is input stably, after minimum of t1=1ms, please input the DVDD. Please firstly ON and lastly OFF the VCC.
(*2)…When DVDD is input stably, after minimum of t2=1ms, please input the I2C command.
(*3)…Input the analog dimming signal (ADIM, ADIM_P) and PWM dimming signal. Above figure shows when ADIM_P is being input, but it will get charged by ADIM capacitance, thus ADIM voltage will gradually rise.
(*4)…Making STB=L→H will make REG9V to start up. During PWM signal is not being input condition, SS terminal will not get charged and booster will not start.
(*5)…SS terminal is started to charge at PWM=L→H edge and soft start interval will start. When SS terminal is below 0.8V, N terminal boost pulse will not be output. Regardless of PWM or OVP level etc., SS terminal will continuously 3μA charge.
(*6)…When SS terminal voltage Vss became 4.0V, soft start interval is finished, it should boost to set LED current flowing voltage. At this point, LED OPEN and SHORT abnormality detection will start. LED current, ILED in SS as in the description, the waveform is been simplified.
(*7)…When STB=L, instantly N=L and SS=L and boost operation will stop.

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3.8.2 Normal operation sequence 2 (PWM signal input after STB)

Please refer to “1.13 register map” for figure initial command and dimming command differentiation.



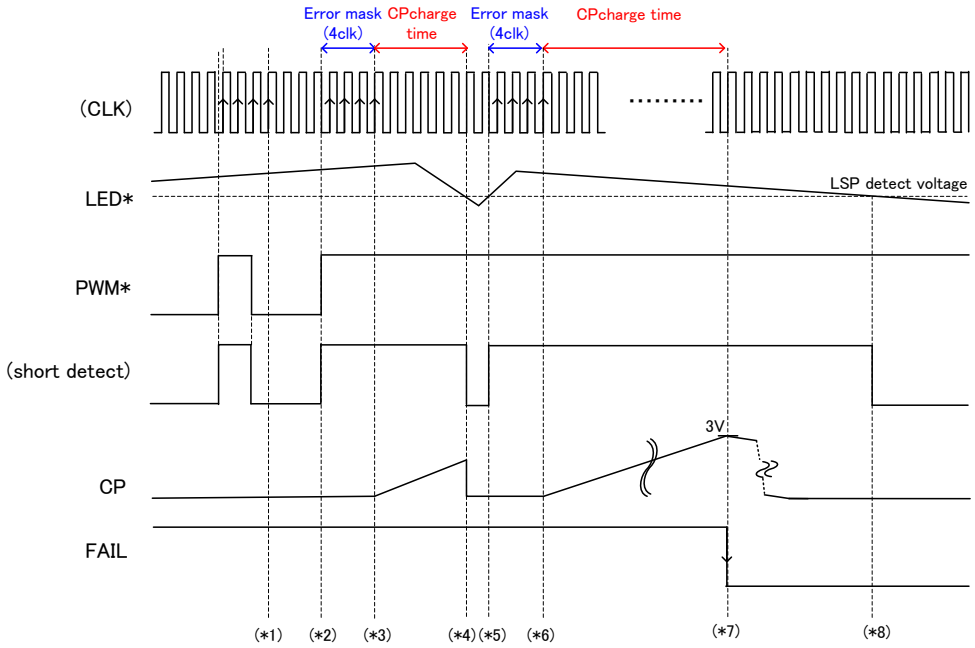
(*1)…When VCC is input stably, after minimum of t1=1ms, please input the DVDD. Please firstly ON and lastly OFF the VCC.
(*2)…When DVDD is input stably, after minimum of t2=1ms, please input the I2C command.
(*3)…Making STB=L→H will make REG9V to start up. During PWM signal is not being input condition, SS terminal will not get charged and booster will not start.
(*4)…SS terminal is started to charge at PWM=L→H edge and soft start interval will start. When SS terminal is below 0.8V, N terminal boost pulse will not be output. Regardless of PWM or OVP level etc., SS terminal will continuously 3μA charge.
(*5)…When SS terminal voltage Vss became 4.0V, soft start interval is finished, it should boost to set LED current flowing voltage. At this point, LED OPEN and SHORT abnormality detection will start. LED current, ILED in SS as in the description, the waveform is been simplified.
(*6)…When STB=L, instantly N=L and SS=L and boost operation will stop.

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3.8.3 During FAIL_MODE=L protection operation states transition sequence

CP is performed when abnormality is detected and will stop after certain constant time. The operation will remain stop even abnormality is released. Please also refer to section 3.2 condition table.

Below shows the LED short protection chart. CLK has same frequency as DCDC oscillating frequency.



(*1)…CP will not charge when PWM=H interval is 4count and below.

(*3)…When abnormality state (LEDx>5*VLSP) of PWM=H interval is 4count and above is continued, CP terminal charge will start. Once it started, the normal and abnormality is not judged based on PWM logic.

(*4)…During the CP charge, releasing the abnormality will make CP terminal discharge. (CP=Low)

(*5)…When abnormality happened again, until CP charge, the judgement takes place to determine whether the manner is same as (2*) when PWM=H is 4count and abnormal or not.

(*7)…When CP charge reached 3V, it will be judged as abnormal, the corresponded channel will stop and FAIL=Low will be output.

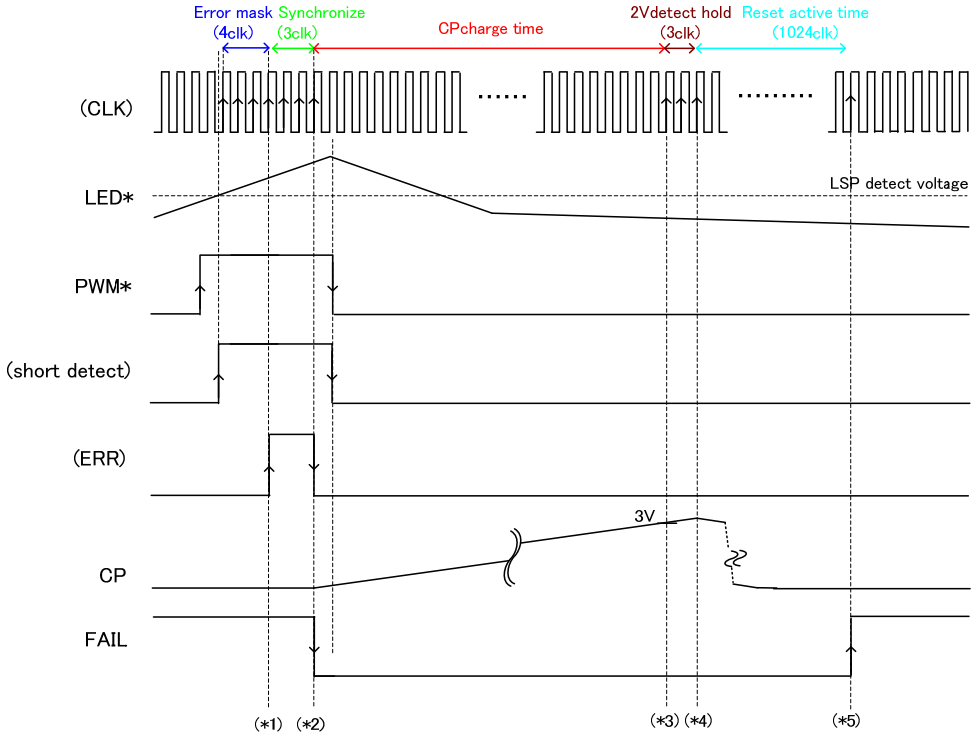
(*8)…Once it stopped, even the abnormal state is been released, the corresponded channel will remain stop (latch OFF). In order to re-start the operation, either STB is set to L or FAIL_RST=H (during standalone) is input, please set register FAILSORST=1. (during I2C)

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3.8.4 During FAIL_MODE=H protection operation sequences

If abnormality is detected, constant time of FAIL=Low will be output. FAIL output will return to FAIL=Hi-Z after "CP charge time and Reset active time" are passed from the abnormality is been released. In the meantime, we can assume that the stop signal is being input from external. Please refer to section 3.3 for condition table.
Below shows the LED short protection chart. CLK has same frequency as DCDC oscillating frequency.

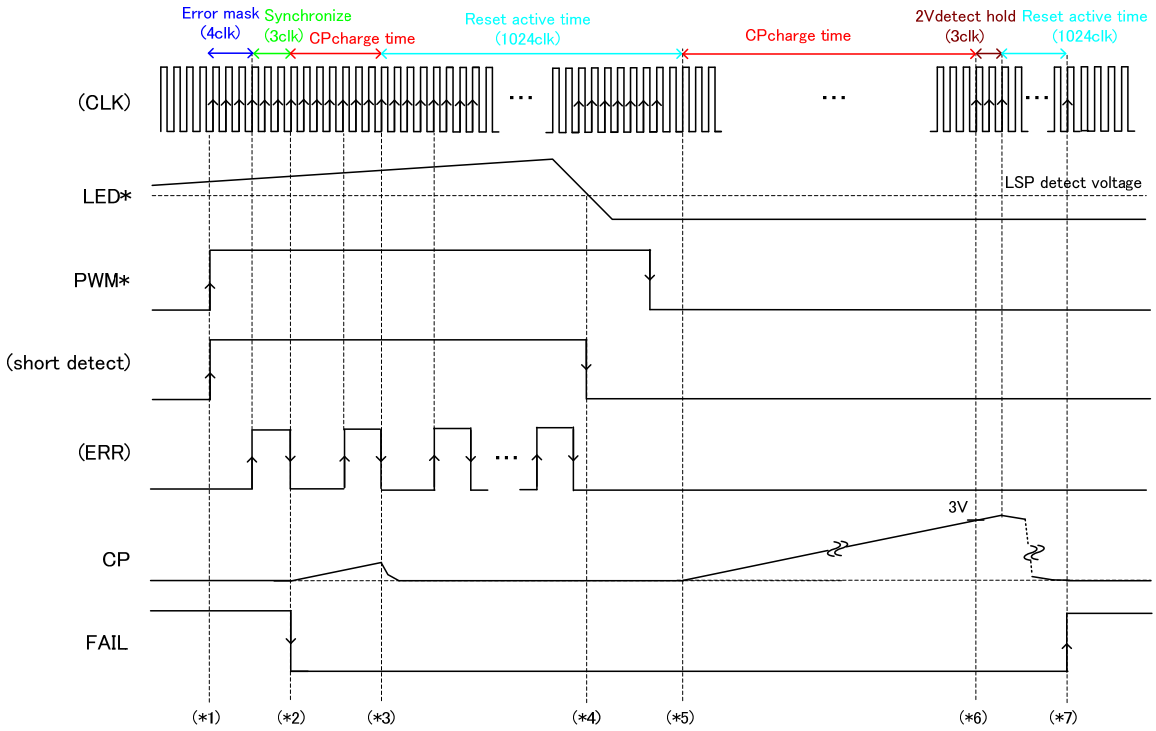
3.8.4.1 Basic operation (abnormal state instantly released)



(*1)…The internal during 4count and below will be masked even the abnormal condition is input. At 4count and above, internal signal will be ERR=H.
(*2)…When it continues and abnormal is input, and if 3count is been input, ERR will return to L then FAIL will be Low. CP charge will start. Here, after that abnormal is released instantly.
(*3)…When it reached at CP=3V, CP will discharge after 3count.
(*4)…When CP is discharged, reset effective timer (1024count) will operate and CP=Low and FAIL=Low is output.
(*5)…When reset active timer is finished, FAIL will return to Hi-Z.

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3.8.4.2 Abnormal state not instantly released



(*2)…When CP charge starts, ERR will return to L and FAIL will become Low. Here, abnormal state will continue and let say short detection=H.
(*3)…ERR signal will repeatedly become H and L and CP will discharge at second negative edge. Fail will remain L. Reset active timer (1024count) will operate, in the meantime CP=L, FAIL=L is being output.
(*4)…Abnormal state is been released and short detection will become L.
(*5)…Reset active timer will be finished, if it is normal operation, CP will charge again.
(*6)…When it reached at CP=3V, CP will be discharged after 3count.
(*7)…When reset active timer is finished, FAIL will return to Hi-Z.

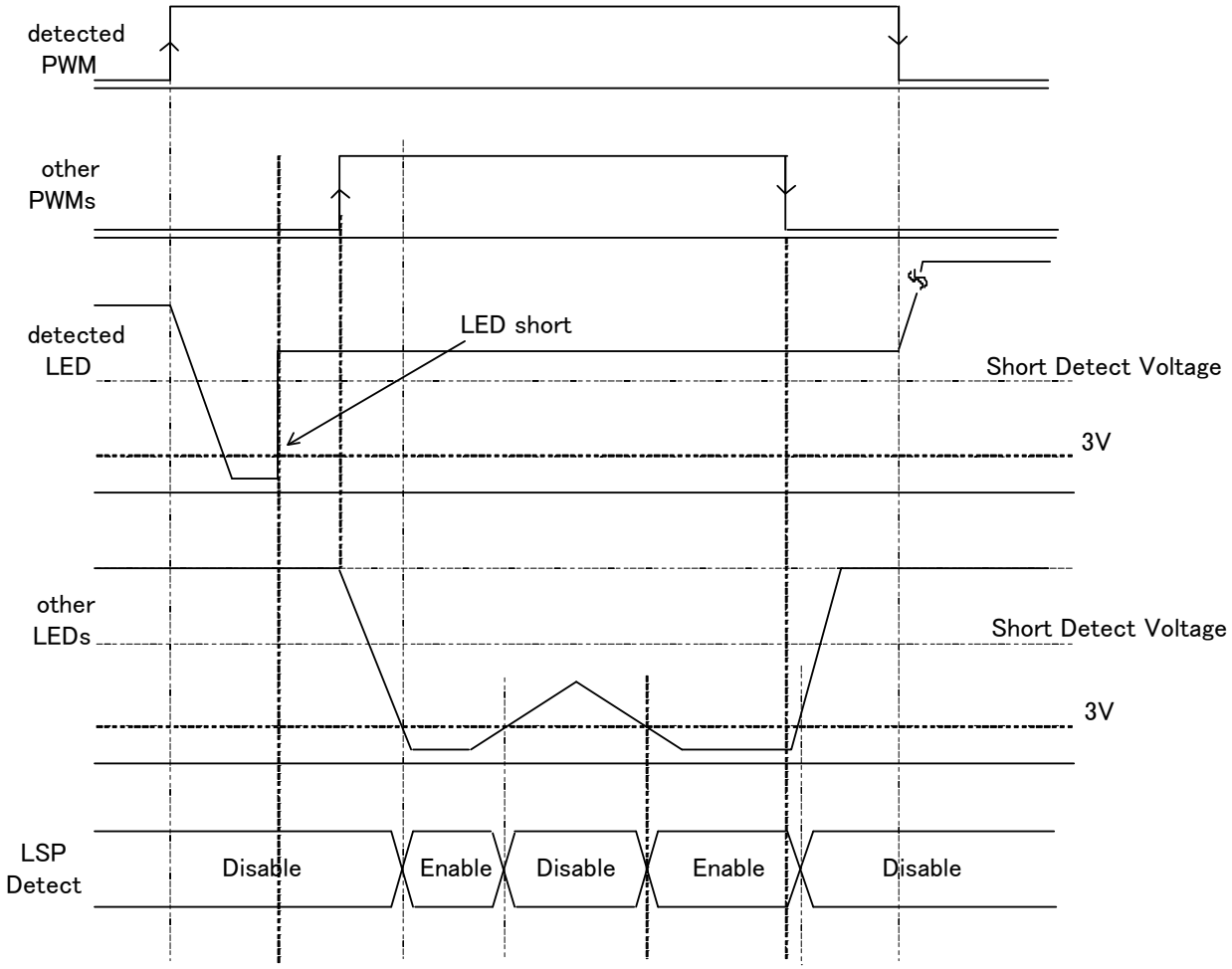
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3.8.5 LED SHORT detection

LED SHORT detection will not work as 1ch drive operation. Detection needs below conditions.

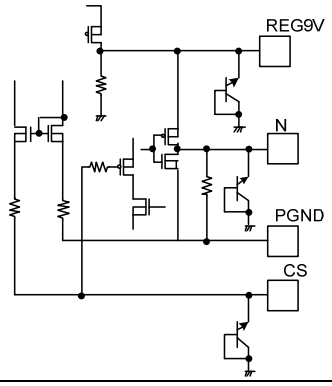
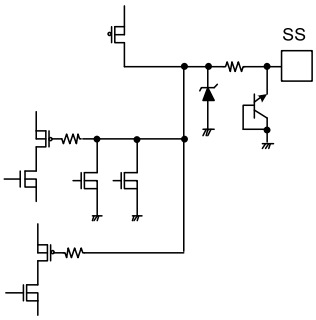
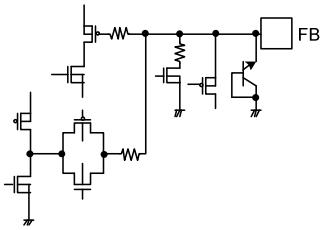
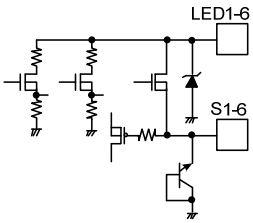
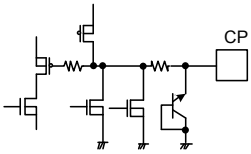
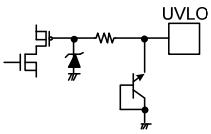
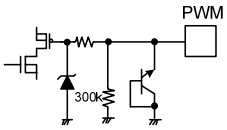
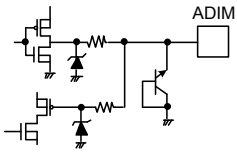
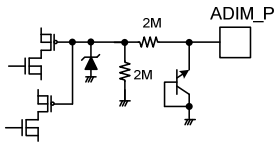
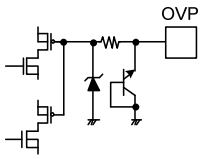
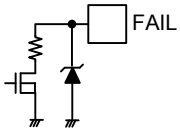
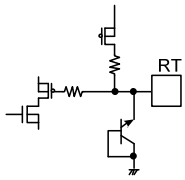
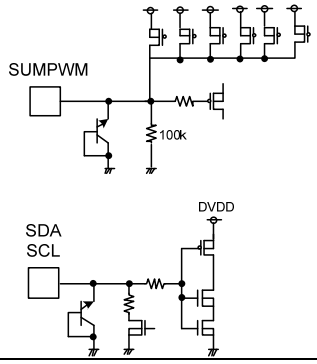
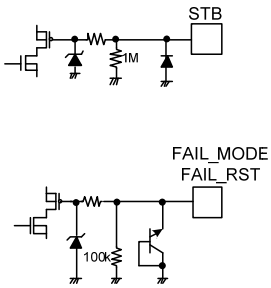
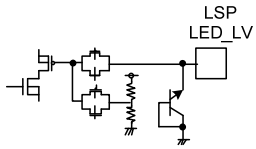
- Target CH detection is PWM=H and LED terminal voltage is over SHORT detection voltage.
- Other than that, any 1ch is PWM=H and LED terminal 3V and below.
- Above two conditions continuously with DCDC oscillator frequency over 4clk.

The detection sequences are as following. (4clk mask is not shown)



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3.9 I/O equivalent circuit diagram

REG9V / N / PGND / CS	SS	FB
		
LED1~6 / S1~6	**CP**	**UVLO**
		
PWM	**ADIM**	**ADIM_P**
		
OVP	**FAIL**	**RT**
		
SUMPWM / SDA / SCL	**STB / FAIL_MODE / FAIL_RST**	**LSP / LED_LV**
		

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

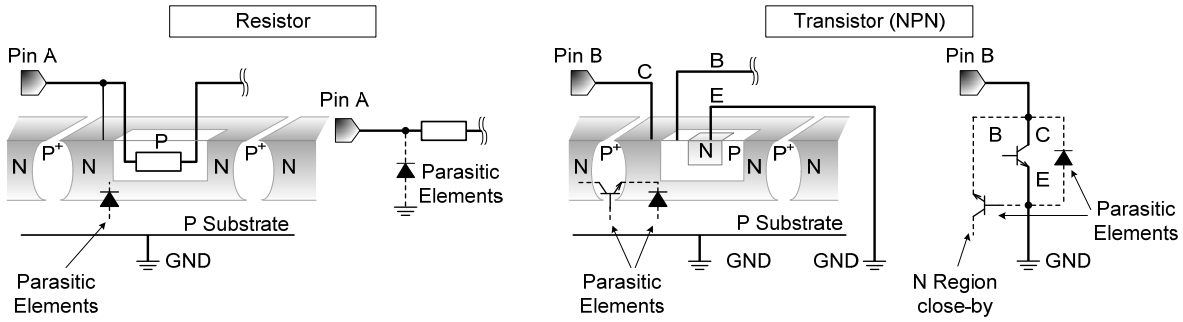


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

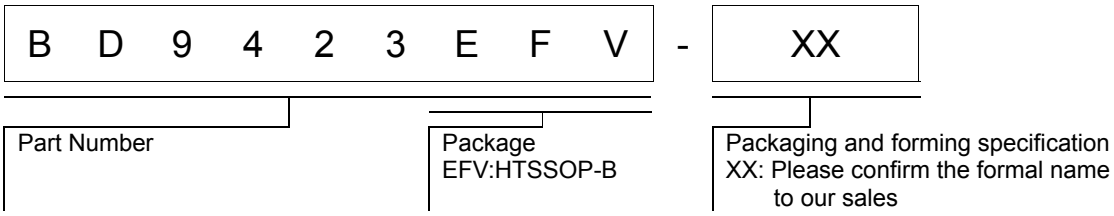
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

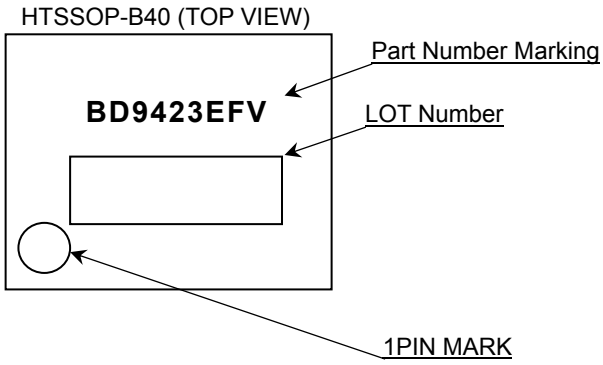
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information



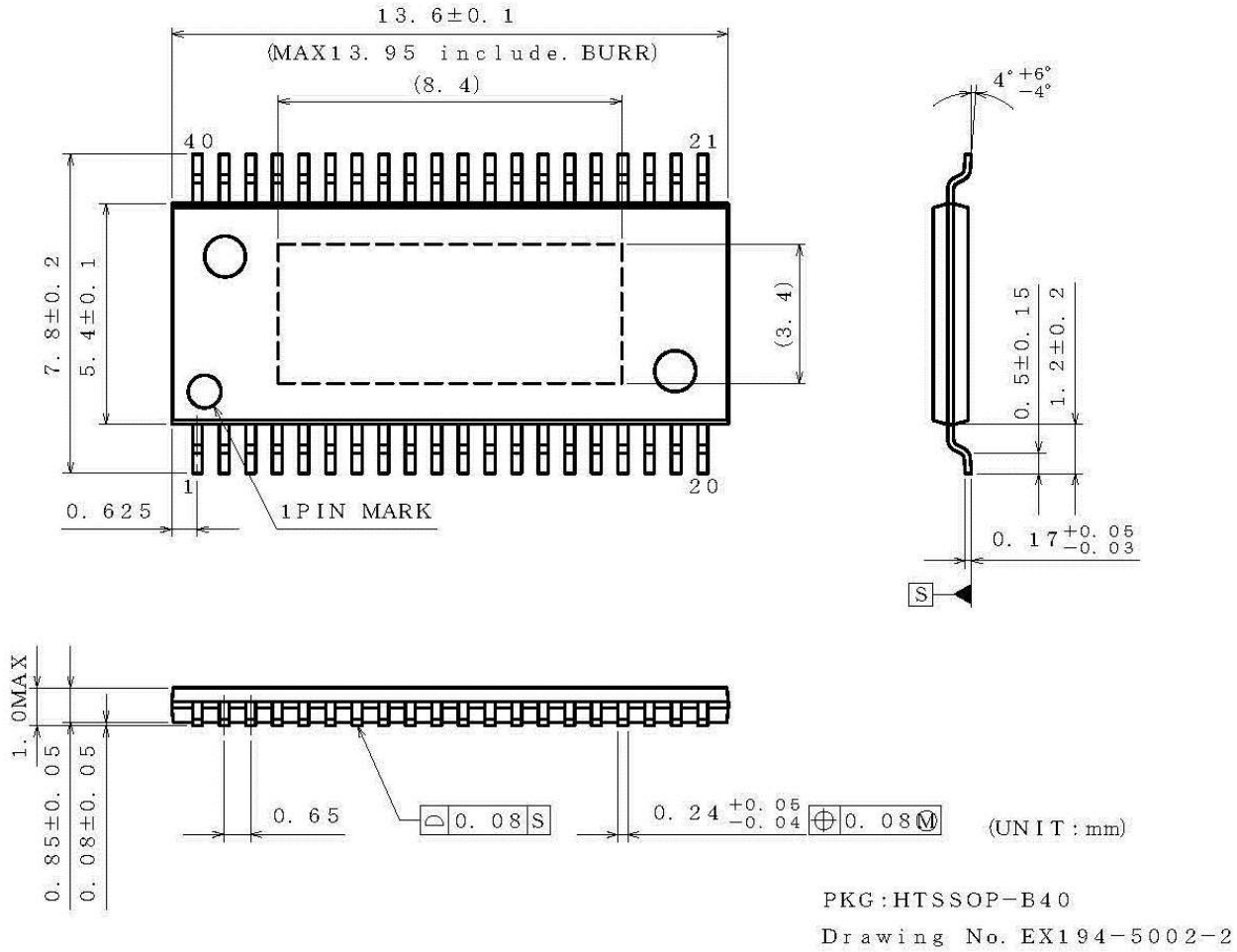
Marking Diagrams



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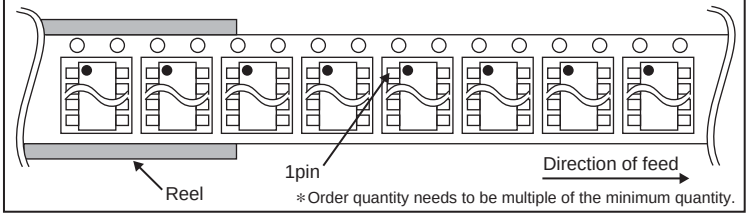
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
9.Oct.2015	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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