Bt8370/75/76

Fully Integrated T1/E1 Framer and Line Interface

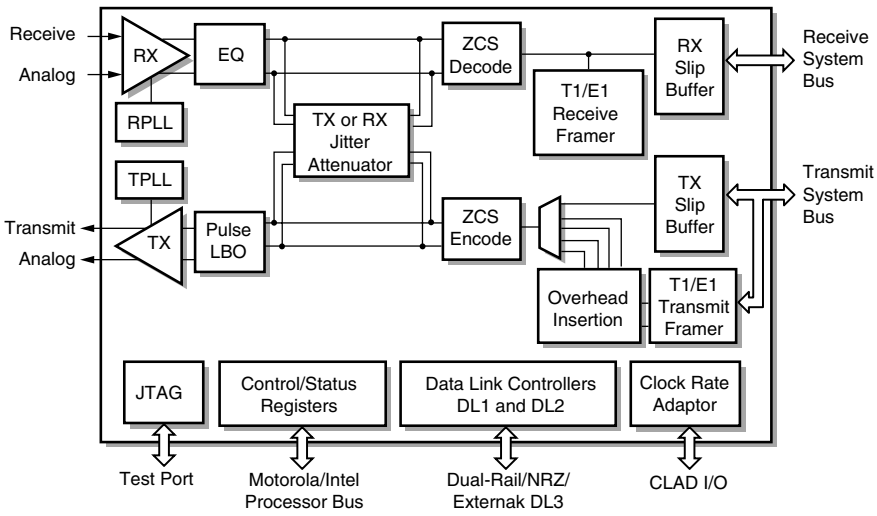
The Bt8370/75/76 is a family of single-chip transceivers for T1/E1 and Integrated Service Digital Network (ISDN) primary rate interfaces, operating at 1.544 Mbps or 2.048 Mbps. These devices combine a sophisticated framer, transmit and receive slip buffers, and an on-chip physical line interface to provide a complete T1/E1 transceiver.

The fully featured Bt8370 and short haul Bt8375 and Bt8376 devices provide a programmable clock rate adapter for simplifying system bus interfacing. The adapter synthesizes standard clock signals from the receive or transmit line rate clocks or from an external reference.

Operations are controlled through memory-mapped registers accessible via a parallel microprocessor port. Current ANSI, ETSI, ITU-T, and Telcordia standards are supported for alarm and error monitoring, signaling supervision (e.g., LAPD/SS7), per-channel trunk conditioning, and Facility Data Link (FDL) maintenance. A serial Time Division Multiplexed (TDM) system bus interface allows the backplane Pulse Code Modulation (PCM) data highway to operate at rates from 1.536–8.192 Mbps. Extensive test and diagnostic functions include a full set of digital and analog loopbacks, PRBS test pattern generation, BER meter, and forced error insertion.

The physical line interface circuit recovers clock and data from analog signals with +3 to –43 dB cable attenuation, appropriate for both short (–18 dB) and long haul T1/E1 applications. Receive line equalization (EQ) and transmit Line Build Out (LBO) filters are implemented using Digital Signal Processor (DSP) circuits for reliable performance. Data and/or clock jitter attenuation can be inserted on either the receive or transmit path. The transmit section includes precision pulse shaping and amplitude pre-emphasis for cross connect applications, as well as a set of LBO filters for long haul Channel Service Unit (CSU) applications. A complementary driver output is provided to couple 75/100/120 Ω lines via an external transformer.

Functional Block Diagram



Distinguishing Features

- Single-chip T1/E1 framer with short/long haul physical line interface
- Frames to popular T1/E1 standards:
  - T1—SF, ESF, SLC® 96, T1DM
  - E1—PCM-30, G.704, G.706, G.732 ISDN primary rate
- On-chip physical line interface compatible with:
  - DSX-1/E1 short haul signals
  - DS-1 (T1.403) and ETSI long haul signals
- Two-frame transmit and receive PCM slip buffers
- Clock rate adapter synthesizes jitter attenuated system clocks from an internal or external reference
- Parallel 8-bit microprocessor port supports Intel or Motorola buses
- Automated Facility Data Link (FDL) management
- BERT generation and counting
- Two full-duplex HDLC controllers for data link and LAPD/SS7 signaling
- B8ZS/HDB3/Bit 7 zero suppression
- 80-pin MQFP surface-mount package
- Operates from a single +5 Vdc ±5% power supply
- Low-power CMOS technology

Applications

- T1/E1 Channel Service Unit/Data Service Unit (CSU/DSU)
- Digital Access Cross-Connect Systems (DACS)
- T1/E1 Multiplexer (MUX)
- PBXs and PCM channel bank
- T1/E1 HDSL terminal unit
- ISDN Primary Rate Access (PRA)

Ordering Information

Model Number	Package	Operating Temperature	Reduced Features[1]
Bt8370EPF	80-Pin MQFP	–40 to 85 °C	none
Bt8370KPF	80-Pin MQFP	0 to 70 °C	none
Bt8375EPF	80-Pin MQFP	–40 to 85 °C	Short haul
Bt8375KPF	80-Pin MQFP	0 to 70 °C	Short haul
Bt8376EPF	80-Pin MQFP	–40 to 85 °C	Short haul; no CLAD output
Bt8376KPF	80-Pin MQFP	0 to 70 °C	Short haul; no CLAD output

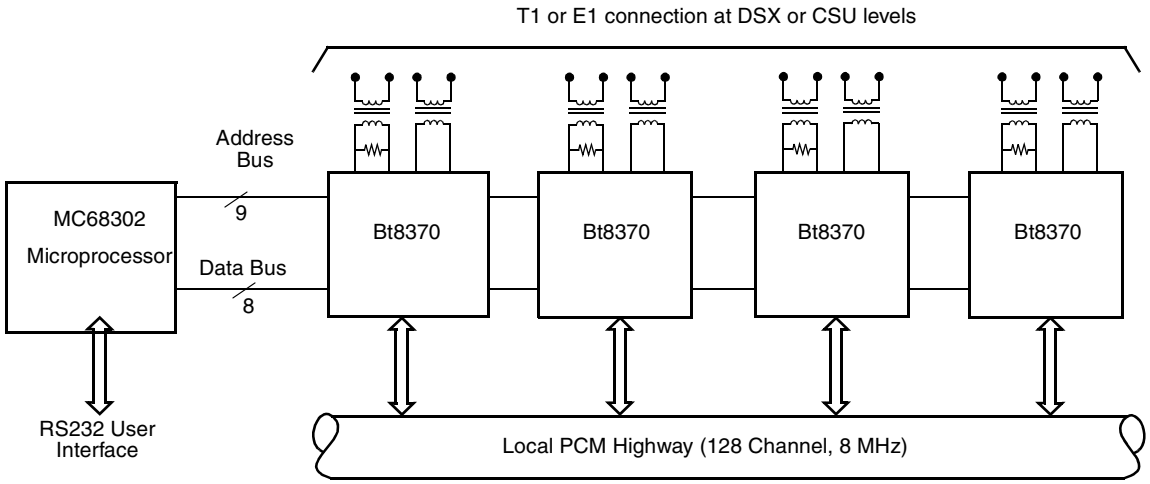
FOOTNOTE:

(1) Cost reduced Bt8375 and Bt8376 are pin- and register-compatible versions of Bt8370 with reduced features. Contact the local sales representative for ordering information and pricing.

Revision History

Rev	Description
A	Initial release.
B	Technical corrections.
C	Technical corrections.
D	Technical corrections (added changes for Bt8375 and Bt8376).
E	Technical corrections and additions.
A	New document #500030A; formerly document #100051E. Incorporated errata document #500184A in Appendix D and product bulletin #100679C in the Application chapter. Modified Intel synchronous read and write timing, added basic configurations in Appendix E, enhanced description of SEF for T1 and E1. Added detailed feature summary.
B	Deleted transmit chip side secondary surge protection blocks in Figures 4-2 and 4-4. Revised part numbers from Bt28370/75/76 to Bt8370/75/76.

Bt8370EVM—Bt8370 Evaluation Module, Quad T1/E1 ISDN PRI Board



An evaluation module is available and provides a convenient platform to test and evaluate Bt8370 performance and features. The Bt8370EVM provides up to four T1/E1 transceivers, all necessary line interface circuitry for T1 and E1 connections, and a simple RS232 serial user interface for setting device parameters and displaying status information on any VT100-compatible terminal.
Contact the local sales representative for ordering information and pricing.

Detailed Feature Summary

Frame Alignment

- Framed Formats:
  - Independent transmit and receive framing modes
  - T1: FT/SF/ESF/SLC
  - T1DM
  - E1: FAS/MFAS/FAS+CAS/MFAS+CAS
- Maximum Average Reframe Time (MART) <50 ms
- Transmitter alignment modes:
  - Align to system bus data
  - Align to system bus sync
  - Align to buffer data (embedded framing)
- Unframed mode

Signaling

- T1: 2-,4-, or 16-state, robbed-bit ABCD signaling
- E1: Channel Associated Signaling (CAS) in any time slot
- Per-channel receive signaling stack
- Signaling state change interrupt
- Automatic and manual signaling freeze
- Debounce signaling (2-bit integration)
- Unicode detection
- Signaling reinsertion on PCM system bus
- Separate I/O for system bus signaling
- Per-channel transparent

Clock Rate Adapter

- Outputs jitter attenuated system bus clock (CLADO) (not available on Bt8376)
- Outputs jitter attenuated line rate clock (JCLK)
- Supports all output clock combinations:
  - JCLK = 1544 k (T1) or 2048 k (E1)
  - CLADO = JCLK x 2^N, N = 0 to 3
  - CLADO = 1536 k or 2560 k
- Programmable input timing reference:
  - RXCLK = Recovered Clock
  - TXCLK = Transmit Clock
  - REFCKI = Internal Clock
  - CLADI = Clock Rate Adapter Input
- Subrate CLADI timing reference:
  - Line rate x ($1/2^N$), N = 0 to 8
  - References as low as 8 kHz

Line Interface Unit

- Short haul interfaces:
  - T1.102-1993
  - G.703 at 1.544 or 2.048 Mbps
  - ITU-T recommendation 1.430
- ITU-T Recommendation 1.431
- Long haul interfaces (Bt8370 only):
  - ANSI T1.403-1995 customer-to-network metallic interface
  - Telcordia TR-303 integrated digital loop carrier

- Analog receive line interface:
  - 100/120 Ω load impedance for 19-26 #AWG (0.4–0.9 mm) UTP cables
  - 75 Ω load impedance for coaxial cable
  - Equalizer compensation for –20 or –30 dB bridged monitor levels
  - Analog signal level meter
- Analog transmit line interface:
  - Pulse shapes for 0–655 ft., in 133 ft. steps (T1 DSX-1)
  - LBO filters for 0–22.5 dB, in 7.5 dB steps per FCC Part 68
  - External termination for improved return loss
  - Line driver enable/disable for protection switching
  - Output short circuit protection (for BABT applications)
  - Analog drive level monitor
- Jitter Attenuator (JAT) elastic store:
  - Receive or transmit direction
  - 8-, 16-, 32-, 64-, or 128-bit depth
  - Automatic and manual centering
- Bipolar Alternate Mark Inversion (AMI) line coding
- Optional Zero Code Suppression (ZCS):
  - Independent transmit and receive
  - T1: Binary with 8 Zero Substitution (B8ZS)
  - E1: High Density Bipolar of Order 3 (HDB3)
  - T1DM: Unassigned MUX Code (UMC)
  - Per-channel B7ZS
  - Receive ZCS signature detector
  - Pulse density violation monitor/enforcer
- Analog bypass mode for framer-only or LIU-only applications

Loopbacks

- Remote loopback towards line
  - With or without JAT
  - Retains BPV transparency
- Payload loopback
- Per-channel DSO remote loopback
- Local loopback towards system
  - Analog line loopback
  - Framer digital loopback
  - Per-channel DSO local loopback
- Inband loopback code detection/generation
- Simultaneous local and remote line loopbacks

Processor Interface

- Parallel 8-bit bus
- Data strobes (Motorola) or address latch enable (Intel)
- Multiplexed or non-multiplexed address/data bus
- Synchronous or asynchronous data transfers
- 36 MHz synchronous without wait states (50 ns access)
- Open drain interrupt output with maskable sources

Out-of-Service Testing and Maintenance

- Pseudorandom Bit Sequence (PRBS):
  - Independent transmit and receive
  - 2^{11}, 2^{15}, 2^{20}, 2^{23} patterns
  - Framed or unframed mode
  - Optional 7/14 zero limit
  - Bit Error Counter (BERR)
- Single error insertion:
  - PRBS error
  - Framing error
  - CRC error
  - BPV/LCV error
  - COFA error

In-Service Performance Monitoring

- One-second timer I/O to synchronize reporting
- Receive error detectors with accumulators:
  - Bipolar/Line Code Violations (LCV)
  - Excessive Zeros (EXZ)
  - Loss of Frame (RLOF)
  - Framing Errors (FERR)
  - CRC Errors (CERR)
  - Far End Block Errors (FEBE)
  - Severely Errored Frames (SEF)
  - Change of Frame Alignment (COFA)
- Transmit Error Detectors:
  - Loss of Frame (TLOF)
  - Framing errors (TFERR)
  - Multiframe Errors (TMERR)
    CRC Errors (TCERR)
  - Loss of Transmit Clock (TLOC)
  - Transmit Short Circuit (TSHORT)
- Receive alarm detectors:
  - Alarm Indication Signal (AIS)
  - Loss of Signal (RLOS)
  - Loss of Analog Input (RALOS)
  - RAI/Yellow Alarm (YEL)
  - Multiframe Yellow (MYEL)
  - Lost Frame Alignment (FRED)
  - Lost Multiframe Alignment (MRED)
- Controlled Frame Slip (RFSLIP) Uncontrolled Frame Slip (RUSLIP)
- Automatic and on-demand transmit alarms:
  - AIS following RLOS and/or TLOC
  - Automatic AIS clock switching
  - YEL following FRED
  - MYEL following MRED
  - FEBE following CERR

System Bus Interface (SBI)

- System bus data rates:
  - 1536 k (T1 without F-bits)
  - 1544 k (T1)
  - 2048 k (E1)
  - 4096 k (2E1)
  - 8192 k (4E1)
- Clock operation at 1x or 2x data rate
- Selectable I/O clock edges
- Master, slave, or mixed bus timing
- Bit and time slot frame sync offsets
- Bus shares up to four Bt8370/75/76 devices without external MUX
- DSO drop/insert indicators for external MUX
- Embedded T1 framing transport per G.802
- Receive and transmit slip buffers:
  - Bypass, 2-frame, or 64-bit depth
  - Slip detection with directional status
  - Slip buffer phase status
  - Per-channel idle code insertion
  - Processor-accessible data buffers
- Direct connection to upper layer devices:
  - Link layer: Bt8071A, Bt8474
  - SMDS layer: Bt8210
  - ATM layer: Bt8215, Bt8222
- Supported system bus formats:
  - AT&T Concentration Highway Interface (CHI)
  - Multi-Vendor Integration Protocol (MVIP)
  - Mitel S/T
  - H.100

Device Differences Summary

Device Differences Summary			
Device	**Line Interface Unit**	**Data Link Controllers**	**Clock Rate Adapter**
Bt8370 (Full Featured)	Short haul/ long haul	Two Controllers	Full Featured
Bt8375	Short haul only	Two Controllers	Full Featured
Bt8376	Short haul only	One Controller	No CLAD Output

Data Links

- Two full-featured data link controllers (DL1 and DL2) (Bt8370, Bt8375) or one data link controller (DL1) (Bt8376):
  - 64-octet transmit and receive FIFOs
  - HDLC Message Oriented Protocol (MOP)
  - Unformatted data transfer
  - Unformatted circular buffer
  - End of message/buffer interrupt
  - Near full/empty interrupts at selected depth
- Access any bit combination in any time slot:
  - ISDN D-channels at 16, 32, or 64 Kbps
  - National/spare bits (SA-bits) in 4 Kbps increments
  - CCS/SS7
  - T1DM R-bits
- Access T1 F-bits in even, odd, or all frames:
  - Automatic Performance Report Message (PRM) generator
  - ESF Facility Data Link (FDL)
  - Unformatted SLC-96 overhead
  - Bit-Oriented Protocol (BOP) priority code word generation and detection
- Separate I/O for external data link (DL3)

Contents

Figures

Tables

1.0 Pin Descriptions

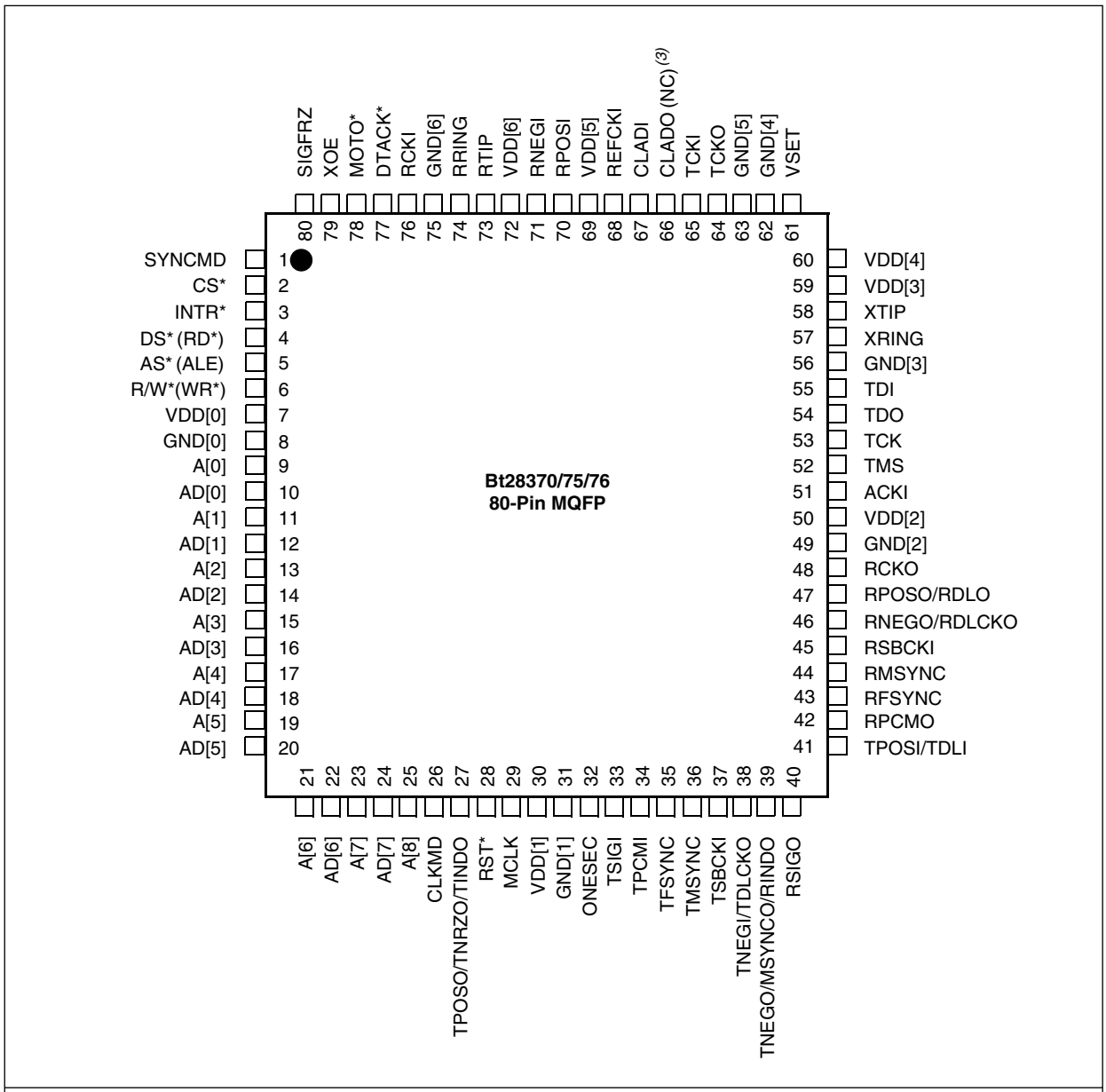
1.1 Pin Assignments

Bt8370/75/76 is packaged in an 80-pin Metric Quad Flat Pack (MQFP). A pinout diagram of this device is illustrated in Figure 1-1. Figure 1-2 details a Bt8370/75/76 logic diagram. Pin labels, names, I/O functions, and descriptions are provided in Table 1-1.

The input pins listed below contain an internal pull-up resistor (>50 kΩ) and can remain unconnected if the active-high input state is desired. All other unused input pins should be either pulled up or grounded.

1	A[7:0]	Address lines unused in INTEL bus mode
2	XOE	Active-high enables analog bipolar output
3	MOTO*	Pullup selects INTEL bus mode if unconnected
4	SYNCMD	Pullup selects synchronous processor interface
5	RCKI	Receive clock unused if analog inputs enabled
6	TDI	Unused if JTAG not connected
7	TMS	Disables JTAG if not connected
8	RST*	Disables hardware reset if not connected
9	TDLI	Unused if no external data link
10	TSIGI	Unused if signaling data not supported by system bus

Figure 1-1. Bt8370/75/76 Pinout Diagram

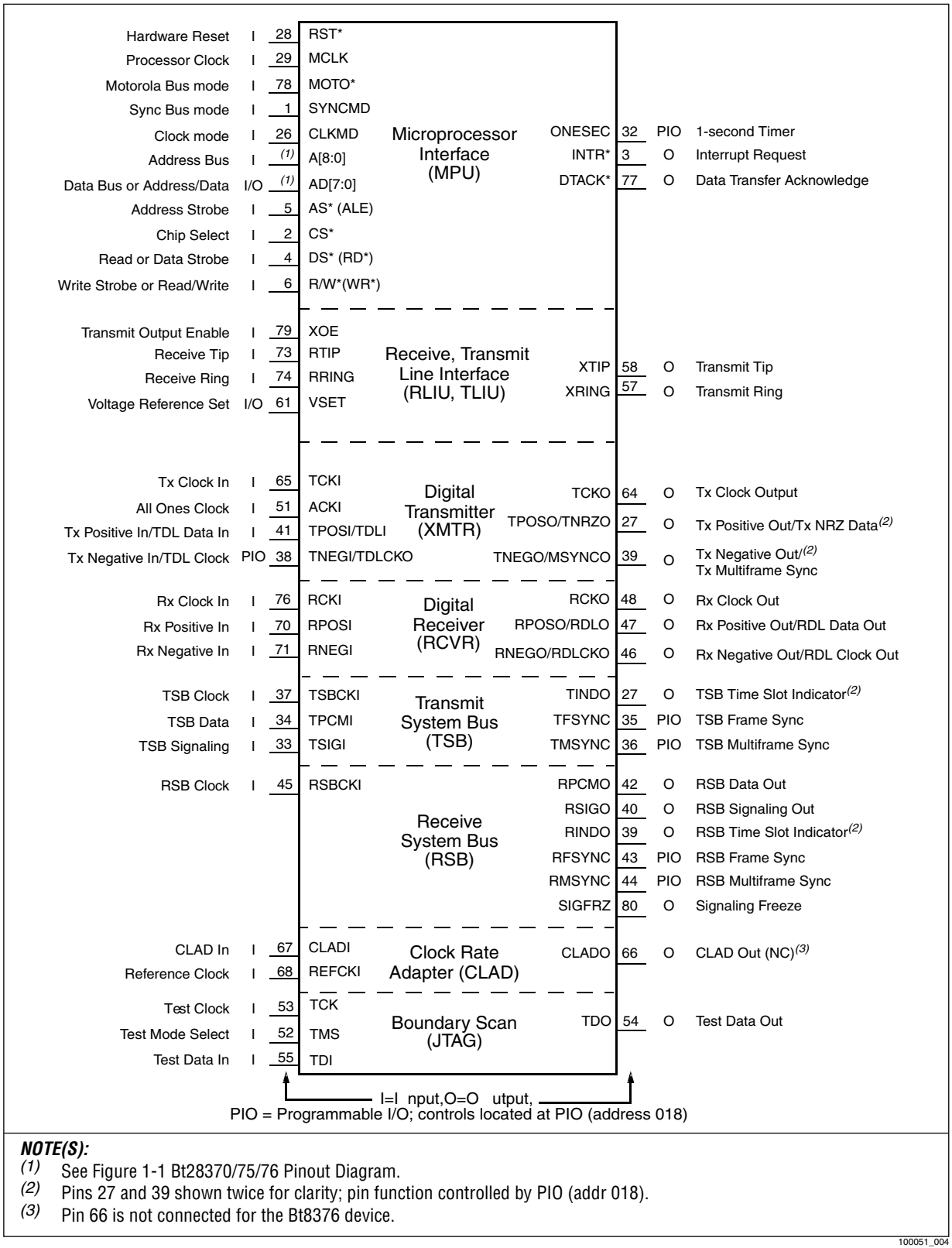


NOTE(S):

1. Default pin assignments listed first for pins with multiple modes.
2. Motorola-style processor pin names listed first with Intel pins in parentheses.
3. Pin 66 is not connected for the Bt8376 device.

100051 _003

Figure 1-2. Bt8370/75/76 Logic Diagram



NOTE(S):

(1) See Figure 1-1 Bt28370/75/76 Pinout Diagram.

(2) Pins 27 and 39 shown twice for clarity; pin function controlled by PIO (addr 018).

(3) Pin 66 is not connected for the Bt8376 device.

100051_004

Table 1-1. Hardware Signal Definitions (1 of 8)

Pin Label	Signal Name	I/O	Definition
Microprocessor Interface (MPU)			
RST*	Hardware Reset	I	RST* low-to-high transition forces registers to their default, power-up state and forces all PIO pins to the input state. RST* is not mandatory, because internal power on reset circuit performs an identical function. RST* can be applied asynchronously, but must remain asserted for a minimum of 2 clock cycles (external MCLK or internal 32 MHz) for the low-to-high transition to be sampled and detected (see also [RESET; addr 001]).
MCLK	Processor Clock	I	System applies MCLK in the range of 8–36 MHz for external clock (CLKMD = 1) and synchronous bus modes (SYNCMD = 1). During internal clock modes (CLKMD = 0), the Bt8370/75/76 uses an internally generated 32 MHz clock to control processor timing, and MCLK input is ignored.
MOTO*	Motorola Bus mode	I	Selects Intel- or Motorola-style microprocessor interface. DS*, R/W*, A[8:0], and AD[7:0] functions are affected. 0 = Motorola; AD[7:0] is data, A[8:0] is address, DS* is data strobe, and R/W* indicates the read (high) or write (low) data direction. 1 = Intel; AD[7:0] is multiplexed address/data, A[7:0] ignored, A[8] is address line, DS* is read strobe (RD*), and R/W* is write strobe (WR*).
SYNCMD	Sync mode	I	Selects whether read/write cycle timing is synchronous with MCLK. Supports Intel- or Motorola-style buses: 0 = Asynchronous bus; read data enable and write data input latch are asynchronously controlled by CS*, DS*, and R/W* signals. Latched write data is still synchronized internally to 32 MHz clock for transfer to addressed register. 1 = Synchronous bus; applicable only if the external clock is also selected (CLKMD = 1). MCLK rising edge samples CS*, DS*, and R/W* to determine valid read/write cycle timing. Allows 0 wait state processor cycles for MCLK speeds up to 36 MHz, for M68000 type buses.
CLKMD	Clock mode	I	Selects whether MCLK is enabled (high) or ignored (low). When enabled, MCLK frequency determines update rate of internal registers and sampling rate of CS*, DS*, and R/W* signals.
A[8:0]	Address Bus	I	AS* falling edge asynchronously latches A[8:0] (Motorola) or A[8] (Intel) to identify one register for subsequent read/write data transfer cycle.
AD[7:0]	Data Bus or Address Data	I/O	Multiplexed address/data (Intel) or only data (Motorola). See MOTO* signal definition.
AS* (ALE)	Address Strobe	I	For all processor bus modes, AS* falling edge asynchronously latches address from A[8:0] (Motorola) or from A[8] and AD[7:0] (Intel). For sync modes (SYNCMD = 1), each read/write data cycle requires both AS* and CS* active-low on MCLK rising edge.
CS*	Chip Select	I	Active-low enables read/write decoder. Active-high ends current read or write cycle and places data bus output in high impedance.
DS*(RD*)	Data Strobe or Read Strobe	I	Active-low read data strobe (RD*) for MOTO* = 1, or read/write data strobe (DS*) for MOTO* = 0.
R/W*(WR*)	Read/Write Direction or Write Strobe	I	Active-low write data strobe (WR*) for MOTO* = 1, or read/write data select (R/W*) for MOTO = 0.

Table 1-1. Hardware Signal Definitions (2 of 8)

Pin Label	Signal Name	I/O	Definition
Microprocessor Interface (MPU) (Continued)			
ONESEC	1-second Timer	PIO	Controls or marks 1-second interval used for status reporting. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each 1-second interval. Typically, one device in a multi-line system is configured to output ONESEC to synchronize other Bt8370/75/76 status reports on a common 1-second interval.
INTR*	Interrupt Request	O	Open drain active-low output signifies one or more pending interrupt requests. INTR* goes to high-impedance state after processor has serviced all pending interrupt requests.
DTACK*	Data Transfer Acknowledge	O	Open drain active-low output signifies in-progress data transfer cycle. DTACK* remains asserted (low) for as long as AS* and CS* are both active-low. DTACK* is only implemented during synchronous Motorola processor interface modes. See the timing diagrams in Section 5.5.
Line Interface Unit (LIU)			
XOE	Transmit Output Enable	I	Active-high input enables XTIP and XRING output drivers; otherwise, both outputs are placed in high-impedance state. XOE contains internal pull-up so systems that do not require three-stated outputs can leave XOE unconnected. XOE needs to be disabled during Power-On Reset (POR) and re-enabled after configuring the part. See Power-On Reset procedure in Section 2.10.4.
RTIP, RRING	Receive Tip/Ring	I	Differential AMI data inputs for direct connection to receive transformer.
VSET	Voltage Reference Set	I/O	Constant voltage output. Must be connected to an external 1% resistor equal to 14 kΩ to ground (GND[4] pin 62). The VSET resistor sets the internal precision current reference of 100 μA and also controls the transmit pulse height.
XTIP, XRING	Transmit Tip/Ring	O	Complementary AMI data outputs for direct connection to transmit transformer. Optionally, both outputs are three-stated when XOE is negated.
Digital Transmitter (XMTR)			
TCKI	Tx Clock Input	I	Primary TX line rate clock applied on TCKI, or the system chooses from one of four different clocks to act as TX clock source (see [CMUX; addr 01A]). The selected source is used to clock digital transmitter signals TPOSI, TNEGI, TPOSO, TNEGO, TNRZO, MSYNCO, TDLI, and TDLCKO. If TSLIP is bypassed, selected source also clocks TSB signals.
ACKI	All 1s Clock	I	System optionally applies ACKI for AIS transmission, if the selected primary transmit clock source fails. ACKI is either manually or automatically switched to replace TCKI (see [AISCLK; addr 068]). Systems without an AIS clock must tie ACKI to ground.

Table 1-1. Hardware Signal Definitions (3 of 8)

Pin Label	Signal Name	I/O	Definition
Digital Transmitter (XMTR) (Continued)			
TPOSI	TX Positive Rail Input	I	Line rate data input on TCKI falling edge. Replaces all data that would otherwise be supplied by ZCS encoder. Bt8370/75/76 default power on state selects TPOSI/TNEGI as source for all transmitted XTIP/XRING output pulses, encoded as follows: TPOSI / TNEGI / TX Pulse Polarity 0 / 0 / No pulse 0 / 1 / Negative AMI pulse 1 / 0 / Positive AMI pulse 1 / 1 / Invalid ***GENERAL NOTE:*** Software must set TDL_IO (addr 018) to enable normal data from internal transmitter.
TNEGI	TX Negative Rail Input	I	Line rate data input on TCKI falling edge. Replaces all data that would otherwise be supplied by ZCS encoder. See TPOSI signal definition.
TPOSO	TX Positive Rail Output	O	Line rate data output from ZCS encoder or JAT on rising edge of TCKO. Active-high marks transmission of a positive AMI pulse. Used to monitor transmit data or for systems that employ an external line interface unit.
TNEGO	TX Negative Rail Output	O	Line-rate data output from ZCS encoder or JAT on rising edge of TCKO. Active-high marks transmission of a negative AMI pulse. Used to monitor transmit data or for systems that use an external line interface unit.
TDLI	TX Data Link Input	I	Selected time slot bits are sampled on TDLCKO falling edge for insertion into the transmit output stream during external data link applications.
TDLCKO	TX Data Link Clock	O	Gapped version of TCKI for external data link applications. TDLCKO high clock pulse coincides with low TCKI pulse interval during selected time slot bits (see [DL3_TS; addr 015]).
TCKO	TX Clock Output	O	Line rate clock used to align XTIP/XRING outputs. TCKO follows TCKI pin during NRZ mode (framer mode only). This is when TNRZ bit in TCRI register [addr 071] is set, and TPOSO/TNEGO/TCKO outputs are selected and enabled. Otherwise, if transmit jitter attenuator (TJAT) is disabled, TCKO equals selected TCKI or ACKI. If TJAT is enabled, TCKO equals the jitter attenuated clock (JCLK).
TNRZO	TX Non Return to Zero Data	O	Line rate data output from transmitter on rising edge of TCKI. TNRZO does not include ZCS encoded bipolar violations.
MSYNCO	TX Multiframe Sync	O	Active-high for one TCKI clock cycle to mark the first bit of TX multiframe coincident with TNRZO. Output on rising edge of TCKI.

Table 1-1. Hardware Signal Definitions (4 of 8)

Pin Label	Signal Name	I/O	Definition
Digital Receiver (RCVR)			
RCKI	RX Clock Input	I	Line rate clock samples RPOSI and RNEGI when RLIU configured to accept dual-rail digital data (see [RDIGI; addr 020]); otherwise, RCKI is ignored.
RPOSI	RX Positive Rail Input	I	Line rate data input on falling edge of RCKI. RPOSI and RNEGI levels are interpreted as received AMI pulses, encoded as follows: RPOSI / RNEGI / RX Pulse Polarity 0 / 0 / No pulse 0 / 1 / Negative AMI pulse 1 / 0 / Positive AMI pulse 1 / 1 / Invalid ***GENERAL NOTE:*** The NRZ data can be input at RPOSI or RNEGI if the other input is connected to ground.
RNEGI	RX Negative Rail Input	I	Line rate data input on falling edge of RCKI. See RPOSI signal definition.
RCKO	RX Clock Output	O	RPLL recovered line rate clock (RXCLK) or jitter attenuated clock (JCLK) output, based on programmed clock selection (see [JAT_CR; addr 002]).
RPOSO	RX Positive Rail Output	O	Line rate data output on rising edge of RCKO. Active-high indicates receipt of a positive AMI pulse on RTIP/RING inputs.
RNEGO	RX Negative Rail Output	O	Line rate data output on rising edge of RCKO. Active-high indicates receipt of a negative AMI pulse on RTIP/RING inputs.
RDLO	RX Data Link Output	O	Line rate NRZ data output from receiver on falling edge of RCKO, all data from RLIU is represented at the RDLO pin. However, selective RDLO bit positions are also marked by RDLCKO for external data link applications.
RDLCKO	RX Data Link Clock Output	O	Gapped version of RCKO for external data link applications. RDLCKO high clock pulse coincides with low RCKO pulse interval during selected time slot bits, else RDLCKO low (see Figure 2-12).

Table 1-1. Hardware Signal Definitions (5 of 8)

Pin Label	Signal Name	I/O	Definition
Transmit System Bus (TSB)			
TSBCKI	TSB Clock Input	I	Bit clock and I/O signal timing for TSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from one of four different clocks to act as TSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals TPCMI, TSIGI, TINDO and sync signals TFSYNC and TMSYNC (see [TPCM_NEG and TSYN_NEG; addr 0D4]). When configured to operate at twice the data rate, TSB clock is internally divided by two before clocking TSB data signals.
TPCMI	TSB Data Input	I	Serial data formatted into TSB frames consisting of DS0 channel time slots and optional F bits. One group of 24 T1 time slots or 32 E1 time slots is selected from up to four available groups; data from the group is sampled by TSBCKI, then sent towards transmitter output. Time slots are routed through transmit slip buffer (see [TSLIPn; addr 140–17F]) according to TSLIP mode (see [TSBI; addr 0D4]). F bits are taken from the start of each TSB frame or from within an embedded time slot (see [EMBED; addr 0D0]) and optionally inserted into the transmitter output (see [TFRM; addr 072] register).
TSIGI	TSB Signaling Input	I	Serial data formatted into TSB frames containing ABCD signaling bits for each system bus time slot. Four bits of TSIGI time slot carry signaling state for each accompanying TPCMI time slot. Signaling state of every time slot is sampled during first frame of the TSB multiframe, and then transferred into transmit signaling buffer [TSIGn; addr 120–13F].
TINDO	TSB Time Slot Indicator	O	Active-high output pulse marks selective transmit system bus time slots as programmed by SBCn [addr 0E0–0FF]. TINDO occurs on TSBCKI rising or falling edges as selected by TPCM_NEG (see [TSBI; addr 0D4]).
TFSYNC	TSB Frame Sync	PIO	Input or output TSB frame sync (see [TFSYNC_IO; addr 018]). TFSYNC output is active-high for one TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB frame and repeating once every 125 μs. When transmit framer is also enabled, TSB timebase and TFSYNC output frame alignment are established by transmit framer's examination of TPCMI serial data input. When TFSYNC is programmed as an input, the low-to-high signal transition is detected and aligns TSB timebase to programmed offset bit value. TSB timebase flywheels at 125 μs frame interval after the last TFSYNC is applied.
TMSYNC	TSB Multiframe Sync	PIO	Input or output TSB multiframe sync (see [TMSYNC_IO; addr 018]). TMSYNC output is active-high for one TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB multiframe and repeating once every 6 ms coincident with TFSYNC. When transmit framer is also enabled, TSB timebase and TMSYNC output multiframe alignment are established by transmit framer's examination of TPCMI serial data input. When TMSYNC is programmed as an input, the low-to-high signal transition is detected and aligns TSB timebase to the programmed offset bit value and first frame of the multiframe. TSB timebase flywheels at 6 ms multiframe interval after the last TMSYNC is applied. If system bus applies TMSYNC input, TFSYNC input is not needed.

Table 1-1. Hardware Signal Definitions (6 of 8)

Pin Label	Signal Name	I/O	Definition
Receive System Bus (RSB)			
RSBCKI	RSB Clock Input	I	Bit clock and I/O signal timing for RSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from one of four different clocks to act as RSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals RPCMO, RSIGO, RINDO and sync signals RFSYNC, RMSYNC (see [RPCM_NEG and RSYN_NEG; addr 0D1]). When configured to operate at twice the data rate, RSB clock is internally divided by 2 before clocking RSB data signals.
RPCMO	RSB Data Output	O	Serial data formatted into RSB frames consisting of DS0 channel time slots, optional F bits, and optional ABCD signaling. Time slots are routed through receive slip buffer (see [RSLIPn; addr 1C0–1FF]) according to RSLIP mode (see [RSBI; addr 0D1]). Data for each output time slot is assigned sequentially from received time slot data according to system bus channel programming (see [ASSIGN; addr 0E0–0FF]). F bits are output at the start of each RSB frame or at the embedded time slot location (see [EMBED; addr 0D0]). ABCD signaling is optionally inserted on a per-channel basis (see [INSERT; addr 0E0–0FF]) from the local signaling buffer (see [RLOCAL; addr 180–19F]) or from the receive signaling buffer [RSIGn; addr 1A0–1BF]. When enabled, robbed bit signaling or CAS reinsertion is performed according to T1/E1 mode: the eighth time slot bit of every sixth T1 frame is replaced, or the 4-bit signaling value in the E1 time slot 16 is replaced.
RSIGO	RSB Signaling Output	O	Serial data formatted into RSB frames consisting of ABCD signaling bits for each system bus time slot. Four bits of RSIGO time slot carry signaling state for each accompanying RPCMO time slot. Local or through signaling bits are output in every frame for each time slot and updated once per RSB multiframe, regardless of per-channel RPCMO signaling reinsertion.
RINDO	RSB Time Slot Indicator	O	Active-high output pulse marks selective receive system bus time slots as programmed by SBCn [addr 0E0–0FF]. RINDO occurs on RSBCKI rising or falling edges as selected by RPCM_NEG (see [RSBI; addr 0D1]).
RFSYNC	RSB Frame Sync	PIO	Input or output RSB frame sync (see [RFSYNC_IO; addr 018]). RFSYNC output is active-high for one RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB frame and repeating once every 125 µs. RSB timebase and RFSYNC output frame alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RFSYNC is programmed as an input, the low-to-high signal transition is detected and aligns RSB timebase to the programmed offset. RSB timebase flywheels at 125 µs frame interval after the last RFSYNC is applied.
RMSYNC	RSB Multiframe Sync	PIO	Input or output RSB multiframe sync (see [RMSYNC_IO; addr 018]). RMSYNC output is active-high for one RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB multiframe and repeating once every 6 ms coinciding with RFSYNC. RSB timebase and RMSYNC output multiframe alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RMSYNC is programmed as input, the low-to-high signal transition is detected and aligns the RSB timebase to the programmed offset and the first frame of the multiframe. RSB timebase flywheels at 6 ms multiframe interval after the last RMSYNC is applied.

Table 1-1. Hardware Signal Definitions (7 of 8)

Pin Label	Signal Name	I/O	Definition
Receive System Bus (RSB) (Continued)			
SIGFRZ	Signaling Freeze	O	Active-high indicates that signaling bit updates are suspended for both receive signaling buffer [RSIGn; addr 1A0–1BF] and stack [STACK; addr 0DA] register. SIGFRZ, clocked by RSB clock, goes high coinciding with receive loss of frame alignment (see RLOF; addr 047) and returns low 6–9 ms after recovery of frame alignment.
GENERAL NOTE: 1. All RSB and TSB outputs can be placed in high-impedance state (see SBI_OE; addr 0D0). 2. Receive System Bus (RSB)			
Clock Rate Adapter (CLAD)			
CLADI	CLAD Input	I	Optional CLAD input timing reference used to phase lock CLADO and JCLK outputs to one of 44 different input clock frequencies selected in the range of 8 kHz to 16384 kHz (see [CLAD registers; addr 090–092]).
REFCKI	Reference Clock	I	System must apply a 10 MHz ±50 ppm clock signal to act as frequency reference for internal Numerical Controlled Oscillator (NCO). REFCKI determines frequency accuracy and stability of CLADO and jitter attenuator (JCLK) clocks when the NCO operates in free running mode (see [JFREE; addr 002]). REFCKI is the baseband reference for all CLAD/JAT functions and is used internally to generate clocks of various frequencies, locked to a selected receive, transmit, or external clock. Hence, REFCKI is always required.
CLADO	CLAD Output	O	CLADO is configured to operate at one of 14 different clock frequencies (see [CSEL; addr 091]) that include T1, E1 or system bus rates. CLADO is typically programmed to supply RSB and TSB clocks that are phase-locked to the selected transmit, receive or CLADI timing reference (see [JEN; addr 002 and CEN; addr 090]). On the Bt8376 device, CLAD0 drives low when enabled.
Test Access			
TDI	JTAG Test Data Input	I	Test data input per *IEEE Std 1149.1-1990*. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected if it is not being used because it is pulled up internally.
TMS	JTAG Test mode Select	I	Active-low test mode select input per *IEEE Std 1149.1-1990*. Internally pulled-up input signal used to control the test-logic state machine. Sampled on the rising edge of TCK. TMS can be left unconnected if it is not being used because it is pulled up internally.
TDO	JTAG Test Data Output	O	Test data output per *IEEE Std 1149.1-1990*. Three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
TCK	JTAG Test Clock	I	Test clock input per IEEE Std 1149.1-1990. Used for all test interface and internal test-logic operations. If unused, TCK must be pulled low.
Power Supply			
VDD[6:0]	Power	I	+5 VDC ±5%
GND[6:0]	Ground	I	0 VDC

Table 1-1. Hardware Signal Definitions (8 of 8)

Pin Label	Signal Name	I/O	Definition
GENERAL NOTE: 1. I = Input, O = Output 2. PIO = Programmable I/O; controls located at address 018. 3. Multiple signal names show mutually exclusive pin functions. 4. All output pins power up in the high-impedance state within 3,000 cycles of the applied REFCKI (see POE; addr 019, SBI_OE; addr 0D0).			

2.0 Circuit Description

2.1 Bt8370/75/76 Block Diagrams

Detailed block diagrams are illustrated in Figure 2-1 (Bt8370), Figure 2-2 (Bt8375), and Figure 2-3 (Bt8376). To show the details of this circuit, individual block diagrams, along with descriptions, appear throughout this section.

1. Receive Line Interface Unit (RLIU)
2. Jitter Attenuator (JAT)
3. Digital Receiver (RCVR)
4. Receive System Bus (RSB)
5. Clock Rate Adapter (CLAD)
6. Transmit System Bus (TSB)
7. Digital Transmitter (XMTR)
8. Transmit Line Interface Unit (TLIU)
9. Microprocessor Interface (MPU)
10. Joint Test Access Group Port (JTAG)

NOTE: The Bt8375 differs from the Bt8370 only in that the Bt8375 does not have LBO filters in the transmit LIU. The Bt8376 differs from the Bt8375 in that Bt8376 has neither a CLADO output nor a DLINK2.

Figure 2-1. Detailed Bt8370 Block Diagram

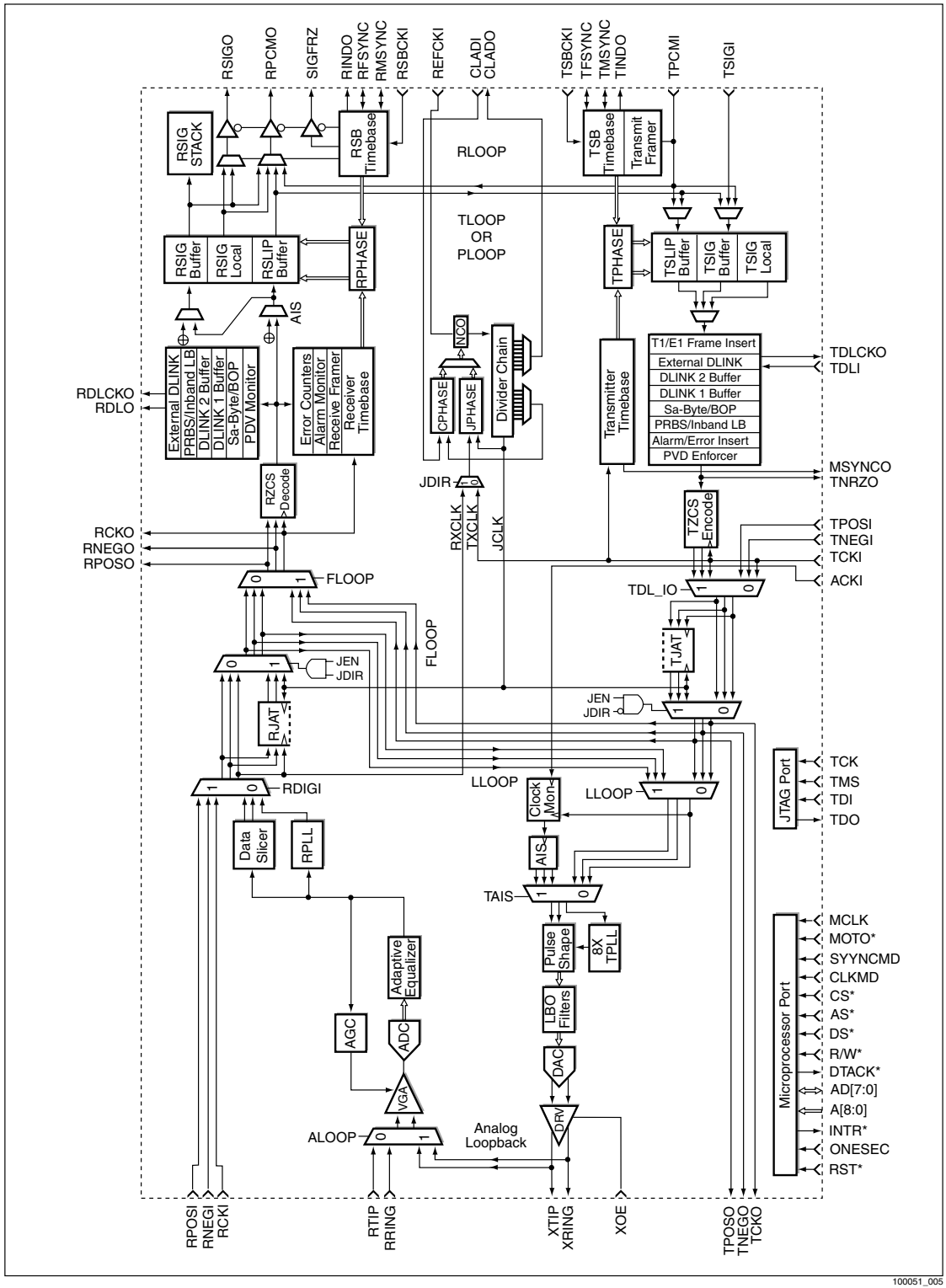


Figure 2-2. Detailed Bt8375 Block Diagram

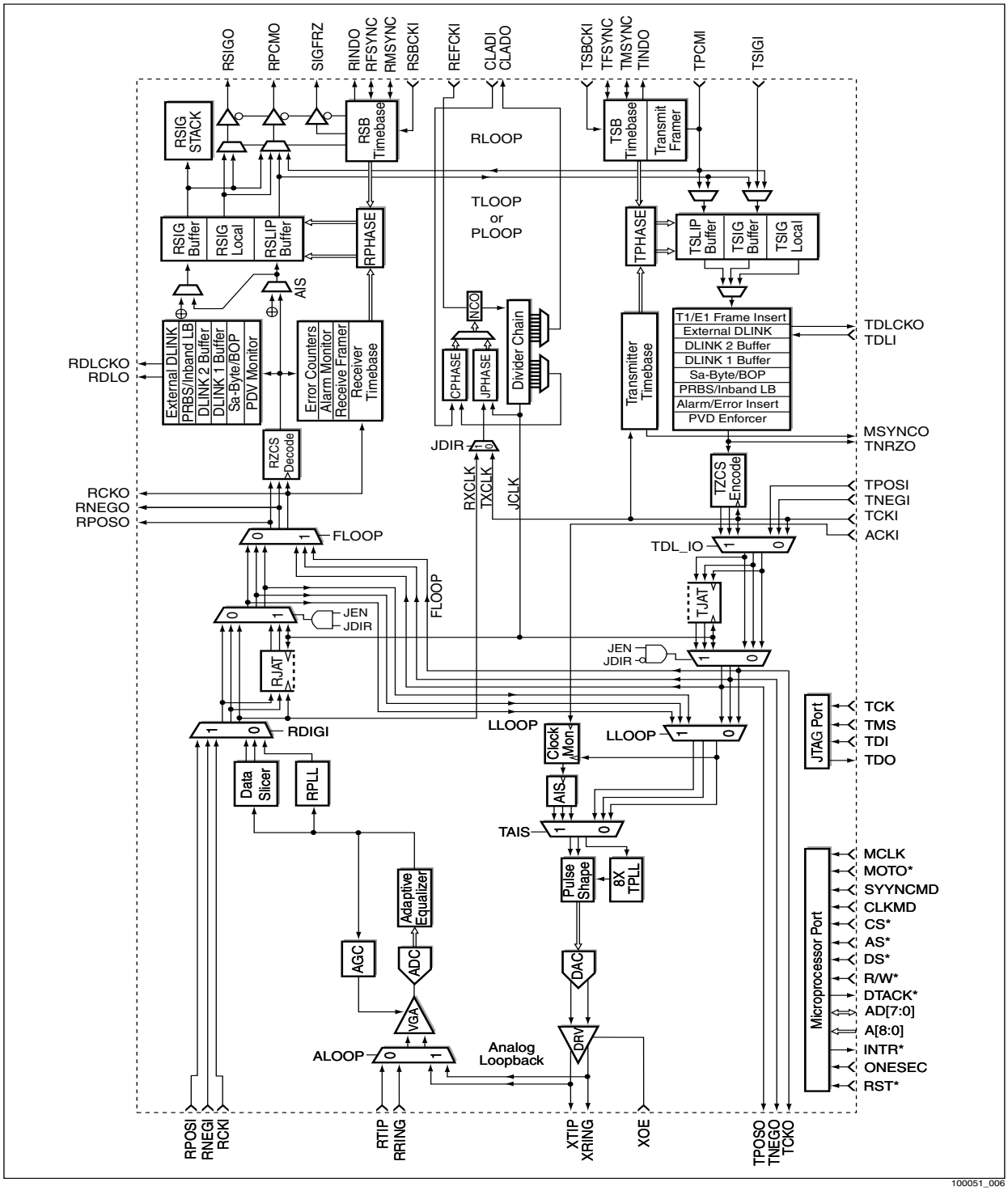
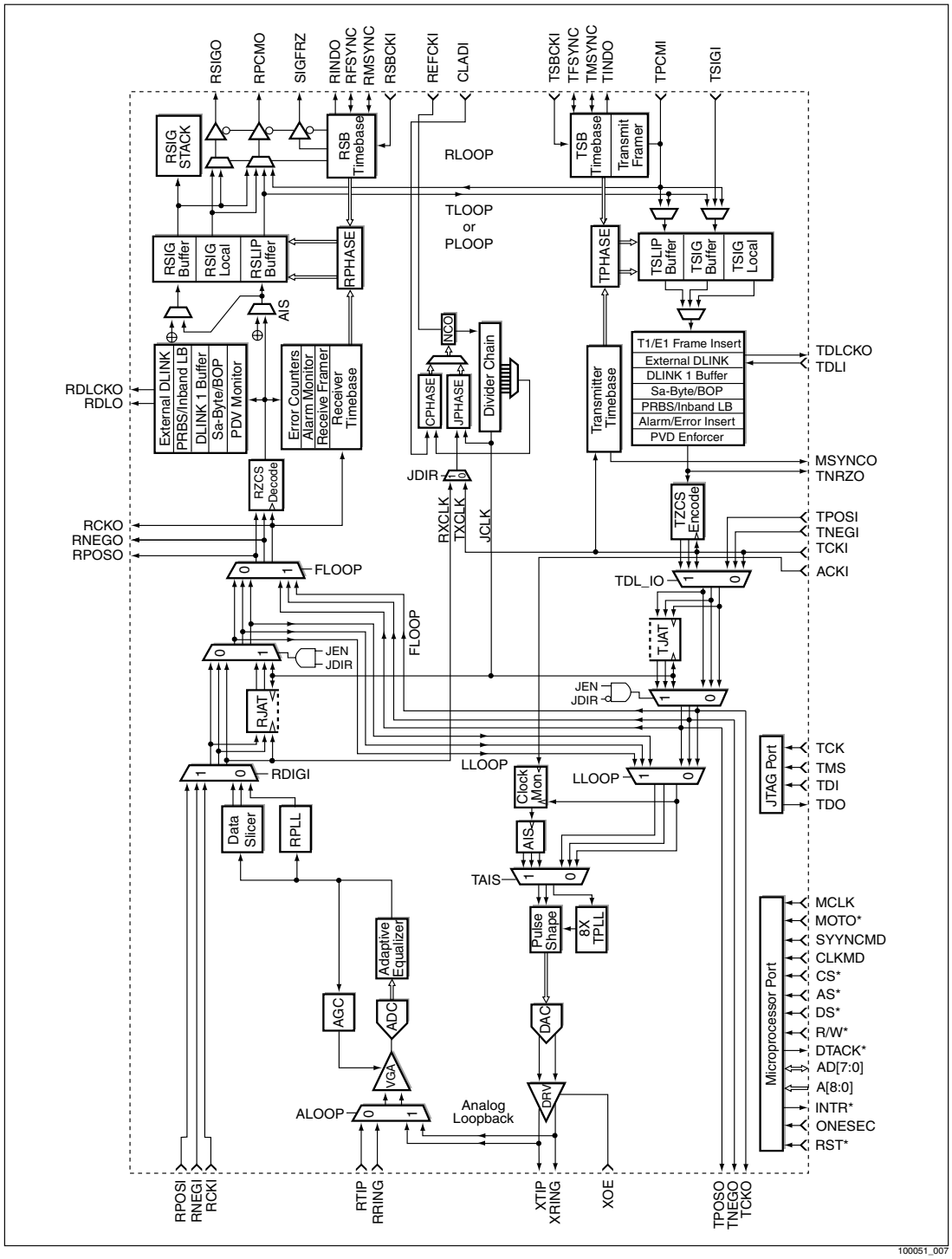


Figure 2-3. Detailed Bt8376 Block Diagram



2.2 Receive Line Interface Unit

The Receive Line Interface Unit (RLIU) recovers clock and data from the bipolar Alternate Mark Inversion (AMI) line signal that has been attenuated and distorted due to the characteristics of the line. In the Bt8370 device, the RLIU is sensitive to signals attenuated in the range of 0 to –48 dB in E1 and T1 modes. In the Bt8375 and Bt8376 devices, RLIU sensitivity is limited for short haul-only applications. In addition, the RLIU interfaces at the DSX-1 Bridge Monitor Level (–20 dB for DS1 and –30 dB for E1/CEPT).

The RLIU converts AMI pulses into P and N rail Non-Return to 0 (NRZ) data. The AMI pulses are input on the receive tip and ring pins RTIP and RRING (Figure 2-4). The P and N rail NRZ data is then passed to the RCVR. The RCVR dual-rail output is available on RPOSO/RNEGO. Figure 2-5 illustrates the relationship between the AMI received signal, the recovered clock, and the RCVR dual-rail outputs.

Figure 2-4. RLIU Diagram

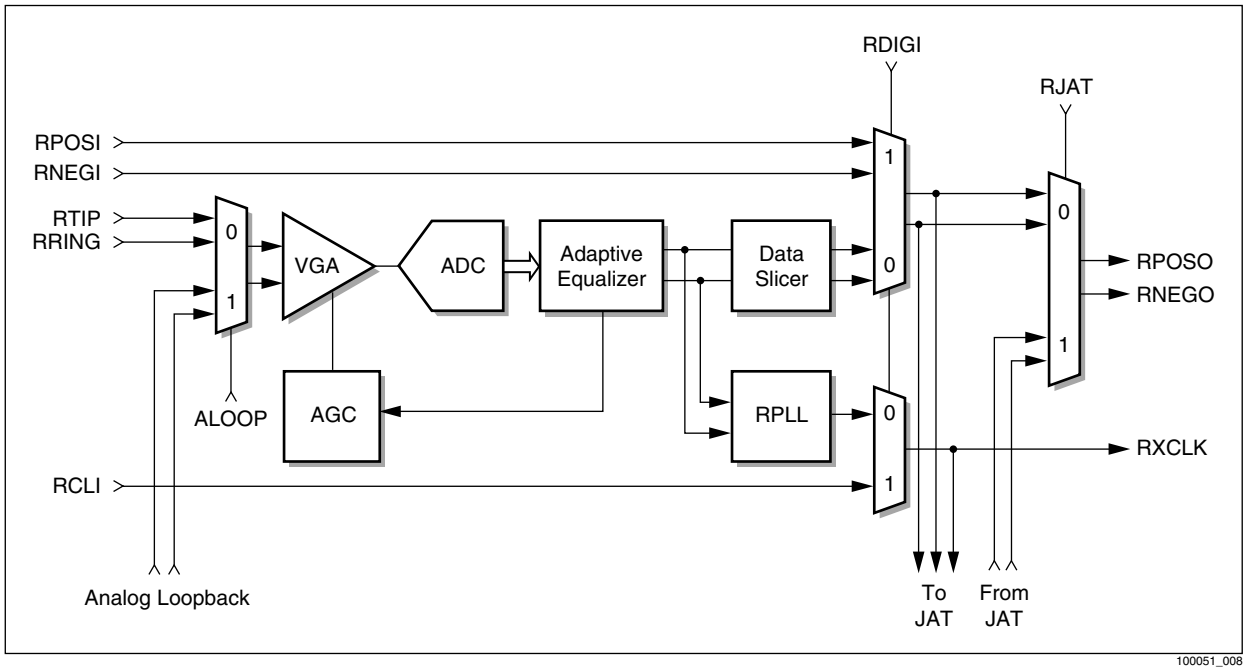
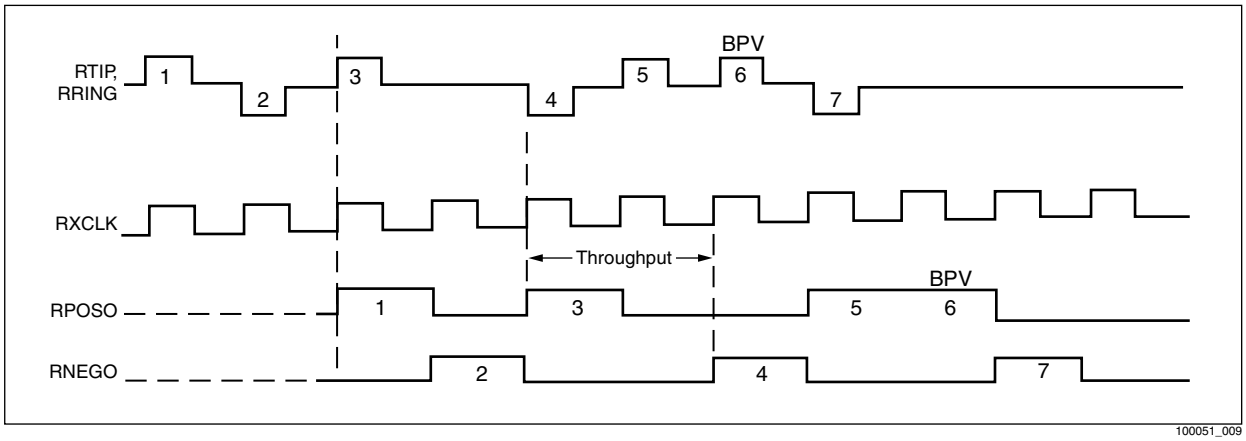
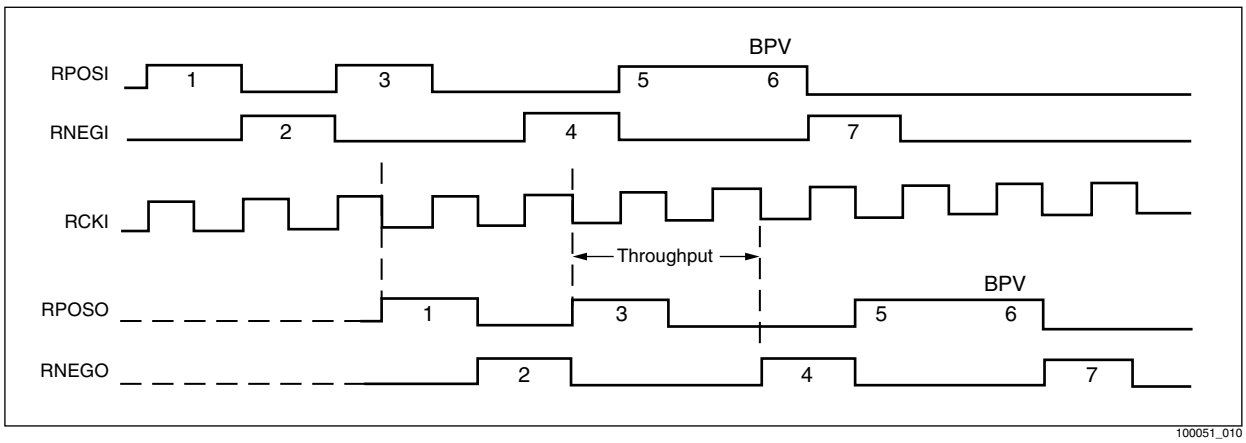


Figure 2-5. RLIU Waveforms—Bipolar Input Signal



If the RLIU functionality is not required, a bypass mode is provided [RDIGI; addr 020]. If the RLIU is bypassed, the RTIP/RRING pins are ignored, RPOSI/RNEGI P and N rail NRZ become inputs, and RCKI becomes the receive timing source. Figure 2-6 illustrates the relationship between the RLIU P and N rail NRZ data, the RLIU receive clock input, and the RCVR dual-rail output.

Figure 2-6. RLIU Waveforms—P and N Rail Digital Input Signal



2.2.1 Data Recovery

The RLIU recovers data from the received analog signal by normalizing the signal with the Variable Gain Amplifier (VGA) and the Automatic Gain Control (AGC), removing distortion with the Adaptive Equalizer, and extracting the data using the Data Slicer.

2.2.1.1 Automatic Gain Control

The AGC circuit adjusts the gain of the incoming differential signal to achieve a normalized level. The normalized level ensures that the input signal to the ADC is 75–100% of full scale. This is done by measuring the peak voltage of the incoming signal with a peak detector, and inversely adjusting VGA gain based on the peak value. The AGC can be forced to a fixed gain for test purposes or limited to a maximum value, which is the normal operating mode (see [FORCE_VGA; addr 020]).

2.2.1.2 Variable Gain Amplifier

The FORCE_VGA bit in the LIU Configuration register [LIU_CR; addr 020] selects whether the AGC operates in Gain Limit mode or Fixed Gain mode. In Gain Limit modes, the RLIU sensitivity is initially set to the maximum (approximately 43 dB), and the gain is adjusted based on the peak value recorded during the AGC observation period. The AGC observation period can be set to 32, 128, 512, or 2048 symbol periods [RLIU_CR; addr 022]. A short observation period allows quick responses to pulse height variations but not possible overshoots. A long observation period minimizes overshoots, but does not react quickly to pulse height variations. The real-time status of the VGA gain setting can be read in the Variable Gain Amplifier Status register [VGA; addr 029] and used to approximate the receive analog signal level.

In Fixed Gain mode, the RLIU sensitivity is set to the value stored in the Variable Gain Amplifier Maximum register [VGA_MAX; addr 024]. VGA_MAX is a 6-bit register that allows up to 64 gain settings in 1.25 dB steps.

2.2.1.3 Adaptive Equalizer

After the input amplitude has been normalized, the adaptive equalizer attempts to remove the distortion introduced by the cable. The transfer function of the equalizer is initially adjusted based on the peak value of the input signal because this value provides some indication of the line length on the input. The Adaptive Equalizer then automatically fine tunes to remove most of the signal distortion due to intersymbol interference, noise, and other cable length effects.

In certain applications the device can be connected to a DSX monitor point that has been resistively attenuated. Because this resistive attenuation adds no phase-versus-frequency distortion, the VGA gain must be adjusted. This is done by configuring the Receive Pad Resistor Compensation (ATTN[1,0]) in the LIU Configuration register [LIU_CR; addr 020]. The resistive attenuation can be configured to be either 0, –10, –20, or –30 dB.

2.2.1.4 Data Slicer

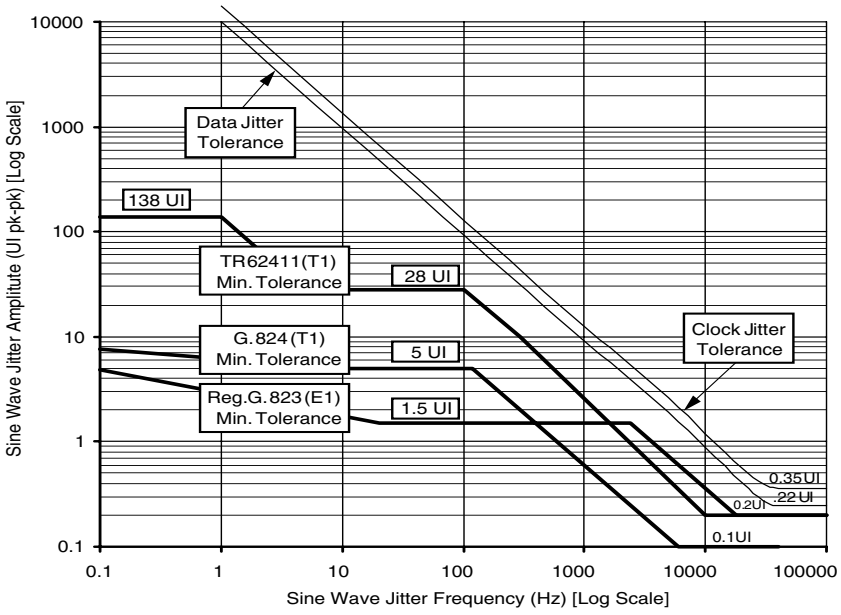
The Data Slicer extracts the data from the equalized signal by comparing the differential inputs to threshold values. The threshold values are dynamically set, based on a percentage of the peak level obtained by the peak detector. The percentage is 50% of peak for both DS1 and CEPT. Dynamically adjusting the threshold values ensures optimum signal-to-noise ratio. If the SQUELCH bit is set in the LIU Configuration register [LIU_CR; addr 020] and the input signal level is below threshold for the entire AGC observation period (EYEOPEN = 0), Data Slicer output is forced to all 0s.

2.2.2 Clock Recovery

2.2.2.1 Phase Locked Loop

The Receive Phase Locked Loop (RPLL) recovers the line rate clock from the Data Slicer dual-rail outputs. The RPLL generates a recovered clock that tracks the jitter in the data from the Data Slicer, and sustains the data-to-clock phase relationship in the absence of incoming pulses. Figure 2-7 illustrates the Receive LIU's input clock and data jitter tolerance.

Figure 2-7. Receive Input Jitter Tolerance



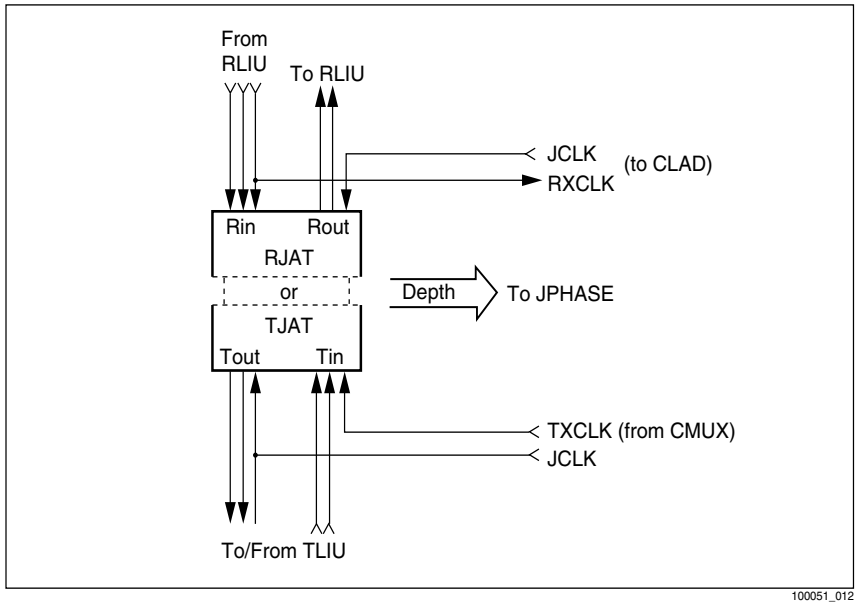
NOTE(S):
This figure shows the jitter tolerance of JAT and CLAD only.
The jitter tolerance of RPLL together with JAD/CLAD would be limited to the jitter tolerance of RPLL, as illustrated in figure titled, "Jitter Attenuator Block Diagram".

100051_011

2.3 Jitter Attenuator

The Jitter Attenuator (JAT), illustrated in Figure 2-8, attenuates jitter in the receive or transmit path, but not both simultaneously. In the receive configuration, the line signal is recovered by the RLIU and is dejittered before it is decoded by the RCVR. In the transmit configuration, the encoded signal from the transmit block is dejittered before it is transmitted by the Transmit Line Interface Unit (TLIU). The JAT receive/transmit configuration is done through the JDIR bit in the Jitter Attenuator Configuration register [JAT_CR; addr 002]. The JAT can also be completely disabled using the Jitter Attenuation (JEN) bit in the JAT_CR register.

Figure 2-8. Jitter Attenuator Block Diagram



2.3.1 Elastic Store

The elastic store size (RJAT or TJAT) is configurable using JSIZE[2:0] in the JAT_CR. The elastic store sizes available are 8, 16, 32, 64, and 128 bits. The 32-bit elastic store depth is sufficient to meet jitter tolerance requirements in cases where the jitter attenuator cutoff frequency is programmed at 6 Hz or below, and when the selected clock reference is frequency-locked. The larger elastic store depths allows greater accumulated phase offsets. For example, the 128-bit depth can tolerate up to ±64 bits of accumulated phase offset.

Because the elastic store is a fixed size, it can overflow and under-run. Overflow occurs when the elastic store is full; under-run occurs when the elastic store is empty. If either of these two conditions occurs, the Jitter Attenuator Elastic Store Limit Error bit (JERR) in the Error Interrupt Status register [ISR5; addr 006] is set. To determine if an overflow or under-run occurs, the Jitter Attenuator Empty/Full bit (JMPTY) must be read from the Receive LIU Status register [RSTAT; addr 021].

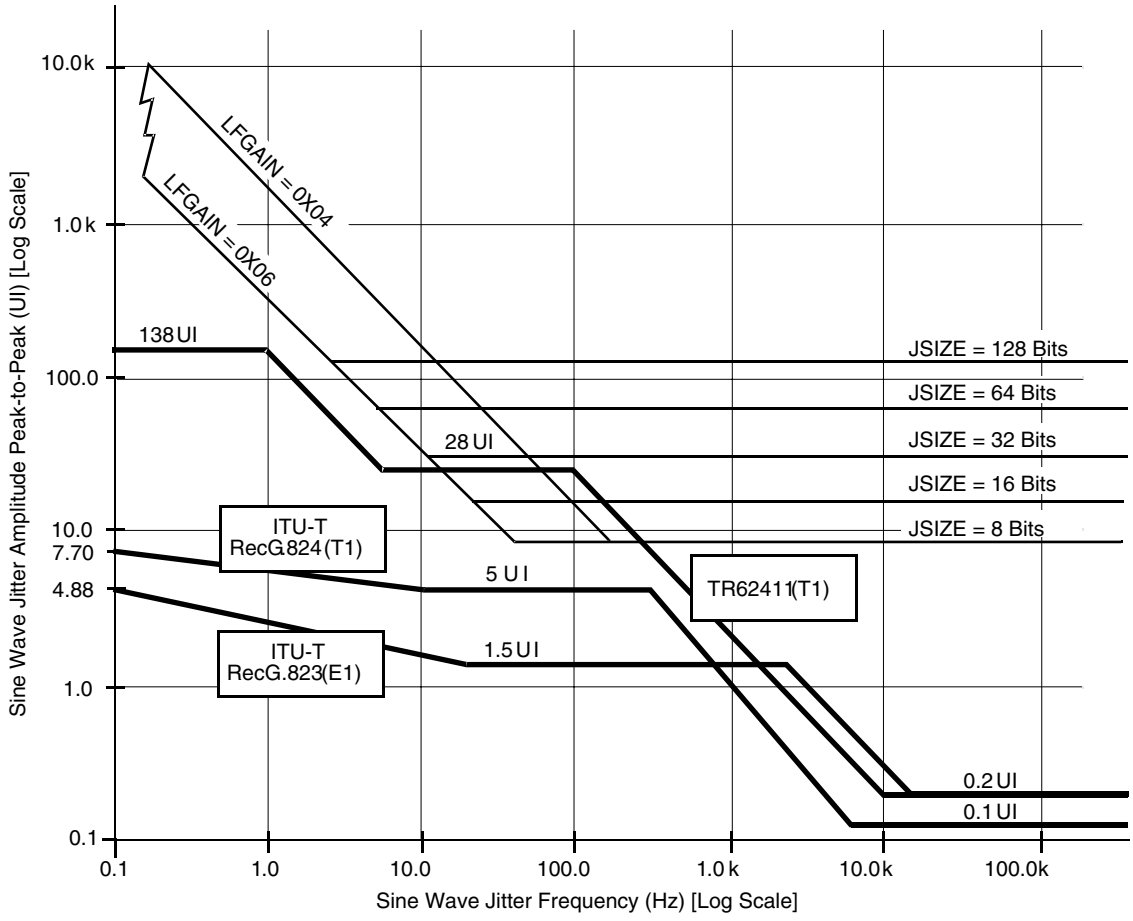
The elastic store is a circular buffer with independent read and write pointers. The difference between the read and write pointers is the phase error (JPHASE) between the input and output clocks of the jitter attenuator, and is used to generate JCLK. The read and write pointers are initialized using JCENTER in the JAT_CR. JCENTER resets the write pointer and forces the elastic store read pointer to half the programmed JSIZE. JCENTER also resets the JMPTY status, so JMPTY must be read before JCENTER is written.

If JDIR is configured to put the jitter attenuator in the receive path, the write pointer is driven by the Receive Clock (RXCLK), and the read pointer is driven by the dejittered recovered clock (JCLK). The dejittered recovered clock output is available on the RCKO pin if the output is enabled using RCKO_OE in the Programmable Output Enable register [POE; addr 019]. The dejittering of the recovered clock is done by the Clock Rate Adapter Block (CLAD). CLAD is described later in this document.

If JDIR is configured to put the jitter attenuator in the transmit path, the write pointer is driven by the Transmit Clock (TXCLK), and the read pointer is driven by the dejittered transmit clock (JCLK). TXCLK can be slaved to four different clock sources: Transmit Clock Input (TCKI), Receive Clock Output (RCKO), Receive System Bus Clock Input (RSBCKI), or Clock Rate Adapter Output (CLADO). The dejittered transmit clock is available on the TCKO pin when the output is enabled using TCKO_OE in POE.

The receive LIU input clock and data jitter tolerance meets *TR 62411-1990*, as illustrated in Figure 2-7. The JAT input jitter tolerance is illustrated in Figure 2-9. The JAT jitter transfer function meets *TR 62411-1990*, as defined in Figure 2-10 and Table 2-1.

Figure 2-9. CLAD/JAT Input Jitter Tolerance



NOTE(S):
This figure shows the jitter tolerance of JAT and CLAD only. The jitter tolerance of RPLL together with JAD/CLAD would be limited to the jitter tolerance of RPLL, as illustrated in Figure 2-8.

Figure 2-10. CLAD/JAT Jitter Transfer Functions

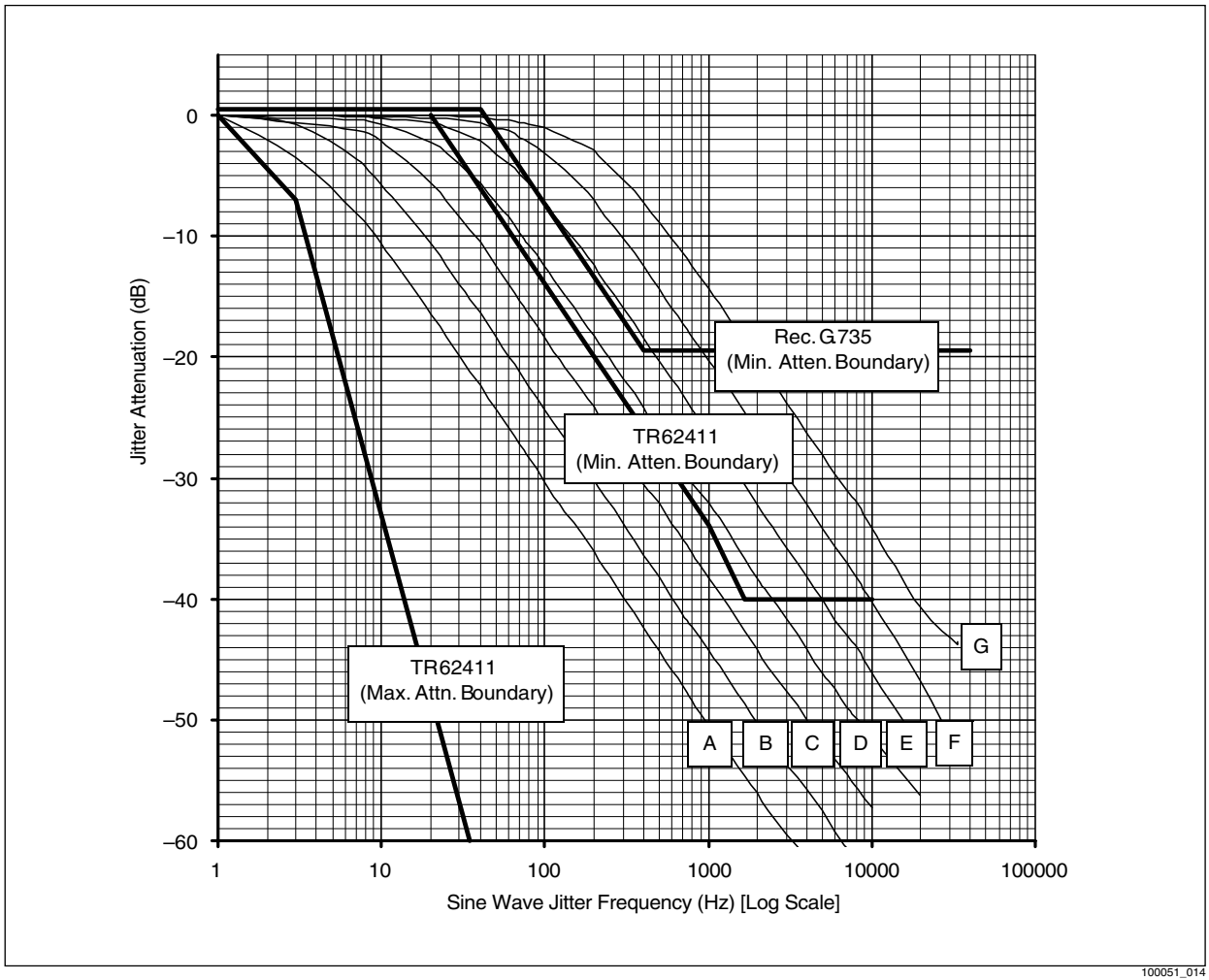


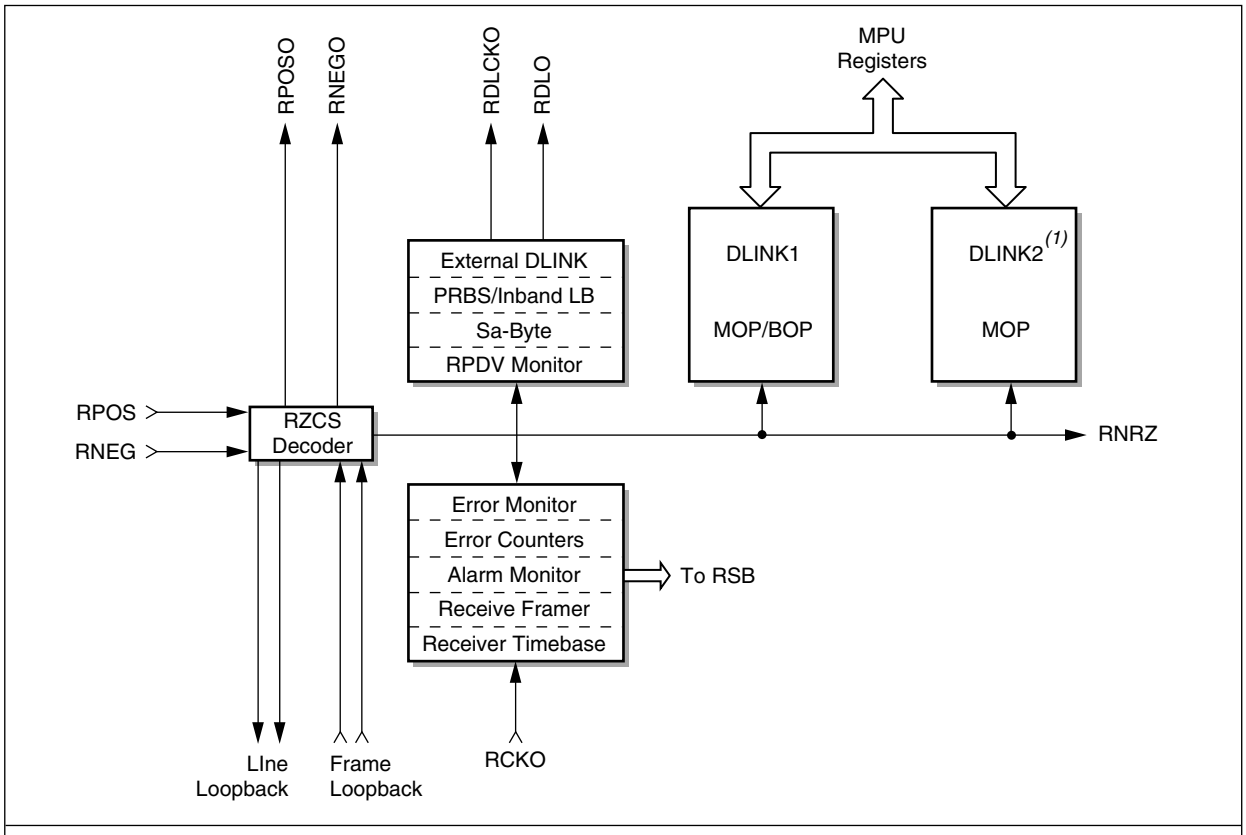
Table 2-1. CLAD/JAT Jitter Transfer Functions

Curve	JAT FIFO Size (bits)	LF Gain
A	128	0x06
B	128 64	0x05 0x06
C	128 64 32	0x04 0x05 0x06
D	64 32 16	0x04 0x05 0x06
E	32 16 8	0x04 0x05 0x06
F	16 8	0x04 0x05
G	8	0x04

2.4 Receiver

The Digital Receiver (RCVR) monitors T1/E1 overhead data and decodes positive and negative rail NRZ data from the RLIU into single rail NRZ data processed by the RSB. The RCVR, illustrated in Figure 2-11, is made up of the following elements: Zero Code Suppression (RZCS) Decoder, In-Band Loopback Code Detector, Error Counters, Error Monitor, Alarm Monitor, Test Pattern Receiver, Receive Framer, External Receive Data Link, and Receive Data Links.

Figure 2-11. RCVR Diagram



NOTE(S):
(1) DLINK2 not available in Bt28376 device.

100051_015

2.4.1 ZCS Decoder

The Receive Zero Code Suppression (RZCS) decoder decodes the dual-rail data (bipolar) into single rail data (unipolar). The Receive AMI bit (RAMI) in the Receiver Configuration register [RCR0; addr 040] controls whether or not the received signal is B8ZS/HDB3 decoded, depending on T1/E1N [addr 001] line rate selection, or depending on whether or not the RZCS decoder is bypassed. If the line code is unknown, the ZCSUB bit in the Receive LIU Status register [RSTAT; addr 021] indicates that one or more B8ZS/HDB3 substitution patterns have been received on the RTIP/RRING input. If the line code is B8ZS/HDB3 encoded, the RZCS bit in RCR0 must be set to keep the LCV counter from counting BPVs that are part of the B8ZS/HDB3 code.

2.4.2 In-Band Loopback Code Detection

The in-band loopback code detector circuitry detects receive data with in-band codes of configurable value and length. These codes can be used to request loopback of terminal equipment signals or other user-specified applications. The two codes are referred to as loopback-activate and loopback-deactivate, although the detectors need not be used only for loopback codes. Generally, any repeating 1–7 bit pattern can be selected. The loopback application is described in Section 9.3.1 of *ANSI T1.403-1995*. The loopback activate code is set in the Loopback Activate Code Pattern register [LBA; addr 043]. The loopback deactivate code is set in the Loopback Deactivate Code Pattern register [LBD; addr 044].

The sequence length for the loopback activate and deactivate codes can be programmed for 4, 5, 6, or 7 bits by setting the code length bits of the Receive Loopback Code Detector Configuration register [RLB; addr 042]. Shorter codes can be programmed by repeating the expected pattern (e.g., 3+3 bit code programmed as 6-bit code).

```
T1 In-Band Loopback Codes
       Activate 00001
       Deactivate 001
```

When a loopback code is detected, the LOOPUP or LOOPDN status bit is set in the Alarm 2 register [ALM2; addr 048], and the corresponding LOOPUP or LOOPDN bit in Alarm 2 Interrupt Status register (ISR6; addr 005] is set. The loopback detection interrupt can be enabled using the Alarm 2 Interrupt Enable register [IER6; addr 00D]. When enabled, a loop-up or loop-down code detection sets the Alarm 2 Interrupt bit [ALARM2] in the Interrupt Request register [IRR; addr 003] and generates an interrupt. Since loopbacks are not automatically initiated, the processor must intercept and interpret the interrupt status condition to determine when it must enable or disable the loopback control mechanism (e.g., LLOOP; addr 014).

The in-band loopback code detector circuitry is only applicable to T1 mode.

2.4.3 Error Counters

The following Performance Monitoring (PM) counters are available in the RCVR: Framing Bit Errors (FERR), CRC Errors (CERR), Line Code Violations (LCV), and Far End Block Errors (FEBE). All PM count registers are reset on read unless LATCH_CNT is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_CNT enables the one-second latching of counts coincident with the one-second timer interrupt [ISR6; addr 005]. One-second latching of PM counts is required if AUTO_PRM responses are enabled. All PM counters can be disabled during RLOF, RLOS, and RAIS, using the STOP_CNT bit in the LATCH register.

NOTE: If STOP_CNT is not enabled, error monitoring during RLOF conditions will detect FERR, CERR, and FEBE according to the last known frame alignment.

2.4.3.1 Frame Bit Error Counter

The 12-bit Framing Bit Error counter [FERR; addr 050 and 051] increments each time a receive Ft, Fs, T1DM, FPS, or FAS error is detected. Fs (T1) and NFAS (E1) errors can be included in the FERR count by setting FS_NFAS in the Receive Alarm Signal Configuration register [RALM; addr 045]. An interrupt is available to indicate that the FERR counter overflowed in the Counter Overflow Interrupt Status register [ISR4; addr 007].

2.4.3.2 CRC Error Counter

The 10-bit Cyclic Redundancy Check Error counter [CERR; addr 052 and 053] increments each time a receive CRC4 (E1) or CRC6 (T1) error is detected. An interrupt is available to indicate that the CERR counter overflowed in ISR4.

2.4.3.3 LCV Error Counter

The 16-bit Line Code Violation Error counter [LCV; addr 054 and 055] increments each time a receive Bipolar Violation (BPV)—not including line coding—is detected. The LCV count can include EXZ if EXZ_LCV in the Receive Alarm Signal Configuration register [RALM; addr 045] is set. EXZ can be configured [RZCS; addr 040] to be 8 or 16 successive 0s, following a 1. An interrupt is available to indicate that the LCV counter overflowed in ISR4.

2.4.3.4 FEBE Counter

The 10-bit Far End Block Error (FEBE) counter [FEBE; addr 056 and 057] increments each time the RCVR encounters an E1 far-end block error. An interrupt is available to indicate that the FEBE counter overflowed in ISR4.

2.4.4 Error Monitor

The following signal errors are detected in the RCVR: Frame Bit Error (FERR), MFAS Error (MERR), CAS Error (SERR), CRC Error (CERR), and Pulse Density Violations (PDVs). Each error type has an interrupt enable bit that allows an interrupt to occur marking the event, and has an interrupt register bit read by the interrupt service routine. All error status registers are reset on read unless the LATCH_ERR bit is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_ERR enables the one-second latching of alarms coincident with the one-second timer interrupt [ISR6; addr 005]. With LATCH_ERR enabled, any error detected during the one-second interval is latched and held during the following one-second interval. LATCH_ERR allows the processor to gather error statistics based on the one-second interval.

FERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. FERR indicates that one or more Ft/Fs/FPS frame bit errors or FAS pattern errors occurred since the last time the interrupt status was read. The FERR type is determined by the receive framer's configuration [CR0; address 001].

While CRC4 framing is enabled, MERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in the Pattern Interrupt Status register [ISR0; addr 00B]. MERR is only applicable in E1 mode and indicates that one or more MFAS pattern errors occurred since the last time the interrupt status was read.

While CAS framing is enabled, SERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. SERR is applicable only in E1 mode. In this mode, SERR indicates that one or more errors were received in the TS16 Multiframe Alignment Signal (MAS) since the last time the interrupt status was read.

CERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. CERR is only applicable in T1 ESF and E1 MFAS modes. In these modes, CERR indicates that one or more bit errors were found in the CRC4/CRC6 pattern block since the last time the interrupt status was read.

A PDV is reported when the receive signal does not meet the pulse density requirements of *ANSI T1.403-1995* (Section 5.6). A PDV is declared whenever more than 15 consecutive 0s or the average 1s' density falls below 12.5%. RPDV is reported for the receive direction in the Alarm 1 Interrupt Status register [ISR7; addr 004].

2.4.5 Alarm Monitor

The following signal alarms are detected in the RCVR: Loss of Frame (LOF), Loss of Signal (LOS), Analog Loss of Signal (ALOS), Alarm Indication Signal (AIS), Remote Alarm Indication (RAI) or Yellow Alarm (YEL), Multiframe Yellow Alarm (MYEL), Severely Errored Frame (SEF), Change of Frame Alignment (COFA), and Multiframe AIS (MAIS). Each alarm has the following: a status register bit that reports the real-time status of the event, an interrupt enable bit that enables an interrupt to mark the event, and an interrupt register bit read by the interrupt service routine to identify the event that caused the interrupt. All alarm status registers are reset on read unless the LATCH_ALM bit is set in Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_ALM enables the one-second latching of alarms coincident with the one-second timer interrupt [ISR6; addr 005]. With LATCH_ALM enabled, any alarm detected during the one-second interval is latched and held during the following one-second interval.

2.4.5.1 Loss of Frame

Receive Loss of Frame (RLOF) is declared when the receive data stream does not meet the framing criteria specified in the Receiver Configuration register [RCR0; addr 040].

If the line rate is E1 [T1/E1N; addr 001], RLOF is the logically ORed status of FAS, MFAS, and CAS alignment. These alignments, FRED, MRED and SRED, respectively, are available separately in the Alarm 3 Status register [ALM3; addr 049]. Once RLOF is declared, the LOF[1:0] bits in ALM3 report the reason for E1 loss of frame alignment. In T1 mode, RLOF is equal to FRED.

The RLOF real-time status is available in Alarm 1 Status register [ALM1; addr 047], and the interrupt status is set in the Alarm 1 Interrupt Status register [ISR7; addr 004]. The RLOF interrupt is enabled by setting RLOF in the Alarm 1 Interrupt Enable register [IER7; addr 00C].

An FRED count [FRED[3:0]; addr 05A] is also available in the SEF/LOF/COFA Alarm Counter [AERR; addr 05A]. An interrupt in Counter Overflow Interrupt Status [ISR4; addr 007] indicates that the FRED counter overflowed. COFA [1:0] is applicable to T1 modes only.

While T1 framing mode is enabled, the RLOF status and RLOF interrupt status are integrated over 2.0–2.5 seconds if the RLOF_INTEG bit is set in the Receive Alarm Signal Configuration register [RALM; addr 045]. The FRED count is unaffected by RLOF_INTEG.

2.4.5.2 Loss of Signal

If the line rate is T1, the criteria for Receive Loss of Signal (RLOS) is 100 contiguous 0s (consistent with the standard requirement of 175 ±75 0s). If the line rate is E1, the criteria for RLOS is 32 contiguous 0s. RLOS is cleared upon detecting an average pulse density of at least 12.5% (occurring during a period of 114 bits starting with the receipt of a pulse, and where no occurrences of 100 or 32 contiguous 0s are detected).

The RLOS real-time status is available in ALM1, and the interrupt is available in ISR7. The XMTR can be configured to automatically generate an Alarm Indication Signal (AIS) in the transmit direction when RLOS is declared (see AUTO_AIS [TALM; addr 075].

2.4.5.3 Analog Loss of Signal

Receive Analog Loss of Signal (RALOS) is declared in analog receive mode, [RDIGI = 0; addr 020], when RTIP/RRING input signal amplitude is less than the programmed (VGA_MAX) threshold. In the digital receive mode, RDIGI = 1, RALOS is declared when the Receive Clock Input (RCKI) remains low for 125 µs. RALOS real-time status is available in ALM1; RALOS interrupt is available in ISR7.

2.4.5.4 Alarm Indication Signal

If the line rate is T1 [T1/E1N; addr 001], the criteria for Receive Alarm Indication Signal (RAIS) is the reception of 4 or fewer 0s in a period of 3 ms (4632 bits), and the assertion of RLOF. If the line rate is E1, RAIS is set when 2 consecutive double frames each contain 2 or fewer 0s out of 512 bits and FAS alignment is lost [FRED; addr 049]. RAIS real-time status is available in ALM1; RAIS interrupt is available in ISR7.

2.4.5.5 Yellow Alarm

The criteria for Yellow Alarm (YEL) is described in Table 3-13. YEL real-time status is available in ALM1; YEL interrupt is available in ISR7.

2.4.5.6 Multiframe YEL

The criteria for Multiframe Yellow Alarm is described in Table 3-13. MYEL real-time status is available in ALM1; MYEL interrupt is available in ISR7.

2.4.5.7 Severely Errored Frame

A SEF is reported when the receive signal does not meet the requirements of ANSI T1.231. SEF real-time status is available in ALM3. A 2-bit counter is also available [SEF; addr 05A]. An interrupt is available in ISR4 to indicate that the SEF counter overflowed. In T1, the SEF detection window consists of 3 ms intervals that start at FPS bit_6 of multiframe_N (i.e., the last FPS bit of a given multiframe) and close after FPS bit #5 of multiframe_N+1. In E1, the SEF detection window uses arbitrarily initialized 2 ms intervals.

2.4.5.8 Change of Frame Alignment

Each COFA increments a 2-bit counter [COFA; addr 05A]. An interrupt is available in ISR4 to indicate that the COFA counter overflowed.

2.4.5.9 Receive Multiframe AIS

Receive Multiframe AIS (RMAIS) is reported when the receive TS16 signal contains 3 or fewer 0s out of 128 bits in each multiframe over 2 consecutive multiframes according to the requirements of *ITU–T Recommendation G.775*. RMAIS is checked only in E1 CAS mode. RMAIS real-time status is available in ALM3 [addr 049].

2.4.6 Test Pattern Receiver

The test pattern receiver circuitry can sync on framed or unframed PRBS patterns and count bit errors. This feature is particularly useful for system diagnostics, production testing, and test equipment applications. The PRBS patterns available include 2E11-1, 2E15-1, 2E20-1, and 2E23-1. Each pattern can optionally include Zero Code Suppression (ZCS).

The Receive Test Pattern Configuration register [RPATT; addr 041] controls the test pattern receiver circuit. BSTART control bit (in RPATT) must be active to enable the test pattern receiver and to begin counting bit errors. RPATT controls the PRBS pattern, ZCS setting (ZLIMIT), and T1/E1 framing (FRAMED). RPATT selects which PRBS pattern the receiver should hunt for pattern sync. ZLIMIT selects the maximum number of consecutive 0s the pattern is allowed to contain. FRAMED mode informs the PRBS pattern receiver not to search for the pattern in the frame bit in T1 mode or search for the pattern in time slot 0 (and time slot 16 if CAS framing is selected) in E1 mode. CAS framing is selected by setting RFRAME[3] to 1 in the Primary Control register [CR0; addr 001]. If FRAMED is disabled, the PRBS pattern receiver searches all time slots for the test pattern.

The RESEED bit in RPATT informs the receive PRBS sync circuit to begin a PRBS pattern search. Once the search begins, any additional writes to RESEED restarts the pattern sync search at a different point in the pattern. The time to sync depends on the pattern and number of bit errors in the pattern.

Pattern sync is reported (when found) in PSYNC status of the Pattern Interrupt Status register [ISR0; addr 00B]. After pattern sync is found, the PRBS Pattern Error counter [BERR; addr 058 and 059] begins counting bit errors detected on the incoming pattern, provided that BSTART remains active. Error counting stops if the BSTART bit is cleared. BERR counter is reset to 0 after every read, or latched on each ONESEC interrupt as selected by LATCH_CNT [addr 046]. An interrupt is available to indicate the BERR counter overflowed in ISR4.

2.4.7 Receive Framing

Two framers are in the receive data stream: an offline framer and an online frame status monitor. The offline framer recovers receive frame alignment; the online framer monitors frame alignment patterns and recovers multiframe alignment in E1 modes. Frame and multiframe synchronization criteria used by the framers and monitoring criteria of the online framer are selected in RFRAME[3:0] of the Primary Control register [CR0; addr 001].

Receive frame synchronization is initiated by the online framer's activation of the Receive Loss of Frame (RLOF) status bit in the Alarm 1 Status register [ALM1; addr 047]. The RLOF criteria is set in the RLOFA, RLOFB, RLOFC, and RLOFD bits of the Receiver Configuration register [RCR01; addr 040]. The online framer supports the following LOF criteria for T1: 2 out of 4, 2 out of 5, and 2 out of 6. For E1, the online framer supports 3 out of 3, with or without 915 out of 1000 CRC errors.

Once RLOF is asserted, the offline framer automatically starts searching the receive data stream for a new frame alignment, provided that receive framing is enabled [RABORT; addr 040]. If receive framing is disabled, the offline framer does not automatically search for the frame alignment, but waits for a reframe command [RFORCE; addr 040] to start a frame alignment search. If RLOF integration is enabled [RLOF_INTEG; addr 045] the RLOF status [ALM1; addr 047] and RLOF interrupt status [ISR7; addr 004] is integrated for 2.0–2.5 seconds.

The online framer continuously monitors for RLOF condition [ALM1; addr 047] and searches for E1 multiframe alignment after basic frame alignment is recovered by the offline framer. Receive multiframe alignment is declared when multiframe alignment criteria are met, as shown in Table 2-2 and 2-3. The receive online framer reports multiframe errors, frame errors, and CRC errors in the Error Interrupt Status register [ISR5; addr 006].

Table 2-2. Receive Framer Modes

T1/E1N	RFRAME[3:0]	Receive Framer Mode
0	000X	FAS Only
0	001X	FAS Only + BSLIP
0	010X	FAS + CRC
0	011X	FAS + CRC + BSLIP
0	100X	FAS + CAS
0	101X	FAS + CAS + BSLIP
0	110X	FAS + CRC + CAS
0	111X	FAS + CRC + CAS + BSLIP
1	0000	FT Only
1	0001	ESF + No CRC (FPS only)
1	0100	SF
1	0101	SF + JYEL
1	0110	SF + T1DM
1	1000	SLC + FSLOF
1	1001	SLC
1	1100	ESF + Mimic CRC
1	1101	ESF + Force CRC

Table 2-3. Criteria for Loss/Recovery of Receive Framer Alignment (1 of 2)

Mode	Description
FAS	Basic Frame Alignment (BFA) is recovered when the following search criteria are satisfied: ♦ FAS pattern (0011011) is found in frame N. ♦ Frame N + 1 contains bit 2 equal to 1. ♦ Frame N + 2 also contains FAS pattern (0011011). During FAS-only modes, BFA is recovered when the following search criteria are satisfied: ♦ FAS pattern (0011011) is found in frame N. ♦ No mimics of the FAS pattern are present in frame N+1. ♦ FAS pattern (0011011) is found in frame N + 2. ***Note***: If FAS pattern is not found in frame N + 2, or if FAS mimic is found in frame N + 1, the search restarts in frame N + 2. Loss of FAS frame alignment (FRED) is declared when one of the following criteria is met: ♦ Three consecutive FAS pattern errors are detected when the FAS pattern consists of a 7-bit (x0011011) pattern in FAS frames, and if FS_NFAS is also active [addr 045], the FAS pattern includes bit 2 of NFAS frames. ♦ Loss of MFAS (MRED) is due to 915 or more CRC errors out of 1000. ♦ Failure to locate two valid MFAS patterns within 8 ms after BFA. ***GENERAL NOTE:*** In all cases, FRED causes next search for FAS alignment to begin 1 bit after the current FAS location.
BSLIP	FAS Bit Slip Enable. Applicable only for Dutch PTT national applications. If BSLIP is enabled, the online framer is allowed to change RX timebase by ±1 bit when a 1-bit FAS pattern slip is detected. BSLIP does not affect the offline framer's search criteria.
MFAS	CRC4 Multiframe Alignment is recovered when the following search criteria are satisfied: ♦ BFA is recovered, identifying FAS and NFAS frames. ♦ Within 8 ms after BFA, bit 1 of NFAS frames contains two MFAS patterns (001011xx). The second MFAS must be aligned with respect to first MFAS, but the second MFAS pattern is not necessarily received in consecutive frames. ♦ Within 8 ms after BFA, bit 1 of NFAS frames contains the second MFAS pattern (001011xx), aligned to first MFAS. Loss of MFAS alignment (MRED) declared when one of the following criteria is met: ♦ 915 or more CRC4 errors out of 1000 (submultiframe) blocks. ♦ Loss of FAS (FRED). ***GENERAL NOTE:*** If Disable 915 CRC Reframe is set [RLOFD; addr 040], then MRED is activated only by FRED.
CAS	CAS Multiframe Alignment is recovered when the following search criteria are satisfied: ♦ BFA is recovered, identifying TS0 through TS31. ♦ MAS (0000xxxx) multiframe alignment signal pattern is found in the first 4 bits of TS16, and 8 bits of TS16 in preceding frame contains non-0 value. Loss of CAS alignment (SRED) is declared when one of the following criteria is met: ♦ Two consecutive MAS pattern errors are detected. ♦ TS16 contains all 0s in 2 multiframes (32 consecutive frames). ♦ Loss of FAS (FRED).
FT Only	Terminal frame alignment is recovered when the following occurs: The first valid Ft pattern (1010) is found in 12 alternate F bit locations (3 ms), where F bits are separated by 193 bits. During Ft-only mode, loss of frame alignment (FRED) is declared when the number of Ft bit errors detected meets selected loss of frame criteria [RLOFA–RLOFC; addr 040].

Table 2-3. Criteria for Loss/Recovery of Receive Framer Alignment (2 of 2)

Mode	Description
SF	Superframe alignment is recovered when terminal frame alignment is recovered, identifying Ft bits. Depends on SF submode: if JYEL, only Ft bits are used; Fs bits are ignored. If no JYEL, SF pattern (001110) found in Fs bits. During any SF mode, loss of frame alignment (FRED) is declared when the number of frame errors detected, either Ft or Fs bit errors, meets selected loss of frame criteria [RLOFA–RLOFC; addr 040]. FS_NFAS [addr 045] determines whether Fs bits are included in error count.
SLC	Superframe alignment is recovered when ♦ Terminal frame alignment is recovered, identifying Ft bits. ♦ SLC pattern (see Table A-3) is found in 16 of 36 Fs bits, according to Telcordia *TR-TSY-000008*. During SLC modes without FSLOF, loss of frame alignment (FRED) is declared when the number of Ft bit errors detected meets selected reframe criteria [RLOFA–RLOFC; addr 040].
FSLOF	FSLOF instructs the online framer to monitor 16 of 36 Fs bits (SLC multiframe pattern) for loss of frame alignment criteria. FS_NFAS [addr 045] must also be set to include Fs bits in loss of frame. FSLOF does not affect the offline framer's search criteria.
ESF	Extended Superframe alignment is recovered when A valid FPS candidate is located (001011). Candidate bits are each separated by 772 digits and are received without pattern errors. If there is only 1 valid FPS candidate and the mode is one of the following: No CRC mode—align to FPS, regardless of CRC6 comparison. Mimic CRC mode—align to FPS, regardless of CRC6 comparison. Force CRC mode—align to FPS, only if CRC6 is correct. If there are two or more valid FPS candidates and the mode is one of the following: No CRC mode—do not align (INVALID status). Mimic CRC mode—align to first FPS with correct CRC6. Force CRC mode—align to first FPS with correct CRC6. During any ESF mode, loss of frame alignment (FRED) is declared when: Number of FPS pattern errors detected meets selected loss of frame criteria [RLOFA–RLOFC; addr 040].
T1DM	During T1DM mode, frame alignment is recovered in two steps: 1. A 6-bit T1DM pattern (10111xx0) is found. 2. A valid F bit pattern (Ft, Fs, or FPS) is found in the first six consecutive frames of the 12-frame cycle aligned to the T1DM pattern. During T1DM mode, loss of frame alignment (FRED) is declared when the number of frame errors detected, either Ft, Fs, or T1DM errors, meets selected loss of frame criteria [RLOFA–RLOFC; addr 040]. Fs_NFAS; addr 046] does not affect T1DM mode. ***Note:*** To meet Telcordia *TA-TSY-000278*, the processor must select SF + T1DM framer mode, RLOFC (2 of 6) reframe criteria, and FS_NFAS inactive.

The offline framer is shared between the RCVR and XMTR and can search in only one direction at any time. Consequently, the processor arbitrates which direction is searched by enabling the reframe request (RLOF and TLOF) for that direction.

The offline framer waits until the current search is complete (see [FSTAT; addr 017]) before checking for pending LOF reframe requests. If both online framers have pending reframe requests, the offline framer aligns to the direction opposite from that which was most recently searched. For example, if TLOF is pending at the conclusion of a receive search which timed out without finding alignment, the offline framer switches to search in the transmit direction. The TLOF switchover is prevented in the preceding example if the processor asserts TABORT to mask the transmit reframe request. TABORT does not affect TLOF status reporting. For applications that frame in only 1 direction, the opposite direction should be masked. If, at the conclusion of a receive search, TLOF status is asserted but masked by TABORT, the offline framer continues to search in the receive direction. For applications that frame in both directions, the processor can allow the offline framer to automatically arbitrate among pending reframe requests, or can elect to manually control reframe precedence. An example of manual control follows:

```
1 Initialize RABORT = 1 and TABORT = 1.

2 Enable RLOF and TLOF interrupts.

3 Read clear pending ISR interrupts.

4 Release RABORT = 0.

5 Call LOF Service Routine if either RLOF or TLOF
        interrupt;

{

(check current LOF status (ALMI, 2; addr 047, 048)

If RLOF recovered and TLOF lost

—Assert RABORT = 1

—Release TABORT = 0

If RLOF lost or TLOF recovered

—Assert TABORT = 1

—Release RABORT = 0

}
```

The status of the offline framer can be monitored for diagnostic purposes using the Offline Framer Status register [FSTAT; addr 017]. The register reports if the offline framer:

- is looking at the receive or transmit data streams (RX/TXN)
- is actively searching for a frame alignment (ACTIVE)
- found multiple framing candidates (TIMEOUT)
- found frame sync (FOUND)
- found no frame alignment candidates (INVALID)

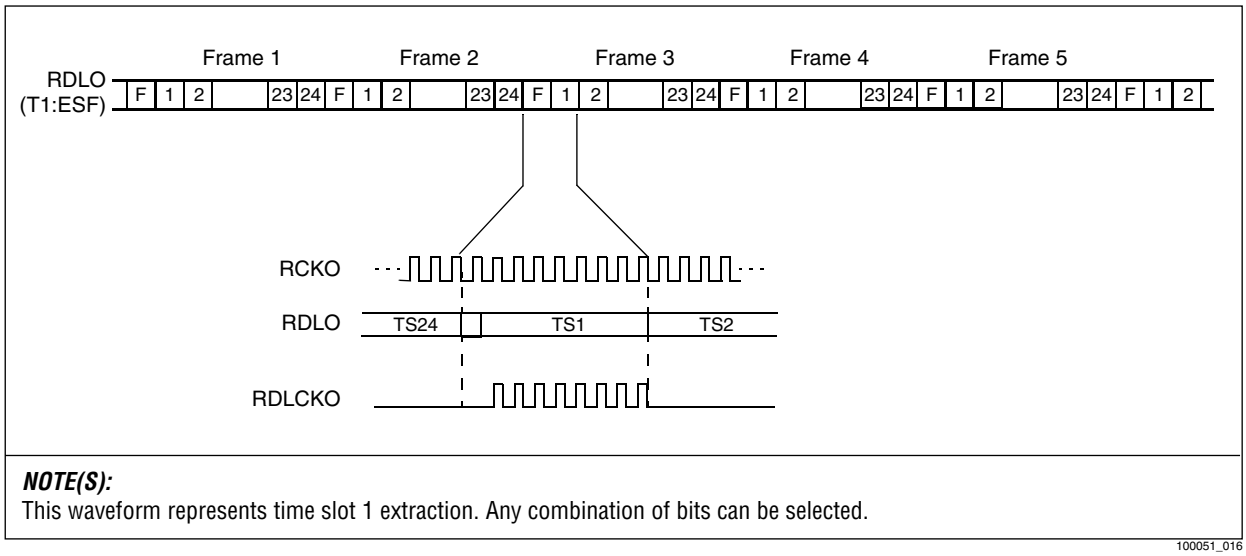
NOTE: These status bits are updated in real time and might be active for only very short (1-bit) periods of time.

2.4.8 External Receive Data Link

The External Data Link (DL3) provides signal access to any bit(s) in any time slot of all frames, odd frames, or even frames, including T1 framing bits. Pin access to the DL3 receiver is provided through RDLCKO and RDLO. These two pins serve as the DL3 clock output (RDLCKO) and data output (RDLO). The data link mode of the pins is selected using the RDL_IO bit in the Programmable Input/Output register [PIO; addr 018].

Control of DL3 is provided in two registers: External Data Link Channel [DL3_TS; add 015] and External Data Link Bit [DL3_BIT; addr 016]. RDL3 is set up by selecting the bit(s) (DL3_BIT) and time slot [TS[4:0]; addr 015] to be monitored, and then enabling the data link [DL3EN; addr 015], which starts the RDLCKO and TDLCKO gapped clock outputs that mark the selected bits, as shown in Figure 2-12.

Figure 2-12. Receive External Data Link Waveforms



NOTE(S):
This waveform represents time slot 1 extraction. Any combination of bits can be selected.

100051_016

2.4.9 Sa-Byte Receive Buffers

The Sa-Byte buffers give read access to the odd frame Sa bits in E1 mode. Five receive Sa-Byte buffers [RSA4 to RSA8; addr 05B to 05F] are available. As a group, the buffers are updated every multiframe from Sa-bits received in TS0. This gives the processor up to 2 ms after the receive multiframe interrupt [RMF; addr 008] occurs to read any Sa-Byte buffer before the buffer content changes.

2.4.10 Receive Data Link

The RCVR contains two independent data link controllers (DL1 and DL2) and a Bit-Oriented Protocol (BOP) transceiver. DL1 and DL2 can be programmed to send and receive HDLC-formatted messages in the Message-Oriented Protocol (MOP) mode. Alternatively, unformatted serial data can be sent and received over any combination of bits within a selected time slot or F-bit channel. The BOP transceiver can preemptively receive and transmit BOP messages, such as ESF Yellow Alarm.

2.4.10.1 Data Link Controllers

The Bt8370 and Bt8375 provide two internal data link controllers, and the Bt8376 provides a single controller (DL1). DL1 and DL2 control two serial data channels operating at multiples of 4 Kbps—up to the full 64 Kbps time slot rate—by selecting a combination of bits from odd, even, or all frames. Both DL1 and DL2 support the following: ESF Facilities Data Link (FDL), SLC-96 Data Link, Sa Data Link, Common Channel Signaling (CCS), Signaling System #7 (SS7), ISDN LAPD channels, Digital Multiplexed Interface (DMI) Signaling in TS24, ETSI V.5.1 and V.5.2 control channels. DL1 and DL2 each contain a 64-byte receive buffer that functions as either programmable length circular buffers or full-length data FIFOs.

Both data link controllers are configured identically, except for their offset in the register map. The DL1 address range is 0A4 to 0AE, and the DL2 address range is 0AF to 0B9. From this point on, DL1 is used to describe the operation of both data link controllers.

DL1 is enabled using the DL1 Control register [DL1_CTL; addr 0A6]. DL1 does not function until it is enabled. DL1_CTL also controls the format of the data. The following data formats [DL1[1:0]; addr 0A6] are supported on the data link: Frame Check Sequence (FCS), non-FCS, PACK8, or PACK6. FCS and non-FCS are HDLC formatted messages. PACK8 and PACK6 are unformatted messages with 8 bits per FIFO access, or 6 bits per FIFO access, respectively (see Table 2-4).

Table 2-4. Commonly Used Data Link Settings

Data Link	Frame	Time Slot	Time Slot Bits	Mode
ESF FDL	Odd	0 (F bits)	Don't Care	FCS
T1DM R Bit	All	24	00000010	FCS
SLC-96	Even	0 (F bits)	Don't Care	PACK6
ISDN LAPD	All	N	11111111	FCS
Sa4	Odd	1	00001000	FCS
GENERAL NOTE: N represents any T1/E1 time slot.				

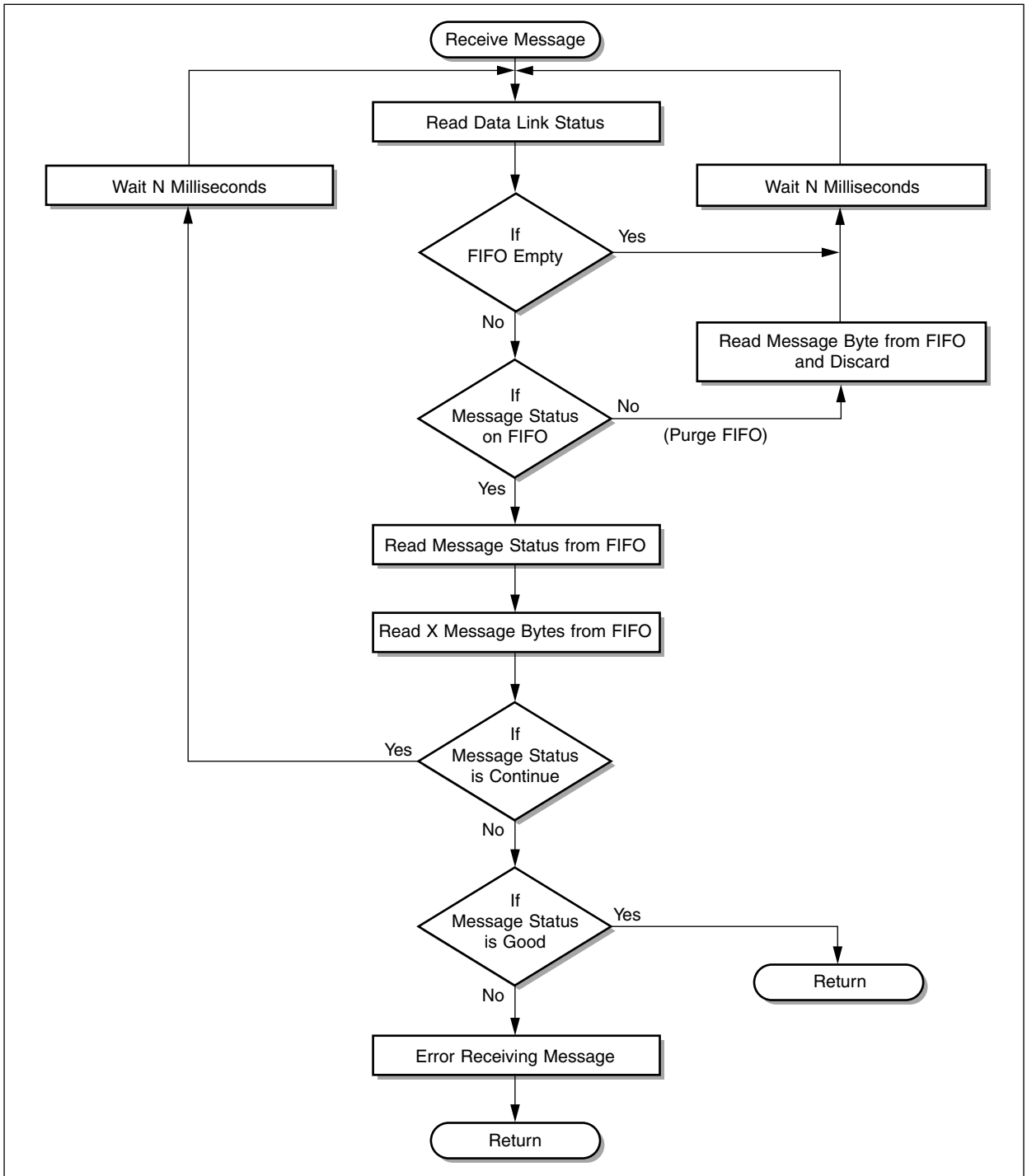
The time slot and bit selection are performed through the DL1 Time Slot Enable register [DL1_TS; addr 0A4] and the DL1 Bit Enable register [DL1_BIT; addr 0A5]. The DL1 Time Slot Enable register selects the frames and time slot to extract the data link. The frame select tells the receiver to extract the time slot in all frames, odd frames, even frames. The time slot enable is a value between 0 and 31 that selects which time slot to extract. The DL1 Bit Enable register selects which bits are extracted in the selected time slot. See Table 2-4 for the common frame, time slot, time slot bits, and modes used.

The Receive Data Link FIFO #1 [RDL1; addr 0A8] is 64 bytes long. The Receive FIFO is formatted differently than the transmit FIFO. The Receive FIFO contains not only received messages, but also a status byte preceding each message that specifies the size of the received message and the status of that message. The message status reports if the message was aborted, received with a correct/incorrect FCS, or continued. A continued message means the byte count represents a partial message. Once all message bytes are read, the FIFO contains another status byte. Message bytes can be differentiated from status bytes in the FIFO by reading the RSTAT1 bit in the RDL #1 Status register [RDL1_STAT; addr 0A9]. RSTAT1 reports if the next byte read from the FIFO is a status byte or some number of message bytes.

The receive data link controller has a versatile microprocessor interface that can be tuned to the system's CPU bandwidth. For systems with one CPU dedicated to one Bt8370, the data link status can be polled. For systems where a single CPU controls multiple Bt8370s, the data link can be interrupt-driven.

See Figures 2-13 and 2-14 for a high-level description of polling and interrupt-driven Receive Data Link Controller software.

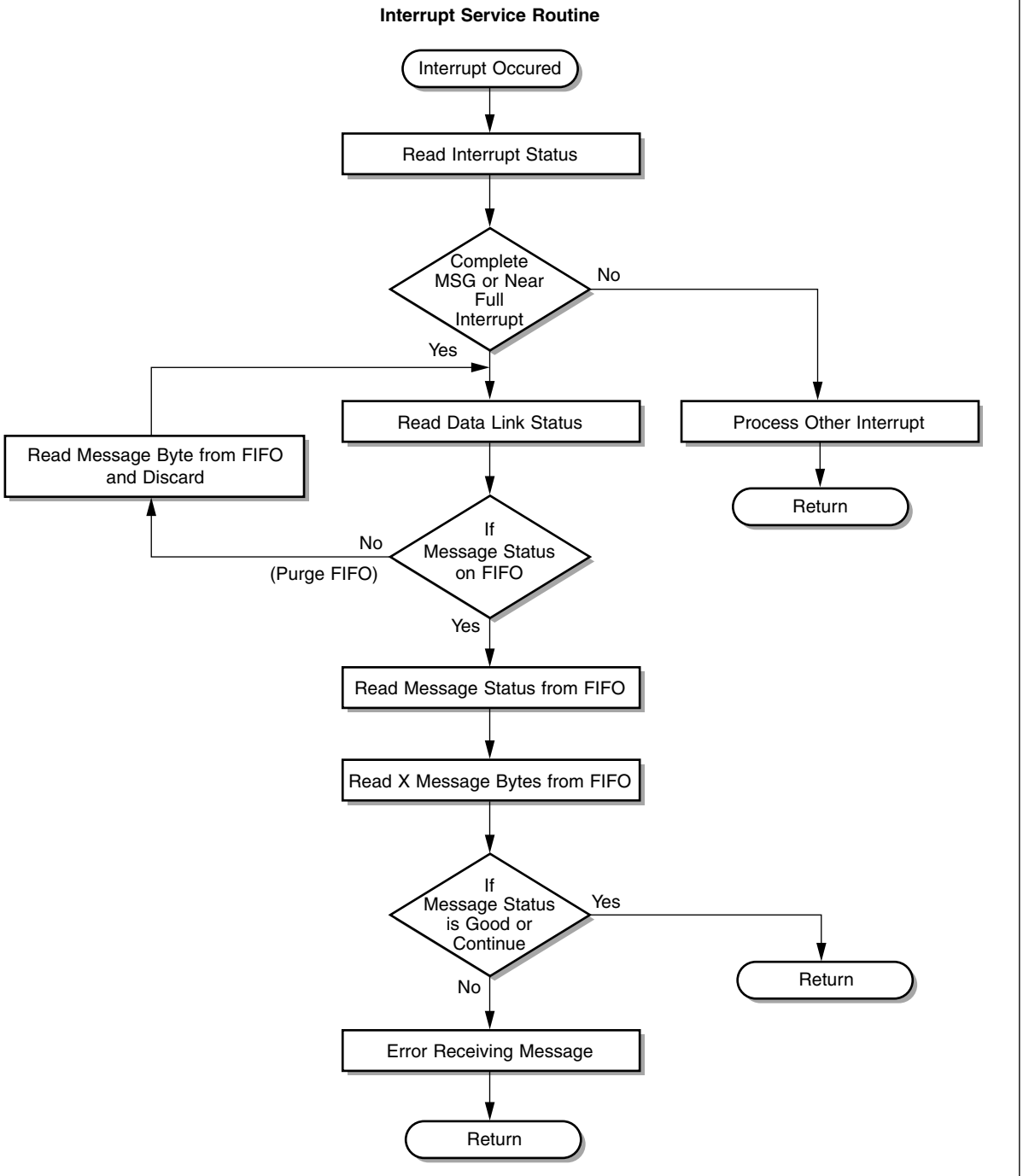
Figure 2-13. Polled Receive Data Link Processing



NOTE(S):
Message status contains number of message bytes (X) in FIFO, where X = 0 during idle channel or errored message.

100051_017

Figure 2-14. Interrupt Driven Receive Data Link Processing



NOTE(S):
Message status contains number of message bytes (X) in FIFO, where X = 0 during idle channel or errored message.

100051_018

Using the receive FIFO, an entire block of data can be received with very little microprocessor interrupt overhead. Block transfers from the FIFO can be controlled by the Near Full threshold in the FIFO Fill Control register [RDL1_FFC; addr 0A7]. The Near Full threshold is a user-programmable value between 0 and 63. This value represents the maximum number of bytes that can be placed into the receive FIFO without the near full being declared. Once the threshold is set, the Near Full Status (RNEAR1) in RDL #1 Status [RDL1_STAT; addr 0A9] is asserted when the Near Full threshold is reached. An interrupt, RNEAR, in Data Link 1 Interrupt Status [ISR2; addr 009], is also available to mark this event.

The Bt8370/75/76 uses a hierarchical interrupt structure, where one top-level interrupt sends register-directing software to the lower levels (see Interrupt Request register; addr 003). Of all the interrupt sources, the two most significant bandwidth requirements are signaling and data link interrupts. Each data link controller has a top-level interrupt status register that reports data link operations (see Data Link 1 and 2 Interrupt Status registers [ISR2, ISR1; addr 009 and 00A). The processor uses a two-step interrupt scheme for the data link:

1. It reads the Interrupt Request register.
2. It uses that register value to read the corresponding Data Link Interrupt Status register.

2.4.10.2 RBOP Receiver

The Receive Bit-Oriented Protocol (RBOP) receiver receives BOP messages, including the ESF Yellow Alarm, which consists of repeated 16-bit patterns with an embedded 6-bit code word as shown in this example:

```
0xxxxxx0 11111111 (received right to left)
[543210] RBOP = 6-bit code word
```

The BOP message channel is configured to operate over the same channel selected by Data Link #1 [DL1_TS; addr 0A4]. It must be configured to operate over the FDL channel so RBOP can detect priority, command, and response code word messages according to ANSI T1.403, Section 9.4.1.

RBOP is enabled using the RBOP_START bit in Bit Oriented Protocol Transceiver register [BOP; address 0A0]. BOP code words are received in the Receive BOP Code Word register [RBOP; addr 0A2], which contains the 6-bit code word, a valid flag (RBOP_VALID), and a lost flag (RBOP_LOST). The valid flag is set each time a new code word is put in RBOP, and is cleared on reading the code word. The lost flag indicates a new code word overwrote a valid code word before the processor read it.

The BOP receiver can be configured to update RBOP using a message length filter and integration filter. The receive BOP message length filter [RBOP_LEN; addr 0A40] sets the number of successive identical messages required before RBOP is updated. RBOP_LEN can be set to 1, 10, and 25 messages. When enabled, the RBOP integration filter [RBOP_INTEG; add 0A0] requires receipt of two identical consecutive 16-bit patterns, without gaps or errors between patterns, to validate the first code word. RBOP integration is needed to meet the code word detection criteria while receiving 1 1/1000 bit error ratio.

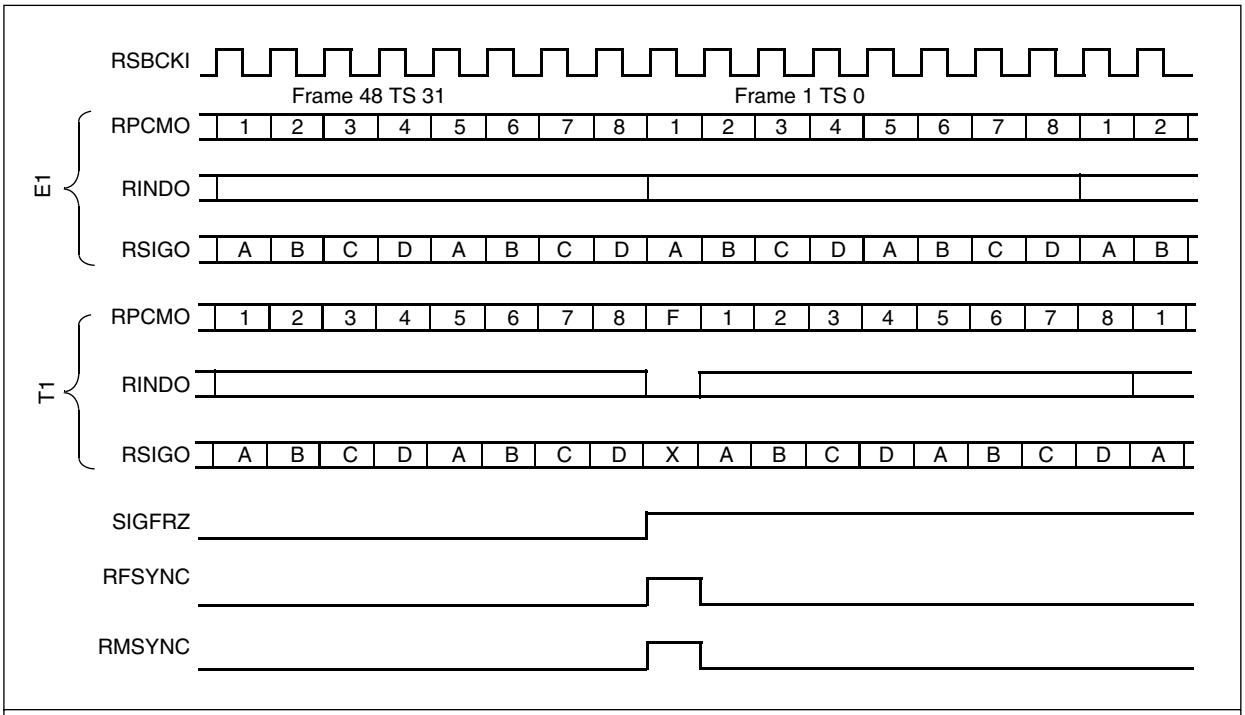
The real-time status of the code word reception can be monitored using the RBOP_ACTIVE bit in the BOP Status register [BOP_STAT; addr 0A3]. Each time a message is put in RBOP register, an interrupt is generated, and the RBOP bit is set in the Data Link 2 Interrupt Status register [ISR1; addr 00A].

2.5 Receive System Bus

The Receive System Bus (RSB) provides a high-speed, serial interface between the RCVR and the system bus. The system bus is compatible with the Mitel ST-Bus, the Siemens PEB Bus, and the AT&T CHI Bus, and directly connects to other Mindspeed serial TDM bus devices with no need for any external circuitry.

The RSB has the following seven pins: Receive System Bus Clock (RSBCKI), Receive PCM Data (RPCMO), Receive Signaling Data (RSIGO), Receive Frame Sync (RFSYNC), Receive Multiframe Sync (RMSYNC), Receive Time Slot Indicator (RINDO), and Signaling Freeze (SIGFRZ). Figure 2-15 illustrates the relationship between these signals. (Pin definitions are provided in Table 1-1.) RSB data outputs can be configured to output on the rising or falling edge of RSBCKI. See the Receive System Bus Configuration register [RSB_CR; addr 0D1].

Figure 2-15. RSB Waveforms



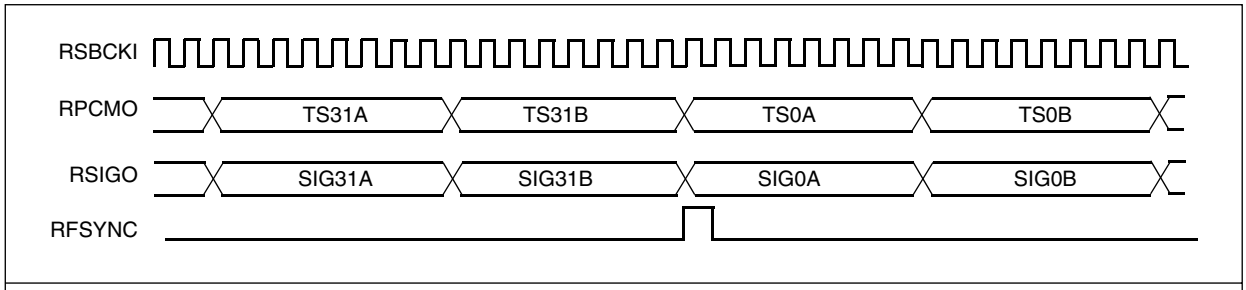
NOTE(S):
The Receive Multiframe Sync (RMSYNC) occurs every 6 ms for 48 T1 or 48 E1 frames.

100051_019

The RSB supports five system bus rates (MHz): 1.536, 1.544, 2.048, 4.096, and 8.192. The T1 rate without a framing bit is 1.536 MHz, consisting of 24 time slots. The T1 rate with a framing bit 1.544 MHz. The E1 rate is 2.048 MHz, consisting of 32 time slots. Twice the E1 rate is 4.096 MHz, consisting of 64 time slots. Four times the E1 rate is 8.192 MHz, consisting of 128 time slots. The 4.096 and 8.192 MHz bus modes contain multiple bus members (A, B, C, D) which allow multiple T1/E1 signals to share the same system bus.

This is done by interleaving the time slots to a maximum of four Bt8370s without external circuitry (see Figures 2-16 and 2-17). The system bus rate is independent of the line rate and must be selected using the System Bus Interface Configuration register [SBI_CR; addr 0D0].

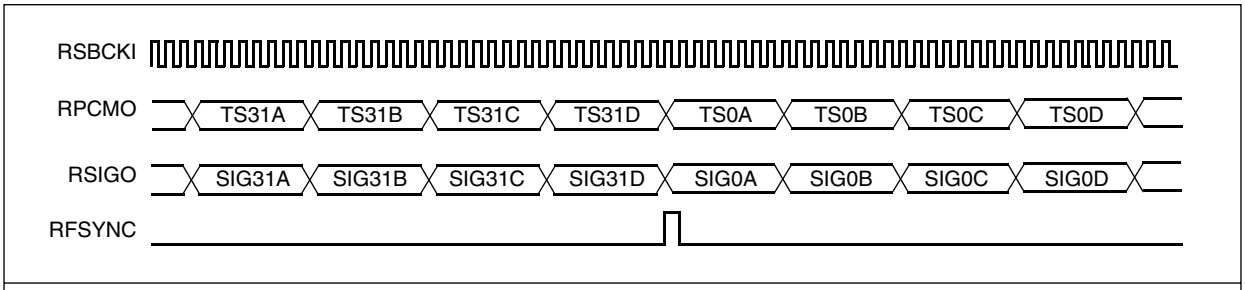
Figure 2-16. RSB 4.096 MHz Bus Mode Time Slot Interleaving



NOTE(S):
A and B time slot data comes from different Bt8370s. Output data on rising edge clock, RCPM_NEG = 0 [addr oD1]. Output sync on rising edge clock, RSYNJ_NEG = 0 [addr 0D1]. RSBCKI operates at 1 times the data rate. RSB.OFFSET = 0.

100051_020

Figure 2-17. RSB 8.192 MHz Bus Mode Time Slot Interleaving



NOTE(S):
A ,B ,C, and D slot data comes from different Bt8370s. Output data on rising edge clock, RCPM_NEG = 0 [addr oD1]. Output sync on rising edge clock, RSYNJ_NEG = 0 [addr 0D1]. RSBCKI operates at 1 times the data rate. RSB.OFFSET = 0.

100051_021

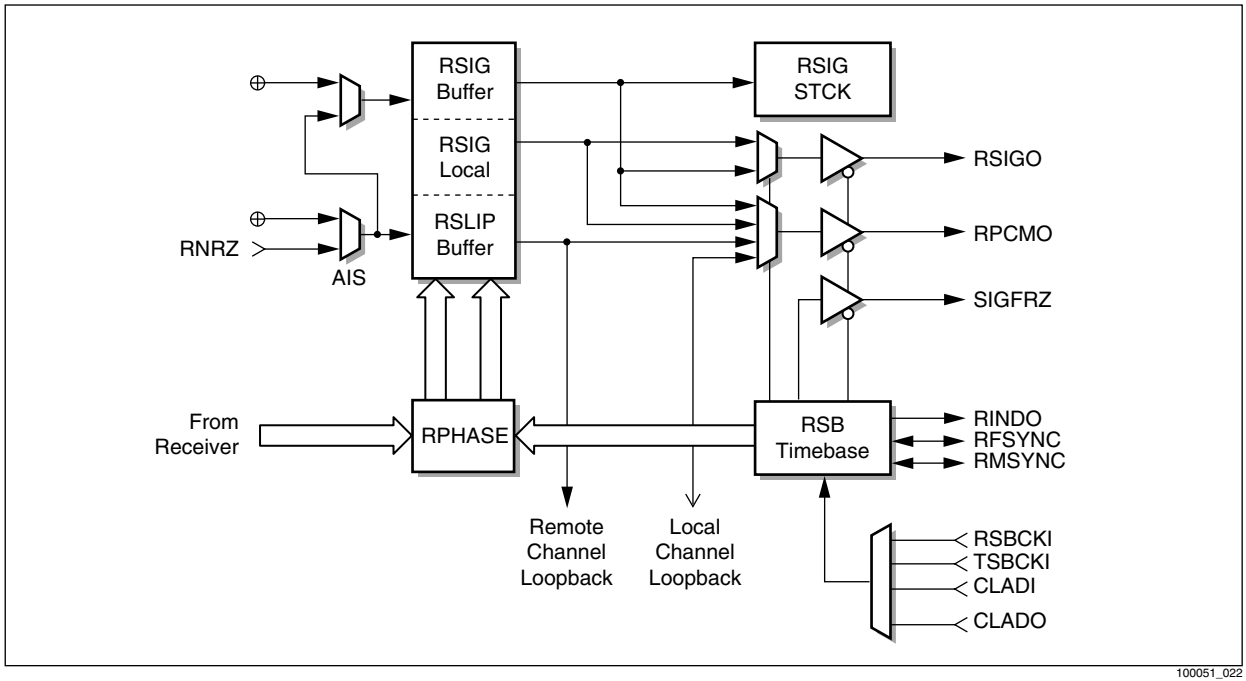
The RSB maps line rate time slots to system bus time slots. The 24- (DS1) or 32- (CEPT) line rate time slots can be mapped to 24, 32, 64, or 128 system bus time slots as listed in Table 2-5. The system bus rate must be greater than or equal to the line rate, except for 1.536 MHz bus mode.

Table 2-5. RSB Interface Time Slot Mapping

Line Rate (MHz)	Source Channels	System Bus Rate (MHz)	Destination Time Slots
1.544	24	1.536	24
	24	1.544	24
	24	2.048	32
	24	4.096	64
	24	8.192	128
2.048	32	2.048	32
	32	4.096	64
	32	8.192	128

The RSB, illustrated in Figure 2-18, consists of a timebase, slip buffer, signaling buffer, and signaling stack.

Figure 2-18. RSB Diagram



2.5.1 Timebase

The RSB timebase synchronizes RFSYNC, RMSYNC, and RINDO with the Receive System Bus Clock (RSBCKI). The RSBCKI can be slaved to four clock sources: Receive System Bus Clock Input (RSBCKI), Transmit System Bus Clock Input (TSBCKI), Clock Rate Adapter Input (CLADI), or Clock Rate Adapter Output (CLADO). The RSB clock selection is made through the Clock Input Mux register [CMUX; addr 01A]. The system bus clock can also be configured to run at twice the data rate by setting the X2CLK bit in the System Bus Interface Configuration register [SBI_CR; addr 0D0].

RFSYNC and RMSYNC can be individually configured as inputs or outputs [PIO; addr 018]. RFSYNC and RMSYNC must be configured as inputs when the RSB timebase is slaved to the system bus [SBI_OE; addr 0D0]. RFSYNC and RMSYNC must be configured as outputs when the RSB timebase is master of the system bus. RFSYNC and RMSYNC can also be configured as rising or falling edge outputs [RSB_CR; addr 0D1]. In addition to having RFSYNC and RMSYNC active on the frame boundary, a programmable offset is available to select the time slot and bit offset in the frame. See the Receive System Bus Sync Time Slot Offset [RSYNC_TS; addr 0D3] and the Receive System Bus Sync Bit Offset [RSYNC_BIT; addr 0D2] registers.

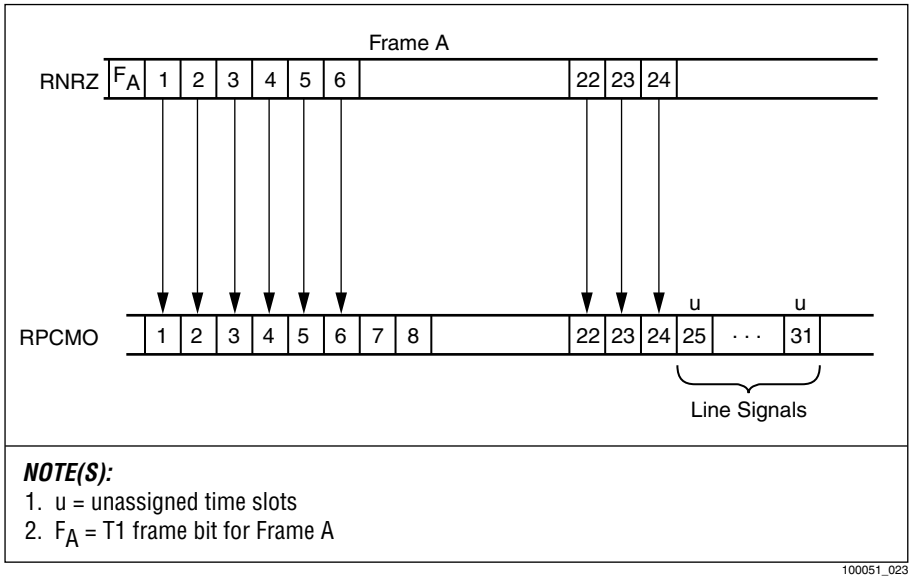
2.5.2 Slip Buffer

The 64-byte Receive PCM Slip Buffer [RSLIP; addr 1C0 to 1FF] resynchronizes the Receiver Clock (RXCLK) and data (RNRZ) to the Receive System Bus Clock (RSBCK) and data (RPCMO). RSLIP acts like an elastic store by clocking RNRZ data in with RXCLK and clocking PCM data out on RPCMO with RSBCK.

If the system bus rate is greater than the line rate (i.e., T1 line rate and E1 system bus rate), there is a mismatched number of time slots. The mapping of line rate time slots to system bus time slots is done by time slot assignments with the ASSIGN bit in the System Bus Per-Channel Control register [SBC0 to SBC31; addr 0E0 to 0FF]. ASSIGN selects which system bus time slots are used to transport line rate time slots. Time slot mapping is done by mapping the first line rate time slot to the first assigned system bus time slot. For example, T1 to E1 mapping is assigned as illustrated in Figure 2-19.

NOTE: All line rate time slots must be assigned to a system bus time slot.

Figure 2-19. T1 Line to E1 System Bus Time Slot Mapping



NOTE(S):
1. u = unassigned time slots
2. F_A = T1 frame bit for Frame A

100051_023

RSLIP has four modes of operation: Two-Frame Normal, 64-bit Elastic, Two-Frame Short, and Bypass. RSLIP mode is set in the Receive System Bus Configuration register [RSB_CR; addr 0D1]. RSLIP is organized as a 2-frame buffer. This allows MPU access to frame data, regardless of the RSLIP mode selected. Each byte offset into the frame buffer is a different time slot: offset 0 in RSLIP is always time slot 0 (TS0), offset 1 is always TS1, etc. The slip buffer has processor read/write access.

In Two-Frame Normal mode, the slip buffer total depth is two 193-bit frames (T1) or two 256-bit frames (E1). Data is written to the slip buffer using RXCLK and read from the slip buffer using RSBCK. If a slight rate difference between the clocks occurs, the slip buffer changes from its initial condition—approximately half full—by either adding or removing frames. If RXCLK writes to the slip buffer faster than RSBCK reads the data, the buffer fills up. When the slip buffer in Normal mode is full, an entire frame of data is deleted. Conversely, if RSBCK reads the slip buffer faster than RXCLK writes the data, the buffer becomes empty. When the slip buffer in Normal mode is empty, an entire frame of data is duplicated. When an entire frame is deleted or duplicated it is known as a Frame Slip (FSLIP), which is always one full frame of data. The FSLIP status is reported in the Slip Buffer Status register [SSTAT; addr 0D9]. In T1 mode, the F bit is treated as part of the frame and can slip accordingly.

In 64-bit Elastic mode, the slip buffer total depth is 64 bits, and the initial throughput delay is 32 bits, half of the total depth. Similar to Normal mode, Elastic mode allows the system bus to operate at any of the programmable rates, independent of the line rate. The advantage of this mode over Normal mode is that throughput delay is reduced from 1 frame to an average of 32 bits, and the output multiframe always retains its alignment with respect to the output data. The disadvantage of this mode is handling the full and empty buffer conditions. In Elastic mode, an empty or full buffer condition causes an Uncontrolled Slip (USLIP). Unlike an FSLIP, a USLIP is of unknown size within the range of 1 to 256 bits of data. The USLIP status is reported in SSTAT.

The Two-Frame Short mode combines the depth of the Normal mode with the throughput delay of the Elastic mode. The Two-Frame Short mode begins in the Elastic mode with a 32-bit initial throughput delay, and switches to Normal mode when the buffer becomes empty or full; thereafter, the Two-Frame Short and Normal mode perform identically. If the slip buffer is full (two frames) in the Two-Frame Short mode, an FSLIP is reported, after which the slip buffer and Two-Frame mode perform identically.

In Bypass mode, data is immediately clocked through RSLIP from the RCVR to RSB, and RCKO internally replaces the system bus clock.

2.5.3 Signaling Buffer

The 32-byte Receive Signaling Buffer [RSIG; addr 1A0 to 1BF] stores a single multiframe of signaling data. Each byte offset into RSIG contains signaling data for a different time slot: offset 0 stores TS0 signaling data, offset 1 stores TS1 signaling data, etc. The signaling data is stored in the least significant 4 bits of RSIG. The output signaling data is stored in the most significant 4 bits of RSIG. Similar to RSLIP, RSIG buffer has read/write processor access to read or overwrite signaling information. RMSYNC extracts robbed-bit signaling from RSIG onto RPCMO; RFSYNC extracts ABCD signaling from RSIG onto RSIGO.

The RSIG buffer has the following configurable features:

- transparent, robbed-bit signaling
- signaling freeze
- debounce signaling
- Unicode detection

Each feature is available in the Receive Signaling Configuration register [RSIG; addr 0D7]. See the registers section for more details.

2.5.4 Signaling Stack

The Receive Signaling Stack (RSTACK) allows the processor to quickly extract signaling changes without polling every channel. RSTACK is activated on a per-channel basis by setting the Received Signaling Stack (SIG_STK) control bit in the Receive Per-Channel Control register [RPC0 to RPC31; addr 180 to 19F]. The signaling stack stores the channel and the A, B, C, and D signaling bits that changed in the last multiframe. The stack has the capacity to store signaling changes for all 24 (T1) or 30 (E1) PCM channels.

At the end of any multiframe where 1 or more ABCD signaling values have changed, an interrupt occurs with RSIG set in the Timer Interrupt Status register [ISR3; addr 008]. The processor then reads the Receive Signaling Stack [STACK; addr 0DA] twice to retrieve the channel number (WORD = 0) and the new ABCD value (WORD = 1), and continues to read from STACK until the MORE bit in STACK is cleared, indicating the RSIG stack is empty.

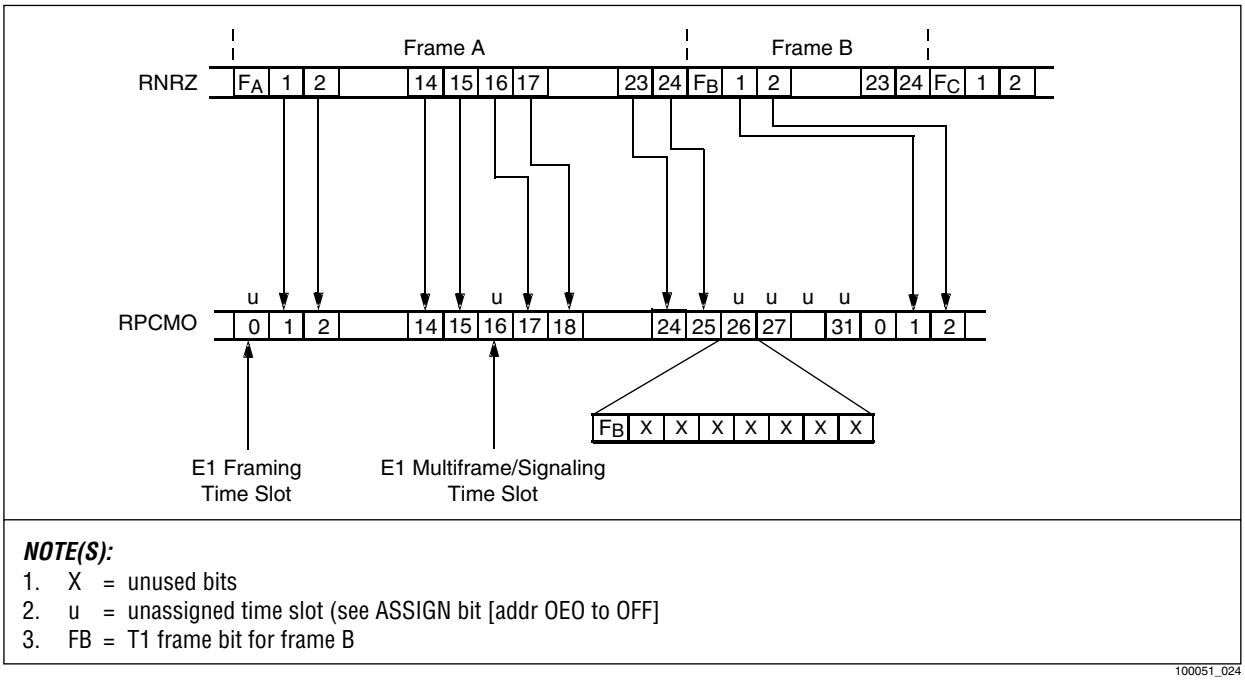
Optionally, the processor can select RSIG interrupt (SET_RSIG; addr 0D7) to occur at each multiframe boundary in T1 modes, regardless of signaling change. This mode provides an interrupt aligned to the multiframe to read the RSIG buffer rather than RSTACK.

2.5.5 Embedded Framing

Embedded Framing mode bit (EMBED; addr 0D0) instructs the RSB to embed framing bits on RPCMO while in T1 mode.

The G.802 Embedded mode supports *ITU-T Recommendation G.802*, which describes how 24 T1 time slots and 1 framing bit (193 bits) are mapped to 32 E1 time slots (256 bits). This is done by leaving TS0 and TS16 unassigned, by storing the 24 T1 time slots in TS1 to TS15 and TS17 to TS25, and by storing the frame bit in bit 1 of TS26 (see Figure 2-20). TS26 through TS31 are also unassigned.

Figure 2-20. G.802 Embedded Framing



NOTE(S):

1. X = unused bits
2. u = unassigned time slot (see ASSIGN bit [addr OEO to OFF]
3. FB = T1 frame bit for frame B

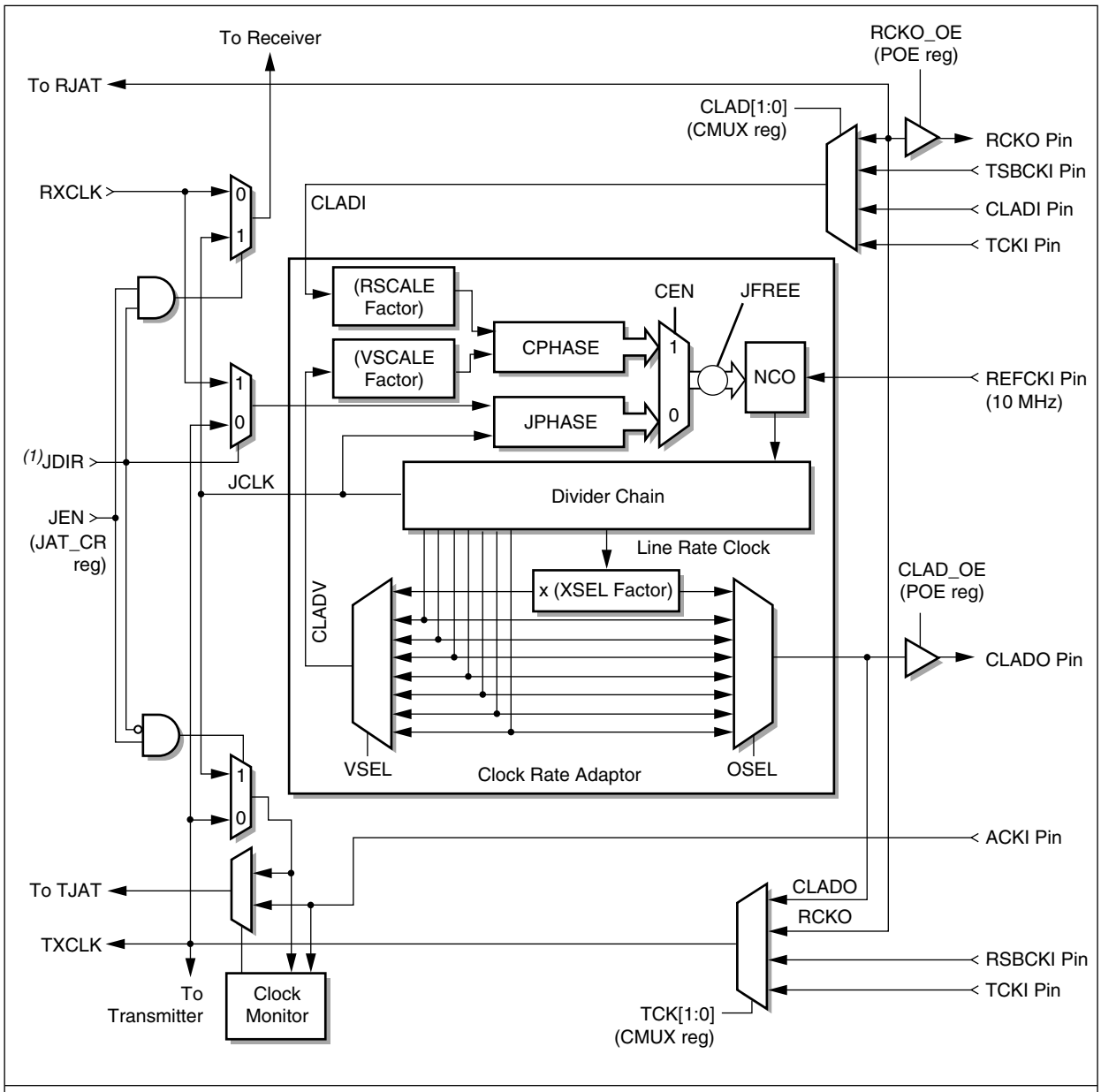
100051_024

2.6 Clock Rate Adapter

The full function Clock Rate Adapter is included in all Bt8370 and Bt8375 devices. In the Bt8376, the CLADO output is not implemented.

The Clock Rate Adapter (CLAD) illustrated in Figures 2-21 and 2-22 uses an input clock reference at a particular frequency (range 8–16,384 kHz) to synthesize an output clock (CLADO and JCLK) at a different frequency (range 1024–16,384 kHz). The CLAD also controls the read or write pointers of the elastic store by synthesizing a Jitter-attenuated Line rate Clock (JCLK); thus, it is an integral part of the Jitter Attenuator (JAT). The CLAD input clock jitter tolerance and jitter transfer functions are illustrated in Figures 2-9 and 2-10. These diagrams are illustrated for various programmed loop filter gain values (LFGAIN; addr 090).

Figure 2-21. Clock Rate Adapter/Jitter Attenuator Block Diagram (Bt8370 and Bt8375 Devices)

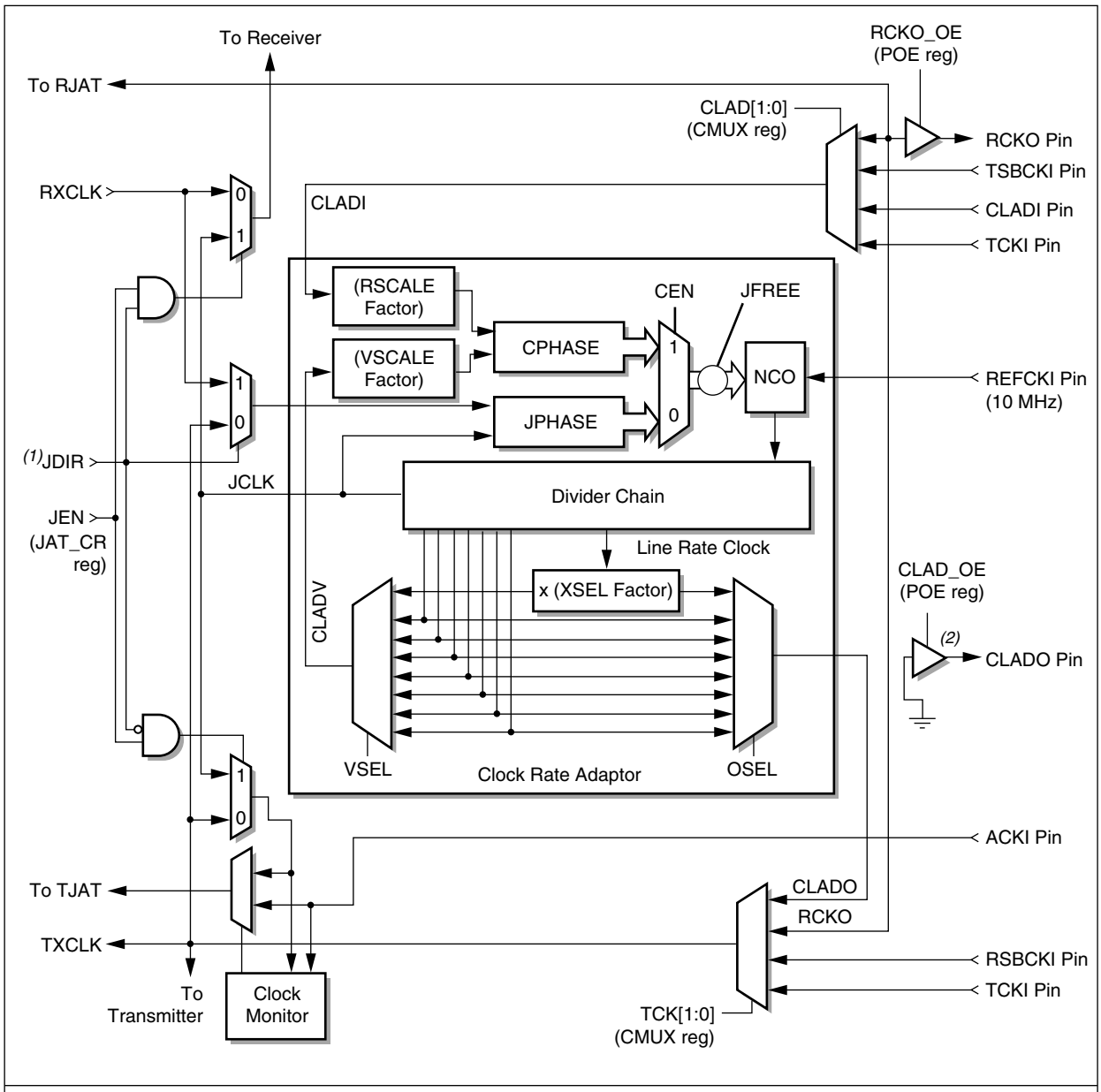


FOOTNOTE(S):

(1) JDIR controlled in JAT_CR [addr 002].

100051_025

Figure 2-22. Clock Rate Adapter/Jitter Attenuator Block Diagram (Bt8376 Device Only)



FOOTNOTE(S):

(1) JDIR controlled in JAT_CR [addr 002].

(2) CLADO signal is grounded in the Bt28376 and a logical 0 is driven out on CLADO pin if enabled.

100051_026

JCLK and CLADO are locked to the selected timing reference. The reference frequency can operate at T1 or E1 line rates, or at any rate supported by the clock rate adapter. See RSCALE[2:0] [addr 092] to select timing reference frequency. See Table 2-6 for the JCLK/CLADO timing reference.

Table 2-6. JCLK/CLADO Timing Reference

CEN	JEN	JFREE	JDIR	CLADO/JCLK Reference
0	0	1	X	REFCKI—Free running 10 MHz clock
0	1	1	0	REFCKI—Free running 10 MHz clock with transmit JAT
0	1	1	1	REFCKI—Free running 10 MHz clock with receive JAT
0	1	0	0	TXCLK—TCKI or ACKI per [AISCLK; addr 068]
0	1	0	1	RXCLK—RPLL or RCKI per [RDIGI; addr 020]
1	0	0	X	CLADI—System clock bypass JAT elastic store
1	1	0	0	CLADI—System clock with transmit JAT
1	1	0	1	CLADI—System clock with receive JAT

GENERAL NOTE:
1. JCLK always operates at T1 or E1 line rate selected by [T1/E1N; addr 001]

CLAD output jitter meets jitter generation requirements of AT&T TR62411, as listed in Table 2-7.

Table 2-7. Jitter Generation Requirements

Filter Applied	Maximum Output Jitter	Measured
None (Broadband)	0.05 UI peak-peak	.015 UI
10 Hz to 40 kHz	0.025 UI peak-peak	.015 UI
8 kHz to 40 kHz	0.025UI peak-peak	.015 UI
10 Hz to 8 kHz	0.02UI peak-peak	.015 UI

CLAD modes are selected using the Clock Rate Adapter Configuration register [CLAD_CR; addr 090], the Clock Rate Adapter Frequency Select [CSEL; addr 091], and the Clock Rate Adapter Phase Detector Scale Factor [CPHASE; addr 092].

If the CLAD Phase Detector (CPHASE) is disabled [CEN; addr 090], the CLAD input timing reference is determined by the JEN and JFREE bits (addr 002).

If the CLAD Phase Detector is enabled [CEN; addr 090], the CLAD input timing reference is selected using CLADI[1:0] in the Clock Input Mux register [CMUX; addr 01A]. The input timing reference can consist of the Clock Rate Adapter Input Pin (CLADI); the Receive Clock Output (RCKO, prior to the output buffer); the Transmit Clock Input Pin (TCKI); or the Transmit System Bus Clock Input Pin (TSBCKI). See Figures 2-21 and 2-22 for more details.

Tables 2-8 and 2-9 list examples of program values for selecting various CLADO and CLADI frequencies. Typically, only one selection is needed for a given system configuration. The processor reconfigures the timing reference [CEN; addr 090] as needed to respond to system conditions where the primary reference is unavailable.

2.6.1 Configuring the CLAD Registers

Step 1 Choose a CLADO output frequency. Table 2-8 lists all possible CLADO output clock frequencies. For system bus applications, valid CLADO frequencies are 1544 kHz, 1536 kHz, 2048 kHz, 4096 kHz, and 8192 kHz.

Step 2 Configure OSEL and XSEL from Table 2-8. OSEL and XSEL together select the CLADO output frequency. In some cases, there are two options for generating the desired output signal. Selecting an option with both T1/E1 and XSEL settings equal to don't-care (X in the table) allows greater flexibility in subsequent options below, and also results in a fixed CLADO frequency when switching framer operation between T1 and E1 modes.

Table 2-8. CLADO Frequencies Selection

CLADO (kHz)	T1/$\overline{E1}$	OSEL	XSEL
1024	X	0	X
2048	X	1	X
	0	7	0
4096	X	2	X
	0	7	1
8192	X	3	X
	0	7	2
2560	X	4	X
1536	X	6	X
1544	1	7	0
	X	5	X
3088	1	7	1
6176	1	7	2
12352	1	7	3
16384	0	7	3
	X	8	X
GENERAL NOTE: X = Don't care			

Step 3 If CLADI is the timing reference source (CEN = 1), select the desired CLAD timing reference frequency from Table 2-9. If CEN = 0, the CLAD reference is RXCLK (line rate), TXCLK (line rate), or free run (REFCKI) and Table 2-9 is not applicable.

Step 4 Configure RSCALE, VSCALE, VSEL, and XSEL from Table 2-9 which contains configuration examples. Again, in some cases, two or more configurations are possible for each frequency option. Many other RSCALE and VSCALE values are also applicable. RSCALE is a programmable frequency divider which scales the CLADI clock frequency before it is applied to the CLAD phase detector, CPHASE. Similarly, VSCALE scales the CLAD internal feedback clock, CLADV. These two clocks must have the same frequency at the phase detector's input for the CLAD loop to properly lock. The rule is

(CLADI Reference freq) ÷ (RSCALE factor) = (CLADV freq) ÷ (VSCALE factor).

Table 2-9. Common CLADI Reference Frequencies and CLAD Configuration Examples (1 of 2)

CLADI Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	T1/$\overline{E1}$	VSEL	XSEL
8	0	8	7	1024	X	0	X
16	0	16	6	1024	X	0	X
32	0	32	5	1024	X	0	X
64	0	64	4	1024	X	0	X
128	0	128	3	1024	X	0	X
256	0	256	2	1024	X	0	X
512	0	512	1	1024	X	0	X
1024	0	1024	0	1024	X	0	X
2048	0	2048	0	2048	X	1	X
	7	16	7	2048	X	1	X
	0	2048	0	2048	0	7	0
4096	0	4096	0	4096	X	2	X
	7	32	7	4096	X	2	X
	1	2048	1	4096	0	7	1
8192	0	8192	0	8192	X	3	X
	7	64	7	8192	X	3	X
	2	2048	2	8192	0	7	2
16384	0	16384	0	16384	X	8	X
	7	128	8	1024	X	0	X
	0	16384	0	16384	0	7	3
1536	2	384	2	1536	X	6	X
1544	2	386	2	1544	X	5	X
	2	386	2	1544	1	7	0
3088	2	772	1	1544	X	5	X
	2	772	1	1544	1	7	0

Table 2-9. Common CLADI Reference Frequencies and CLAD Configuration Examples (2 of 2)

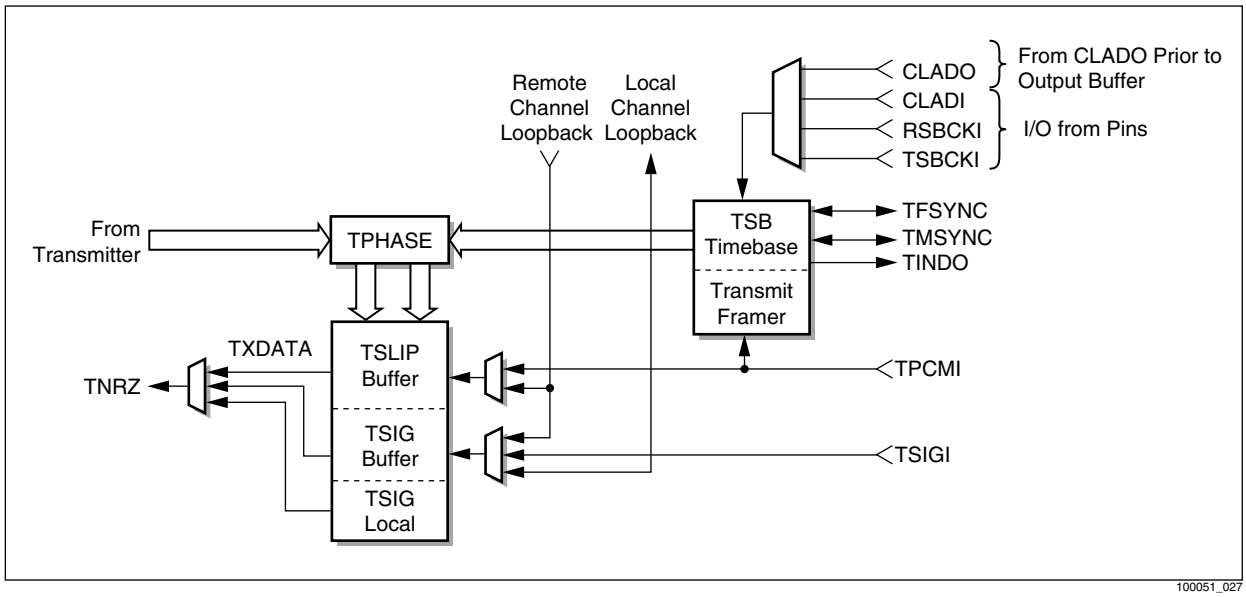
CLADI Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	T1/$\overline{E1}$	VSEL	XSEL
6176	2	1544	0	1544	X	5	X
	2	1544	0	1544	1	7	0
12352	3	1544	0	1544	X	5	X
	3	1544	0	1544	1	7	0

GENERAL NOTE: X = Don't care

2.7 Transmit System Bus

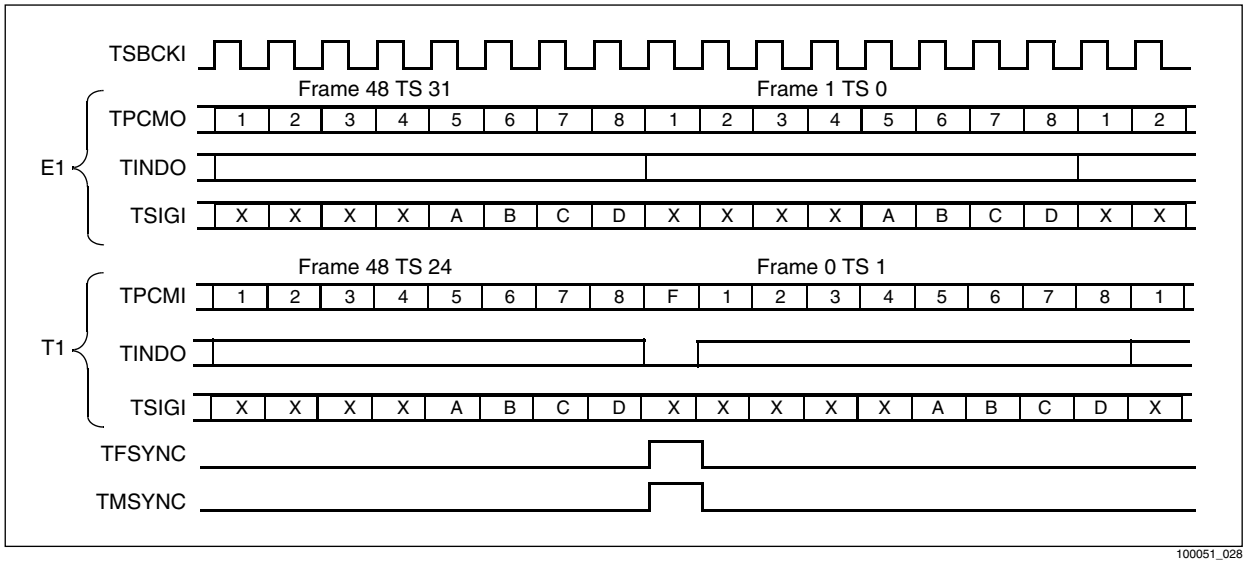
The Transmit System Bus (TSB) consists of a timebase, slip buffer, signaling buffer, and transmit framer (Figure 2-23). It provides a high-speed serial interface between the XMTR and system bus. The system bus is compatible with the Mitel ST-Bus, the PEB Bus, and the AT&T CHI Bus. TSB directly interfaces to other Mindspeed devices with no need for external circuitry.

Figure 2-23. TSB Interface Block Diagram



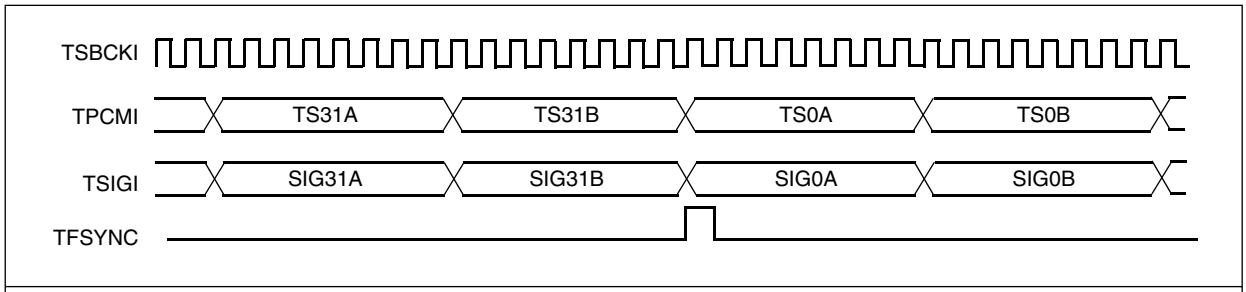
The TSB contains the following six pins: Transmit System Bus Clock (TSBCKI), Transmit PCM Data (TPCMI), Transmit Signaling Data (TSIGI), Transmit Frame Sync (TFSYNC), Transmit Multiframe Sync (TMSYNC), and Transmit Time Slot Indicator (TINDO). See Figure 2-24 for the relationship between these signals. These pins are further defined in Table 1-1.

Figure 2-24. Transmit System Bus Waveforms



The TSB supports five system bus rates (MHz): 1.536, 1.544, 2.048, 4.096, and 8.192. The T1 rate, with 24 time slots and without framing bits, is 1.536 MHz. The T1 rate with framing bits is 1.544 MHz. The E1 rate, with 32 time slots, is 2.048 MHz. The 4.096 MHz rate is twice the E1 rate, with 64 time slots. The 8.192 MHz rate is 4 times the E1 rate, with 128 time slots. The 4.096 and 8.192 MHz bus modes contain multiple bus members (A, B, C, and D), of which 1 bus member is selected by the SBI [3:0] bits in the System Bus Interface Configuration register [SBI_CR; 0D0]. See Figures 2-25 and 2-25. The system bus rate is independent of the line rate and must be selected using the System Bus Interface Configuration register.

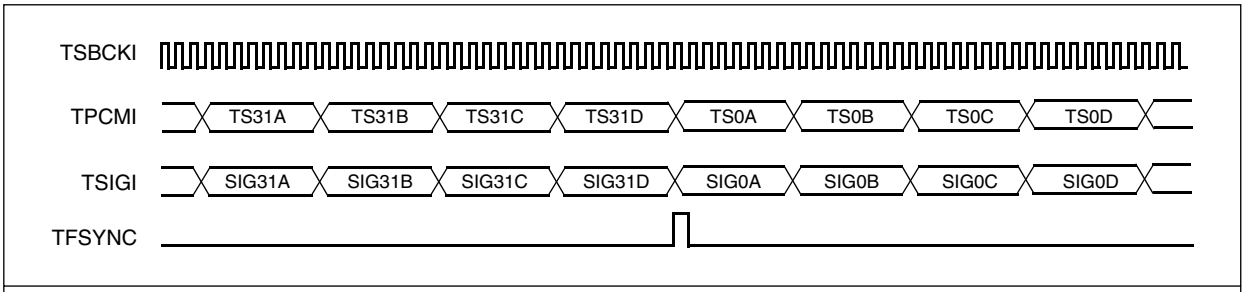
Figure 2-25. TSB 4.096 MHz Bus Mode Time Slot Interleaving



NOTE(S):
A and B time slot data come from different Bt8370s. TSBCKI can be operated at 1 or 2 times the data rate.

100051_029

Figure 2-26. TSB 8.192 MHz Bus Mode Time Slot Interleaving



NOTE(S):
A, B, C, and D time slot data comes from different Bt8370s. TSBCKI can be operated at 1 or 2 times the data rate.

100051_030

2.7.1 Timebase

The TSB timebase synchronizes TPCMI, TFSYNC, TMSYNC, and TINDO with the Transmit System Bus Clock (TSBCK). The TSBCK can be slaved to five different clock sources: Transmit Clock Input (TCKI), Transmit System Bus Clock Input (TSBCKI), Receive System Bus Clock Input (RSBCKI), Clock Rate Adapter Input (CLADI), or Clock Rate Adapter Output (CLADO).

NOTE: The CLADO signal is not available in the Bt8376 device.

The TSB clock selection is made through the Clock Input Mux register [CMUX; addr 01A]. TCKI is automatically selected when the transmit slip buffer is bypassed. The system bus clock can also be configured to run at twice the data rate by setting the X2CLK bit in the System Bus Interface Configuration register [SBI_CR; addr 0D0] when TSLIP is not in Bypass mode.

TFSYNC and TMSYNC can be individually configured as inputs or outputs [PIO; addr 018]. TFSYNC and TMSYNC should be configured as inputs when the TSB timebase is slaved to the system bus, when the transmit framer is disabled [TABORT; addr 071], or when TSB carries embedded T1 framing. TFSYNC and TMSYNC should be configured as outputs when the TSB timebase is master of the system bus, or when the transmit framer is enabled. TFSYNC and TMSYNC can also be configured as rising or falling edge outputs [TSB_CR; addr 0D4]. In addition to having TFSYNC and TMSYNC active on the frame boundary, a programmable offset is available to select the time slot and bit offset in the frame. See the Transmit System Bus Sync time slot Offset [TSYNC_TS; addr 0D6] and Transmit System Bus Sync Bit Offset [TSYNC_BIT; addr 0D5] registers.

2.7.2 Slip Buffer

The 64-byte Transmit PCM Slip Buffer [TSLIP; addr 140 to 17F] resynchronizes the Transmit System Bus Clock (TSBCK) and data (TPCMI) to the Transmit Clock (TXCLK) and data (TNRZ). TSLIP acts like an elastic store by clocking PCM data in on TPCMI with TSBCK, and by clocking TNRZ data out with TXCLK. TPCMI can be configured to sample on the rising or falling edge of TSBCKI. See the Transmit System Bus Configuration register [TSB_CR; addr 0D4].

TSLIP has four modes of operation: Two-Frame Normal, 64-bit Elastic, Two-Frame Short, and Bypass. TSLIP mode is set in the Transmit System Bus Configuration register [TSB_CR; addr 0D4]. It is organized as a two-frame buffer, with high-frame and low-frame buffers. This allows MPU access to frame data, regardless of the TSLIP mode selected. Each byte offset into the frame buffer is a different time slot: offset 0 in TSLIP is always time slot 0 (TS0), offset 1 is always TS1, etc. The slip buffer has processor read/write access.

In Normal mode, the slip buffer total depth is two 193-bit frames (T1), or two 256-bit frames (E1). Data is written to the slip buffer using TSBCK and read from the slip buffer using TXCLK. If there is a slight rate difference between the two clocks, the slip buffer changes from its initial condition—approximately half full—by either adding or removing frames. If TSBCK writes to the slip buffer faster than TCKI reads the data, the buffer becomes full. When the slip buffer in Normal mode is full, an entire frame of data is deleted. Conversely, if TXCLK is reading the slip buffer at a faster rate than TSBCK is writing the data, the buffer eventually empties. When the slip buffer in Normal mode is empty, an entire frame of data is duplicated. When an entire frame is deleted or duplicated, it is known as a Frame Slip (FSLIP). An FSLIP is always one full frame of data. The FSLIP status is reported in the Slip Buffer Status register [SSTAT; addr 0D9].

In 64-bit Elastic mode, the slip buffer total depth is 64 bits, and the initial throughput delay is 32 bits, or half of the total depth. Similar to Normal mode, Elastic mode allows the system bus to operate at any of the programmable bus rates, independent of the line rate. The advantage of this mode over the Two-Frame mode is that throughput delay is reduced from one frame to an average of 32 bits, and the transmit multiframe can retain its alignment with respect to the transmit data. The disadvantage of this mode is handling the full and empty buffer conditions. In 64-bit Elastic mode, an empty or full buffer condition causes an Uncontrolled Slip (USLIP). Unlike an FSLIP, a USLIP is of unknown size, ranging from 1 to 256 bits of data. The USLIP status is reported in SSTAT.

The Two-Frame Short mode combines the depth of the Normal mode with the throughput delay of the Elastic mode. This mode begins in Elastic mode with a 32-bit initial throughput delay, and switches to Normal modes when the buffer is empty or full; thereafter, the Two-Frame Short and Normal modes perform identically. If the slip buffer is full (two frames) in the Two-Frame Short and Normal modes, an FSLIP is reported; thereafter, the slip buffer performs exactly like Normal mode.

In Bypass mode, data is clocked through TSLIP from the TSB to the XMTR using TXCLK as selected by the TCKI input clock mux.

2.7.3 Signaling Buffer

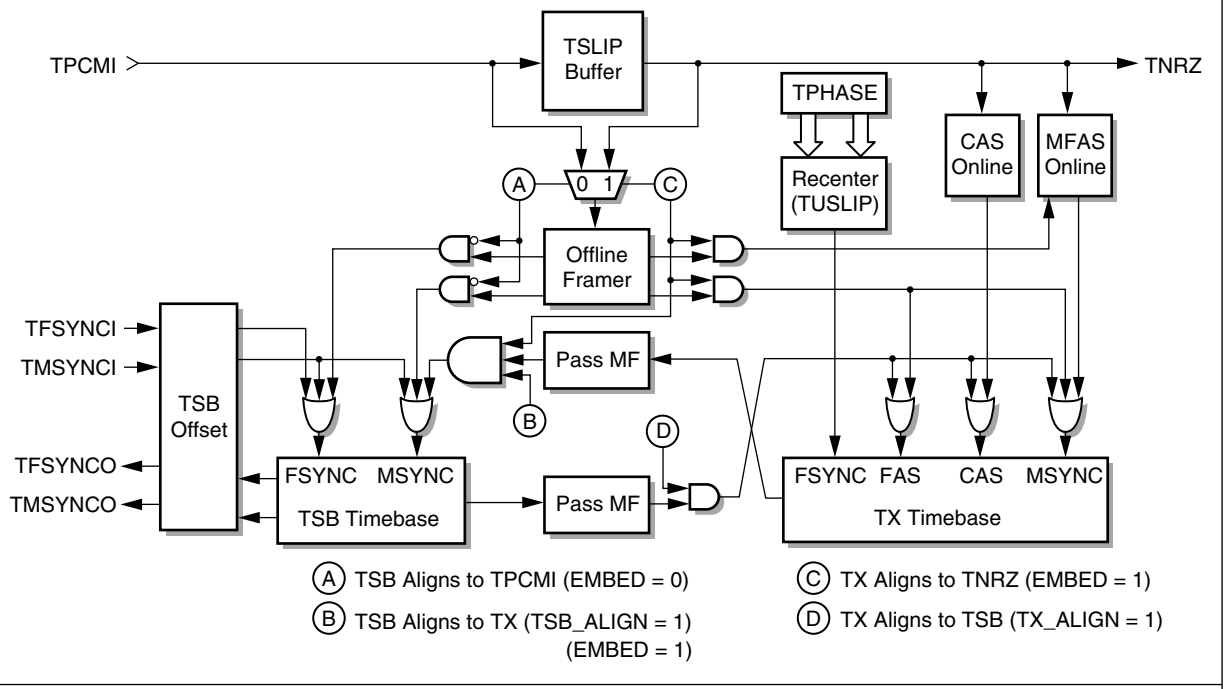
The 32-byte Transmit Signaling Buffer [TSIG; addr 120–13F] stores a single multiframe of signaling data input from the TSIGI pin and is updated as each time slot is received in every TSB frame. Each byte offset into TSIG represents a different time slot for signaling data: offset 0 stores TS0 signaling data, offset 1 stores TS1 signaling data, etc. The signaling data is stored in the least significant 4 bits of the signaling buffer. Similar to TSLIP, TSIG has read/write processor access for accessing or overwriting signaling information. The signaling buffer uses TFSYNC to identify the frame boundaries in the TSIGI data stream.

2.7.4 Transmit Framing

The transmit data stream has two framing functions: an offline framer and an online framer. Figure 2-27 illustrates these functions. The offline framer recovers the transmit frame alignment (TFSYNC). The online framer monitors the frame alignment found by the offline framer and recovers multiframe alignment (TMSYNC).

Transmit frame resynchronization is initiated by activating the Transmit Loss of Frame (TLOF) status bit in Alarm 2 status [ALM2; addr 048] register by the online framer. The TLOF criteria is set in the TLOFA, TLOFB, and TLOFC bits of the Transmitter Configuration register [TCR1; addr 071]. The online framer supports the following LOF criteria for T1: 2 frame bit errors out of 4; 2 out of 5; or 2 out of 6. For E1, it supports 3 out of 3.

Figure 2-27. Transmit Framing and Timebase Alignment Options



NOTE(S):

1. EMBED located in SBI_CR (addr 0D0).
2. TSB_ALIGN and TX_ALIGN located in TSB_DR (addr 0D4).
3. EMBED = 0 is only applicable if TPCMI is operating at the line rate.

100051_031

When TLOF is asserted, the offline framer searches the transmit data stream for a new frame alignment, provided transmit framing is enabled [TABORT; addr 071]. If embedded framing is enabled [EMBED; addr 0D0], the offline framer examines the TSLIP buffer output, TNRZ, for transmit frame alignment. If embedded framing is disabled, the offline framer examines the slip buffer input (TPCMI) for transmit frame alignment. This case (EMBED = 0) is only applicable if TPCMI is configured to operate at the line rate: 2,048 Kbps E1, or 1,544 Kbps T1. If transmit framing is disabled, the offline framer waits for a reframe command [TFORCE; addr 071] before beginning frame alignment search.

After the offline framer recovers frame alignment, the online framer monitors TLOF and searches for multiframe alignment; the search uses the criteria defined by the Transmit Frame mode [TFRAME; addr 070]. The online framer conducts a multiframe alignment search each time the offline framer recovers transmit frame alignment, as reported by high-to-low transition of transmit loss of frame status [TLOF; addr 048]. After TLOF recovery, the online framer searches continuously for multiframe alignment until the correct pattern sequence is located, or until basic frame alignment is lost (TLOF goes active-high). After multiframe alignment recovery, the online framer checks subsequent multiframes for errored alignment patterns, but does not use those errors as part of the criteria for loss of basic frame alignment.

NOTE: The online framer's multiframe search status is not directly reported to the processor, but instead is monitored by examination of transmit error status: TMERR, TSERR, and TCERR [addr 00B]. If the system incorporates a certain number of multiframe pattern errors (or a certain error ratio) into the loss of transmit frame alignment criteria, the processor must count multiframe pattern errors to determine when to force a transmit reframe [TFORCE; addr 071].

The frame synchronization criteria used by the offline framer is set in the TFRAME[3:0] of the Transmit Framer Configuration register [TCR0; addr 070]. (Tables 3-15 and 3-16 illustrate supported transmit framing formats. Also, see Tables 3-17 and 3-18, Criteria for Loss/Recovery of Transmit Frame Alignment.)

The offline framer is shared between the RCVR and XMTR and can only search in one direction at a time. Consequently, the host processor can manually arbitrate between RCVR and XMTR reframe requests by manipulating the ABORT and FORCE controls, or by allowing the framer to automatically arbitrate LOF requests.

The offline framer waits until the current search is complete [FSTAT; addr 017] before checking for pending LOF reframe requests. If both online framers have pending reframe requests, the offline framer aligns to the opposite direction of that most recently searched. For example, if TLOF is pending at the conclusion of a receive search that timed out without finding alignment, the offline framer switches to search in the transmit direction. The TLOF switchover is prevented in the preceding example if the processor asserts TABORT to mask the transmit reframe request. TABORT does not affect TLOF status reporting. For applications that frame in only one direction, framing in the opposite direction must be masked. If, at the conclusion of a receive search time-out, TLOF status is asserted but masked by TABORT, the offline framer continues to search in the receive direction.

For applications that frame in both directions, the processor can manually arbitrate among pending reframe requests by controlling the reframe precedence. An example of manual control follows:

```
1 Initialize RABORT = 1 and TABORT = 1.

2 Enable RLOF and TLOF interrupts.

3 Read clear pending ISR interrupts.

4 Release RABORT = 0.

5 Call LOF Service Routine if either RLOF or TLOF
        interrupt;

{

(check current LOF status (ALMI, 2; addr 047, 048)

If RLOF recovered and TLOF lost

—Assert RABORT = 1

—Release TABORT = 0

If RLOF lost or TLOF recovered

—Assert TABORT = 1

—Release RABORT = 0

}
```

The status of the offline framer can be monitored using the Offline Framer Status register [FSTAT; addr 017]. The register reports if the offline framer:

- is looking at the receive or transmit data streams (RX/TXN)
- is actively searching for frame alignment (ACTIVE)
- found multiple framing candidates (TIMEOUT)
- found frame sync (FOUND)
- found no frame alignment candidates (INVALID)

2.7.5 Embedded Framing

Embedded framing mode [EMBED; addr 0D0] instructs the transmit framer to search TSLIP buffer output (TNRZ) for framing bits while in T1 mode, or for MFAS and CAS in E1 mode. Embedded framing allows the transmit timebase to align with the transmit framer multiframe alignment of the PCM signal transported across the system bus.

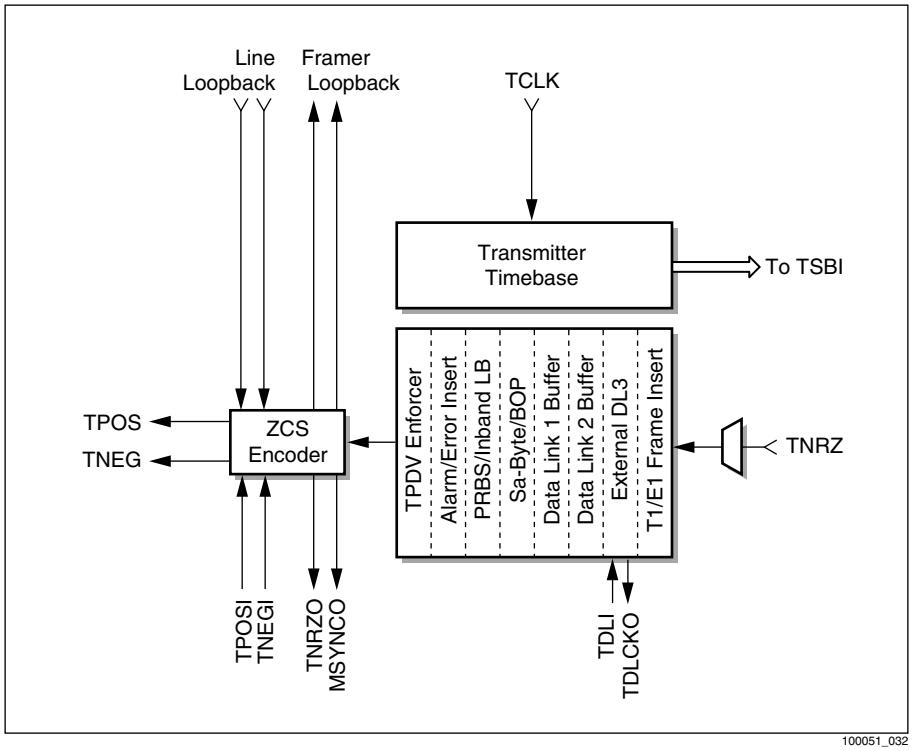
The G.802 Embedded mode supports ITU-T *Recommendation G.802*, which describes how 24 T1 time slots and framing bit (193 bits) are mapped to the 32 E1 time slots (256 bits): by leaving TS0 and TS16 unassigned, by storing the 24 T1 time slots in TS1 to TS15, and in TS17 to TS25, and by storing the frame bit in bit 1 of TS26 (see Figure 2-20).

2.8 Transmitter

The Digital Transmitter (XMTR) inserts T1/E1 overhead data and encodes single rail NRZ data from the TSB into P and N rail NRZ data, suitable for transmission by the TLIU.

The XMTR, illustrated in Figure 2-28, consists of the following elements: two Transmit Data Links, Test Pattern Generator, In-Band Loopback Code Generator, Overhead Pattern Generator, Alarm Generator, Zero Code Suppression (ZCS) Encoder, External Transmit Data Link, CRC Generation, Framing Pattern Insertion, and Far End Block Error Generator.

Figure 2-28. XMTR Diagram

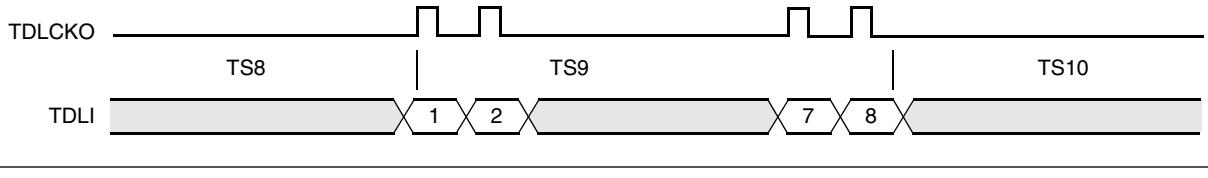


2.8.1 External Transmit Data Link

The External Data Link (DL3) allows the system to supply externally any bits in any time slot of all frames, odd frames, or even frames, including T1 framing bits. Pin access to the DL3 transmitter is provided through TDLCKO and TDLI, which serve as the TDL3 clock output (TDLCKO) and data input (TDLI). The mode of the pins is selected using TDL_IO bit in the Programmable Input/Output register [PIO; addr 018].

Control of DL3 format is provided in two registers: External Data Link Time Slot [DL3_TS; addr 015] and External Data Link Bit [DL3_BIT; addr 016]. Transmit DL3 is set up by selecting the bit(s) [DL3_BIT], and time slot [TS[4:0]; addr 015] to be overwritten, and then enabling the data link [DL3EN; addr 015]. Enabling the data link starts TDLCKO for gating the NRZ data provided on TDLI. Figure 2-29 illustrates the external transmit data link waveforms.

Figure 2-29. External Transmit Data Link Waveforms



NOTE(S):
This example shows bits 1, 2, 7, and 8 of TS9 selected. Any combination of time slot bits can be selected.

100051_033

2.8.2 Transmit Data Links

The XMTR contains two independent data link controllers (DL1, DL2): a Performance Report Message (PRM) generator and a Bit-Oriented Protocol (BOP) transceiver. DL1 and DL2 can be programmed to send and receive HDLC-formatted messages in the Message Oriented Protocol (MOP) mode, or unformatted serial data can be sent and received in any combination of bits within a selected time slot or F bit channel. The PRM message generator can automatically send 1-second performance reports. The BOP transceiver can preemptively transmit BOP messages, such as ESF Yellow Alarm.

2.8.2.1 Data Link Controllers

The Bt8370 and Bt8375 provide two internal data link controllers, and the Bt8376 provides a single controller. DL1 and DL2 control the serial data channels, which operate in multiples of 4 Kbps to the maximum 64 Kbps time slot rate. This is done by selecting a combination of bits from either odd, even, or all frames. Both data link controllers support ESF Facilities Data Link (FDL), SLC-96 data link, Sa data link, Common Channel Signaling (CCS), Signaling System #7 (SS7); ISDN LAPD channels; Digital Multiplexed Interface (DMI) signaling in TS24; and the latest ETSI V.51 and V.52 signaling channels. DL1 and DL2 each contain a 64-byte transmit buffer which functions either as a programmable length circular buffer in transparent (unformatted) mode, or a full-length data FIFO in formatted (HDLC) mode.

DL1 and DL2 are configured identically, except for their offset in the register map. The DL1 address range is 0A4 to 0AE, and the DL2 address range is 0AF to 0B9. From this point on, the DL1 is used to describe the operation of both data link controllers. Transmit Data Link 1 (TDL1) can be viewed as having a higher priority than Transmit Data Link 2 (TDL2) because TDL1 overwrites the primary rate channel after TDL2. Thus, any data that TDL2 writes to the primary rate channel can be overwritten by TDL1, if TDL1 is configured to transmit in the same time slot as TDL2.

The TDL1 is enabled using the DL1 Control register [DL1_CTL; addr 0A6]. TDL1 does not overwrite time slot data until it is enabled. DL1_CTL also controls the data format and the circular buffer/FIFO mode.

The following data formats [DL1[1,0]; addr 0A6] are supported on the data link: Frame Check Sequence (FCS), non-FCS, PACK8, or PACK6. FCS and non-FCS are HDLC-formatted messages. PACK8 and PACK6 are unformatted messages with 8 bits per FIFO access, and 6 bits per FIFO access, respectively.

The Circular Buffer/FIFO control bit [TDL1_RPT; addr 0A6] allows the FIFO to act as a circular buffer; in this mode, a message can be transmitted repeatedly. This feature is available only for unformatted transmit data link applications. The processor can repeatedly send fixed patterns on the selected channel by writing a 1- to 64- byte message into the circular buffer. The programmed message length repeats until the processor writes a new message. The first byte of each unformatted message is output automatically aligned to the first frame of the 12-, 24-, or 16-frame transmit multiframe (SF/ESF/MFAS). This allows the processor to source overhead or data elements aligned to the TX timebase.

NOTE: Each unformatted message written is output-aligned only after the preceding message completes transmission. Therefore, data continuity is retained during the linkage of consecutive messages, provided that the contents of each message consists of a multiple of the multiframe length.

Time slot and bit selection is done through the DL1 Time Slot Enable [DL1_TS; addr 0A4] and DL1 Bit Enable [DL1_BIT; addr 0A5] registers. DL1_TS selects which frames and which time slot are overwritten. The frame select allows TDL1 to overwrite the time slot in all frames, odd frames, even frames. The time slot word enable is a value between 0 and 31 that selects which time slot is filled with data from the transmit data link buffer. DL1_BIT selects which bits are overwritten in the time slot selected. Table 2-10 lists commonly used data link settings.

Table 2-10. Commonly Used Data Link Settings

Data Link	Frame	Time Slot	Time Slot Bits	Mode
ESF FDL	Odd	0 (F bits)	Don't Care	FCS
T1DM R Bit	All	24	00000010	FCS
SLC-96	Even	0 (F bits)	Don't Care	PACK6
ISDN LAPD	All	N	11111111	FCS
CEPT Sa4	Odd	1	00001000	FCS
GENERAL NOTE: N represents any T1/E1 time slot.				

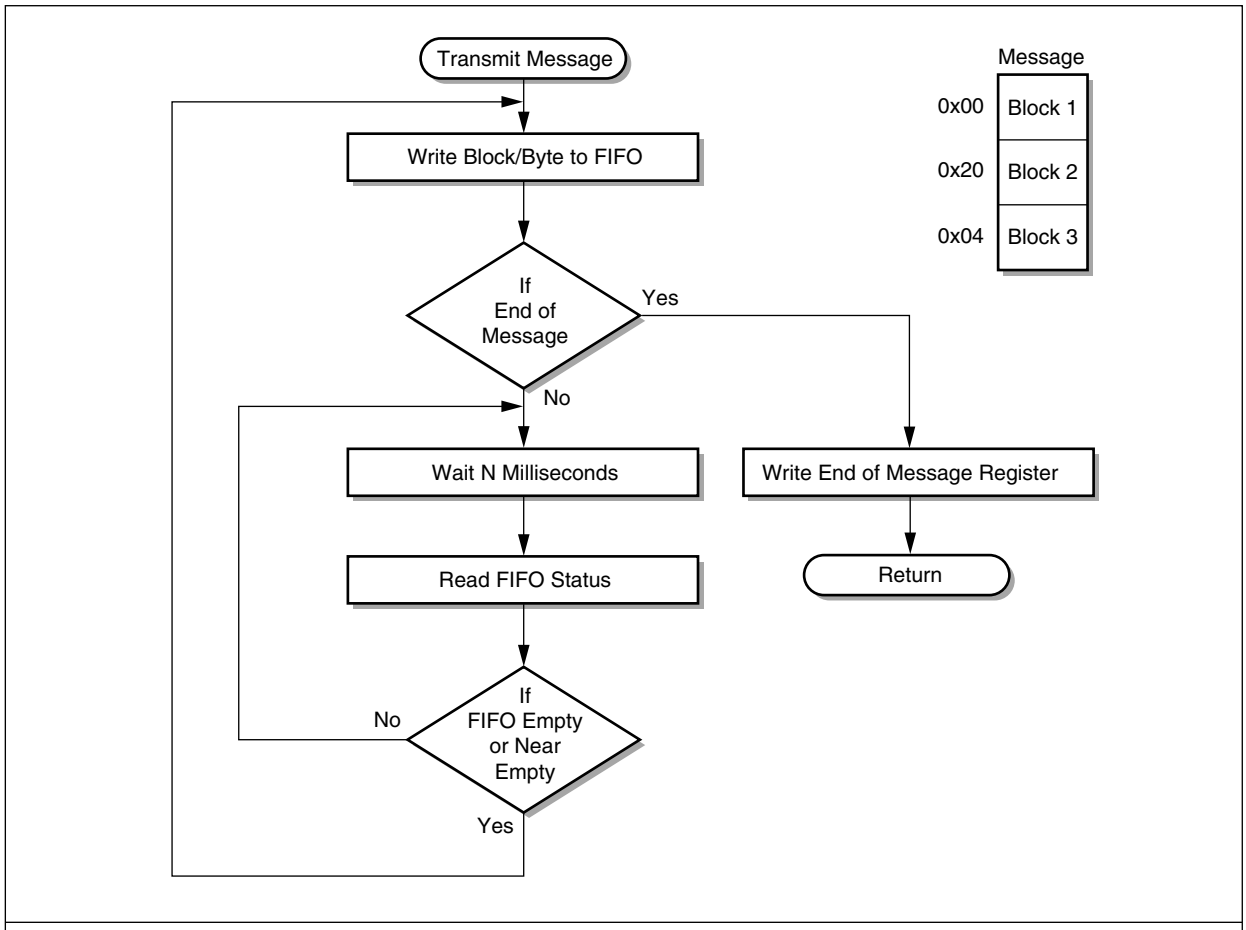
The Transmit Data Link FIFO #1 [TDL1; addr 0AD] is 64 bytes and very versatile. It can be used as a single-byte transmit buffer or in any number of bytes, up to a maximum of 64. As a single-byte FIFO, the Transmit FIFO Empty Status (TMPTY1) in TDL #1 Status [TDL1_STAT; addr 0AE] and Transmit FIFO Empty Interrupt (TEMPTY) in Data Link 1 Interrupt Status [ISR2; addr 009] can be used for byte-by-byte transmissions.

Using the Transmit Data FIFO, an entire block of data can be transmitted with very little microprocessor-interrupt overhead. Block transfers to the FIFO can be controlled by the Near Empty threshold in the FIFO Empty Control register [TDL1_FEC; addr 0AB]. The Near Empty threshold is a user-programmable value between 0 and 63 that represents the minimum number of bytes that can remain in the transmit FIFO before near empty is declared. Once the threshold is set, the Near Empty Status (TNEAR1) in TDL #1 Status [TDL1_STAT; addr 0AE] is asserted whenever the Near Empty threshold is reached. An interrupt, TNEAR in the Data Link 1 Interrupt Status register [ISR2; addr 009], is also available to mark this event.

Once an entire message is written into the transmit FIFO or circular buffer, the processor must indicate the end of message by writing any value to the TDL #1 End of Message (EOM) Control [TDL1_EOM; addr 0AC]. In FCS mode, the EOM indicates that the FCS is to be calculated and transmitted following the last byte in the FIFO; in the Circular Buffer mode, the EOM indicates the end of the transmit circular buffer.

The Transmit Data Link Controller can be programmed according to the CPU bandwidth of your system. For systems with one CPU dedicated to one Bt8370, the data link status can be polled, and the 64-byte transmit FIFO can be used like a single-byte transmit buffer. For systems where a single CPU controls multiple Bt8370s, the data link can be interrupt-driven and the entire 64-byte transmit FIFO can be used to store entire messages. See Figures 2-30 and 2-31 for a high-level description of polling and interrupt-driven Transmit Data Link Controller software.

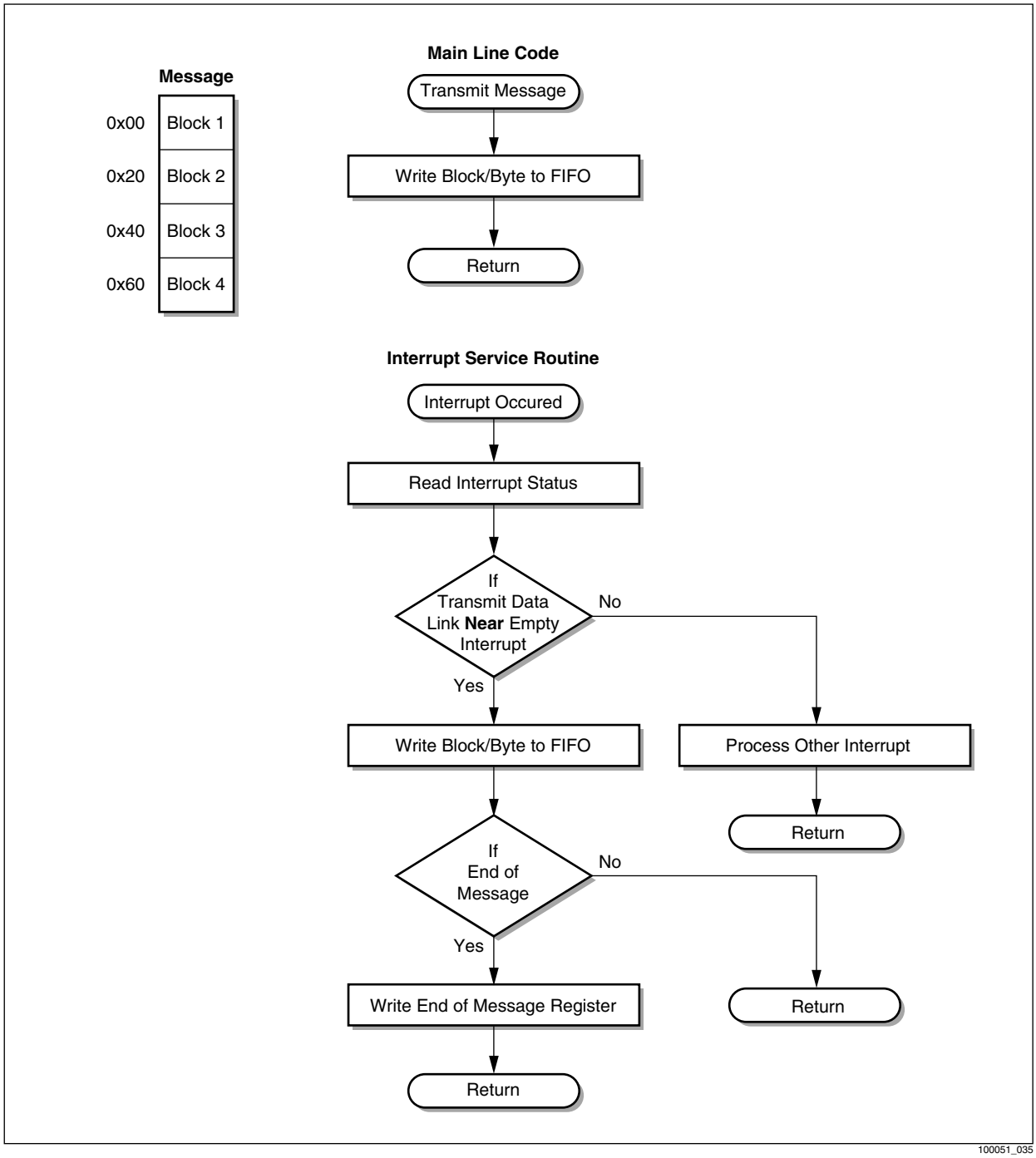
Figure 2-30. Polled Transmit Data Link Processing



NOTE(S):
Selected N based on the data rate of link.

100051_034

Figure 2-31. Interrupt-Driven Transmit Data Link Processing



The Bt8370/75/76 uses a hierarchical interrupt structure, with one top-level Interrupt Request register [IRR; addr 003] directing software to the lower levels. Of all the interrupt sources, the two most significant bandwidth requirements are signaling and data link interrupts. Each data link controller has a top-level interrupt status register that reports data link operations (see Data Link 1 and 2 Interrupt Status registers [ISR2; addr 009, and ISR1; 00A]). The processor uses a two-step interrupt scheme for the data link: it reads the Interrupt Request register, then uses that register value to read the corresponding Data Link Interrupt Status register.

2.8.2.2 PRM Generator

Performance Report Messages (PRMs) are HDLC messages containing path identification and performance monitoring information. If automatic performance report insertion is selected [AUTO_PRM; addr 0AA], a performance report is generated each second and begins transmitting coincident with the one-second timer interrupt [ONESEC; addr 005]. The PRM is sent immediately if the processor sets the SEND_PRM bit in the Performance Report Message register [PRM; addr 0AA]. All performance monitoring fields of the message are automatically filled in when a PRM is generated. The remaining PRM bit fields are application-specific and can be configured using the Performance Report Message register.

For systems with a single processor and multiple Bt8370s, the automatic PRM generation can off-load a significant portion of CPU bandwidth.

TBOP Transmitter

The Transmit Bit-Oriented Protocol (TBOP) transmitter sends BOP messages, including ESF Yellow Alarm, which consists of repeated 16-bit patterns with an embedded 6-bit code word. The TBOP is configured to operate over the same channel selected by Data Link #1 [DL1_TS; addr 0A4]. The TBOP must be configured to operate over the FDL channel. This is required for TBOP to convey Priority, Command, and Response code word messages according to *ANSI T1.403, Section 9.4.1*. The precedence of transmitted BOP messages with respect to current DL1 transmit activity is configurable using the Transmit BOP mode bits [TBOP_MODE[1,0]; addr 0A0]. BOP messages can also be transmitted during E1 mode, although the 16-bit code word pattern has not currently been adopted as an E1 standard. The length of the BOP message [TBOP_LEN[1,0]; addr 0A0] can be set to a single pattern, 10 patterns, 25 patterns, or continuous.

```
0xxxxxx0 11111111 (transmitted right to left)
[543210] TBOP = 6-bit code word
```

BOP code words are transmitted by writing to the Transmit BOP Code Word register [TBOP; addr 0A1]. The real-time status of the code word transmission can be monitored using TBOP_ACTIVE in the BOP Status register [BOP_STAT; addr 0A3]. A begin BOP transmit interrupt is available in Data Link 1 Interrupt Status [ISR2; addr 009].

2.8.3 Sa-Byte Overwrite Buffer

Five transmit Sa-Byte buffers [TSA4 to TSA8; addr 07B to 07F] are available; they insert Sa-bits into the odd frames of TS0. The entire group of 40 bits is sampled every 16 frames, coincident with the Transmit Multiframe bit interrupt boundary [TMF; addr 008]. Bit 0 from each TSA register is then inserted during frame 1, bit 1 is inserted during frame 3, bit 2 is inserted during frame 5, etc., which gives the processor a maximum of 2 ms after TMF interrupt to write new Sa-Byte buffer values. Transmit Sa-bits maintain a fixed relationship to the transmit CRC multiframe. Each of the 5 Sa-Byte transmit buffers can be individually enabled using the Manual Sa-Byte Transmit Enable in the Transmit Manual Sa-Byte/FEBE Configuration register [TMAN; addr 074].

2.8.4 Overhead Pattern Generator

The transmit overhead generation circuitry provides the ability to insert all overhead associated with the Primary Rate Channel. The following types of overhead pattern generation are supported: Framing patterns, Alarm patterns, Cyclic Redundancy Check (CRC), and Far-End Block Error (FEBE).

2.8.4.1 Framing Pattern Generation

The framing pattern generation circuitry inserts the following patterns into the data stream: the 2-bit terminal framing (Ft) pattern, the 6-bit signaling frame (Fs) pattern, the 6-bit FPS pattern, the 8-bit FAS/NFAS pattern, and the 6-bit MFAS pattern.

The Ft pattern in SF, SLC-96, and T1DM is inserted into the transmit data stream by enabling the INS_FBIT in the Transmit Frame Format register [TFRM; addr 072]. The Fs pattern in SF is inserted by enabling the INS_MF bit. The FPS pattern in ESF and the FAS/NFAS pattern in E1 mode are inserted by enabling the INS_FBIT bit. The MFAS pattern is inserted by enabling the INS_MF bit.

2.8.4.2 Alarm Generator

The Transmit Alarm Generation circuitry generates Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI/Yellow Alarm).

AIS Generation

AIS is defined as an unframed all-1s pattern and is normally transmitted when the data source is lost. AIS transmission can be enabled as follows:

- Manually
- Automatically upon detection of transmit loss of clock
- Automatically upon loss of received signal or loss of receive clock

Typical applications require transmission of AIS toward the line when the DTE transmit data or clock is not present. In most applications, DTE data and clock are isolated from the transmitter, requiring manual AIS transmission under software control. Manual insertion of AIS is controlled by the TAIS bit in the Transmit Alarm Signal Configuration register [TALM; addr 075]. Setting this bit overwrites the currently transmitted data with the AIS pattern. If AISCLK [TLIU_CR; addr 068] is also set, AIS is transmitted using AIS Clock Input (ACKI); otherwise it uses the clock present at TCKI MUX output [CMUX; addr 01A].

Automatic transmission of AIS can be controlled by detection of transmit loss of clock [TLOC; addr 048]. This mode is enabled by setting AISCLK and providing an alternate transmit line rate clock on the ACKI clock input pin.

By setting AUTO_AIS in the TALM register, automatic transmission of AIS can also be controlled by detection of Receiver Loss of Signal [RLOS; addr 047] or Receiver Loss of Clock [RLOC; addr 047], if an analog or digital line interface option [RDIGI; addr 020] is used. This mode is typically used to transmit AIS (keep-alive) during line loopback if the received signal is lost. Setting AUTO_AIS simultaneously with setting LLOOP [LOOP; addr 014] enables this operation.

Yellow Alarm Generation

Yellow Alarm, also referred to as RAI (Remote Alarm Indication), is a bit pattern inserted into the transmit stream to alert far-end equipment that the local receiver cannot recover data. Yellow Alarm/RAI is typically transmitted during Receive Loss of Frame and is defined differently depending upon the transmit frame format configured [TFRAME; addr 070]. Table 2-11 describes the Yellow Alarm/RAI action taken for each frame format.

Table 2-11. Yellow Alarm Generation

Frame Format	Yellow Alarm Location	Mode
SF	Bit 2 of every time slot set to 0	YB2
ESF(1)	Bit 2 of every time slot set to 0	YB2
SLC-96	Bit 2 of every time slot set to 0	BY2
SF/JYEL	F bit 12 of every superframe set to 1	YJ
T1DM	Y bit of the sync byte set to 0	Y24
E1	A bit of TS0 set to 1	Y0

FOOTNOTE:

(1) Yellow Alarm/RAI for T1-ESF framing is defined as a BOP priority code word in the FDL channel. This is called T1 Multiframe Yellow Alarm in the Bt8370. T1-ESF Multiframe Yellow Alarm/RAI(YF) is not transmitted using the procedure described below. Instead, T1- ESF Multiframe Yellow Alarm/RAI(YF) is generated by configuring DL1 to continuously transmit an all 0s BOP priority code word. See the Transmit Data Links section under TBOP Transmitter.

Transmission of Yellow Alarm(YB2) is controlled by the register bits listed in Table 2-12.

Table 2-12. Yellow Alarm Register Bits

Bit Name	Register
INS_YEL	[TFRM; addr 072]
TYEL	[TALM; addr 075]
AUTO_YEL	[TALM; addr 075]
RLOF	[ALM1; addr 047]
RLOF_INTEG	[RALM; addr 045]

The insertion of Yellow Alarm/RAI into the transmit stream is controlled by INS_YEL. Yellow Alarm/RAI is inserted only when INS_YEL is set. Otherwise, these bit positions are supplied by data from TPCMI. Yellow Alarm/RAI generation can be done manually or automatically.

Manual generation of Yellow Alarm/RAI is controlled by TYEL. Setting this bit immediately and unconditionally overwrites the Yellow Alarm signal bit(s) in the transmitted data stream with the appropriate pattern.

Automatic generation of Yellow Alarm is controlled by AUTO_YEL, RLOF, and RLOF_INTEG. If AUTO_YEL is set, Yellow Alarm is generated during a Receive Loss of Frame alignment (RLOF (FRED Status) = 1). Optionally, RLOF integration can be enabled by setting RLOF_INTEG. In this case, both RLOF indication and Yellow Alarm/RAI generation are delayed for approximately 2.5 seconds if a continuous out-of-frame condition exists. RLOF_INTEG mees the *T1.408* specification. In order to meet the requirements of *TR62411,* "Conditions Causing the Initiation of Carrier Failure Alarms," the Receive Loss of Frame condition reported by RLOF (addr 047) must be integrated before initiating Yellow Alarm transmission. This can be accomplished in software by integrating RLOF during an RLOF Interrupt (ISR7; addr 004), with RLOF_INTEG bit cleared. Yellow Alarm/RAI generation continues for at least one second after RLOF clears.

Multiframe Yellow Alarm Generation

In T1, ESF framing mode, Multiframe Yellow Alarm or RAI is transmitted using BOP Codeword Transmitter [TBOP; addr 0A1] and does not depend on INS_MYEL. Transmitting Yellow Alarm/RAI toward the line can be done upon receiving Receive Loss of Frame. T1 multiframe Yellow Alarm must be generated by configuring TDL1 to transmit an all-0s BOP code word. See Section 3.15.

In E1, CAS framing modes, Multiframe Yellow Alarm is inserted into the transmit stream to alert far-end equipment that local received multiframe alignment is not recovered. E1 Multiframe Yellow Alarm is transmitted by setting the Y bit in time slot 16, frame 0.

See Table 2-13 for T1/E1 multiframe yellow alarm generation.

Table 2-13. Multiframe Yellow Alarm Generation

Line Rate	Multiframe Yellow Alarm Action	Mode
T1	Facilitates Yellow Alarm Action (requires programming TDL1)	YF
E1	Set Y bit TS16 in frame 0 to 1	Y16

Transmission of Multiframe Yellow Alarm is controlled by the register bits listed in Table 2-14.

Table 2-14. Multiframe Yellow Alarm Register Bits

Bit Name	Register
INS_MYEL	[TFRM; addr 072]
TMYEL	[TALM; addr 075]
AUTO_MYEL	[TALM; addr 075]
SRED	[ALM3; addr 049]

The insertion of E1 Multiframe Yellow Alarm is controlled by INS_MYEL. E1 Multiframe Yellow Alarm is inserted only when INS_MYEL is set. Multiframe Yellow Alarm generation can be initiated manually or automatically.

Manual insertion of Multiframe Yellow Alarm is controlled by TMYEL. Setting this bit unconditionally overwrites the Multiframe Yellow Alarm signal bit in the transmitted data stream.

Automatic insertion of Multiframe Yellow Alarm is controlled by AUTO_MYEL in the TALM register. When set, the AUTO_MYEL mode sends a yellow alarm for the duration of a Receive Loss of CAS Multiframe Alignment [SRED; addr 049].

2.8.4.3 CRC Generation

The CRC generation circuitry computes the value of the CRC-6 code in T1 mode or the CRC-4 code in E1 mode. Once computed, it is inserted into the appropriate position of the transmitted data stream. CRC overwrite is enabled by the INS_CRC bit in Transmit Frame Format [TFRM; addr 072].

If the transmit frame format is configured as ESF, and the INS_CRC bit is active, the 2 Kbps CRC sequence is inserted. (The position of the CRC-6 bits is shown in Table A-4).

If the transmit frame format is configured as E1 and the INS_CRC bit is active, the 4 Kbps CRC sequence is inserted. (The position of the CRC-4 bits is shown in Table A-6.)

2.8.4.4 Far-End Block Error Generation

The Far-End Block Error (FEBE) generation circuitry inserts FEBE bits automatically or manually. Automatic FEBE generation is enabled by the INS_FE bit in TFRM. If the transmit frame format is configured as E1 and the INS_FE bit is active, a FEBE is generated in response to an incoming CRC-4 error by setting an E-bit of TS0 to 0. (See Table A-7 for the location of the E-bits within the E1 frame.)

Manual FEBE generation is enabled by the TFEBE bit of the Transmit Manual Sa-Byte/FEBE Configuration register [TMAN; addr 074]. If the transmit frame format is configured as E1 and the TFEBE bit is active, the FEBE bits are supplied by the processor in FEBE_I and FEBE_II bits [addr 074].

2.8.5 Test Pattern Generator

The transmit test pattern generation circuitry overwrites the transmit data with various test patterns and permits logical and frame-bit error insertion. This feature is particularly useful for system diagnostics, production testing, and test equipment applications. The test pattern can be a framed or unframed PRBS pattern. The PRBS patterns available include 2E11-1, 2E15-1, 2E20-1, and 2E23-1. Each pattern can optionally include Zero Code Suppression (ZCS). Error insertion includes LCV, BPV, Ft, CRC4, CRC6, COFA, PRBS, Fs, MFAS, and CAS.

The Transmit Test Pattern Configuration register [TPATT; addr 076] controls the test pattern insertion circuit. TPATT controls the PRBS pattern (TPATT[1:0]) bits), ZCS setting (ZLIMIT bit), T1/E1 framing (FRAMED bit), and Starting and Stopping transmission (TPSTART bit).

Patterns are generated in accordance with *ITU–T O.150 (10/92), O.151 (10/92)*, and *O.152 (10/92)*. Enabling ZLIMIT modifies the inserted pattern by limiting the number of consecutive 0s. For the 2E11-1 or 2E15-1 PRBS patterns, 8 or more 0s does not occur with ZLIMIT enabled. For the 2E20-1 or 2E23-1 PRBS patterns, 15 or more 0s will not occur with ZLIMIT enabled.

NOTE: The QRSS pattern is a 2E20-1 PRBS with ZLIMIT enabled. This function is performed according to ANSI T1.403 and ITU–T O.151 (10/92).

Frame bit positions can be preserved in the output pattern by enabling FRAMED. In T1 mode, this prevents the test pattern from overwriting the frame bit which occurs every 193 bits. In E1 mode with FRAMED enabled, the test pattern does not overwrite time slot 0 data (FAS and NFAS words) and time slot 16 (CAS signalling word) if CAS framing is also selected. CAS framing is selected by setting TFRAME[3] to 1 in the Transmit Configuration register [TCR0; addr 070]. The test pattern is stopped during these bit periods according to *ITU-T O.151, (10/92)*. If FRAMED is disabled, the test pattern is transmitted in all time slots.

2.8.6 Transmit Error Insertion

The Transmit Error Insert register [TERROR; addr 073] controls error insertion during pattern generation. Writing 1 to a TERROR bit injects a single occurrence of the respective error on TPOSO/TNEGO and XTIP/XRING outputs. Writing a 0 has no effect. Multiple transmit errors can be generated simultaneously. Periodic or random bit error rates can also be emulated by software control of the error control bit.

NOTE: Injected errors affect the data sent during a Framer or Analog Loopback [FLOOP or ALOOP; addr 014].

Line Code Violations (LCV) are inserted via the TVERR bit of the TERROR register. In T1 mode, if TVERR is set, a BPV is inserted between two consecutive 1s. TVERR is latched until the BPV is inserted into the transmit data stream, and then it is cleared. In E1 mode with HDB3 selected, two consecutive BPVs of the same polarity are inserted. This is registered as a single LCV for the receiving E1 equipment.

Ft, FPS, and FAS bit errors are inserted using the TFERR bit in the TERROR register. TFERR commands a logical inversion of the next frame bit transmitted.

CRC4 (E1) and CRC6 (T1) bit errors are inserted using the TCERR bit in the TERROR register. TCERR commands a logical inversion of the next CRC bit transmitted.

Change of Frame Alignments (COFAs) are controlled by the TCOFA and BSLIP bits in the TERROR register. TCOFA commands a 1-bit shift in the location of the transmit frame alignment by deleting (or inserting) a 1-bit position from the transmit frame. During E1 modes, BSLIP determines which direction the bit slip occurs. In T1 modes, only 1-bit deletion is provided.

NOTE: TCOFA alters extraction rate of data from transmit slip buffer; thus, repeated TCOFAs eventually cause a controlled frame slip where 1 frame of data is repeated (T1/BSLIP = 0), or where 1 frame of data is deleted (BSLIP = 1).

PRBS test pattern errors are inserted by TBERR in the TERROR register. TBERR commands a single PRBS error by logically inverting the next PRBS generator output bit.

Fs and MFAS errors are controlled by the TMERR bit in the TERROR register. TMERR commands a single Fs bit error in T1, or MFAS bit error in E1 by logically inverting the next multiframe bit transmitted.

CAS Multiframe (MAS) errors are controlled by the TSERR bit in the TERROR register. TSERR commands a single MAS pattern error by logically inverting the first MAS bit transmitted.

2.8.7 In-Band Loopback Code Generator

The in-band loopback code generator circuitry overwrites the transmit data with in-band codes of configurable value and length. These codes are sequences with periods of 1 to 7 bits and may, in some applications, overwrite the framing bit. The Transmit Inband Loopback Code Configuration register [TLB; addr 077] controls the functions required for this operation.

A loopback code is generated in the transmit data stream by writing the loopback code to the Transmit Inband Loopback Code Pattern register [LBP; addr 078], and then by setting the Start Inband Loopback (LBSTART) and Loopback Length (LB_LEN) bits in the Transmit Inband Loopback Code Configuration register [TLB; addr 077]. The TLB register optionally allows the loopback code to overwrite framing bits using the UNFRAMED bit. The LB_LEN provides loopback code pattern lengths of 4 to 7 bits. Patterns of 2 or 3 bits can be achieved by repeating the pattern in 4- or 6-bit modes, respectively. Framed or unframed all 1s or all 0s can also be achieved by setting the pattern to all 0s or all 1s. The in-band loopback code generator is applicable only to T1 mode.

2.8.8 ZCS Encoder

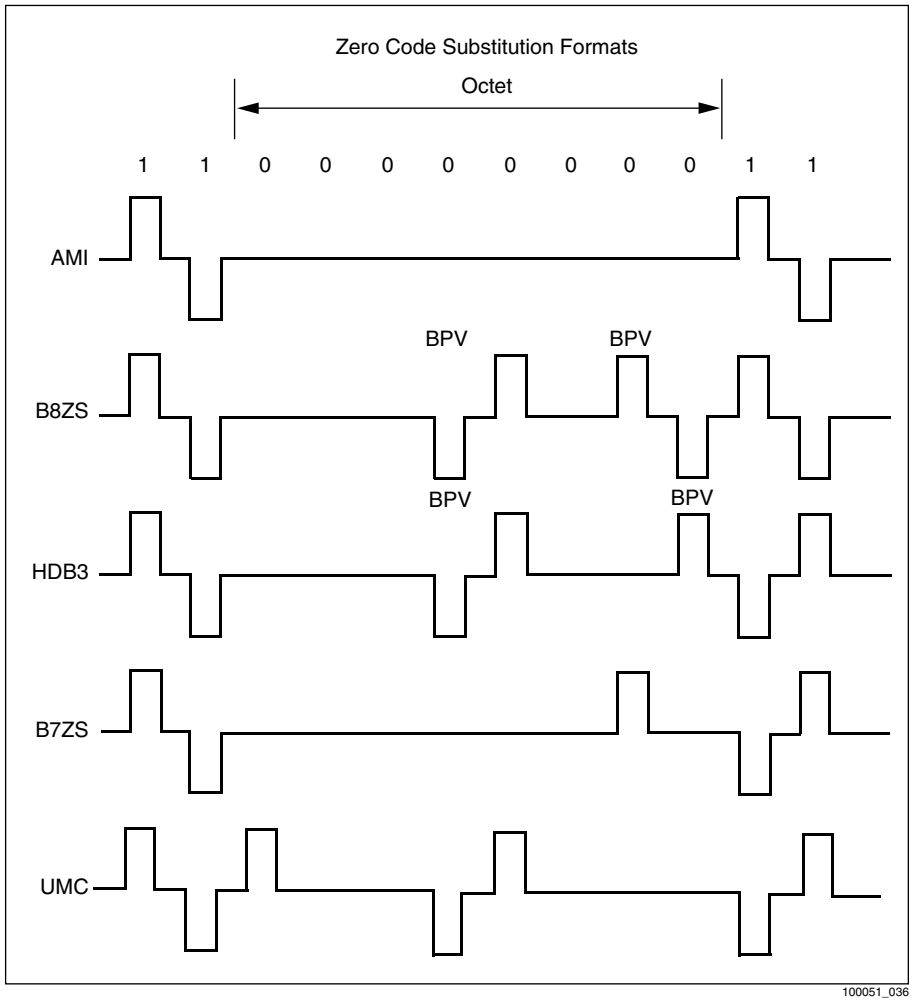
The ZCS encoder encodes the single rail clock and data (unipolar) into dual-rail data (bipolar). The Transmit Zero Code Suppression Bits (TZCS[1,0]) in the Transmitter Configuration register [TCR1; addr 071] selects ZCS and Pulse Density Violation (PDV) enforcement options for XTIP/XRING and TPOSO/TNEGO output pins. TZCS supports the following: Alternate Mark Inversion (AMI), High Density Bipolar of order 3 (HDB3), Bipolar with 8 Zero Suppression (B8ZS), Pulse Density Violation (PDV), and Unassigned Mux Code (UMC).

NOTE: ZCS encoding, which alters data content, is performed prior to the CRC calculation so the outgoing CRC will always be correct.

The AMI line code requires at least 12.5% average 1s density and no more than 15 consecutive 0s. A 1 is encoded as either a positive or negative pulse; a 0 is the absence of a pulse. Two consecutive pulses of the same polarity are referred to as a Bipolar Violation (BPV).

The HDB3 line code replaces 4 consecutive 0s by 000V or B00V code, where B is an AMI pulse and V is a bipolar violation (see Figure 2-32). ZCS encoder selects the code that forces the BPV output polarity opposite to the prior BPV.

Figure 2-32. Zero Code Substitution Formats



The B8ZS line code replaces strings of 8 consecutive 0s or no pulses with the B8ZS octet 000VB0VB, where B represents a normal bipolar pulse and V represents a BPV. A BPV that is not part of B8ZS octet is a BPV error.

B7ZS replaces bit 7 of all assigned time slots with a 1 if the contents are all 0. B7ZS encoding is enabled on a per-channel basis in the Transmit Per-Channel Control register [TPC0 to TPC31; addr 100 to 11F].

PDV enforcer overwrites transmit 0s that would otherwise cause output data to fail to meet the minimum required pulse density, per ANSI T1.403 sliding window.

NOTE: The enforcer never overwrites a framing bit and is not applicable during E1 mode.

UMC forces DS0 channels containing eight 0s to be replaced with the 10011000 code, per Telcordia *TA-TSY-000278*.

NOTE: RCVR's ZCS decoder cannot recover original data content from a UMC or B7ZS encoded signal, or from a PDV-enforced one.

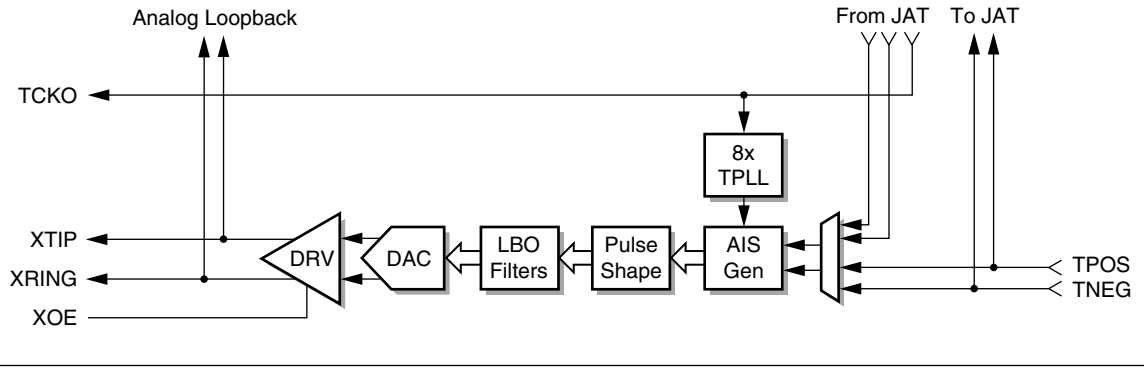
The TPOSO/TNEGO output pins provide access to the P and N rail unipolar data before it is sent to the TLIU. The output on TPOSO/TNEGO can be changed from dual-rail unipolar to NRZ unipolar data (TNRZO) and to multiframe sync clock (MSYNCO), using the Transmit NRZ Data (TNRZ) bit in TCR1[addr 071]. The TNRZ setting does not affect the XTIP/XRING output.

2.9 Transmit Line Interface Unit

The Transmit Line Interface Unit (TLIU), illustrated in Figure 2-33, converts P and N rail NRZ data to AMI pulses. The P and N rail NRZ data is generated by the XMTR, converted to AMI bipolar pulses by the TLIU, and output on the transmit tip and ring pins, XTIP and XRING. The TLIU has a configurable line rate, pulse shape, Line Build Out (LBO), external termination resistor, and transformer turns ratio.

The TLIU consists of a control circuit, a pulse template ROM, a set of LBO filters, a Digital-to-Analog Converter (DAC), and a line driver.

Figure 2-33. TLIU Diagram

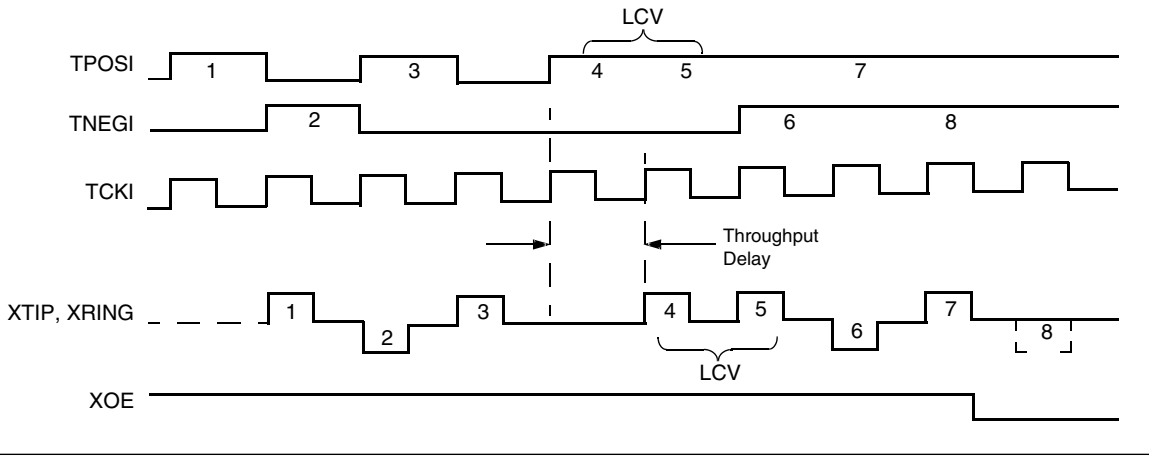


NOTE(S):
1. LBO filter block is not present in short haul devices: Bt28375 and Bt28376.

100051_037

The TLIU can be used independently of the XMTR by applying P and N rail NRZ data to the TPOSI and TNEGI pins. Figure 2-34 shows the relationship between the P and N rail NRZ data, the transmit clock input, and XTIP/XRING. The transmit clock input can be supplied on the Transmit Clock Input pin (TCKI) or can be slaved to other clocks in the system using the Clock Input Mux register [CMUX; addr 01A]. This figure also shows the XTIP/XRING outputs being three-stated using the XOE pin.

Figure 2-34. TLIU Waveform



NOTE(S):
1. Transmit jitter attenuation bypassed.

100051_038

2.9.1 Pulse Shape

Normalized and isolated AMI output pulses fit the T1/E1 pulse templates in Figures 2-35 and 2-37 when measured in accordance with the test circuits in Figures 2-36 and 2-38. Table 2-15 through Table 2-22 list the pulse template corner points. An isolated pulse is defined as a 1 followed by seven 0s for T1, and a 1 followed by three 0s for E1. The pulse templates shown in Figures 2-35 and 2-37 come from *ANSI T1.403-1995*, *ITU-T G.703*, and *ANSI T1.102-1993*.

Figure 2-35. Standard DS1 Pulse Template

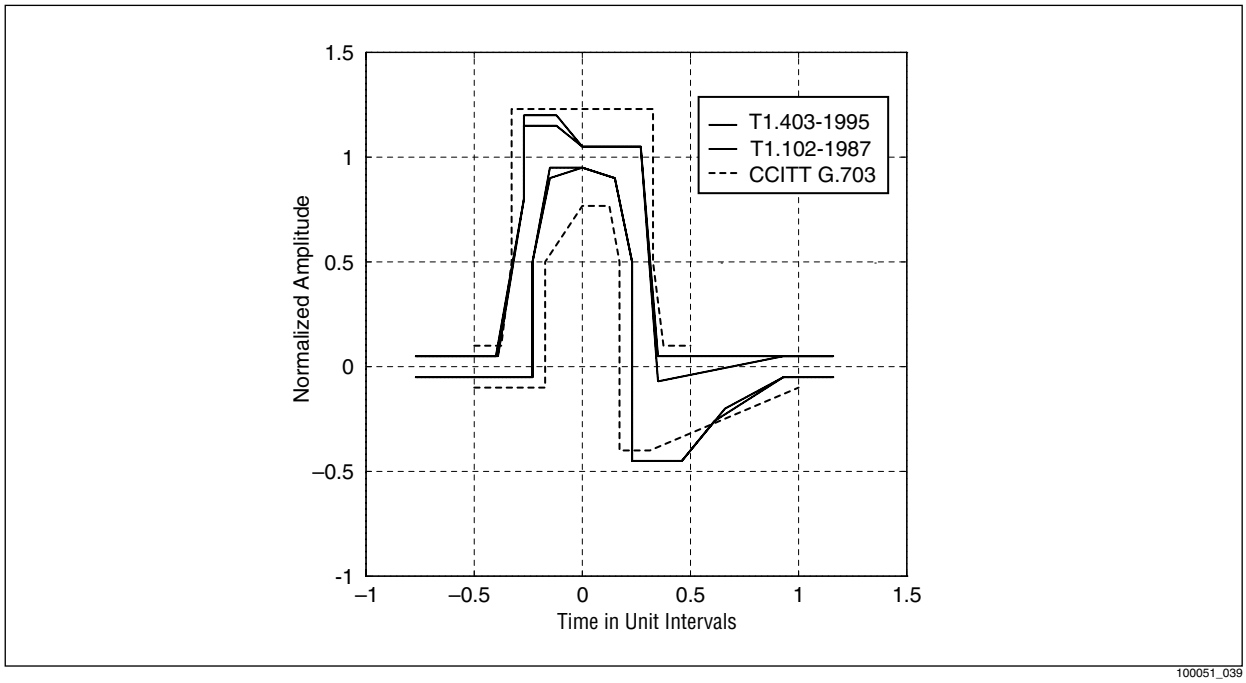
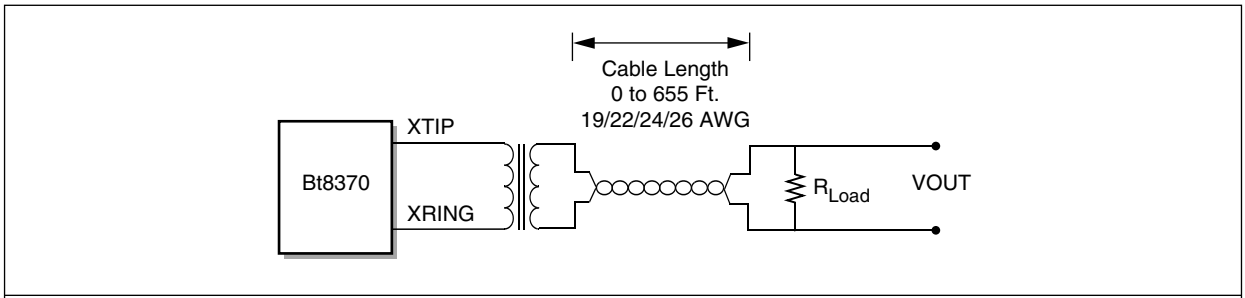


Figure 2-36. T1 Pulse Template Test Circuit



NOTE(S):
1. R_{Load} = 100 Ω ± 5%.

Figure 2-37. Standard E1 (G.703) Pulse Template

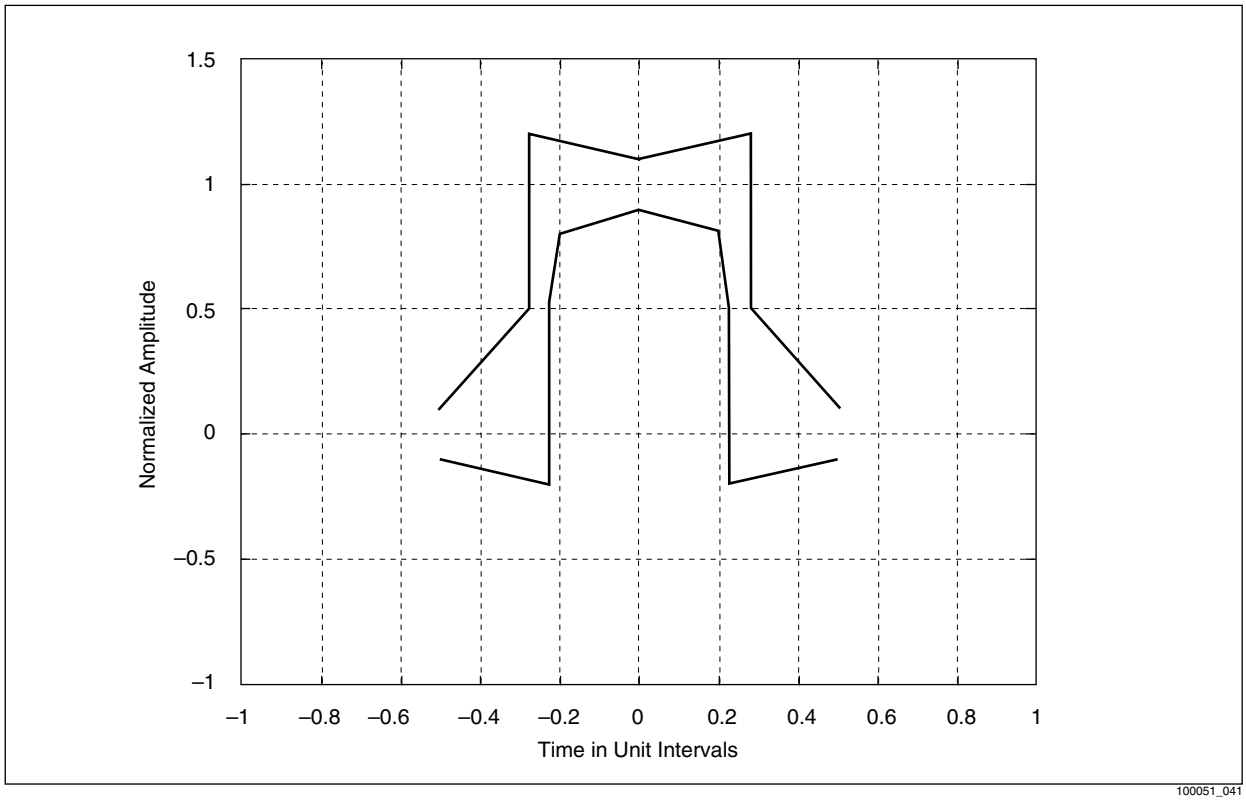


Figure 2-38. E1 (G.703) Pulse Template Test Circuit

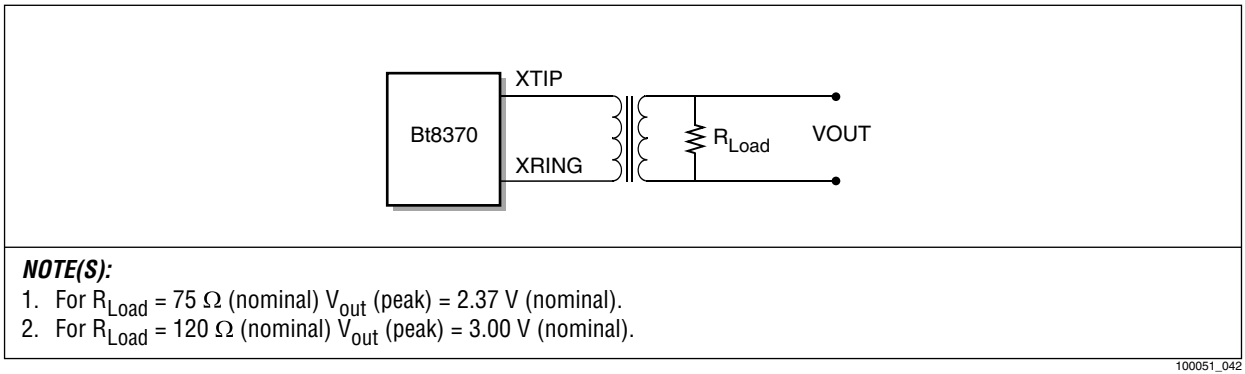


Table 2-15. ANSI T1.102, 1993–DS1 Pulse Template Corner Points, Maximum Curve

Time (ns)	–400	–253	–175	–175	–75	0	175	228	602	700
Time (UI)	–0.62	–0.39	–0.27	–0.27	–0.12	0	0.27	0.35	0.93	1.08
Normalized Amplitude	0.05	0.05	0.80	1.15	1.15	1.05	1.05	–0.07	0.05	0.05

Table 2-16. ANSI T1.102, 1993–DS1 Pulse Template Corner Points, Minimum Curve

Time (ns)	–400	–150	–150	–100	0	100	150	150	300	427	602	700
Time (UI)	–0.62	–0.23	–0.23	–0.15	0	0.15	0.23	0.23	0.46	0.66	0.93	1.08
Normalized Amplitude	–0.05	–0.05	0.50	0.95	0.95	0.90	0.50	–0.45	–0.45	–0.20	–0.05	–0.05

Table 2-17. ANSI T1.403, 1995–DS1 Pulse Template Corner Points, Maximum Curve

Time (ns)	–400	–253	–175	–175	–75	0	175	228	500	700
Time (UI)	–0.62	–0.39	–0.27	–0.27	–0.12	0	0.27	0.34	0.77	1.08
Normalized Amplitude	0.05	0.05	0.80	1.20	1.20	1.05	1.05	–0.05	0.05	0.05

Table 2-18. ANSI T1.403, 1995–DS1 Pulse Template Corner Points, Minimum Curve

Time (ns)	–400	–150	–150	–100	0	100	150	150	300	396	600	700
Time (UI)	–0.62	–0.23	–0.23	–0.15	0	0.15	0.23	0.23	0.46	0.61	0.93	1.08
Normalized Amplitude	–0.05	–0.05	0.50	0.90	0.95	0.90	0.50	–0.45	–0.45	–0.26	–0.05	–0.05

Table 2-19. G.703, 1988–DS1 Pulse Template Corner Points, Maximum Curve

Time (ns)	–400	–243	–187	–187	187	187	243	700
Time (UI)	–0.62	–0.38	–0.29	–0.29	0.29	0.29	0.38	1.08
Normalized Amplitude	0.05	0.05	0.50	1.23	1.23	0.50	0.05	0.05

Table 2-20. G.703, 1988–DS1 Pulse Template Corner Points, Minimum Curve

Time (ns)	–400	–137	–137	0	81	137	137	203	700
Time (UI)	–0.62	–0.21	–0.21	0	0.13	0.21	0.21	0.32	1.08
Normalized Amplitude	–0.05	–0.05	0.50	0.77	0.77	0.50	–0.40	–0.40	–0.10

Table 2-21. G.703, 1988–Pulse Template Corner Points, Maximum Curve

Time (ns)	–244	–135	–135	0	135	135	224
Time (UI)	–0.50	–0.276	–0.276	0	0.276	0.276	0.50
Normalized Amplitude	–0.10	0.50	1.20	1.10	1.20	0.50	0.10

Table 2-22. G.703, 1988–Pulse Template Corner Points, Minimum Curve

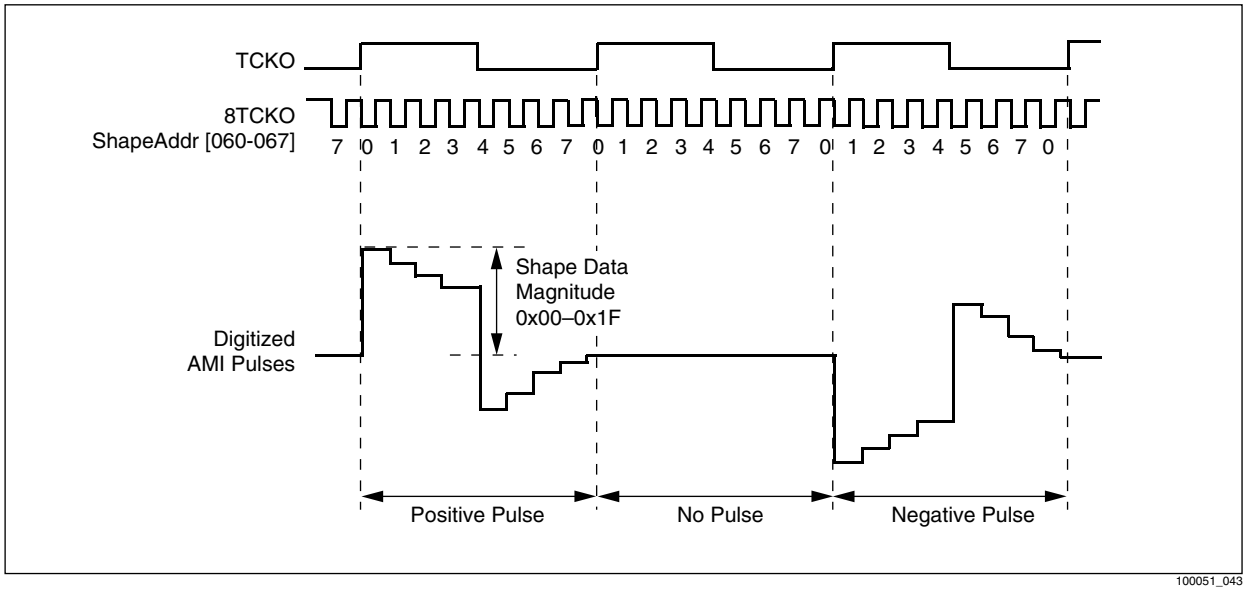
Time (ns)	–244	–110	–110	–97	0	97	110	110	244
Time (UI)	–0.500	–0.225	–0.225	–0.198	0	0.198	0.225	0.225	0.500
Normalized Amplitude	–0.10	–0.20	0.50	0.80	0.90	0.800	0.50	–0.20	–0.10

The pulse shape block receives P and N rail NRZ data. For each mark, it produces a set of eight 6-bit values which define the pulse shape to be transmitted, as illustrated in Figure 2-39. One of eight preprogrammed pulse shapes is selected via the Transmit LIU Configuration register [TLIU_CR; addr 068]. The TLIU control circuit downloads the code values associated with the selected pulse shape from the ROM to the Transmit Pulse Shape Configuration registers [SHAPE; addr 060–067], whenever the TLIU register is written to or when the device is reset. The SHAPE registers can be directly accessed via the microprocessor interface when a custom pulse shape is desired.

NOTE: Any modification to the TLIU register initiates another download to the SHAPE registers. The data stored in the pulse shape ROM and the SHAPE registers is 5-bit magnitude only.

The TLIU control circuit converts the 5-bit magnitude to 6-bit 2s complement data. The first 4 code values of the pulse (first half of the symbol) are forced to be positive, and the last 4 values (last half of the symbol) are forced to be negative, with respect to output pulse polarity.

Figure 2-39. Digitized AMI Pulse Shape



The VSET resistor not only provides a bias current to RPLL and TPLL but also controls the height of the transmit pulse. The VSET value can be fine tuned according to the total resistance on the line side. (See Figures 4-1 through 4-4 for the recommended front-end circuitry.)

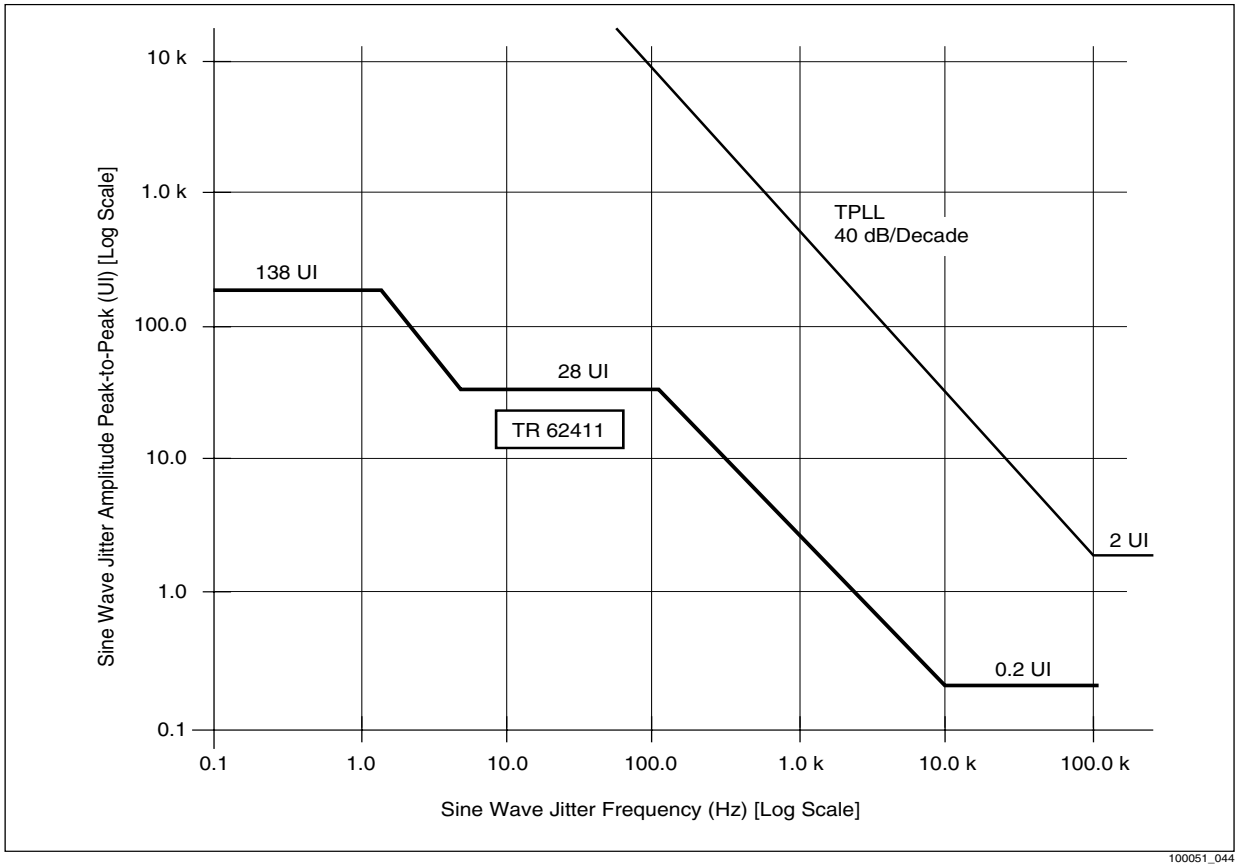
2.9.2 Transmit Phase Lock Loop

The Transmit Phase Lock Loop (TPLL) operates at a nominal rate of either 1.544 MHz or 2.048 MHz, selected by T1/E1N [CR0; addr 001]. The pull-in and hold-in range of the TPLL is ±200 ppm. The TPLL produces the transmit clock (TCKO) and an 8x clock that is used by the pulse shape block to generate the AMI pulses from TCKI clock mux, or JCLK.

2.9.2.1 Clock Reference

The TPLL reference clock is provided on the TCKO pin. If the jitter attenuator is enabled in the transmit direction [JDIR; addr 002], TCKO is the dejittered TCKI clock, or JCLK (if CLAD is enabled); otherwise, TCKO equals TCKI. The TCKI source is selected by TCKI[1:0] [CMUX; addr 01A]. TCKI can have the following selections: Recovered Receive Clock (RCKO), Receive System Bus Clock Input (RSBCKI), Clock Rate Adapter Output (CLADO), or an external clock, which is provided on the TCKI pin. The input clock jitter tolerance of the TPLL is illustrated in Figure 2-40.

Figure 2-40. TPLL Input Clock Jitter Tolerance



2.9.2.2 Output Jitter

The maximum output jitter generated on XTIP/XRING depends on the transmit clock source selected. See CLAD and JAT descriptions.

2.9.3 Line Build Out

In the Bt8370 long haul device, three Line Build Out (LBO) filter networks can be enabled in the TLIU to attenuate XTIP/XRING outputs in 7.5 dB steps, per the signal transfer function defined by FCC Part 68 Regulations. (See LBO[1:0] in TLIU_CR.) The number of LBO filters selected is based on the attached cable length. For short line lengths, larger LBO attenuation prevents far-end crosstalk. For longer line lengths, the appropriate LBO must be selected. The following equation lists the transfer function for each of the 7.5 dB LBO filters:

$$\frac{V_{out}}{V_{in}} = \frac{n_2 S^2 + n_1 S + n_0}{d_3 S^3 + d_2 S^2 + d_1 S + d_0}$$

where:

$$n_0 = 1.6049 \times 10^{6}$$

$$n_1 = 7.9861 \times 10^{-1}$$

$$n_2 = 9.2404 \times 10^{-8}$$

$$d_0 = 2.1612 \times 10^{6}$$

$$d_1 = 1.7223$$

$$d_2 = 4.575 \times 10^{-7}$$

$$d_3 = 3.8307 \times 10^{-14}$$

$$S = j2\pi f$$

$$f = frequency(Hz)$$

Pulse templates for each of the LBO settings are illustrated in Figure 2-41 through Figure 2-44.

Figure 2-41. 0 dB LBO Isolated Pulse Template

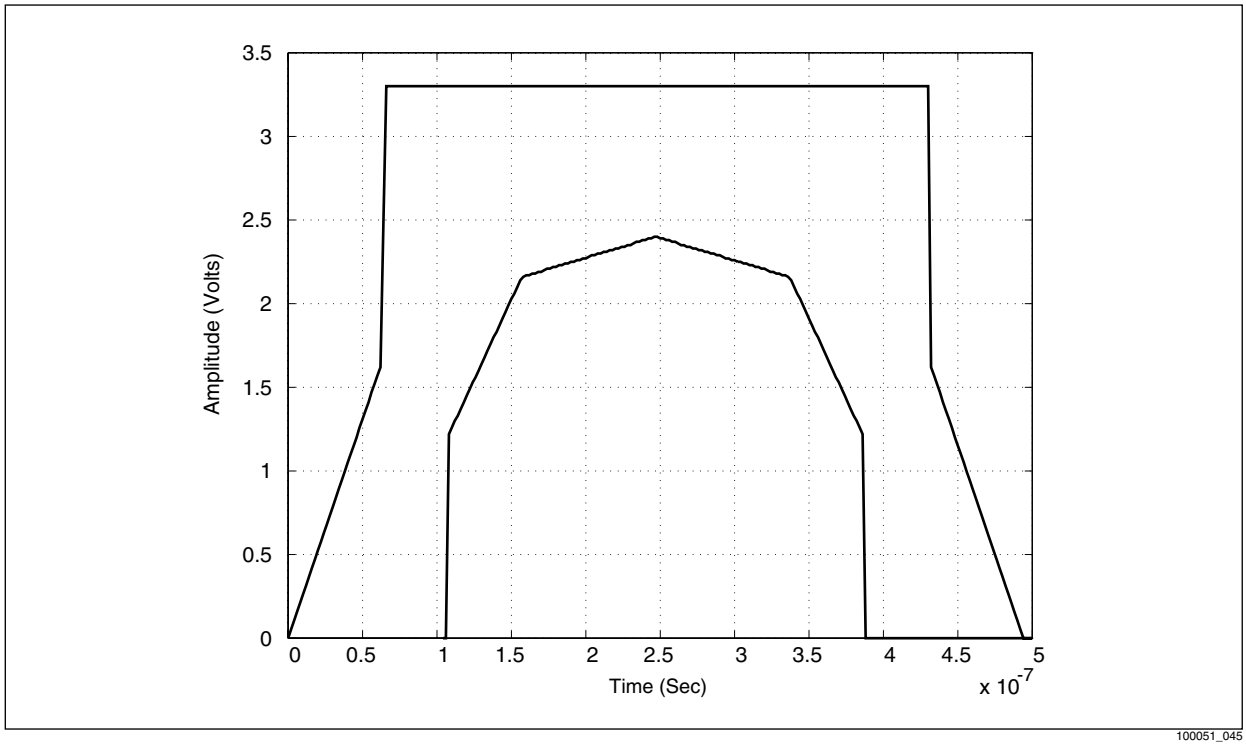


Figure 2-42. 7.5 dB LBO Isolated Pulse Template

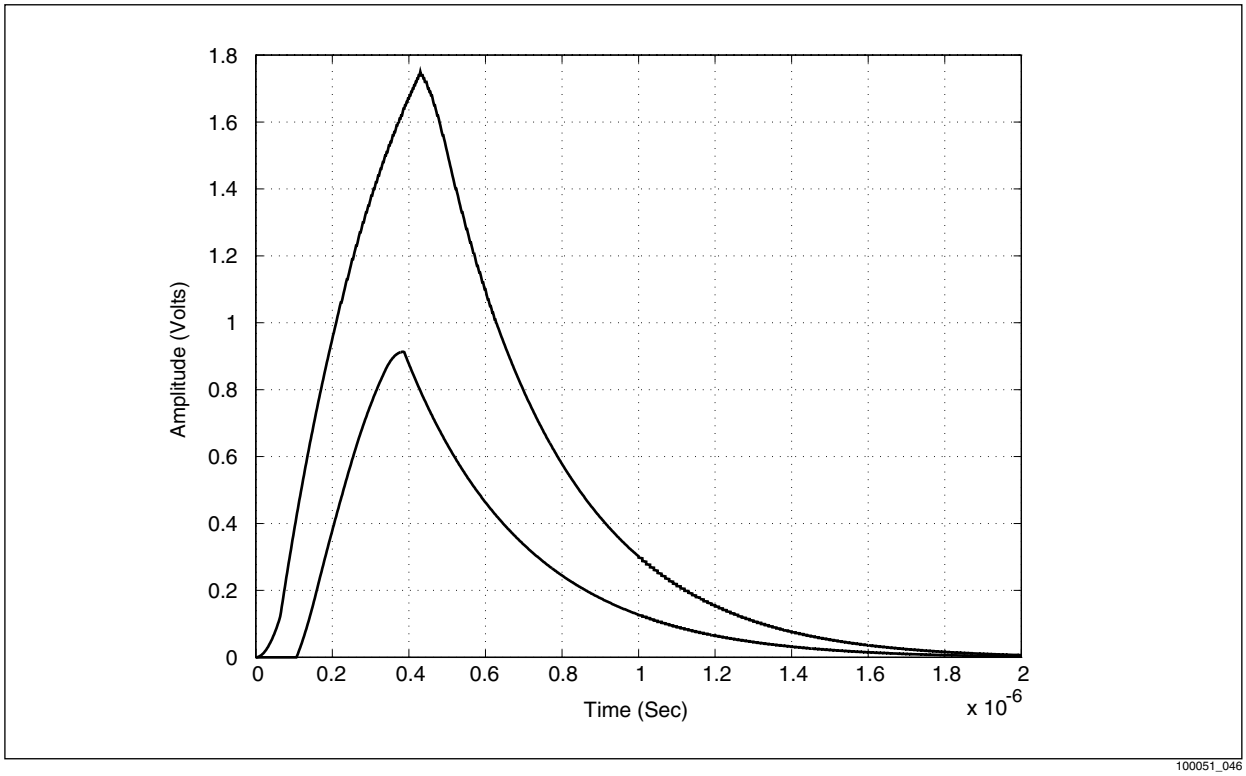


Figure 2-43. 15.0 dB LBO Isolated Pulse Template

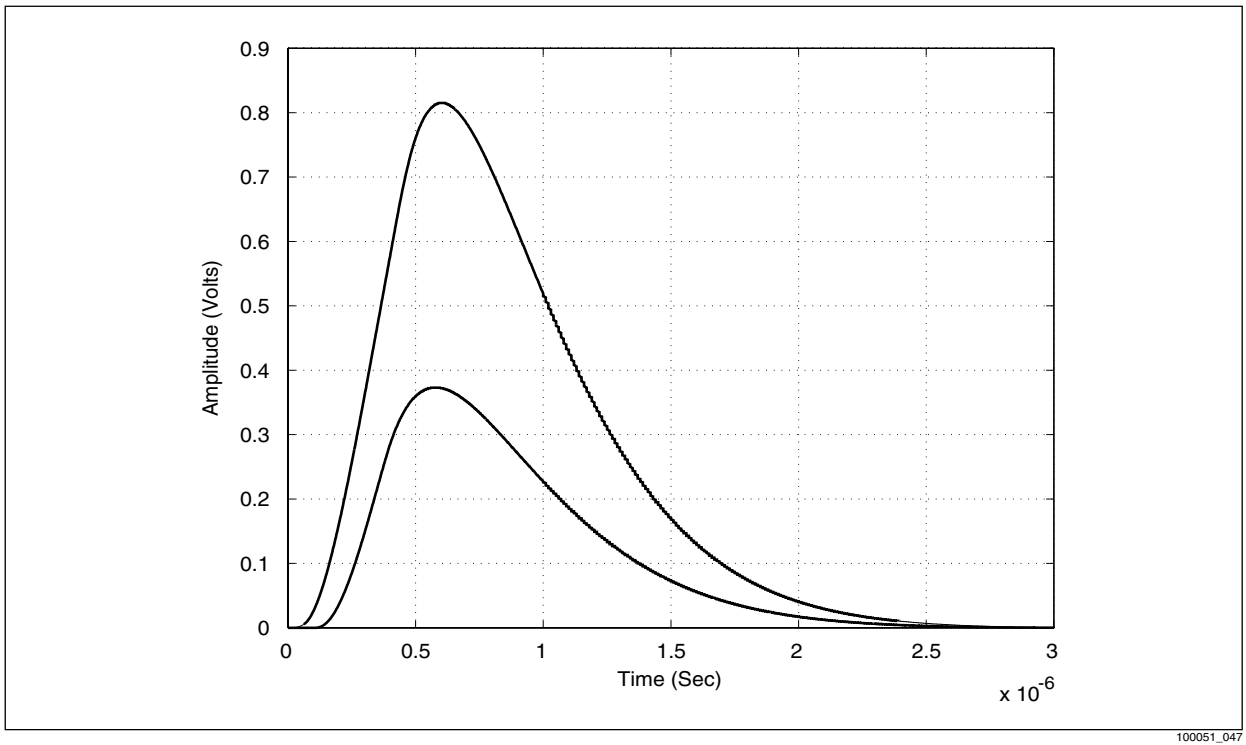
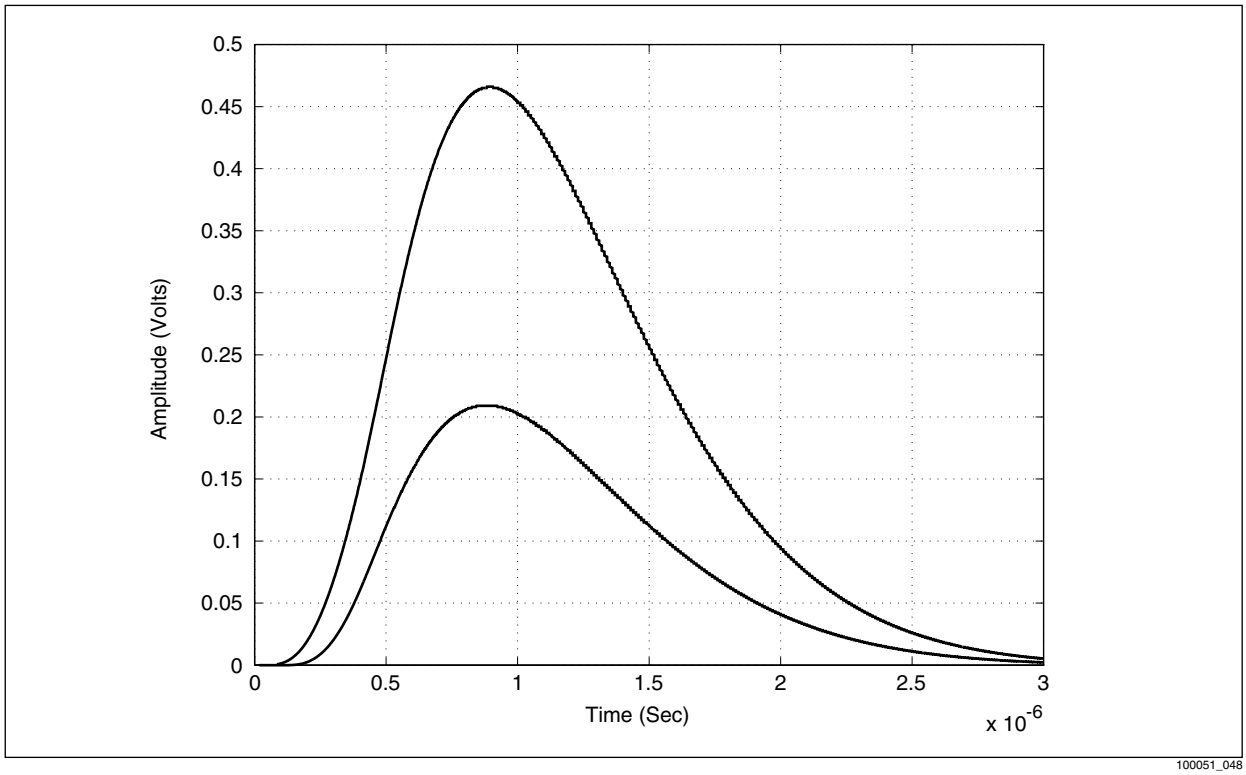


Figure 2-44. 22.5 dB LBO Isolated Pulse Template



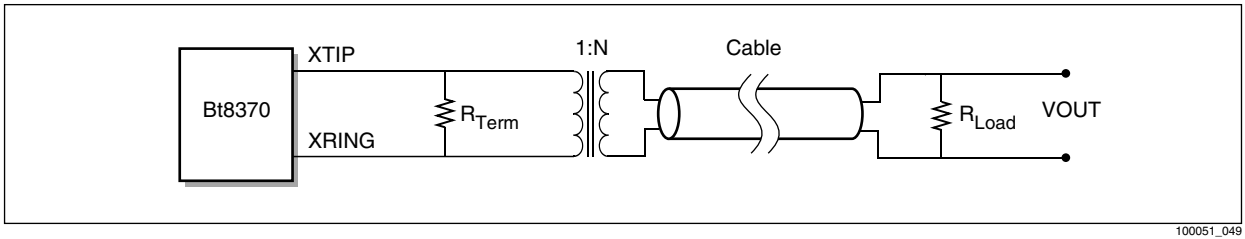
2.9.4 Line Driver

The line driver provides current drive to the low-power, bipolar analog signal from the transmit Digital-to-Analog Converter (DAC). The transmit DAC converts the coded pulse shape values to properly scaled, analog bipolar signals which drive the line transformer. The coded pulse shape values can optionally be filtered during T1 Longhaul by LBO filter options. The internal sensing circuits limit the drive current to less than 50 mA when a shorted line condition is detected for more than 48 transmitted pulses. Normal drive levels are restored when the short is removed. Typically, this is caused by a transmit cable short circuit or a transient transmission line current surge. The activation sets the TSHORT bit in Alarm 2 Status register [ALM2; addr 048].

2.9.4.1 Termination Impedance

If an external termination resistor is used, the TERM bit in TLIU_CR must be set. The transformer setting must also be set via the TURNS bit in TLIU_CR. An external termination resistor can be used only if the transformer turns ratio is 1:1.36. The external termination resistor (RTerm) is placed in parallel across XTIP/XRING, as illustrated in Figure 2-45.

Figure 2-45. External Termination Resistor Placement



2.9.4.2 Return Loss

Return loss is the measure of loss in the return path due to an impedance mismatch. To meet a –18 dB transmitter return loss, independent of the cable type, use a 51.1 Ω termination resistor (see Figure 2-46). To see the effect of different termination resistors on the pulse height, see Figure 2-47.

Figure 2-46. Nominal Return Loss

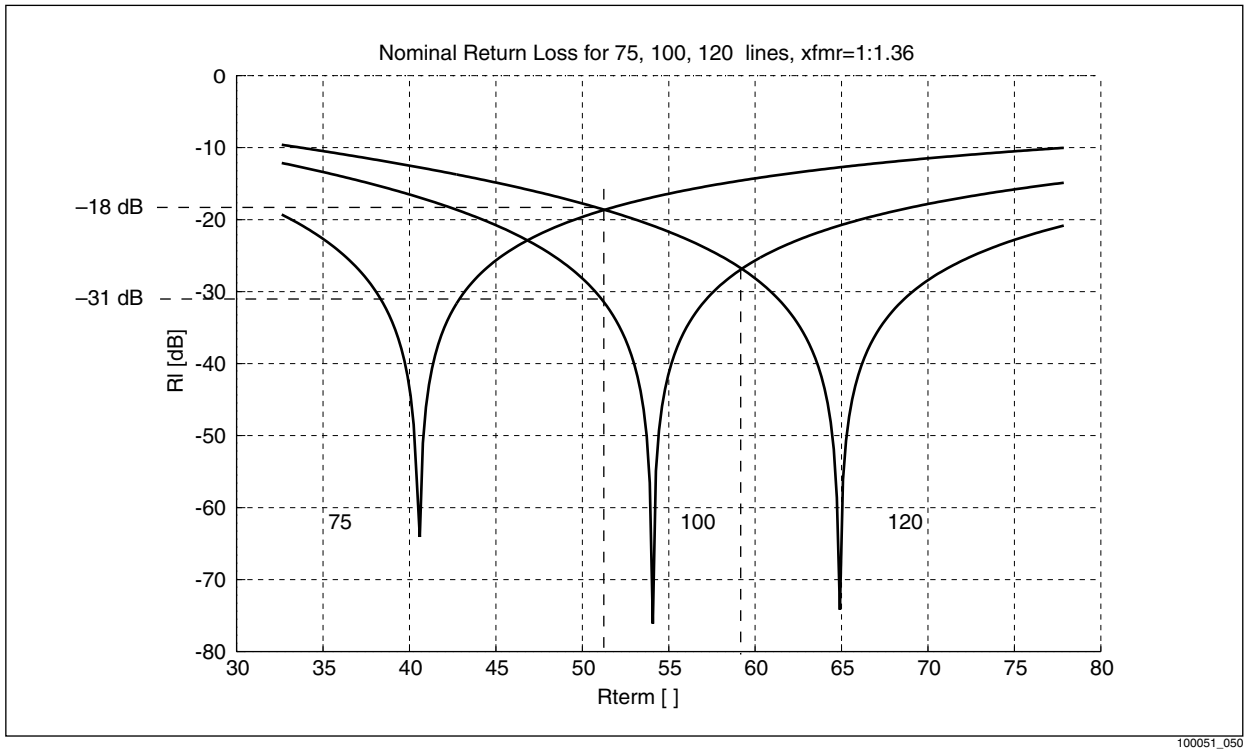
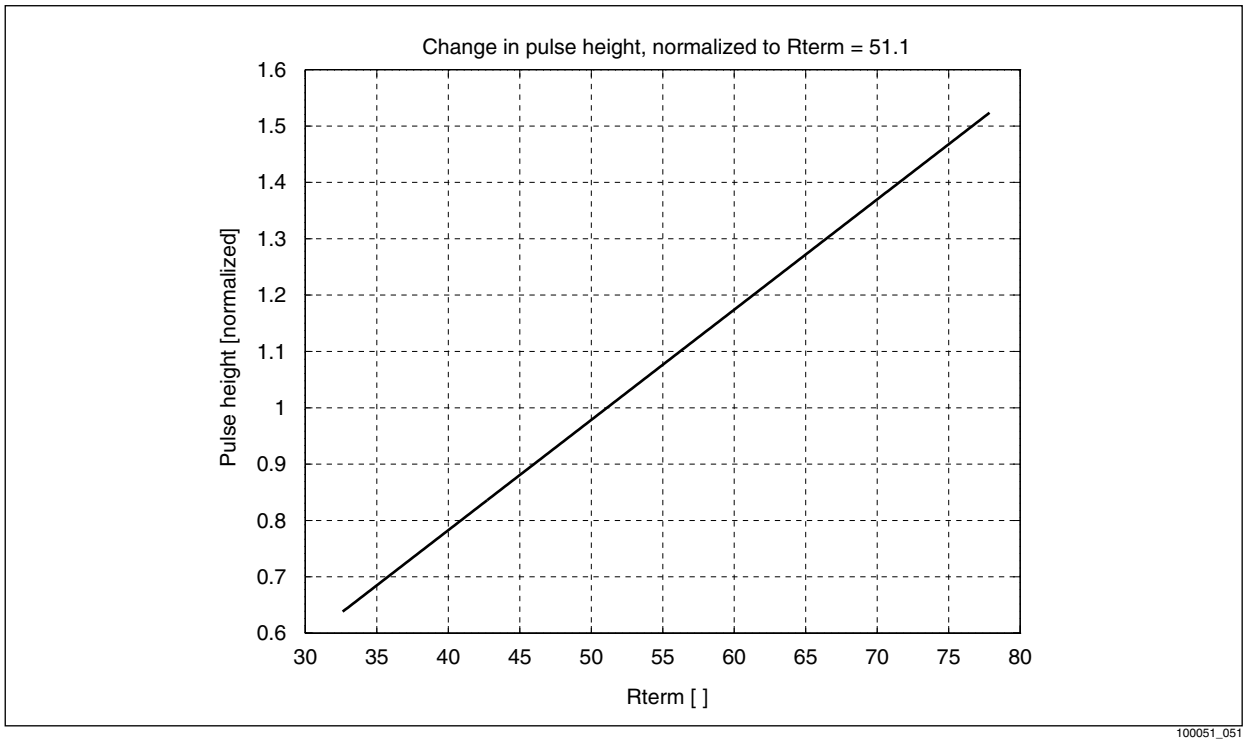


Figure 2-47. Output Pulse Height versus Transmit Termination Impedance



2.9.4.3 Output Enable

The bipolar analog output XTIP/XRING can be enabled or disabled using the XOE pin. This feature allows switching between multiple XTIP/XRING outputs that are tied together.

2.9.5 Pulse Imbalance

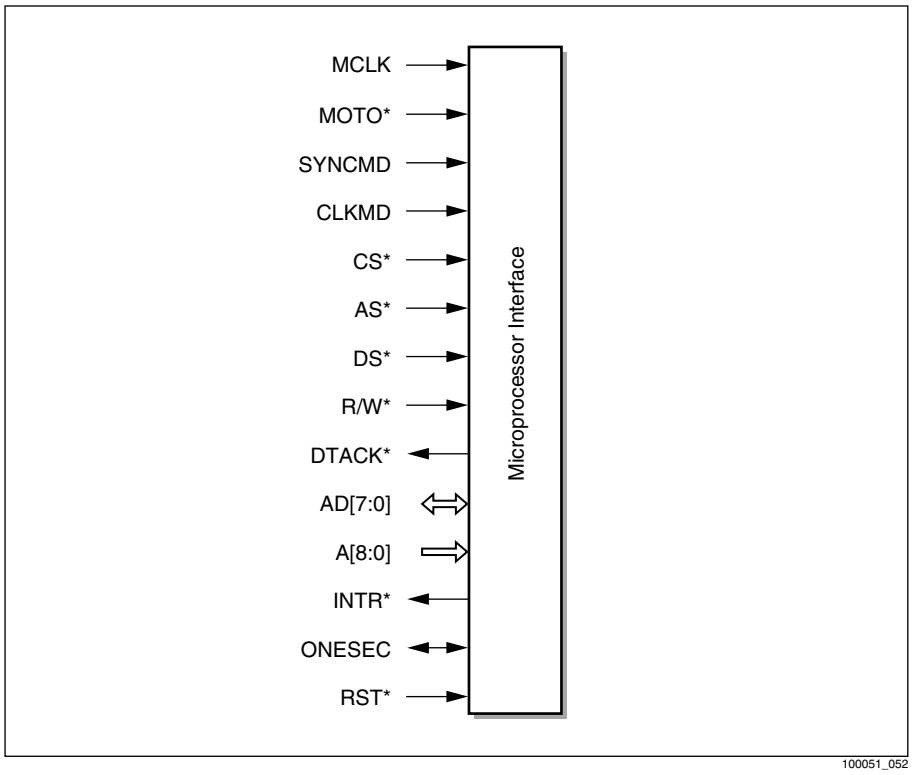
In any window of 17 consecutive primary rate cycles, the maximum variation in pulse amplitude in the absence of 60 Hz variations is <200 mV. The maximum variation in pulse width at half amplitude is <20 ns.

2.10 Microprocessor Interface

The Microprocessor Interface (MPU) provides the capability to configure the Bt8370, read status registers and counters, and respond to interrupts (see Figure 2-48). The interface supports both the Intel 8051 and Motorola 68000-type processors. In the Intel mode, the address and data are multiplexed; in the Motorola mode, the address and data are separate pins. Both synchronous and asynchronous read/write modes are supported. The synchronous mode is optimized for Motorola 68000-type processors with a maximum clock rate of 36 MHz. The asynchronous mode runs internally at 32 MHz, which limits the processor speed to 16 MHz for 8051 processors, and 30 MHz for 68302 processors.

The microprocessor interface consists of the following pins: MCLK, MOTO*, SYNCMD, CS*, AS*, DS*, R/W*, DTACK*, AD[7:0], A[8:0], INTR*, CLKMD, ONESEC, RST*. (A detailed description of the MPU pins is provided in Table 1-1.)

Figure 2-48. Microprocessor Interface Block Diagram



2.10.1 Address/Data Bus

In Non-multiplexed Address mode, A[8:0] provides the address for register access; in Multiplexed Address mode, A[8] and AD[7:0] provide the address. In both modes, the data bytes flow over the shared bidirectional, byte-wide bus, AD[7:0].

2.10.2 Bus Control Signals

Four signals control the operation of the interface port: AS*, CS*, RD*, and R/W*. An additional pin, MOTO*, selects whether the interface signals are of a Motorola or Intel flavor.

When MOTO* is low, indicating a Motorola-style interface, CS*, AS*, R/W*, and DS* signals are expected. When MOTO* is high, indicating an Intel-style interface, CS*, ALE, RD*, and WR* signals are expected.

When MOTO* is high, the address lines are multiplexed with the data. This pin is usually tied high for Intel devices and low for Motorola devices. SYNCMD puts the interface into the Synchronous Processor Interface mode. Motorola 68000 processors typically have SYNCMD tied high if MCLK is connected to the MPU clock source, while Intel 8051 processors have SYNCMD tied low (see Table 2-23).

Table 2-23. Microprocessor Interface Operating Modes

MOTO*	SYNCMD	CLKMD	Description
0	0	0	Asynchronous Motorola, internal clock
0	1	1	Synchronous Motorola, external clock
1	0	0	Asynchronous Intel, internal clock
1	1	1	Synchronous Intel, external clock

2.10.3 Interrupt Requests

The INTR* output is an active-low, open-drain type output which allows the interrupt request line from multiple devices to connect to a common microprocessor interrupt request line. All Bt8370/75/76 interrupts are requested on this pin. However, each interrupt source can be individually enabled or disabled.

Interrupts are associated with three types of microprocessor interface registers:

1. Interrupt Enable register—a 1 in a given bit of IER[7:0] enables the corresponding interrupt, a 0 (initial condition) disables it.
2. Interrupt Status register [ISR; 7:0]—events are latched into these registers whether the corresponding interrupt enable bit is set or not. The processor must read the ISR registers to clear all latched bits.
3. Interrupt Request register [IRR; addr 003]—reading this register along with the corresponding ISR register, the microprocessor can determine the cause of an interrupt. Active interrupts are indicated by bits that are high. Inactive interrupts are indicated by bits that are low. Reading from the IRR clears the entire register; writing has no effect.

2.10.4 Device Reset

The Bt8370/75/76 contains three reset methods: internal power-on reset (POR), hardware reset which uses the RST* pin, and software reset which uses the RESET bit in register CR0 [addr 001]. All three methods result in device outputs placed in a high-impedance state and configuration registers set to default values as shown in Table 3-1. In all reset methods, both REFCLK and MCLK (internal or external) must be present during the reset process for proper operation. MCLK (internal or external) performs the actual register initialization. Therefore, if the CLKMD pin is connected high to enable external MCLK, the external MCLK must be applied during reset, and if the CLKMD pin is low during reset, the internal clock (33 MHz) is used.

After hardware reset, software reset, or internal power-on reset, the microprocessor must initialize Bt8370/75/76 control registers and buffer memory registers to the desired state.

2.10.4.1 Power-On Reset (POR)

An internal POR process is initiated during power-up. When VDD has reached approximately 3 V, the internal reset process begins and continues for 2048 REFCLK cycles (approximately 205 µs) if REFCLK is applied. If REFCLK is not present, the Bt8370/75/76 remains in the reset state and does not terminate until detecting 2048 REFCLK cycles have been detected. The RESET bit in register CR0 [addr 001] can be monitored to determine when POR is complete. MCLK (internal or external) must be present during the POR concurrent with REFCLK to allow register initialization.

The LOOP register [addr 014] is not reset during power-on reset or internal reset so the device may occasionally power-on in a loopback state. If this occurs, several other registers (e.g., several IER registers) may not properly reset to their default values. To avoid this, after power-on or hardware reset, write the Loop register to 0 and then initiate a software reset using the RESET bit in the Primary Control register [CR0; addr 001]. After this procedure, all default registers have their default values. XOE needs to be disabled during the power-on reset period and re-enabled after configuring the part. The device must not be in Framer Loopback State when the software reset is written.

2.10.4.2 Hardware Reset

A hardware reset is initiated by bringing the RST* pin active (low) for a minimum of 4 µs. If CLKMD is high (using external MCLK), external MCLK must be present while RST* is low to allow register initialization. After RST* is deactivated, the internal reset process continues for 5 µs, and register access must be avoided. The RESET bit in register CR0 [addr 001] can be monitored to determine when the reset process is complete.

2.10.4.3 Software Reset

A software reset is initiated by writing the RESET bit [register CR0; addr 001] to 0, delaying at least 6 µs, then writing RESET to 1. Once initiated, the reset process continues for 15 µs maximum and register access must be avoided. The RESET bit can be monitored to determine when the reset process has completed. As with the other reset methods, both REFCLK and MCLK (internal or external) must be present during the reset process.

2.11 Loopbacks

The Bt8370/75/76 provides a complete set of loopbacks for diagnostics, maintenance, and troubleshooting.

2.11.1 Remote Line Loopback

The remote line loopback loops the RCVR inputs to the XMTR outputs. The loopback provides BPV transparency and the ability to override the looped data with AIS. The RCVR data path is not affected by the activation of this loopback. Remote line loopback is activated by setting the Remote Line Loopback (LLOOP) bit in the Loopback Configuration register [LOOP; addr 014]. It is possible to operate the remote line loopback simultaneously with the local framer loopback. If receive jitter attenuator is also enabled, RJAT is placed in the line loopback path. TJAT, if enabled, is not present in the line loopback path.

2.11.2 Remote Payload Loopback

The remote payload loopback loops all DS0 channels from the RCVR input to the XMTR output. Loopback payload retains time slot integrity, such that numbered time slots from each receive frame are transferred to the same numbered time slots in the transmit frame. Transmit overhead bits—F bits in T1 mode or TS0 in E1 mode—are supplied by the transmit frame formatter or by the TSB, depending on TFRM [addr 072] settings. Existing transmit frame alignment and clock timing are not altered by [PLOOP; addr 014] activation or deactivation, allowing system operation with independent receive and transmit timing. Controlled frame slips are performed in the payload loopback path if receive and transmit clocks are asynchronous, although these slips are not reported to the processor as slip buffer errors. Multiframe integrity is not maintained during PLOOP; therefore, DS0 and signaling channel loopbacks [TPCn; addr 100–11F] must be used to implement payload loopback if transparent or forced signaling is desired. PLOOP does not override by transmit per-channel remote loopback selection (TLOOP bit in TPCn).

2.11.3 Remote Per-Channel Loopback

The remote per-channel loopback loops the RCVR input DS0 channel to the XMTR output DS0 channel. The remote per-channel loopback is activated by setting TLOOP in the Transmit Per-Channel Control register [TPC0 to TPC31; addr 100 to 11F].

2.11.4 Local Analog Loopback

RLIU provides a local analog loopback to internally route bipolar data from XTIP/XRING to RTIP/RRING. In the local analog loopback mode, externally applied data on RTIP/RRING inputs is ignored, and XTIP/XRING output data is unaffected. The local analog loopback is configured using the ALOOP bit in the Loopback Configuration register [LOOP; addr 014]. If RCKO is selected as the TCKI clock source [CMUX; addr 01A], an alternate transmit clock source must be provided when this loopback is activated. Possible configurations include selecting the TCKI pin or CLADO as the transmit clock source, or programming the JAT in the transmit direction and setting JFREE to enable the free-running 10 MHz reference [JAT_CR register; addr 002]. After activating or deactivating this loopback, the RLIU must be reset using RST_LIU in the LIU Configuration register [LIU_CR; addr 020]. The transmitter outputs must connect to a cable termination or a transmit termination resistor for local analog loopback to pass bipolar signals. If no cable and no resistor termination are supplied, then ALOOP cannot pass bipolar signals to RTIP/RRING.

2.11.5 Local Framer Loopback

The local framer loopback loops the transmit line encoder outputs to the receive line encoder inputs. The TLIU output is not affected by the activation of this loopback. The local framer loopback is activated by setting the Local Framer Loopback (FLOOP) bit in the Loopback Configuration register [LOOP; addr 014]. If RCKO is selected as the TCKI clock source [CMUX; addr 01A], then an alternate transmit clock source must be provided when this loopback is activated. Possible configurations include selecting the TCKI pin or CLADO as the transmit clock source, or programming the JAT in the transmit direction and setting JFREE to enable the free running 10 MHz reference [JAT_CR register; addr 002]. It is possible to operate the local framer loopback simultaneously with the remote line loopback. If transmit jitter attenuator is also enabled, TJAT is placed in the framer loopback path. RJAT, if enabled, is not present in the framer loopback path.

2.11.6 Local Per-Channel Loopback

The local per-channel loopback loops the TSB PCM and signaling inputs to the RSB PCM and signaling outputs on a per-channel basis. The local per-channel PCM loopback is activated by setting RLOOP in the System Bus Per-Channel Control registers [SBC0 to SBC31; addr 0E0 to 0FF]. The local per-channel signaling loopback is activated by setting SIG_LP in System Bus Per-Channel Control registers.

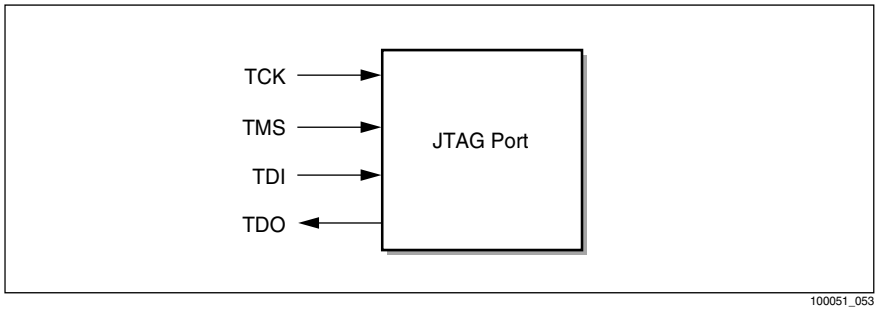
2.12 Joint Test Access Group

The Bt8370/75/76 incorporates printed circuit board testability circuits in compliance with IEEE Std. P1149.1a–1993, *IEEE Standard Test Access Port and Boundary–Scan Architecture*, commonly known as JTAG (Joint Test Action Group).

The JTAG includes a Test Access Port (TAP) and several data registers. The TAP provides a standard interface through which instructions and test data are communicated (see Figure 2-49). A Boundary Scan Description Language (BSDL) file for the Bt8370/75/76 is available from the factory upon request.

The test access port consists of the TDI, TCK, TMS, and TDO pins. An internal power-on reset circuit resets the JTAG port.

Figure 2-49. JTAG Diagram



2.12.1 Instructions

In addition to the required BYPASS, SAMPLE/PRELOAD, and EXTEST instructions, IDCODE instruction is supported. There are also two private instructions. Table 2-24 lists the JTAG instructions and their codes.

Table 2-24. JTAG Instructions

Instruction	Code
BYPASS	111 111
SAMPLE/PRELOAD	000 001
EXTEST	000 000
IDCODE	000 010
Private	xxx xxx
Private	xxx xxx

2.12.2 Device Identification Register

The JTAG ID register consists of a 4-bit version, a 16-bit part number, and an 11-bit manufacturer number (see Tables 2-25 through 2-27).

Table 2-25. Bt8370/75/76 Device Identification JTAG Register

Version[1]	Part Number	Manufacturer ID	
1 0 0 1	1 0 0 0 0 0 1 1 0 1 1 1 0 0 0 0	0 0 0 1 1 0 1 0 1 1 0 1	TDO
0x9	0x8370	0x0D6	
4 bits	16 bits	11 bits	

FOOTNOTE:
(1) Consult factory for current version number.

Table 2-26. Bt8375 Device Identification JTAG Register

Version[1]	Part Number	Manufacturer ID	
1 0 0 1	1 0 0 0 0 0 1 1 0 1 1 1 0 1 0 1	0 0 0 1 1 0 1 0 1 1 0 1	TDO
0x9	0x8375	0x0D6	
4 bits	16 bits	11 bits	

FOOTNOTE:
(1) Consult factory for current version number.

Table 2-27. Bt8376 Device Identification JTAG Register

Version[1]	Part Number	Manufacturer ID	
1 0 0 1	1 0 0 0 0 0 1 1 0 1 1 1 0 1 1 0	0 0 0 1 1 0 1 0 1 1 0 1	TDO
0x9	0x8376	0x0D6	
4 bits	16 bits	11 bits	

FOOTNOTE:
(1) Consult factory for current version number.