



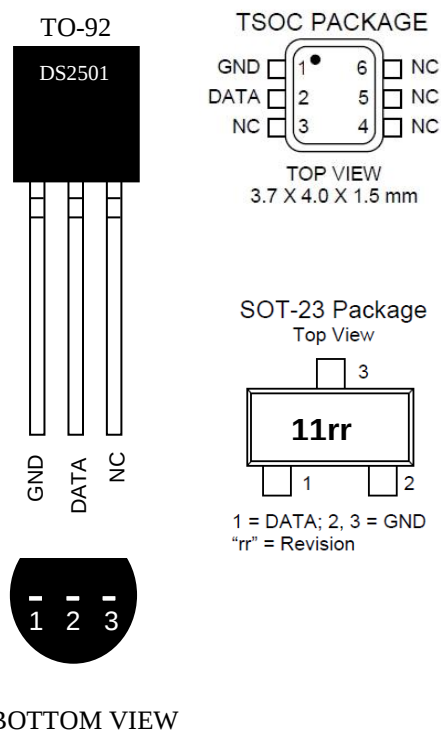
DS2501

512-Bit Add-Only Memory

FEATURES

- 512 bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- EPROM partitioned into two 256-bit pages for randomly accessing packetized data
- Each memory page can be permanently write-protected to prevent tampering
- Device is an “add-only” memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3 kbps
- 8-bit family code specifies DS2501 communications requirements to reader
- Presence detector acknowledges when the reader first applies voltage
- Low cost TO-92, TSOC, or SOT-23 package
- Reads over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C; programs at 11.5V to 12.0V from -40°C to +50°C

PIN ASSIGNMENT



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2501+T&R	-40°C to +85°C	3 TO-92 (2K)
DS2501P+	-40°C to +85°C	6 TSOC
DS2501P+T&R	-40°C to +85°C	6 TSOC (4K)
DS2501R+T&R	-40°C to +85°C	3 SOT23 (3K)

Note: The leads of TO-92 packages on tape and reel are formed to approximately 100-mil (2.54mm) spacing. For details see the Package Information section.

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

SILICON LABEL DESCRIPTION

The DS2501 512-bit add-only memory identifies and stores relevant information about the product to which it is associated. This lot- or product-specific information can be accessed with minimal interface—for example, a single port pin of a microcontroller. The DS2501 consists of a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit family code (11h) plus 512 bits of EPROM that is user-programmable. The power to program and read the DS2501 is derived entirely from the 1-Wire[®] communication line.

Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write-protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a stand-alone database. The 48-bit serial number that is factory-lasered into each DS2501 provides a guaranteed unique identity which allows for absolute traceability. Typical applications include storage of calibration constants, product attribute identification, asset tracking, product revision status, and access codes.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2501. The DS2501 has three main data components: 1) 64-bit lasered ROM, 2) 512-bit EPROM, and 3) EPROM Status Bytes. The device derives its power for read operations entirely from the 1-Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this “parasite” power source during the low times of the 1-Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1-Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1-Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1-Wire line a special high voltage detect circuit within the DS2501 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64-bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1-Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 10. After a ROM Function Command is successfully executed, the memory functions that operate on the EPROM portions of the DS2501 become accessible and the bus master may issue any one of the five Memory Function Commands specific to the DS2501 to read or program the various data fields. The protocol for these Memory Function Commands is described in Figure 5. All data is read and written least significant bit first.

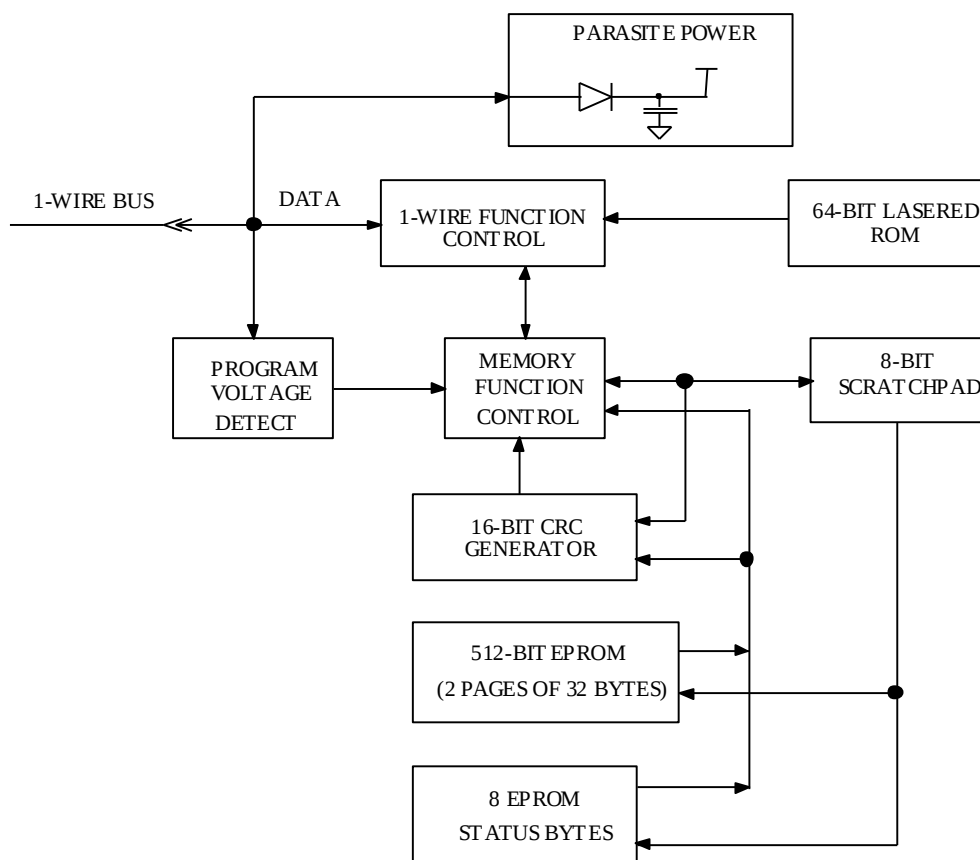
64-BIT LASERED ROM

Each DS2501 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3). The 64-bit ROM and ROM Function Control section allow the DS2501 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section “1-Wire Bus System.” The memory functions required to read and program the EPROM sections of the DS2501 are not accessible until the ROM function

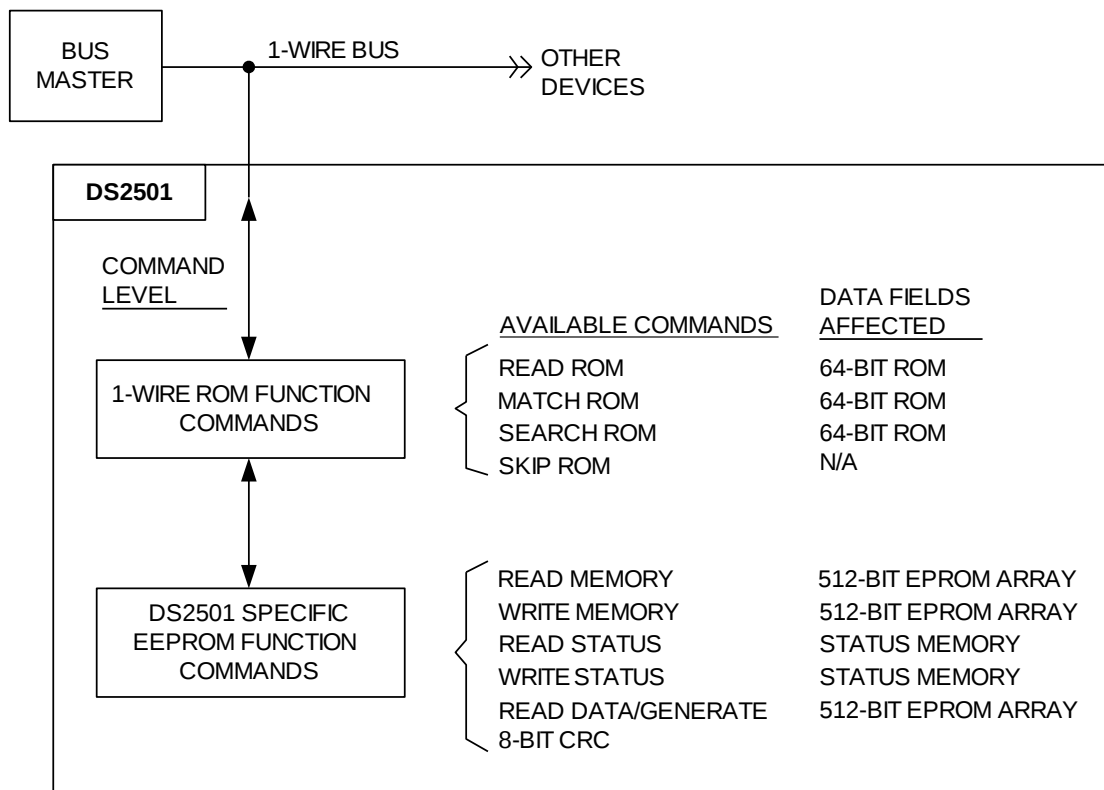
protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 9). The 1-Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, or 4) Skip ROM. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS2501 (Figure 6).

The 1-Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Figure 4 shows a hardware implementation of this CRC generator. Additional information about the Maxim 1-Wire Cyclic Redundancy Check is available from Application Note 27. The shift register acting as the CRC accumulator is initialized to 0. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

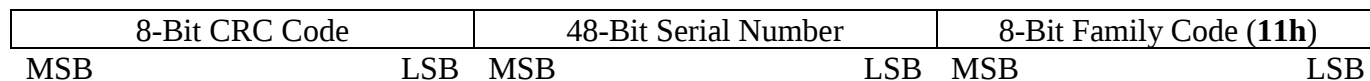
DS2501 BLOCK DIAGRAM Figure 1



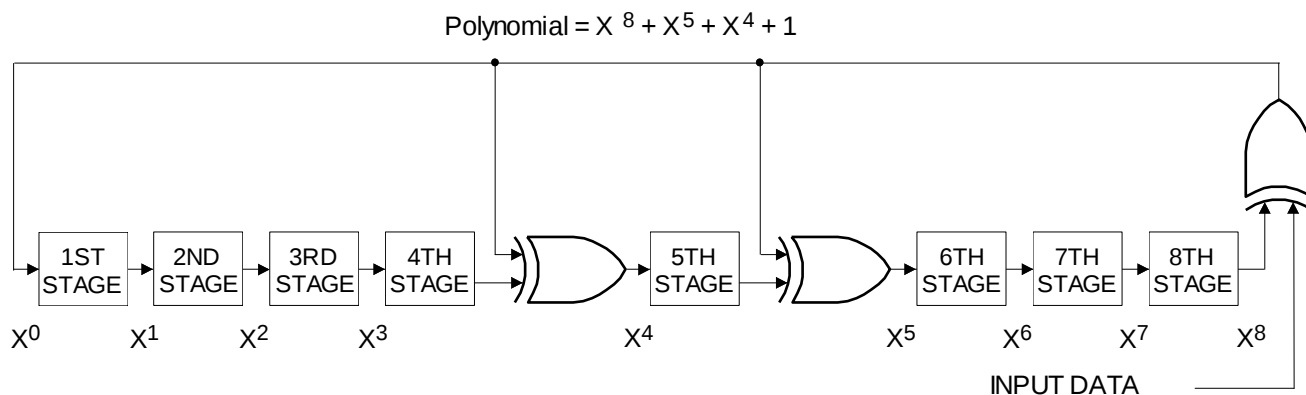
HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



512-Bit EPROM

The memory map in Figure 5 shows the 512-bit EPROM section of the DS2501 which is configured as two pages of 32 bytes each. The 8-bit scratchpad is an additional register that acts as a buffer when programming the memory. Data is first written to the scratchpad and then verified by reading an 8-bit CRC from the DS2501 that confirms proper receipt of the data. If the buffer contents are correct, a programming voltage should be applied and the byte of data will be written into the selected address in memory. This process ensures data integrity when programming the memory. The details for reading and programming the 512-bit EPROM portion of the DS2501 are given in the Memory Function Commands section.

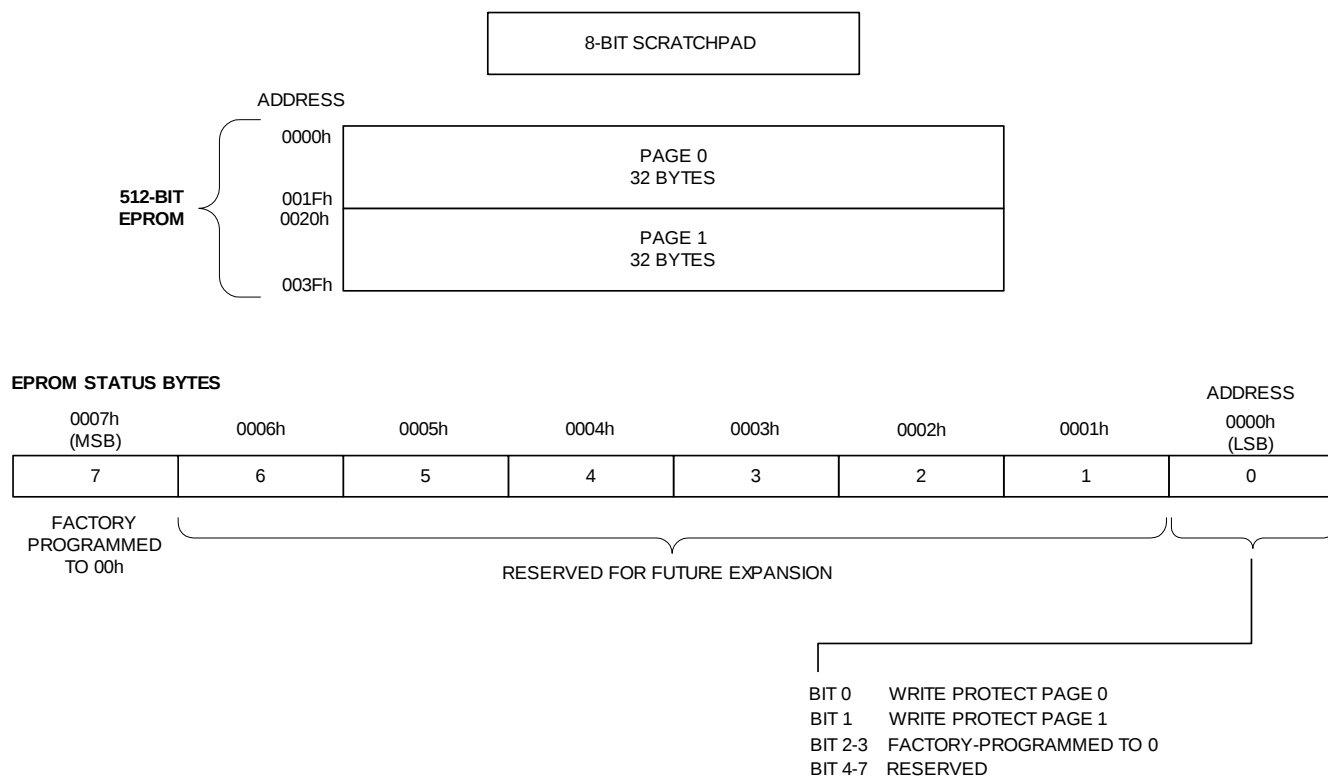
EPROM STATUS BYTES

In addition to the 512 bits of data memory the DS2501 Status Memory accessible with separate commands. While the Status Memory is comprised of 8 EPROM bytes, only 1 byte (address 0000h) is used. The first byte of the EPROM Status Memory contains the Write Protect Page bits which inhibit programming of the corresponding page in the 512-bit main memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page byte, the entire 32-byte page that corresponds to that bit can no longer be altered but may still be read.

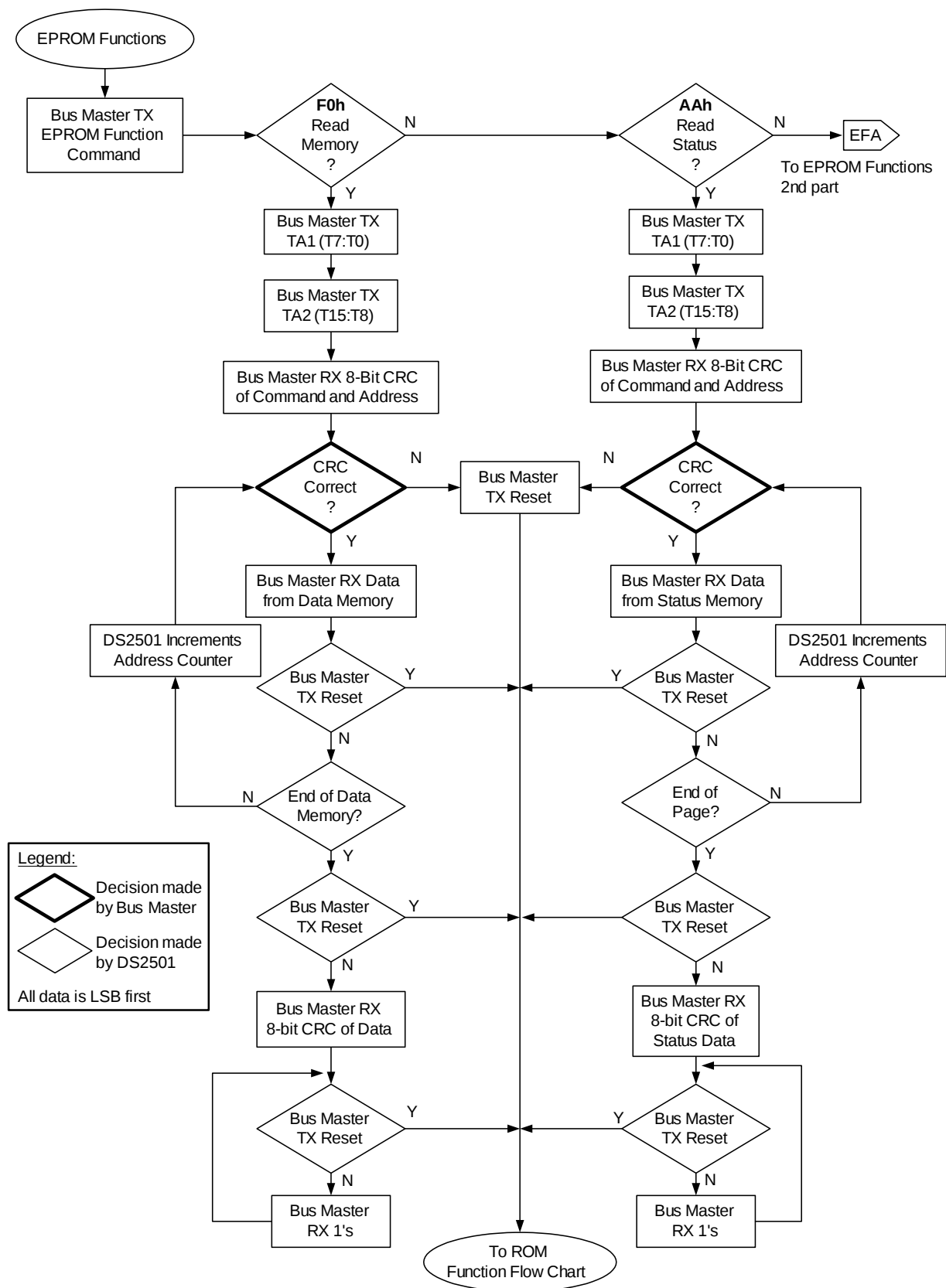
MEMORY FUNCTION COMMANDS

The “Memory Function Flow Chart” (Figure 6) describes the protocols necessary for accessing the various data fields within the DS2501. The Memory Function Control section, 8-bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A 3-byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field. The command byte indicates if the device is to be read or written. Writing data involves not only issuing the correct command sequence by also providing a 12-volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS2501 and received back by the bus master are sent least significant bit first.

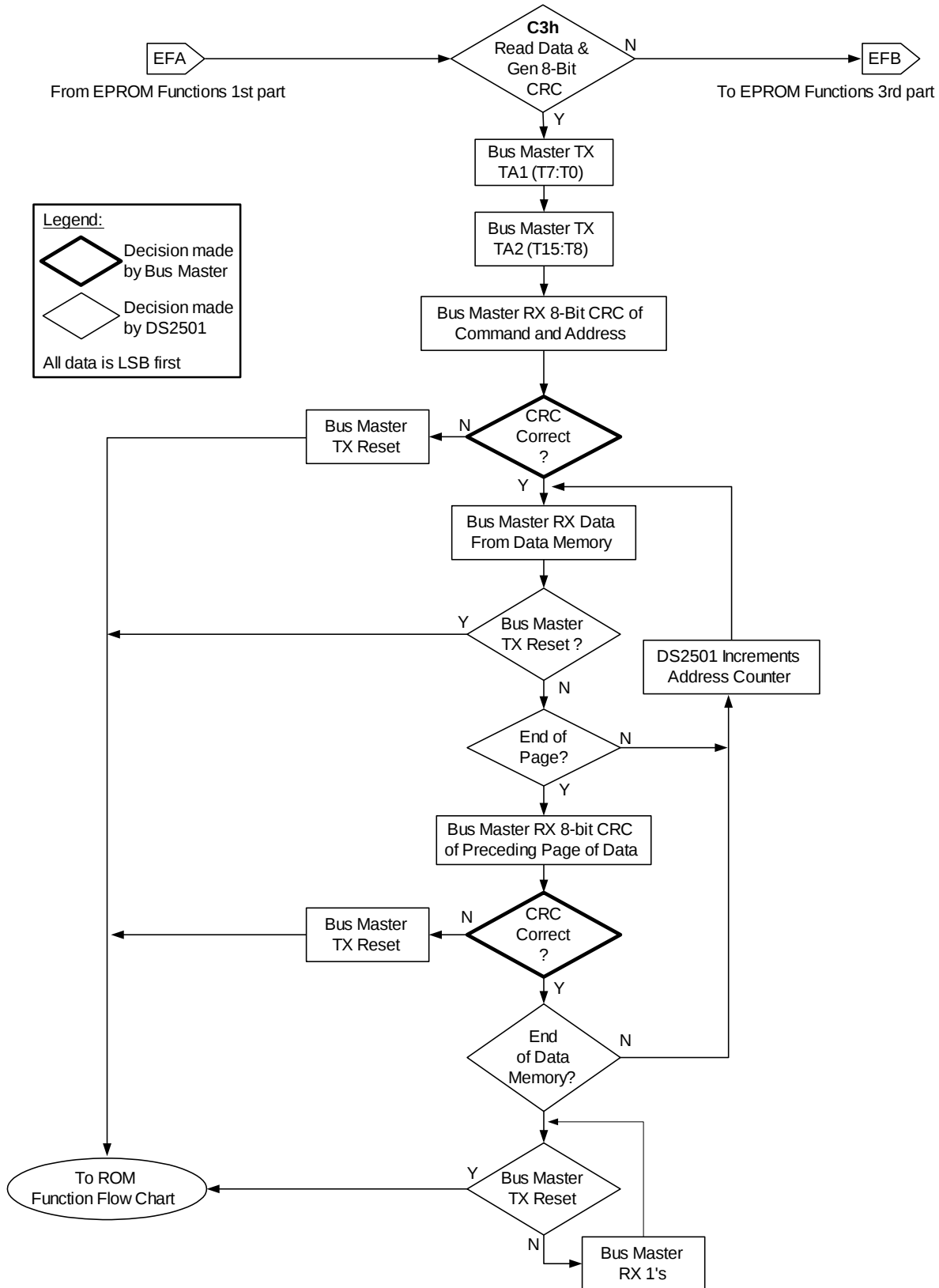
DS2501 MEMORY MAP Figure 5



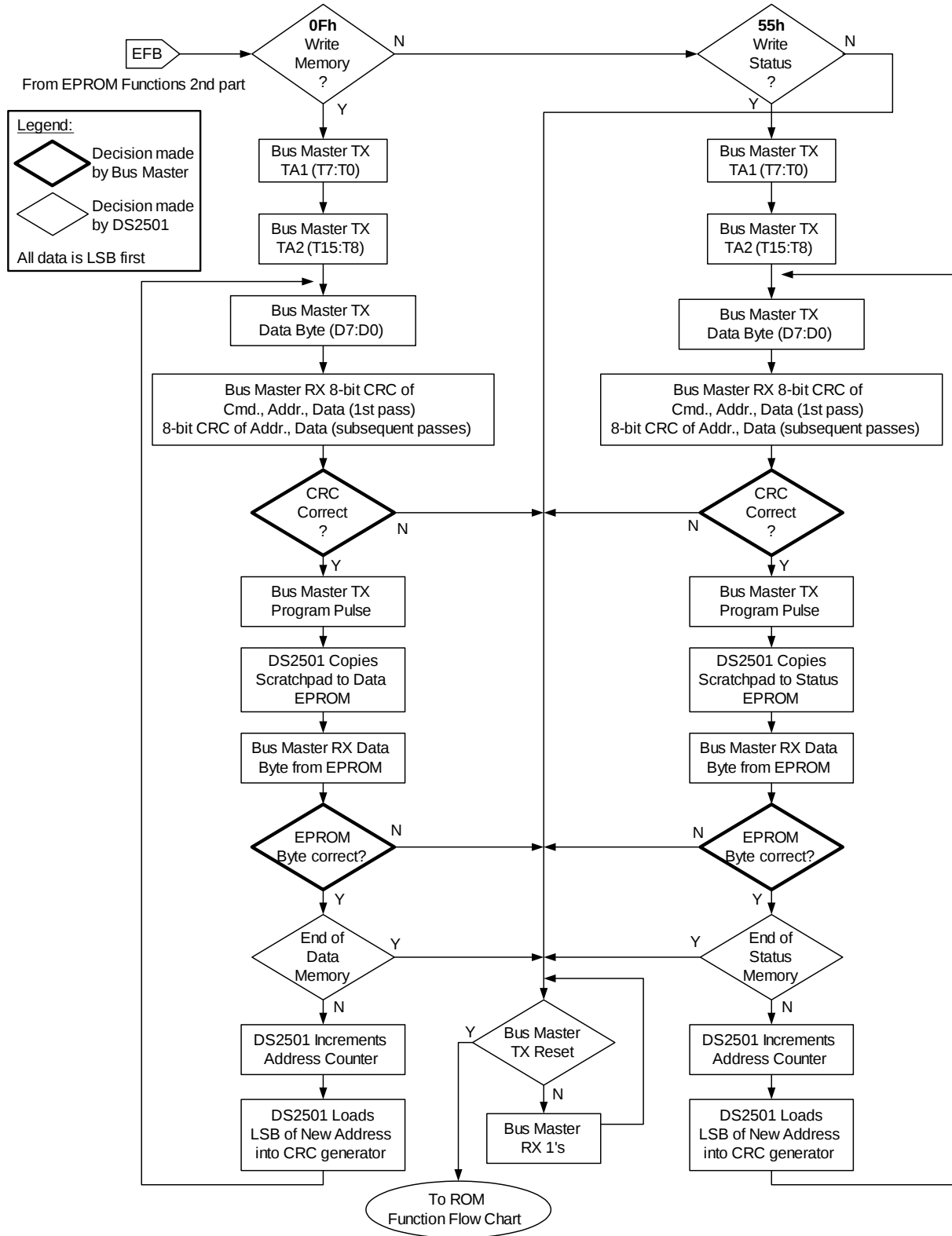
MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION FLOW CHART Figure 6 (continued)



MEMORY FUNCTION FLOW CHART Figure 6 (continued)



READ MEMORY [F0H]

The Read Memory command is used to read data from the 512-bit EPROM data field. The bus master follows the command byte with a 2-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8-bit CRC of the command byte and address bytes is computed by the DS2501 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2501 starting at the initial address and continuing until the end of the 512-bit data field is reached or until a reset pulse is issued. If reading occurs through the end of memory space, the bus master may issue eight additional read time slots and the DS2501 will respond with a 8-bit CRC of all data bytes read from the initial starting byte through the last byte of memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a reset pulse is issued. Any reads ended by a reset pulse prior to reaching the end of memory will not have the 8-bit CRC available.

Typically a 16-bit CRC would be stored with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. If CRC values are imbedded within the data, a reset pulse may be issued at the end of memory space during a Read Memory command.

READ STATUS [AAH]

The Read Status command is used to read data from the EPROM Status data field. The bus master follows the command byte with a 2-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8-bit CRC of the command byte and address bytes is computed by the DS2501 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2501 starting at the supplied address and continuing until the end of the EPROM Status data field is reached. At that point the bus master will receive an 8-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte through the final factory-programmed byte that contains the 00h value.

This feature is provided since the EPROM Status information may change over time making it impossible to program the data once and include an accompanying CRC that will always be valid. Therefore, the Read Status command supplies a 8-bit CRC that is based on and always is consistent with the current data stored in the EPROM Status data field.

After the 8-bit CRC is read, the bus master will receive logical 1s from the DS2501 until a reset pulse is issued. The Read Status command sequence can be ended at any point by issuing a reset pulse.

READ DATA/GENERATE 8-BIT CRC [C3H]

The Read Data/Generate 8-bit CRC command is used to read data from the 512-bit EPROM data field. The bus master follows the command byte with a 2-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. An 8-bit CRC of the command byte and address bytes is computed by the DS2501 and read back by the bus master to confirm that the correct command word and starting address were received. If the CRC read by the bus master is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2501 starting at the initial address and continuing until the end of a 32-byte page is reached. At that point the bus master will send

eight additional read time slots and receive an 8-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page. Once the 8-bit CRC has been received, data is again read from the 512-bit EPROM data field starting at the next page. This sequence will continue until the final page and its accompanying CRC are read by the bus master. Thus each page of data can be considered to be 33 bytes long: the 32 bytes of user-programmed EPROM data and an 8-bit CRC that gets generated automatically at the end of each page.

This type of read differs from the Read Memory command which simply reads each page until the end of address space is reached. The Read Memory command only generates an 8-bit CRC at the end of memory space that often might be ignored, since in many applications the user would store a 16-bit CRC with the data itself in each page of the 512-bit EPROM data field at the time the page was programmed.

The Read Data/Generate 8-bit CRC command provides an alternate read capability for applications that are “bit-oriented” rather than “page-oriented” where the 512-bit EPROM information may change over time within a page boundary making it impossible to program the page once and include an accompanying CRC that will always be valid. Therefore, the Read Data/Generate 8-bit CRC command concludes each page with the DS2501 generating and supplying an 8-bit CRC that is based on and therefore is always consistent with the current data stored in each page of the 512-bit EPROM data field. After the 8-bit CRC of the last page is read, the bus master will receive logical 1s from the DS2501 until a reset pulse is issued. The Read Data/Generate 8-Bit CRC command sequence can be exited at any point by issuing a reset pulse.

WRITE MEMORY [0FH]

The Write Memory command is used to program the 512-bit EPROM data field. The bus master will follow the command byte with a 2-byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). An 8-bit CRC of the command byte, address bytes, and data byte is computed by the DS2501 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

The highest starting address within the DS2501 is 003FH. If the bus master sends a starting address higher than this, the nine most significant address bits are set to 0 by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2501 and the CRC calculated by the bus master, indicating an error condition.

If the CRC read by the bus master is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12V on the 1-Wire bus for 480µs) is issued by the bus master. Prior to programming, the entire unprogrammed 512-bit EPROM data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the 512-bit EPROM will be programmed to a logical 0 after the programming pulse has been applied at that byte location.

After the 480µs programming pulse is applied and the data line returns to a 5V level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2501 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM data address. If the EPROM data byte contains 1s in bit positions where the byte issued by the master contains 0s, a reset pulse should be issued and the current byte address should be programmed again. If the DS2501 EPROM data byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2501 will automatically increment its address counter to select the next byte in the 512-bit EPROM data field. The least

significant byte (LSB) of the new two-byte address will also be loaded into the 8-bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2501 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address; the result is an 8-bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the bus master will read this 8-bit CRC from the DS2501 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a reset pulse must be issued and the Write Memory command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Memory flow chart will generate an 8-bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the Write Memory flow chart due to the DS2501 automatically incrementing its address counter will generate an 8-bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2501) is made entirely by the bus master, since the DS2501 will not be able to determine if the 8-bit CRC calculated by the bus master agrees with the 8-bit CRC calculated by the DS2501. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2501. Also note that the DS2501 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Memory command, incorrect programming could occur within the DS2501. The Write Memory command sequence can be exited at any point by issuing a reset pulse.

WRITE STATUS [55H]

The Write Status command is used to program the EPROM status data field. The bus master will follow the command byte with a 2-byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of status data (D7:D0). An 8-bit CRC of the command byte, address bytes, and data byte is computed by the DS2501 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12V on the 1-Wire bus for 480µs) is issued by the bus master. Prior to programming, the first 7 bytes of the EPROM Status data field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM Status data field will be programmed to a logical 0 after the programming pulse has been applied at the byte location. The 8th byte of the EPROM Status Byte data field is factory-programmed to contain 00h.

After the 480µs programming pulse is applied and the data line returns to a 5V level, the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2501 responds with the data from the selected EPROM Status address sent least significant bit first. This byte contains the logical AND of all bytes written to this EPROM Status Byte address. If the EPROM Status Byte contains 1s in bit positions where the byte issued by the master contained 0s, a reset pulse should be issued and the current byte address should be programmed again. If the DS2501 EPROM Status Byte

contains 0s in the same bit positions as the data byte, the programming was successful and the DS2501 will automatically increment its address counter to select the next byte in the EPROM Status data field. The least significant byte of the new 2-byte address will also be loaded into the 8-bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2501 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8-bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the bus master will read this 8-bit CRC from the DS2501 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a reset pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the Write Status flow chart will generate an 8-bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the 2 address bytes, and finally the data byte. Subsequent passes through the Write Status flow chart due to the DS2501 automatically incrementing its address counter will generate an 8-bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2501) is made entirely by the bus master, since the DS2501 will not be able to determine if the 8-bit CRC calculated by the bus master agrees with the 8-bit CRC calculated by the DS2501. If an incorrect CRC is ignored and a program pulse is applied by the bus master, incorrect programming could occur within the DS2501. Also note that the DS2501 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the Write Status command, incorrect programming could occur within the DS2501. The Write Status command sequence can be ended at any point by issuing a reset pulse.

1-WIRE BUS SYSTEM

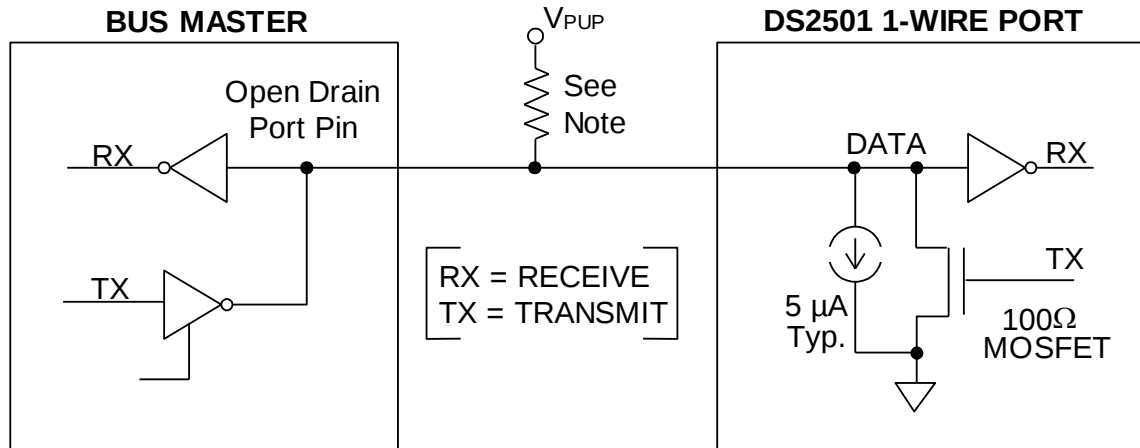
The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2501 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2501 is open drain with an internal circuit equivalent to that shown in Figure 7. Typical configurations of discrete bus master interfaces for EPROM programming are shown in Figure 8. As shown in Figure 9, the bus master interface, including +12V EPROM programming capability, can be significantly simplified by using the Maxim DS2480B.

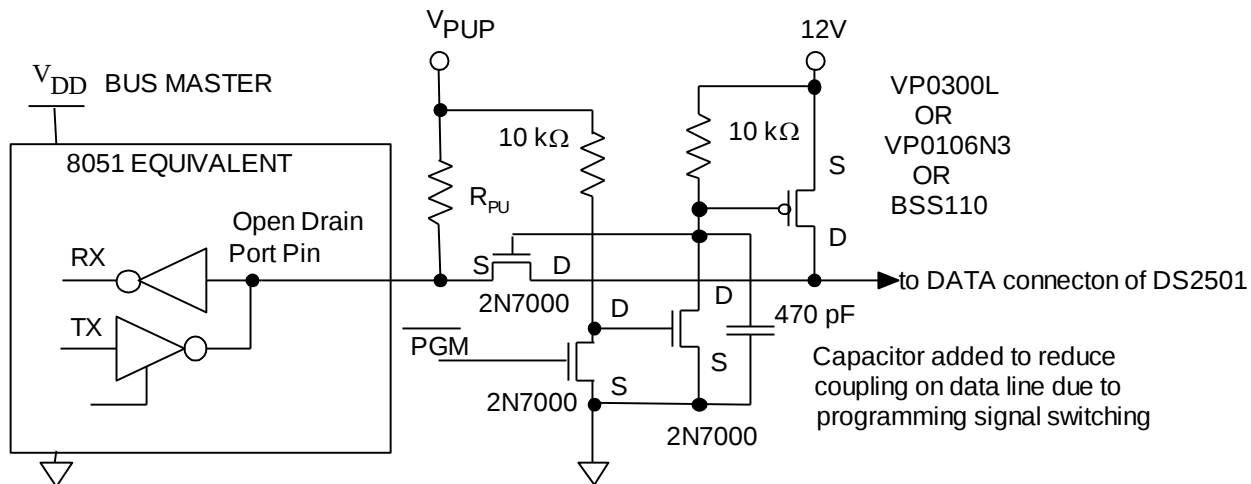
A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. If the bus master is also required to perform programming of the EPROM portions of the DS2501, a programming supply capable of delivering up to 10mA at 12V for 480 μ s is required. The 1-Wire bus requires a pull-up resistor with a value that depends on bus load characteristics, the optimal pull-up resistor value will be in the 1.5k Ω to 5k Ω range.

1-WIRE BUS CONFIGURATION Figure 7



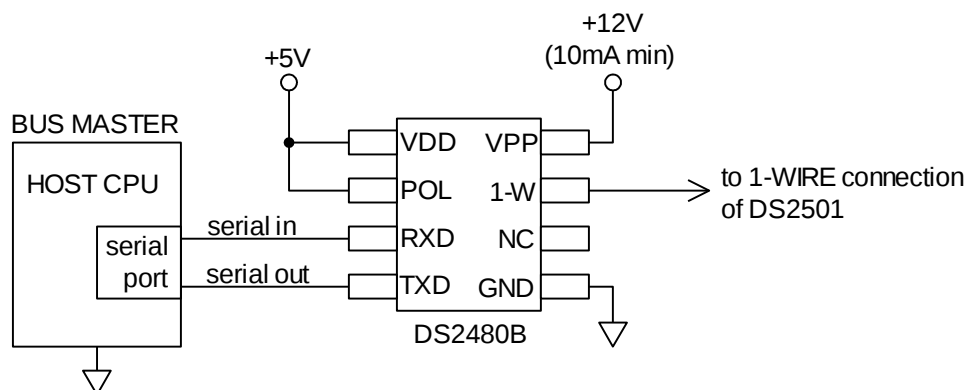
Note: Depending on 1-Wire communication speed, regular or overdrive, and bus load characteristics, the optimal pull-up resistor value will be in the 1.5k Ω to 5k Ω range.

DISCRETE BUS MASTER DRIVER CIRCUIT Figure 8



The interface is reduced to the R_{PU} pull-up resistor if one does not intend to program the EPROM cells. R_{PU} will be in the 1.5K to 5K range depending on bus load characteristics

BUS MASTER WITH DS2480B DRIVER Figure 9



Transaction Sequence

The sequence for accessing the DS2501 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read/Write Memory/Status

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s). Note: At power-up from a cold start, the 1-Wire bus has been low for longer than $t_{RSTLMAX}$. Therefore, the master must issue an initialization sequence to begin communication.

The presence pulse lets the bus master know that the DS2501 is on the bus and is ready to operate. For more details, see the “1-Wire Signaling” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 11):

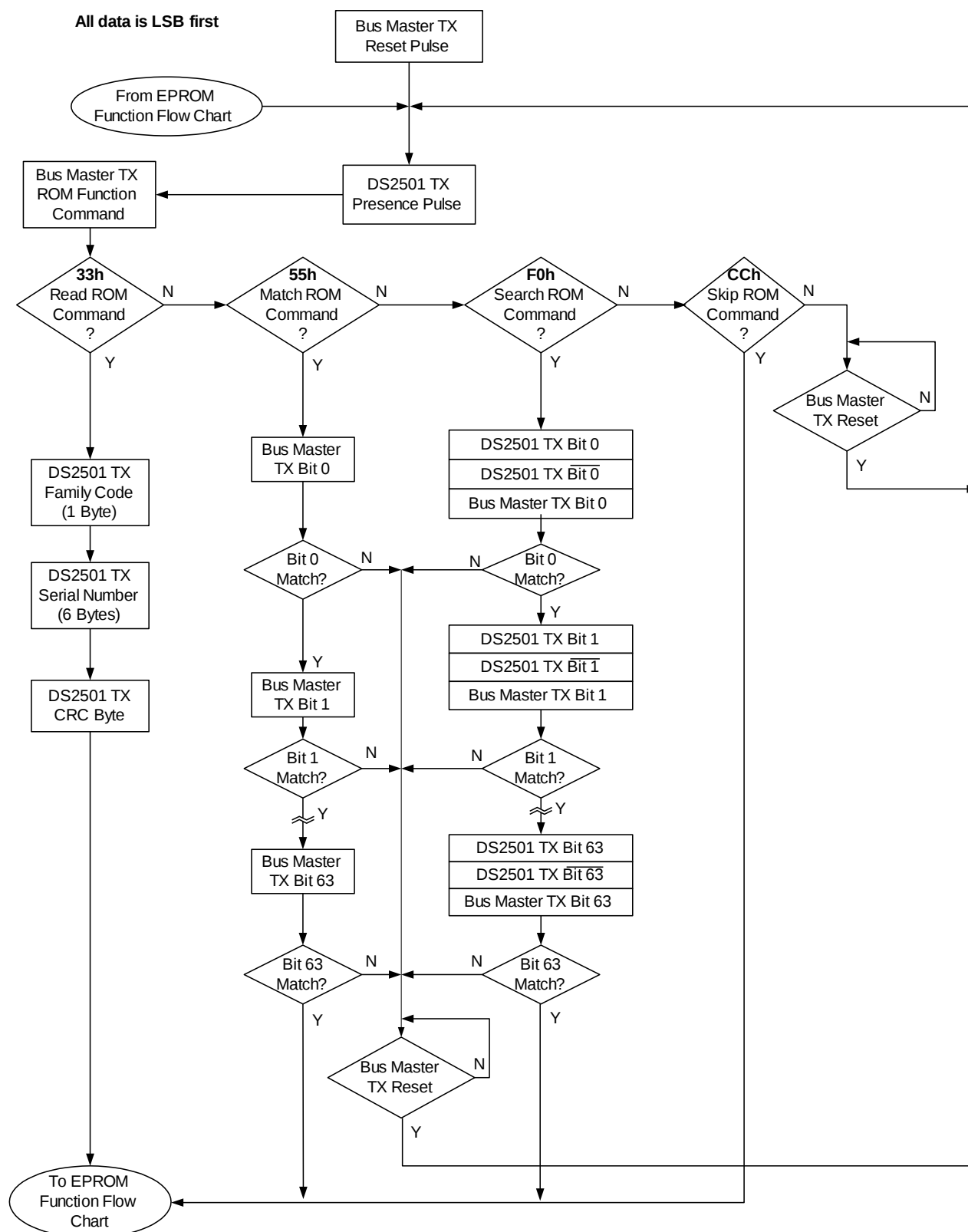
Read ROM [33H]

This command allows the bus master to read the DS2501's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can be used only if there is a single DS2501 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55H]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2501 on a multidrop bus. Only the DS2501 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

ROM FUNCTIONS FLOW CHART Figure 10



Skip ROM [CCH]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open-drain pulldowns will produce a wired-AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple, three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

1-Wire Signaling

The DS2501 requires strict protocols to ensure data integrity. The protocol consists of five types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data, and Program Pulse. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS2501 is shown in Figure 11. A Reset Pulse followed by a Presence Pulse indicates the DS2501 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL} , minimum 480 μ s, maximum 960 μ s). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2501 waits (t_{PDH} , 15 μ s to 60 μ s) and then transmits the presence pulse (t_{PDL} , 60 μ s to 240 μ s).

Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 12. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2501 to the master by triggering a delay circuit in the DS2501. During write time slots, the delay circuit determines when the DS2501 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the DS2501 will hold the data line low overriding the “1” generated by the master. If the data bit is a 1, the device will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8-bit scratchpad to the 512-bit EPROM Memory or Status Memory, a program pulse of 12V is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pullup resistor to a state where the data line is actively driven to a programming voltage of 12V providing a minimum of 1mA of current to the DS2501. This programming voltage (Figure 13) should be applied for 480 μ s, after which the bus master returns the data line to an idle high state controlled by the pullup resistor. Note that due to the high-voltage programming requirements for any 1-Wire EPROM device, it is not possible to multidrop non-EPROM based 1-Wire devices with the DS2501 during programming. An internal diode within the non-EPROM based 1-Wire devices will attempt to clamp the data line at approximately 8V and could potentially damage these devices.

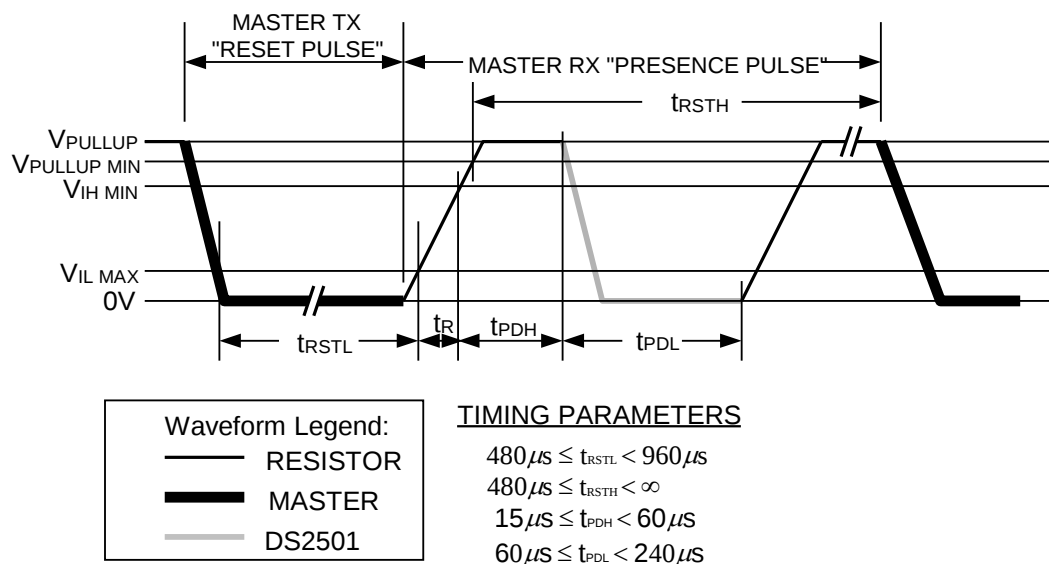
CRC GENERATION

The DS2501 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2501 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$.

Under certain conditions, the DS2501 also generates an 8-bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of command, address, and data bytes from the bus master to the DS2501. The Memory Function Flow Chart of Figure 6 indicates that the DS2501 computes an 8-bit CRC for the command, address, and data bytes received for the Write Memory and the Write Status commands and then outputs this value to the bus master to confirm proper transfer. Similarly the DS2501 computes an 8-bit CRC for the command and address bytes received from the bus master for the Read Memory, Read Status, and Read Data/Generate 8-Bit CRC commands to confirm that these bytes have been received correctly. The CRC generator on the DS2501 is also used to provide verification of error-free data transfer as each page of data from the 512-bit EPROM is sent to the bus master during a Read Data/Generate 8-Bit CRC command, and for the 8 bytes of information in the status memory field.

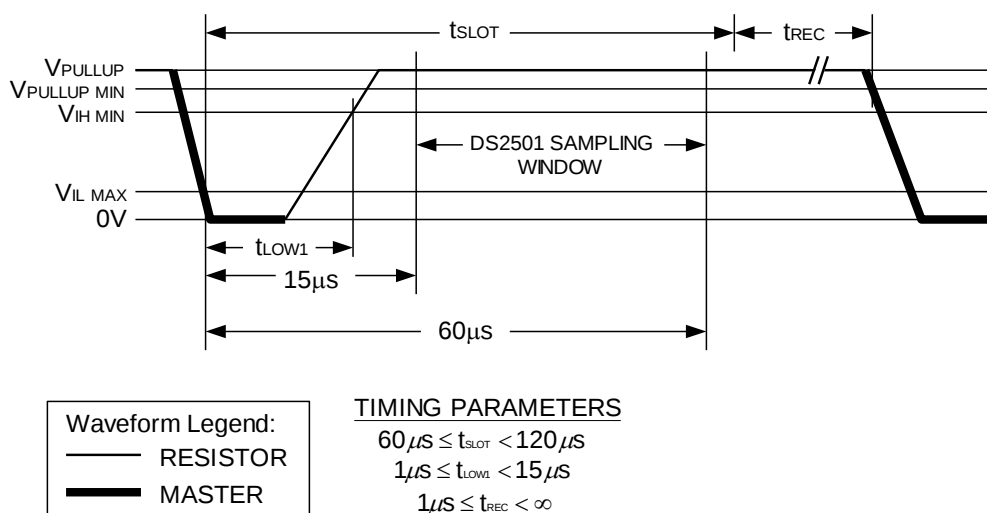
In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the DS2501 (for ROM reads) or the 8-bit CRC value computed within the DS2501. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS2501 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2501 does not match the value generated by the bus master. Proper use of the CRC as outlined in the flow chart of Figure 6 can result in a communication channel with a very high level of integrity.

INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 11



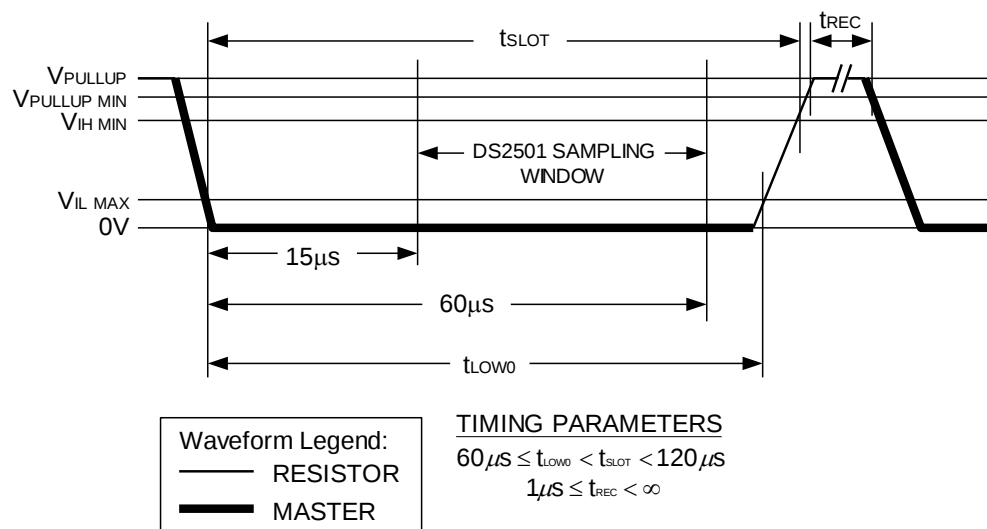
READ/WRITE TIMING DIAGRAM Figure 12

Write-One Time Slot

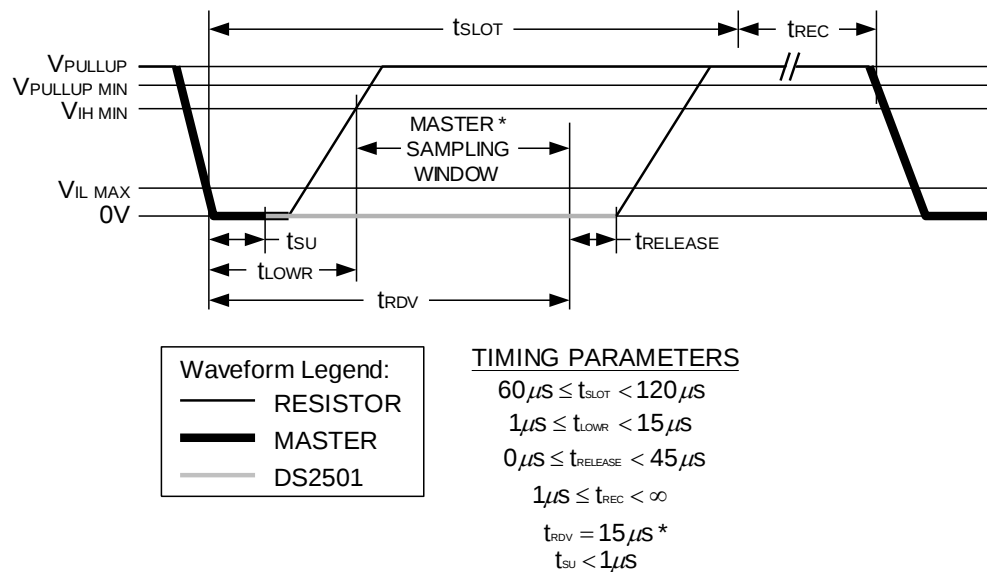


READ/WRITE TIMING DIAGRAM Figure 12 (continued)

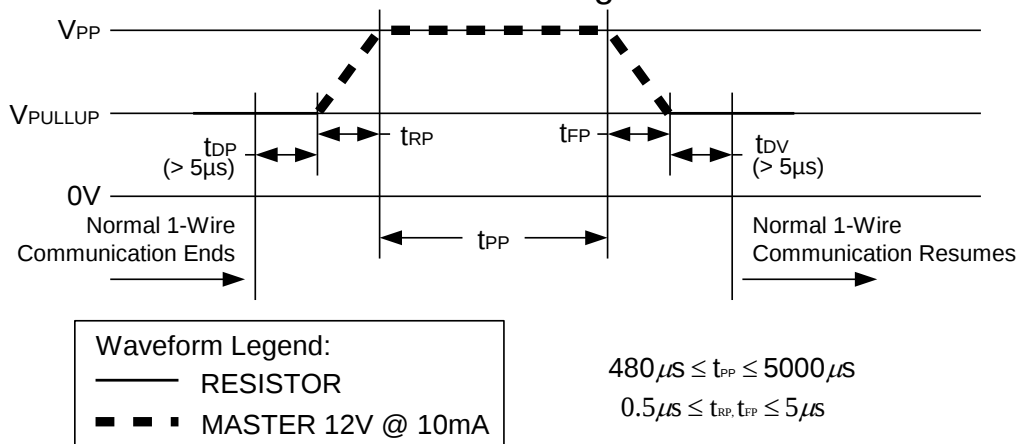
Write-Zero Time Slot



Read-Data Time Slot



PROGRAM PULSE TIMING DIAGRAM Figure 13



ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to Ground.....-0.5V to +12.0V
 Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-55°C to +125°C

Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)
 TO-92.....+250°C
 TSOC, SOT-23+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pullup Voltage	V_{PUP}	2.8		6.0	V	1, 2
Logic 1	V_{IH}	2.2			V	1, 6
Logic 0	V_{IL}	-0.3		+0.3	V	1
Output Logic Low at 4mA	V_{OL}			0.4	V	1
Input Load Current	I_L		5		μA	3
Programming Voltage at 10mA	V_{PP}	11.5		12.0	V	9

CAPACITANCE

($T_A = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	7

AC ELECTRICAL CHARACTERISTICS

($V_{PUP} = 2.8\text{V}$ to 6.0V ; $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	μs	
Write 1 Low Time	t_{LOW1}	1		15	μs	12
Write 0 Low Time	t_{LOW0}	60		120	μs	
Read Low Time	t_{LOWR}	1		15	μs	12
Read Data Valid	t_{RDV}		15		μs	10, 11
Release Time	$t_{RELEASE}$	0	15	45	μs	
Read Data Setup	t_{SU}			1	μs	5
Recovery Time	t_{REC}	1			μs	
Reset Time High	t_{RSTH}	480			μs	4
Reset Time Low	t_{RSTL}	480		960	μs	
Presence Detect High	t_{PDH}	15		60	μs	
Presence Detect Low	t_{PDL}	60		240	μs	
Delay to Program	t_{DP}	5			μs	8
Delay to Verify	t_{DV}	5			μs	8
Program Pulse Width	t_{PP}	480		5000	μs	8, 9
Program Voltage Rise Time	t_{RP}	0.5		5.0	μs	8
Program Voltage Fall Time	t_{FP}	0.5		5.0	μs	8

NOTES:

- 1) All voltages are referenced to ground.
- 2) V_{PUP} = external pullup voltage.
- 3) Input load is to ground.
- 4) An additional reset or communication sequence cannot begin until the reset high time has expired.
- 5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 μ s of this falling edge and will remain valid for 14 μ s minimum. (15 μ s total from falling edge on 1-Wire bus.)
- 6) V_{IH} is a function of the external pullup resistor and the pullup voltage.
- 7) Capacitance on the data pin could be 800pF when power is first applied. If a 5k Ω resistor is used to pullup the data line to V_{CC} , 5 μ s after power has been applied the parasite capacitance will not affect normal communications.
- 8) Maximum 1-Wire voltage for programming parameters is 11.5V to 12.0V; temperature range is -40°C to +50°C.
- 9) The accumulative duration of the programming pulses for each address must not exceed 5 ms.
- 10) Depending on the 1-Wire communication speed and the bus load characteristics, the optimal pullup resistor value will be in the 1.5k Ω to 5k Ω range.
- 11) The optimal sampling point for the master is as close as possible to the end time of the 15 μ s t_{RDV} period without exceeding t_{RDV} . For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.
- 12) The duration of the low pulse sent by the master should be a minimum of 1 μ s with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
3 TO-92 (formed leads)	Q3+4	21-0250	—
6 TSOC	D6+1	21-0382	90-0321
3 SOT-23	U3+5	21-0051	90-0179

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
5/02	Initial release.	—
3/06	Updated the <i>Ordering Information</i> table to include the TSOC package and part numbers of lead free versions; added the TSOC package drawing	1
9/09	Updated the <i>Ordering Information</i> table and added the SOT-23 package to the <i>Pin Assignment</i> .	1
2/10	Added note on power up from a cold start.	15
	Specified maximum t_{RSTL} value.	17, 19, 21
	Deleted redundant statement "In order not to mask..." below Figure 11.	19
	Typo corrections	19, 20, 21
2/12	Style and typo corrections.	3, 11, 13
	Added Junction Temperature to the <i>Absolute Maximum Ratings</i> section and updated the soldering information. Moved V_{PUP} from the <i>Electrical Characteristics</i> table header to table body; deleted the redundant V_{OH} parameter.	21
	Added Land Pattern No. to the <i>Package Information</i> section.	22