Synchronous Step-Down Controller

Description

The FP6339 is a cost effective, constant on-time synchronous buck, pseudo fixed-frequency, PWM controller for voltage regulation in system power applications, such as notebook PCs and other battery operated portable devices.

The FP6339 includes a PWM controller generating output voltage from 0.75V to 5.25V using external resistors. Switching frequency is internally preset to 325KHz. Additional features include cycle-by-cycle current limit, voltage soft-start, under-voltage protection, programmable over-current protection, soft shutdown, automatic power saving and non-overlapping gate drive. The FP6339 also provides an enable input and a power good output.

The FP6339 using constant on-time topology provides fast transient response while requiring less output capacitance than competing fixed-frequency converters. At light load, the automatic power save mode reduces the switching frequency for improved efficiency.

The FP6339 is available in the space saving 16-pin TQFN (3mmX3mm) package.

Features

- High Efficiency and Low Power Consumption
- 1μA Typical Shutdown Current
- ±1% Internal Reference Accuracy
- Wide Input Supply Voltage Range: 3V to 25V
- Output Voltage Range 0.75V to 5.25V
- Fixed Switching Frequency 325kHz
- Constant On-Time for Fast Dynamic Response and Reduced Output Capacitance
- Internal Soft-Start
- Integrated OVP/UVP Fault Protection
- Under-Voltage-Lock-Out Protection
- Low-Side $R_{DS(on)}$ Over-Current Sensing
- Integrated Soft-Stop at Output
- Power-Good Output
- Integrated Over-Temperature Protection
- Low External Part Count
- TQFN-16 (3mmX3mm) Package
- RoHS Compliant

Applications

- Notebook and Sub-Notebook Computers
- I/O Supplies
- System Power Supplies

Pin Assignments

WQ Package TQFN-16 (3mmX3mm)

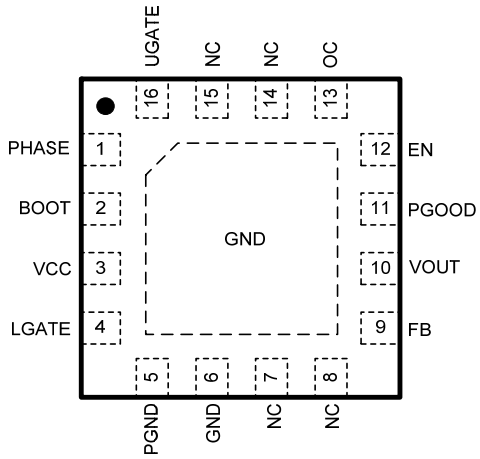


Figure1. Pin Assignment of FP6339

Ordering Information

FP6339□□□

- TR: Tape / Reel
- G: Green
- Package Type
  WQ: TQFN-16(3mmX3mm)

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Typical Application Circuit

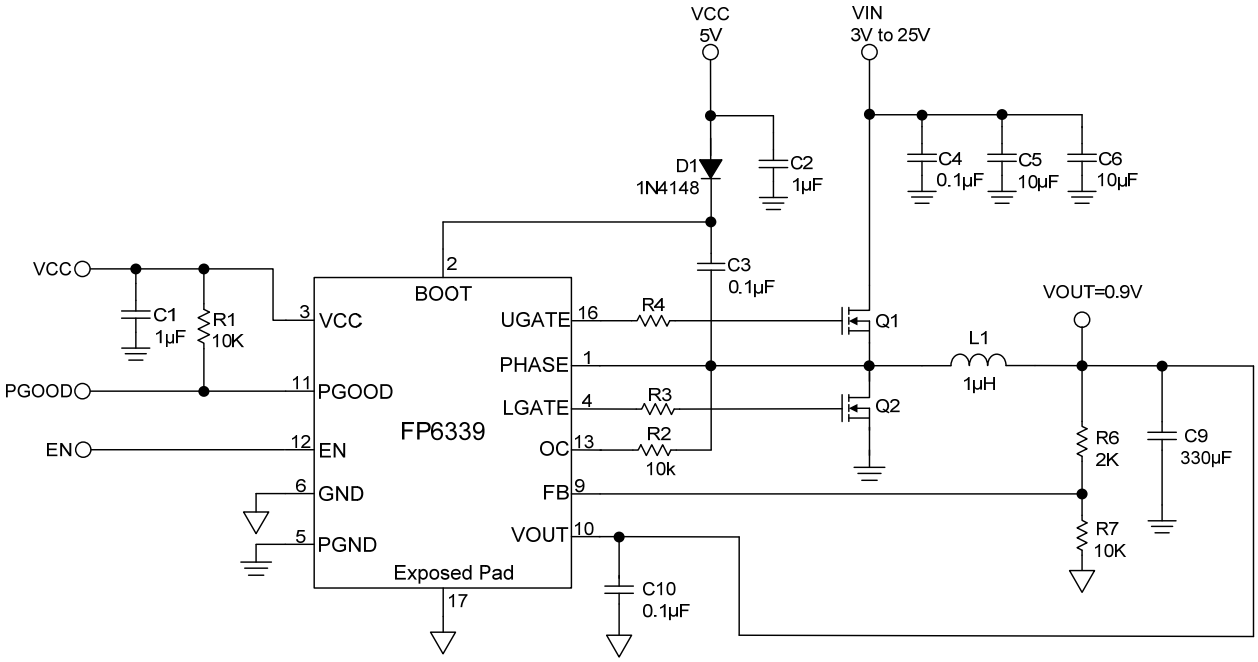


Figure2. Typical Application Circuit of FP6339

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Functional Pin Description

PIN	Pin Name	Pin Function
1	PHASE	High-side N-MOSFET gate driver return
2	BOOT	Supply input for high-side N-MOSFET gate drive. Connect a capacitor from this pin to PHASE node
3	VCC	5V power input for internal analog circuits and gate driver output
4	LGATE	Gate drive output for the low-side external MOSFET
5	PGND	Power ground – the return point for the LGATE driver output and the reference point for the Current Limit and Zero Cross circuits
6	GND	Analog ground for VOUT sense
7	NC	Not connected internally – leave unconnected or connect to GND
8	NC	Not connected internally – leave unconnected or connect to GND
9	FB	Feedback input.
10	VOUT	Output voltage sense point for on-time automatic adjustment
11	PGOOD	Power good output pin. High impedance indicates power is good. An External pull-up resistor is required
12	EN	Enable input – connect EN to GND to disable IC
13	OC	Over current sense point – program the current limit by connecting a resistor from OC to PHASE
14	NC	Not connected
15	NC	Not connected
16	UGATE	Gate drive output for the high-side external MOSFET
17	Exposed Pad	Exposed pad should be soldered to PCB board and connected to GND

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Block Diagram

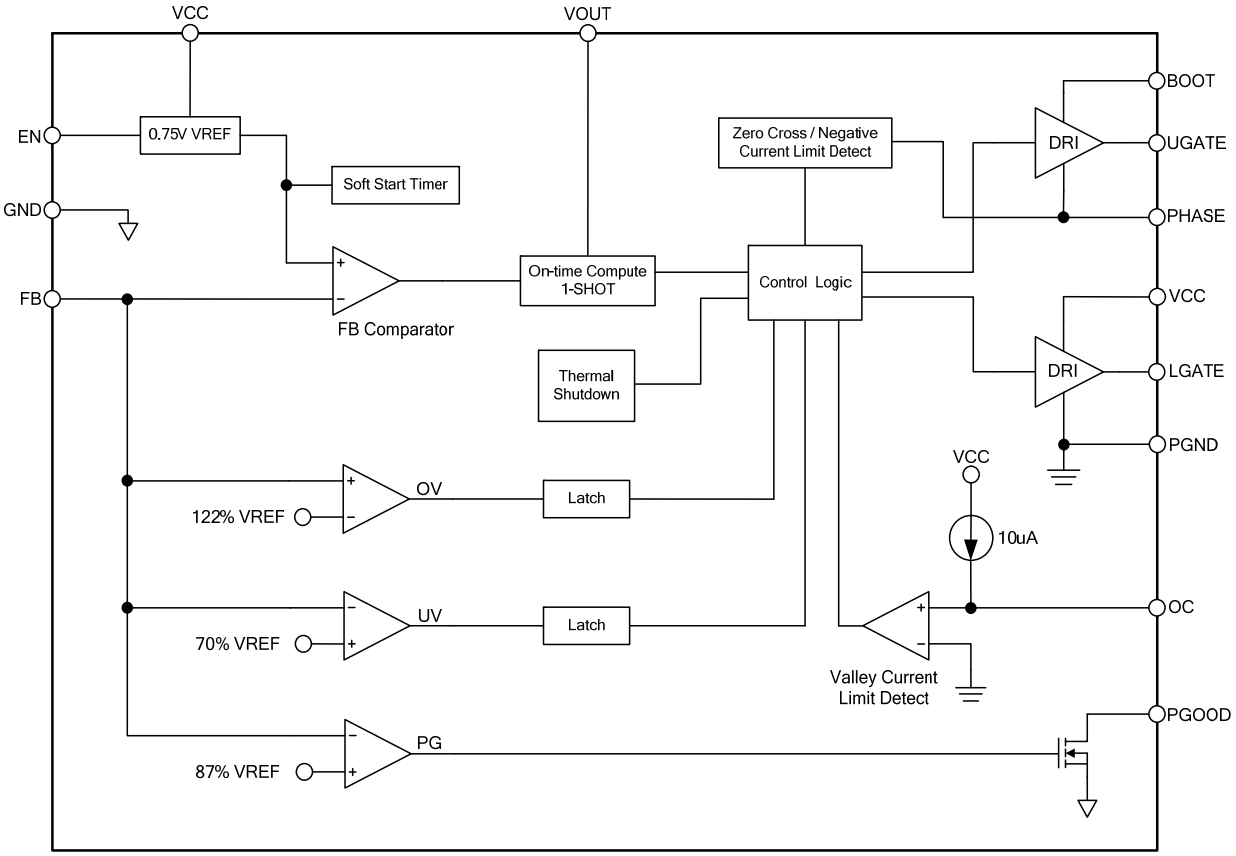


Figure3. Block Diagram of FP6339

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Absolute Maximum Ratings

- UGATE, BOOT to PGND---------- - 0.3V to 30V
- LGATE to PGND---------- - 0.3V to +6V
- PHASE to PGND---------- - 0.3V to +25V
- BOOT to PHASE---------- - 0.3V to +6V
- GND to PGND---------- - 0.3V to +0.3V
- VCC to GND ---------- - 0.3V to +6V
- EN, FB, OC, PGOOD, VOUT to GND ---------- - 0.3V to VCC+0.3V
- Power Dissipation @ T_A=25℃, TQFN-16 (3mmX3mm) (P_D)---------- +1.54W
- Package Thermal Resistance, TQFN -16 (3mmX3mm) (θ_{JA})---------- +65℃/W
- Lead Temperature (Soldering, 10sec.) ---------- +260℃
- Maximum Junction Temperature (T_J) ---------- +150℃
- Storage Temperature (T_{STG}) ---------- -65℃ to 150℃

Note1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Input Voltage (VCC)---------- +4.5V to +5.5V
- Operating Temperature Range (TOPR)---------- -40℃ to +85℃

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Electrical Characteristics

(V_{IN}=15V, V_{OUT}=1.5V, V_{CC}=5V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Input Voltage	V_{IN}		3		25	V
VCC Operating Current	I_{VCC}	EN=5V, VFB>REF		320	600	μA
VCC Shutdown Current	$I_{VCC-SDN}$	EN=0V		0.1	1	μA
VOUT Input Resistance	R_{OUT}			200		kΩ
Controller						
FB Regulation Voltage	V_{FB}		0.7425	0.75	0.7575	V
FB Input Current	I_{FB}	FB=VCC or GND	-1		+1	μA
Line Regulation		Typical Application Circuit		0.04		%/V
Load Regulation		Typical Application Circuit		0.3		%
Timing						
On Time	T_{ON}	Continuous Mode Operation, V_{OUT}=1.15V	200	250	300	ns
Minimum On Time (Note2)	T_{ON-MIN}			100		ns
Minimum Off Time (Note2)	$T_{OFF-MIN}$			350		ns
Soft-Start						
Internal Soft-Start Ramp Time	T_{SS}	I_{OUT}=I_{OC}/2		1.2		ms
Current Sense						
OC Source Current	I_{OC}		9	10	11.5	μA
OC Source Current Temperature Coefficient	TC_{IOC}	On the basis of 25°C		4000		ppm/°C
OC Comparator Offset	V_{OC-OS}			0		mV
Zero-Crossing Detector Threshold	V_{ZCD}	PHASE - PGND		0		mV
Negative Current Limit Detector Threshold	V_{OC-NEG}	PHASE - PGND		80		mV
Fault Protection						
Output Under-Voltage Fault	V_{UVP}	FB with respect to REF	65	70	75	%
Output Over-Voltage Fault	V_{OVP}	FB with respect to REF	118	122	126	%
Over-Voltage Fault Delay	T_{OVP}	FB forced 50mV above Over-Voltage Fault Threshold		1.5		μs
VCC Under Voltage Lockout	V_{UVLO}	Falling Edge (Hysteresis=100mV)	3.7	4	4.35	V
Thermal Shutdown Threshold (Note2)	T_{SDN}			160		°C
Enable Control						
EN Logic High Voltage	V_{ENH}		1.2			V
EN Logic Low Voltage	V_{ENL}				0.4	V
EN Input Current	I_{EN}	EN=VCC or GND	-1		+1	μA

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Electrical Characteristics (Continued)

(V_{IN}=15V, V_{OUT}=1.5V, V_{CC}=5V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Good						
PGOOD Threshold	V_{PGTH}	FB with respect to REF 1% Hysteresis Typical	84	87	90	%
PGOOD Threshold Delay Time	T_{PG}			1.5		µs
PGOOD Output Low Voltage	V_{PG}	R_{PGOOD} = 10KΩ to VCC			0.4	V
PGOOD Leakage Current	I_{PG}				1	µA
Gate Drivers						
Shoot-Through Protection Delay	T_{STD}	UGATE or LGATE Rising		30		ns
LGATE Pull-Down Resistance	$R_{LG-DOWN}$	LGATE Low		0.8		Ω
LGATE Pull-Up Resistance	R_{LG-UP}	LGATE High		2		Ω
LGATE Sink Current	$I_{LG-SINK}$	V_{LGATE}=2.5V		3.1		A
LGATE Source Current	$I_{LG-SOURCE}$	V_{LGATE}=2.5V		1.3		A
UGATE Pull-Down Resistance	$R_{UG-DOWN}$	UGATE Low, BOOT-PHASE = 5V		2		Ω
UGATE Pull-Up Resistance	R_{UG-UP}	UGATE High, BOOT-PHASE = 5V		2		Ω
UGATE Sink Current	$I_{UG-SINK}$	V_{UGATE}=2.5V		1.3		A
UGATE Source Current	$I_{UG-SOURCE}$	V_{UGATE}=2.5V		1.3		A

Note2：The specification is guaranteed by design, not production tested.

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Typical Performance Curves

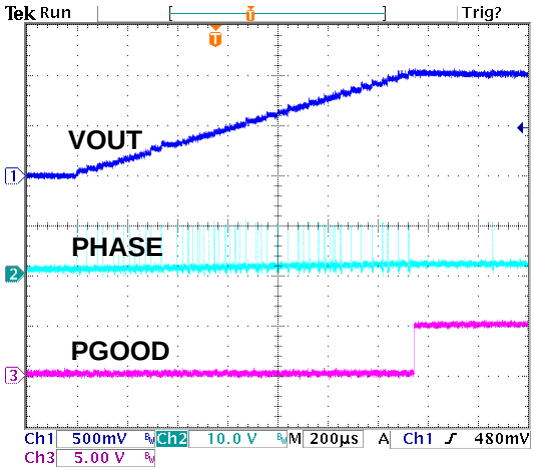


Figure 4. 1.05V Start-up Waveform (V_{IN}=9V, no load)

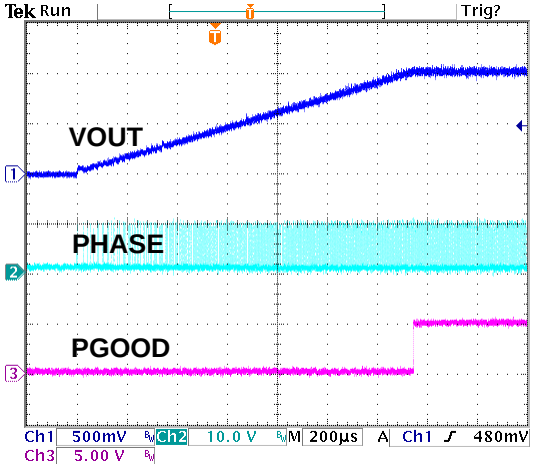


Figure 5. 1.05V Start-up Waveform (V_{IN}=9V, 20A)

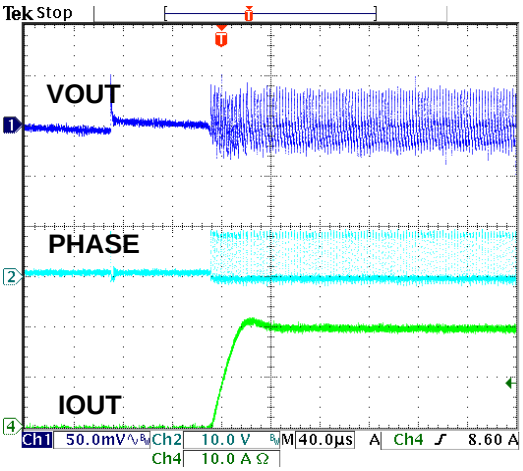


Figure 6. 1.05V Load Transient Response (V_{IN}=9V,0A → 20A)

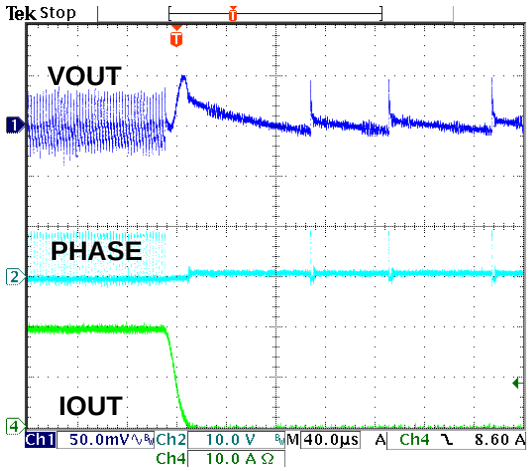


Figure 7. 1.05V Load Transient Response (VIN=9V, 20A → 0A)

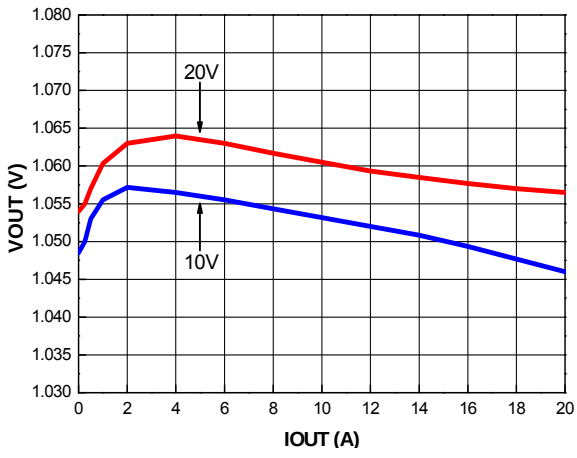
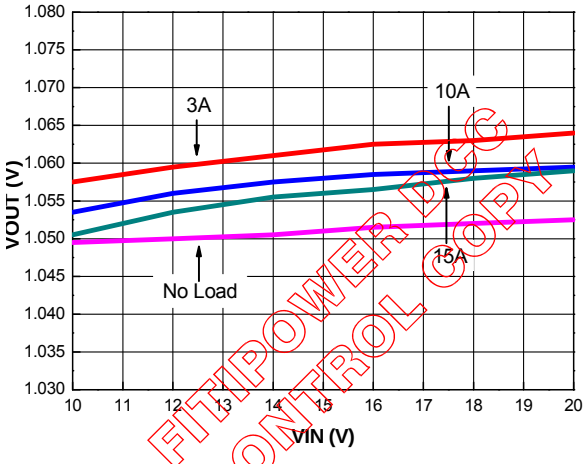


Figure 8. Load Regulation



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Figure 9. Line Regulation

Typical Performance Curves (Continued)

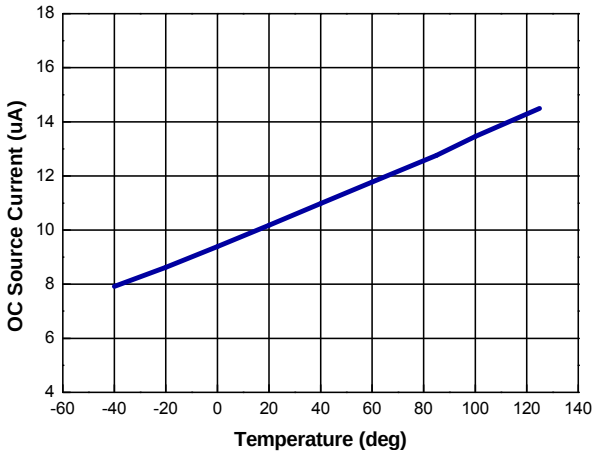


Figure10. OC Source Current vs. Temperature

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Function Description

Operation

The FP6339 synchronous buck controller is designed for powering low voltage circuits. The main control loop, constant on-time, pseudo fixed frequency PWM in the FP6339 is specifically designed for handling fast load transient. The pseudo fixed frequency PWM scheme improves the poor load-transient timing problems of fixed-frequency PWM while avoiding the problems caused by widely varying switching frequencies in constant-on-time and constant-off-time PWM schemes.

The FP6339 provides automatic power saving mode; the FP6339 automatically reduces the switching frequency during a light load condition to maintain high efficiency. The internal zero-cross comparator watches the inductor current falling to zero. When the zero current is detected, the controller enters auto skip mode and turns low-side MOSFET off on each cycle. If the inductor current does not cross zero, the controller immediately exits auto skip. Note the on-time is kept the same from light load to heavy load. The switching frequency increases to the preset value as the output current increases to the inductor current reaches continuous conduction. The threshold between auto skip mode and PWM operation, $I_{OUT(LB)}$, can be calculated as follows:

$$I_{OUT(LB)} = \frac{1}{2L \times f_{sw}} \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

The PWM control scheme is a constant-on-time, pseudo-fixed frequency, current-mode PWM controller. This architecture depends on the ESR (effective series resistance) of output capacitor, see figure11; the output ripple voltage across the ESR provides the PWM ramp signal. The high-side switch on-time is determined by an internal one-shot which pulse width is inversely proportional to input voltage and proportional to output voltage. Another separate one-shot sets a minimum off-time (350ns typ.). The on-time one-shot is triggered if the error comparator is low, the low side switch current is under the current limit threshold, and the minimum off-time one-shot has timed out.

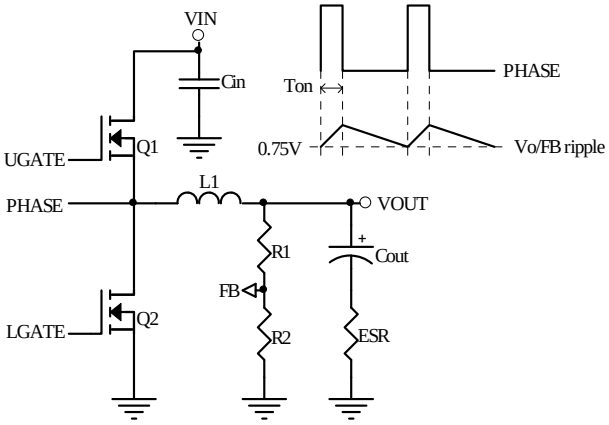


Figure11.

Soft Start

The FP6339 has an internal, 1ms, voltage soft-start with over-current limit. Smooth control of the output voltage is maintained during start up. When the EN becomes high, the reference voltage begins ramping up from 0V to 0.75V in about 12mV increments.

+5V Bias Supply

The FP6339 requires an external +5V bias supply (VCC) in addition to the VIN. The external bias supply to the IC is needed to supply the control circuitry and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated by an external linear regulator. The power input and +5V bias inputs can be connected together if the input source is a fixed 4.5V to 5.5V supply. The 5V bias supply must be power up after to the battery supply is present to ensure startup.

On-Time Control (T_{ON})

The core of pseudo fixed frequency PWM is the one-shot that sets the high-side switch on-time for the controller. The high-side switch on-time is inversely proportional to the input voltage, and proportional to the output voltage, so that the duty ratio is kept as VOUT/VIN technically. The general equation for the on-time is:

$$T_{ON} = 2560 \times (\frac{V_{OUT}}{V_{IN}}) + 35ns$$

The actual switching frequency is approximate to:

$$f_{SW} \approx \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

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Function Description (Continued)

Output Voltage Setting

Output voltage can be set by external resistor divider. The output can be adjusted to a voltage between 0.75V – 5.25V. The output voltage is set by the equation:

$$V_{OUT} = 0.75V \times (\frac{R1}{R2} + 1)$$

Current Limit

The cycle-by-cycle current limit circuit regulates the inductor valley current as Figure12 shown. This means that if the current limit is set to 10A, and the average current through the inductor would be 10A plus half the peak-to-peak ripple current. The current limit threshold is adjusted with an internal 10μA I_{OC} current source and an external resistor on OC pin.

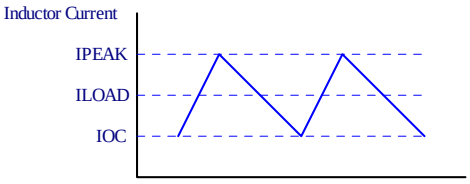


Figure12

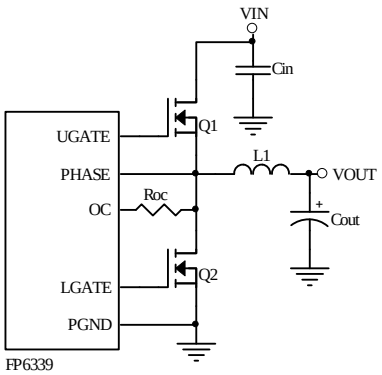


Figure13

The valley current limit threshold in Figure 13 can be calculated as:

$$I_{OC} = 10\mu A \times \frac{R_{OC}}{R_{DS-ON(low-side)}}$$

The current limit circuitry also supports negative current limit that prevents excessive reverse inductor current when VOUT is sinking current. The negative current limit threshold is approximate to

$$I_{OC(NEG)} = \frac{V_{OC-NEG}}{R_{DS-ON(low-side)}} = \frac{80mV}{R_{DS-ON(low-side)}}$$

MOSFET Gate Drivers

The UGATE and LGATE drivers are optimized to drive large high side and low side N-channel MOSFETs. An adaptive dead time circuit monitors the UGATE to prevent the low side MOSFET from turning on until UGATE is fully off ; another circuit monitors the LGATE output and prevents the high side MOSFET from turning on until LGATE is fully off.

Power Good Output

The FP6339 provides a power good (PGOOD) output, which is an open-drain output requiring a pull-up resistor. Typically connect to VCC through a 100kΩ resistor. In shutdown and soft-start period, PGOOD is actively held low. After a soft-start has terminated, PGOOD is released after 1.5us delay time when the output voltage reaches 88% of the target threshold. If the output voltage is lower than -12% or higher than +20% of the target threshold, the PGOOD becomes low immediately. PGOOD is also low when shutdown.

Over Voltage Protection (OVP)

When FB exceeds 20% of nominal value, over voltage protection is triggered after 1.5us internal delay time and the low-side gate driver is forced high. LGATE latches high and the low side MOSFET is turned on and high side MOSFET is turned off. This action discharges the output capacitor rapidly. LGATE stays high and the output latches off until the EN input is recycled or the +5V bias supply is re-started.

Under Voltage Protection (UVP)

When FB drops lower than 30% of nominal value for 8 continuous cycles, the LGATE and UGATE drives are pulled low to turn off the MOSFETs. The FP6339 latches off until its EN input is recycled or the +5V bias supply is re-start. The UVP function is disabled for double soft start time during start-up.

UVLO Protection

Under-voltage lockout circuitry (UVLO) inhibits switching and the FP6339 is off until the +5V bias supply at VCC rises above 4.1V.

Thermal Shutdown Protection

The 160°C junction temperature will trigger thermal shutdown protection, the FP6339 latches off until both junction temperature decrease 30°C and the +5V bias supply is re-start.

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Application Information

Inductor Selection

The inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the ripple current and the ripple voltage of the converter. The ripple current and ripple voltage can be approximated by:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \cdot \frac{V_{OUT}}{V_{IN}}, \qquad \Delta V_{OUT} = \Delta I_L \times ESR$$

The general rule is that higher inductor values have better efficiency at light loads due to lower core losses and lower peak current, but at heavy load the smaller inductors are better because of lower resistance. The inductor selection is based on the ripple current which is typically set between20% to 50% of the maximum load current. Cost, size, efficiency and output ripple all affect the selection process.

MOSFET Selection

The current ability of the output N-channel MOSFETs must be at least more than the peak switching current. The voltage rating V_{DS} of the N-channel MOSFETs should be at least 1.25 times the maximum input voltage. Choose the low R_{DS-ON} MOSFETs for reducing the conduction loss. Choose the low C_{ISS} MOSFETs for reducing the switching loss. But most of time, this two factors are trade-off. Consider the system requirement and define the MOSFETs rating. Choose a high side MOSFET that has conduction loss equal to the switching loss at the optimum input voltage for maximum efficiency. Choose a low side MOSFET that has the lowest R_{DS-ON}.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy the ripple requirements for loop stability. The important capacitor parameters are the Equivalent Series Resistance (ESR), the RMS ripples current rating, the voltage rating, and capacitance value. For the output capacitor of FP6339, the ESR is the most important parameter.

$$ESR(m\Omega) = \frac{\Delta V_{OUT}}{\Delta I_L}$$

The capacitance value required relates to the size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value. The conductive polymer capacitors, such as OS-CON, POSCAP or KO Cap, are recommended to proper high capacitance and low ESR.

FB Ripple Requirement

The on-time control used in the FP6339 regulates the valley of the output ripple voltage. A minimum ESR is required to generate the required ripple voltage for regulation. Due to the pseudo fixed frequency PWM mode not employing an error amplifier in the loop, a sufficient feedback signal needs to be provided from output ripple. The FB pin required ripple signal is approximately 10~15mV. This generates output ripple

$$\Delta V_{OUT} = (V_{OUT} / 0.75) \times 15mV .$$

Stability Consideration

The constant on-time, pseudo fixed frequency PWM scheme has natural frequency jitter. An mV order of noise on the feedback signal can affect the frequency jitter from a few to ten percent. This is normal operation and has little harm to the power supply performance. Unstable operation results from two causes: double pulse and feedback loop instability. Loop instability can cause oscillations at the output as a response to line or load transients. These oscillations may trigger the over voltage protection latch or cause the output voltage drop.
Double pulse occurs because the insufficient ripple at the FB, or the FB and V_{OUT} ripple waveforms are very noisy and trigger the FB comparator. If the ripple at FB is too small, the FB waveform will be interfered with switching noise. The noise causes the FB comparator to trigger too quickly after the 350ns minimum off -time. Double pulse will result in higher output ripple voltage but in most cases is harmless.

Place a small capacitor in parallel with the top divider resistor is a way to couple more ripple into FB from V_{OUT} to correct double pulse. This capacitor can be left out until double pulsing exists. Leave a space on the PCB in advance in case it is needed.

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Application Information (Continued)

Design Procedure

Before select the external component, input voltage range, output voltage tolerance, and load current must be specified. There are two values of load current to consider: continuous and peak load current. Continuous load current is concerned with thermal stresses of MOSFETs. Peak load current determines the components stresses and design of threshold of the current limit. The following guidelines will help calculate the external components of the FP6339 as figure7 circuit.

1. Select R1 and R2. The recommended value for R2 is 10kΩ. $R1 = R2 \times (\frac{V_{OUT} - 0.75}{0.75})$

2. Calculate the on-time and switching frequency, f_{SW}. Switching frequency is determined the factor of efficiency, components size, and cost. The on-time can be calculate by

$$T_{ON} = 2560 \times (\frac{V_{OUT}}{V_{IN}}) + 35ns$$

The typical switching frequency should be:

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

3. Choose inductor. Before determine the inductance, the ripple current, ΔI_L, must be defined, typically set between 20% to 50% of the maximum load current.

The inductor is defined as

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{\Delta I_L \times f_{SW} \times V_{IN(max)}}$$

The inductor current must be rated for maximum peak current.

$$I_{L(PEAK)} = I_{OUT(max)} + \frac{1}{2}\Delta I_L$$

4. Choose output capacitor. The ESR has to choose to meet the minimum ripple requirement, 15mV at the FB. That is

$$ESR(m\Omega) = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{15mV \times V_{OUT}}{\Delta I_L \times 0.75V}$$

And the output capacitance is based on transient ability.

$$C_{OUT(min)} = \frac{L \times (I_{OUT(MAX)} + 0.5\Delta I_L)^2}{\Delta V_{OUT}{}^2 + (2 \times V_{OUT} \times \Delta V_{OUT})}$$

5. MOSFET selection. The RDSON for low side MOSFET is determine the current sensing and current limit protection.

6. Determine the current limit threshold under VIN is minimum and load current is maximum conditions. The ROC determines the reachable current limit accuracy.

$$R_{OC} = \frac{I_{OC} \times R_{DS-ON(low-side)}}{10\mu A}$$

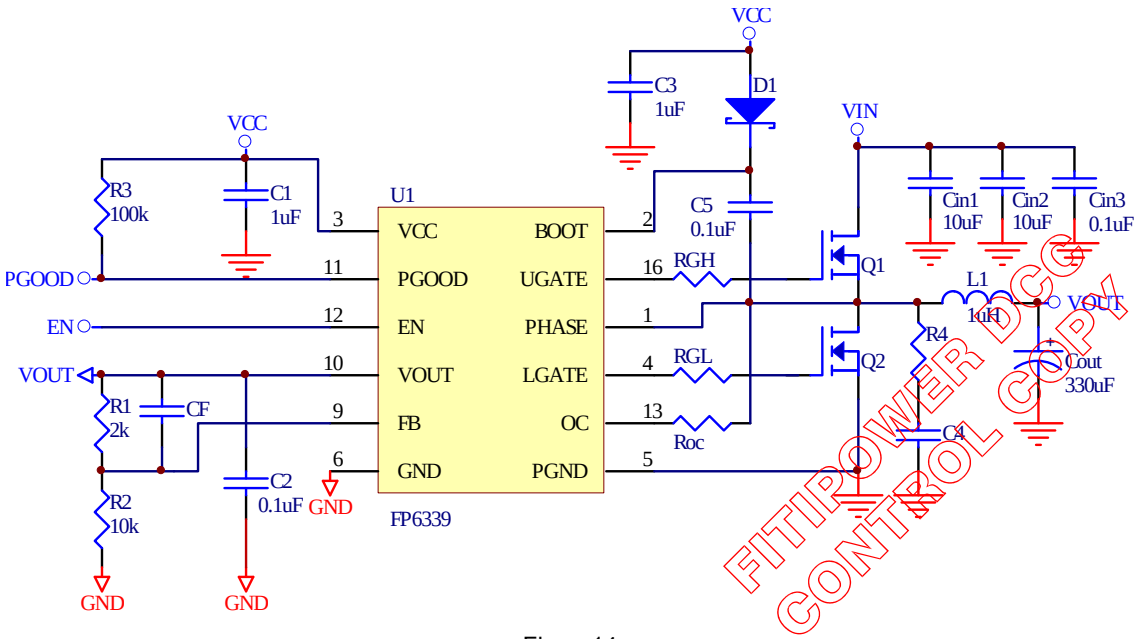


Figure14

Application Information (Continued)

Layout Guideline

A good PCB layout is critical to achieve optimum performance. The switching power stages require more attention. Keep the high current paths short, especially at the ground terminals. Four-layer board is recommended. Use two middle layers as ground planes, with interconnections between top and bottom layers as needed. Using thick copper PC boards (2oz) can improve full load efficiency and thermal performance of the MOSFET.

1. Minimize the low side high current path. The high current path starts at the ground of the low side MOSFET, goes through the low side MOSFET, through the inductor, through the output capacitor, and back to the ground of the low side MOSFET. Minimize the resistance by keeping the power component group together with short and wide trace (60mil at least).

2. Minimize the high side path with short and wide trace. This path starts at VIN, goes through the high side MOSFET, through the inductor, through the output capacitor, through the input capacitor, and back to the input.

3. Power components should be grouped together near the gate drivers. Connect the drivers of UGATE and LGATE to the gate of high side and low side MOSFET with short trace as possible to reduce stray inductance.

4. Keep sensitive analog areas (FB, OC) away from high-speed switching nodes (BOOT, PHASE, UGATE, and LGATE) to avoid coupling.

5. Place feedback resistors R1 and R2 near FB and GND pin with short wire and should be far away to the noise source, such as switching loop. Use ground plane to shield feedback trace from power

6. The current limit setting resistor, R_{OC}, should connect to OC and GND pin directly, next to the IC.

7. Group the analog ground connection of the VCC bypass capacitors and FB. Connect the analog ground plane directly to GND pin of the IC.

8. Group the power ground connection of the VIN capacitor, VOUT capacitor, and the source of the low side MOSFETs as close as possible. Connect this power ground plane directly to PGND pin of the IC.

9. Use plane connection between GND (analog ground) and PGND (power ground) near the IC.

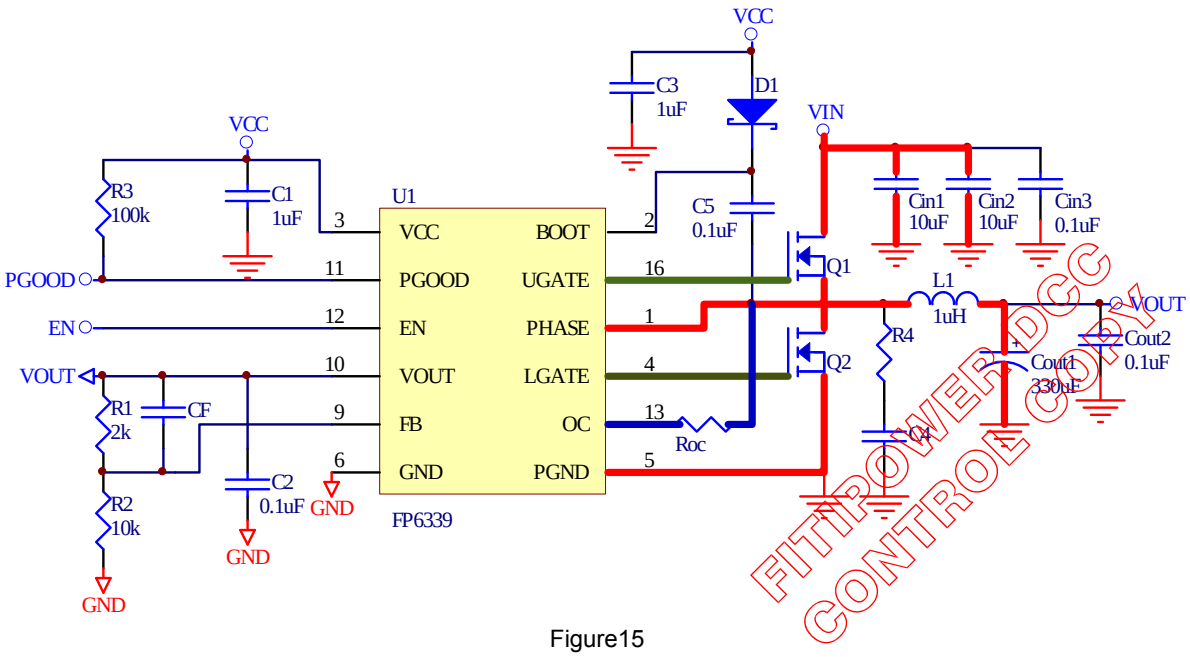
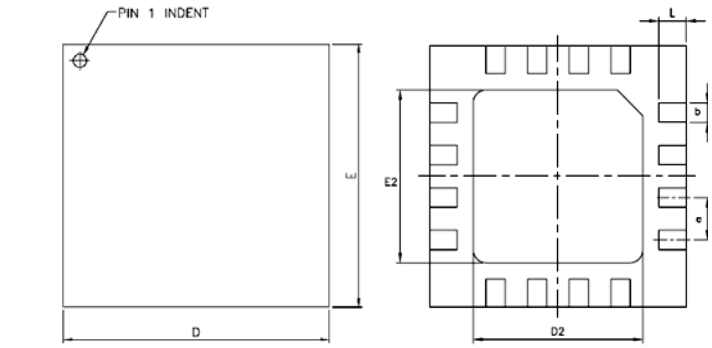
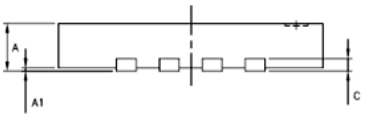


Figure15

Outline Information

TQFN-16 3mmx3mm Package (Unit: mm)





SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.19	0.30
E	2.90	3.10
D	2.90	3.10
L	0.35	0.45
b	0.18	0.30
e	0.45	0.55
E2	1.50	1.75
D2	1.50	1.75

Note :Followed From JEDEC MO-220-J

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