

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4519B

MSI

Quadruple 2-input multiplexer

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple 2-input multiplexer

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MSI

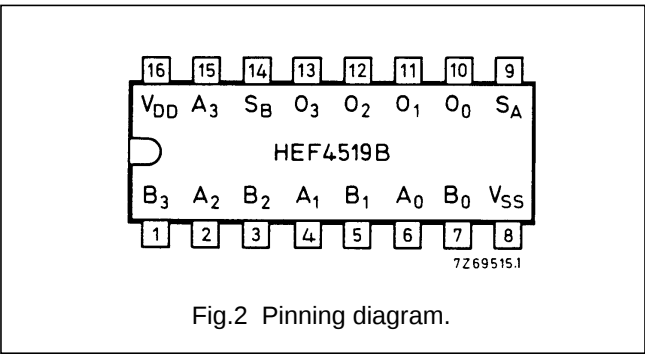
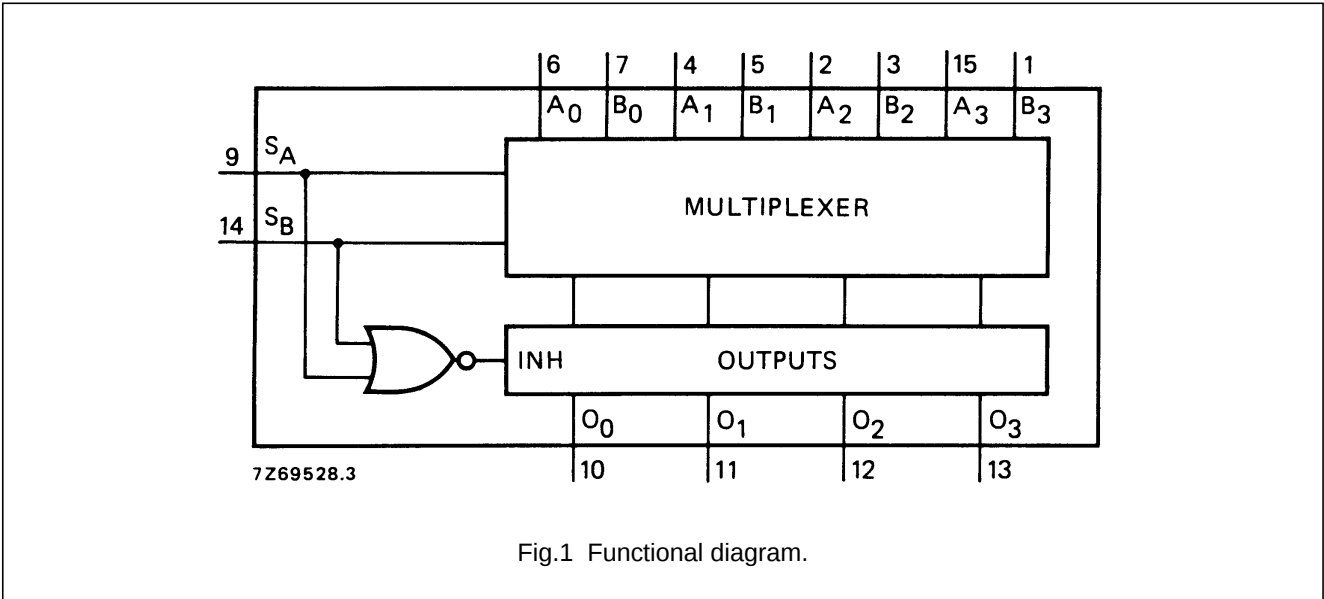
DESCRIPTION

The HEF4519B provides four multiplexing circuits with common select inputs (S_A , S_B); each circuit contains two inputs (A_n , B_n) and one output (O_n). It may be used to select four bits of information from one of two sources.

The 'A' inputs are selected when S_A is HIGH, the 'B' inputs when S_B is HIGH. When S_A and S_B are HIGH, the output (O_n) is the logical EXCLUSIVE-NOR of the A_n and B_n inputs ($O_n = A_n \odot B_n$).

When S_A and S_B are LOW, the output (O_n) is LOW, independent of the multiplexer inputs (A_n and B_n).

The HEF4519B cannot be used to multiplex analogue signals. The outputs utilize standard buffers for best performance.



PINNING

- | | |
|----------------|------------------------------|
| S_A , S_B | selects inputs (active HIGH) |
| A_0 to A_3 | multiplexer inputs |
| B_0 to B_3 | multiplexer inputs |
| O_0 to O_3 | multiplexer outputs |

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4519BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4519BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4519BT(D): 16-lead SO; plastic (SOT109-1)
(): Package Designator North America

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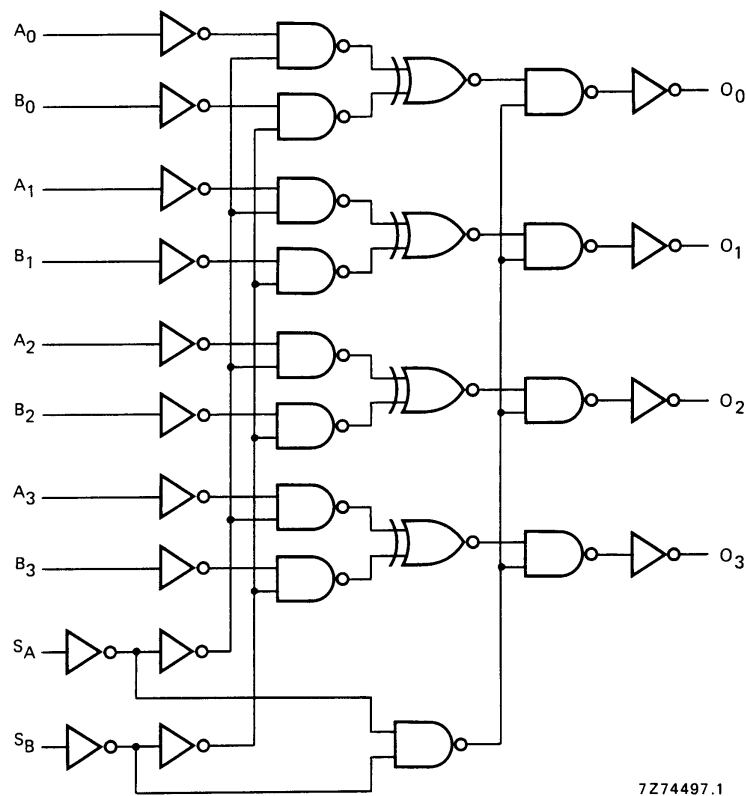


Fig.3 Logic diagram.

FUNCTION TABLE

INPUTS				OUTPUT
S _A	S _B	A _n	B _n	O _n
L	L	X	X	L
H	L	A _n	X	A _n
L	H	X	B _n	B _n
H	H	L	L	H
H	H	H	L	L
H	H	L	H	L
H	H	H	H	H

Notes

- 1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

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AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $A_n, B_n \rightarrow O_n$ HIGH to LOW LOW to HIGH $S_A, S_B \rightarrow O_n$ HIGH to LOW LOW to HIGH	5	t_{PHL}	95	190	ns	68 ns + (0,55 ns/pF) C_L
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}	80	160	ns	53 ns + (0,55 ns/pF) C_L
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PHL}	95	190	ns	68 ns + (0,55 ns/pF) C_L
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}	85	165	ns	58 ns + (0,55 ns/pF) C_L
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$17\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4519B are:

- 2-input multiplexers.
- True/complement selectors.