

IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

0.4A and 0.5A, 60V and 100V, 2.4 and 3.2 Ohm,
N-Channel Power MOSFETs

July 1998

Features

- 0.4A and 0.5A, 60V and 100V
- $r_{DS(ON)} = 2.4\Omega$ and 3.2Ω
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFD1Z0	HEXDIP	IRFD1Z0
IRFD1Z1	HEXDIP	IRFD1Z1
IRFD1Z2	HEXDIP	IRFD1Z2
IRFD1Z3	HEXDIP	IRFD1Z3

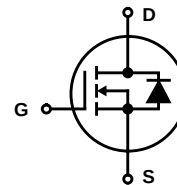
NOTE: When ordering, use the entire part number.

Description

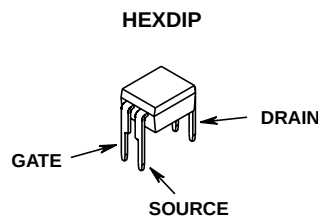
These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

Formerly developmental type TA17451.

Symbol



Packaging



IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	UNITS
Drain to Source (Note 1) V_{DS}	100	60	100	60	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1) V_{DGR}	100	60	100	60	V
Continuous Drain Current I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current I_{DM}	4.0	4.0	3.2	3.2	A
Gate to Source Voltage V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 1)	0.008	0.008	0.008	0.008	$\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s T_L	300	300	300	300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334 T_{pkg}	260	260	260	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 125°C .

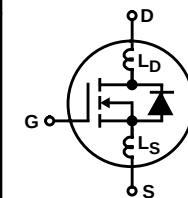
Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRFD1Z0, IRFD1Z2	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (See Figure 9)	100	-	-	V
IRFD1Z1, IRFD1Z3			60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_C = 125^{\circ}\text{C}$	-	-	250	μA
On-State Drain Current (Note 2) IRFD1Z0, IRFD1Z1	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10\text{V}$ (See Figure 6)	0.5	-	-	A
IRFD1Z2, IRFD1Z3			0.4	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2) IRFD1Z0, IRFD1Z1	$r_{DS(ON)}$	$I_D = 0.25\text{A}$, $V_{GS} = 10\text{V}$ (See Figures 7, 8)	-	2.2	2.4	Ω
IRFD1Z2, IRFD1Z3			-	2.8	3.2	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $I_D = 0.25\text{A}$	0.25	0.35	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \equiv 0.5 \times \text{Rated } BV_{DSS}$, $I_D = 0.25\text{A}$, $R_G = 50\Omega$ (Figures 14, 15, 16) $R_L = 198\Omega$ for $BV_{DSS} = 100\text{V}$ $R_L = 118\Omega$ for $BV_{DSS} = 60\text{V}$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	10	20	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	15	25	ns
Fall Time	t_f		-	10	20	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}$, $I_D = 1.2\text{A}$, $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ (Figures 13, 16, 17) Gate Charge is Essentially Independent of Operating Temperature	-	2.0	3.0	nC
Gate to Source Charge	Q_{gs}		-	1.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	1.0	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$ (Figure 10)	-	50	-	pF
Output Capacitance	C_{OSS}		-	20	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	5	-	pF

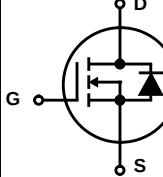
IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Internal Drain Inductance	L_D	Measured From The Drain Lead, 2mm (0.08in) From Package to Center of Die	-	4.0	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 2mm (0.08in) From Header to Source Bonding Pad	-	6.0	-	nH
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	120	$^{\circ}\text{C/W}$



Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current IRFD1Z0, IRFD1Z1	I _{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	0.5	A
IRFD1Z2, IRFD1Z3				-	-	0.4	A
Pulse Source to Drain Current IRFD1Z0, IRFD1Z1	I _{SDM}			-	-	4.0	A
IRFD1Z2, IRFD1Z3				-	-	3.2	A
Source to Drain Diode Voltage (Note 2) IRFD1Z0, IRFD1Z1	V _{SD}	T _A = 25°C, I _{SD} = 0.5A, V _{GS} = 0V		-	-	1.4	V
IRFD1Z2, IRFD1Z3		T _A = 25°C, I _{SD} = 0.4A, V _{GS} = 0V		-	-	1.3	V
Reverse Recovery Time	t _{rr}	T _J = 150°C, I _{SD} = 0.5A, dI _{SD} /dt = 100A/μs		-	100	-	ns
Reverse Recovery Charge	Q _{RR}	T _J = 150°C, I _{SD} = 0.5A, dI _{SD} /dt = 100A/μs		-	0.2	-	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

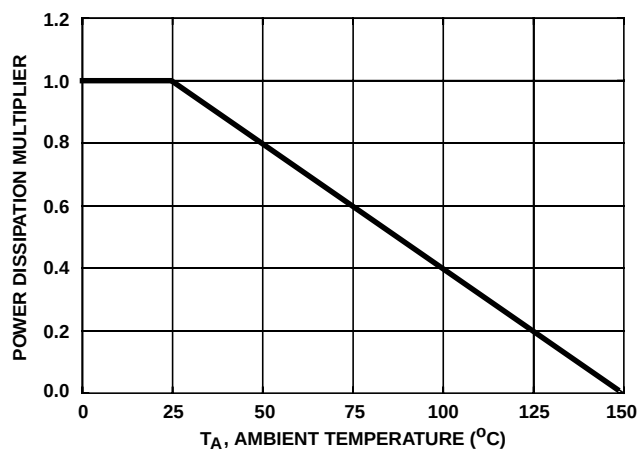


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

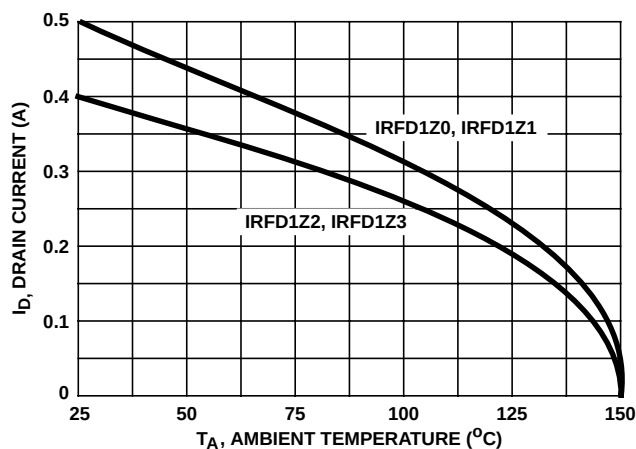


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

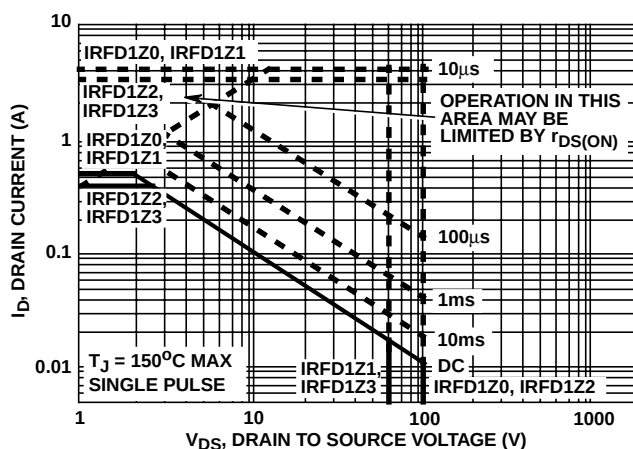


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

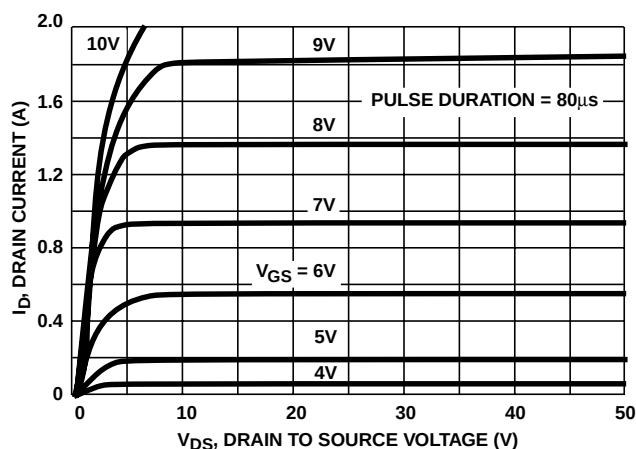


FIGURE 4. OUTPUT CHARACTERISTICS

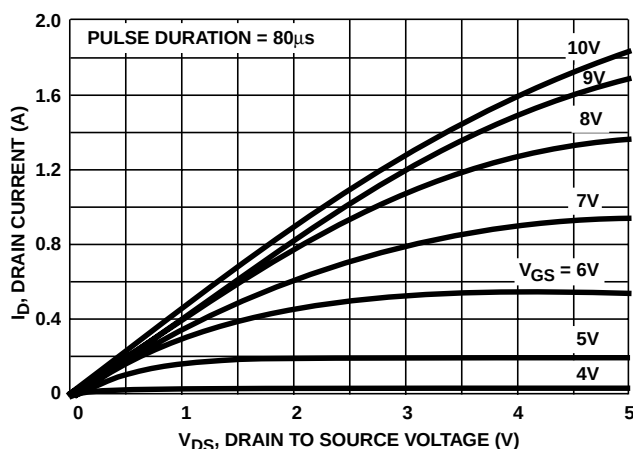


FIGURE 5. SATURATION CHARACTERISTICS

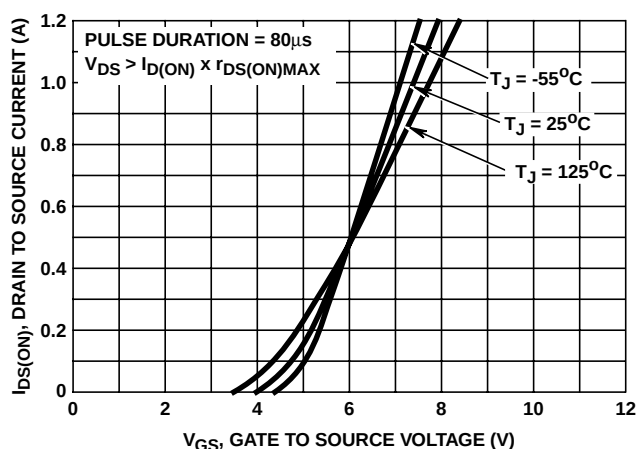
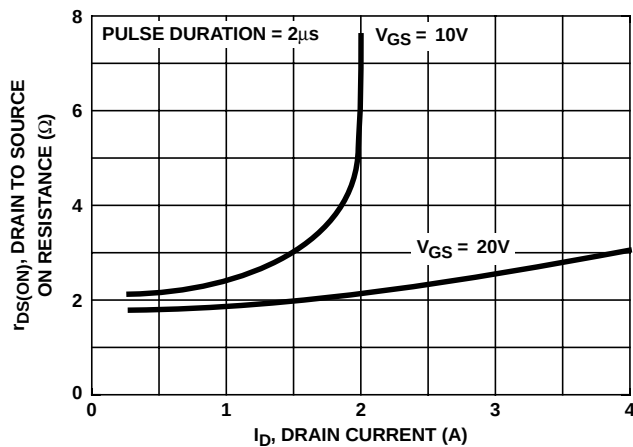


FIGURE 6. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

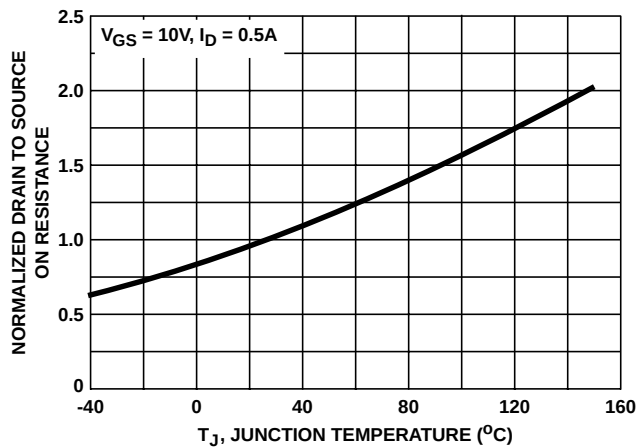


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

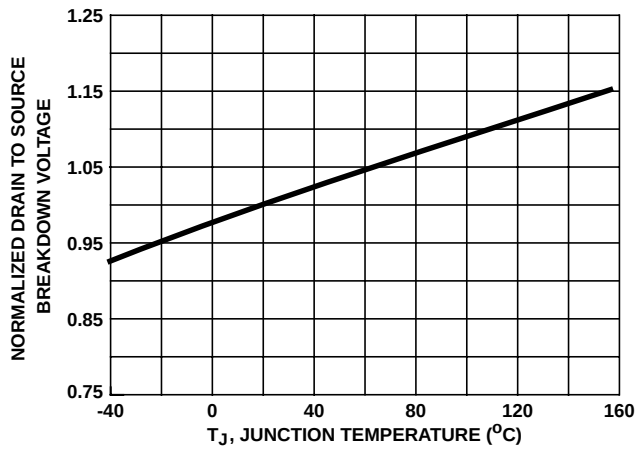


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

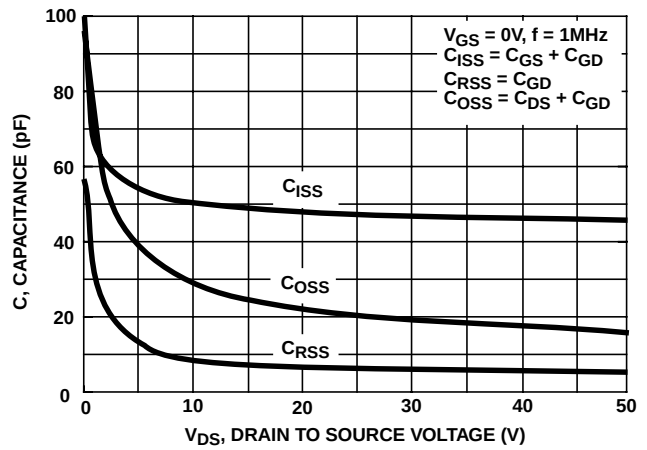


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

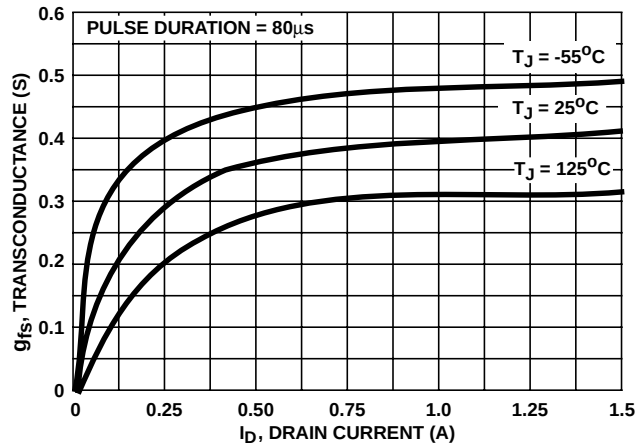


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

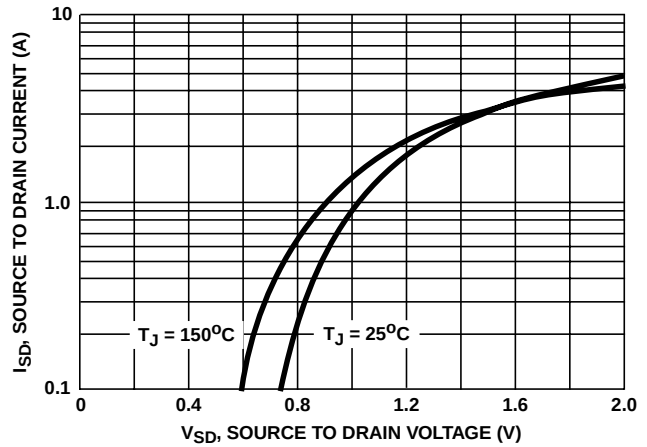


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

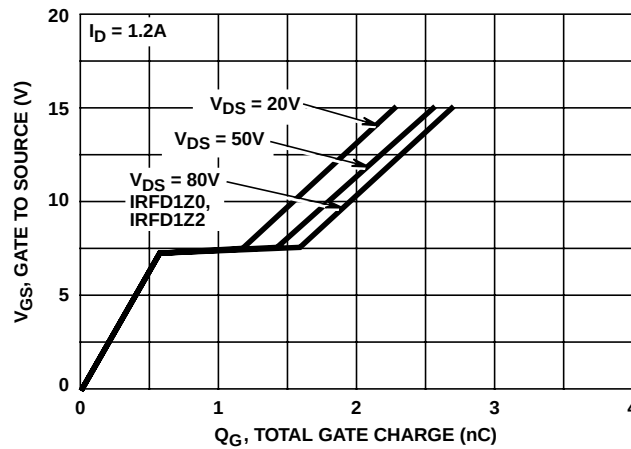


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE VOLTAGE

Test Circuits and Waveforms

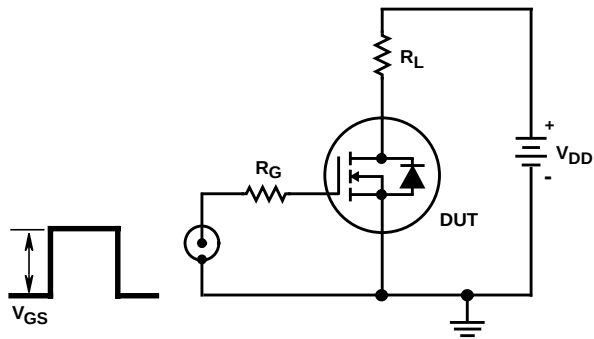


FIGURE 14. SWITCHING TIME TEST CIRCUIT

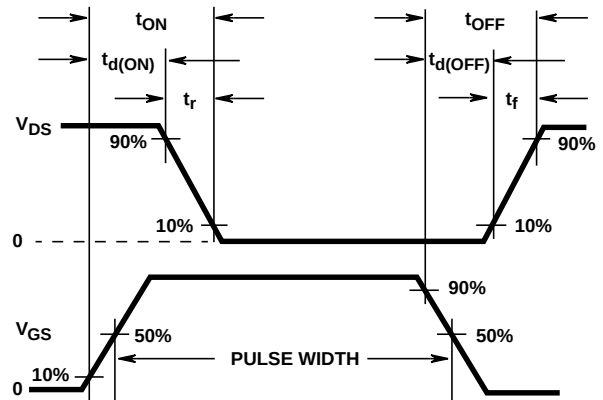


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

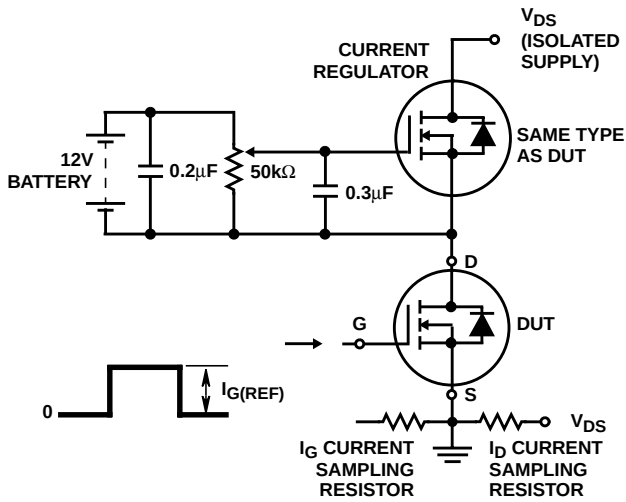


FIGURE 16. GATE CHARGE TEST CIRCUIT

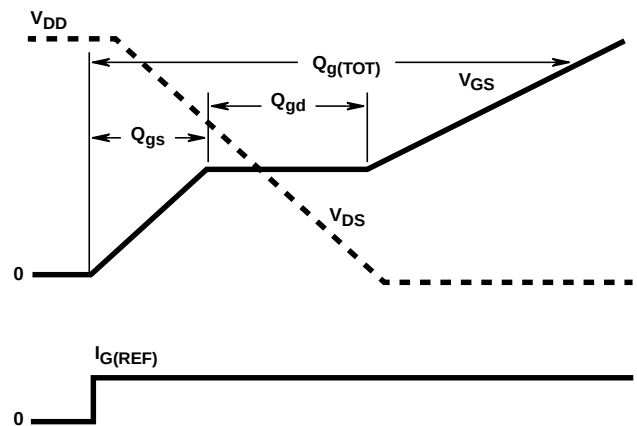


FIGURE 17. GATE CHARGE WAVEFORMS