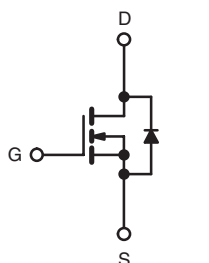
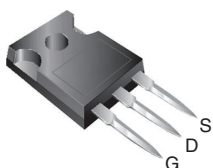


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.27
Q_g (Max.) (nC)	120	
Q_{gs} (nC)	32	
Q_{gd} (nC)	49	
Configuration	Single	

TO-247



N-Channel MOSFET

FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V V_{GS} Rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Isolated Central Mounting Hole
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Lead (Pb)-free Available



RoHS*
COMPLIANT

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Power MOSFETs technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole.

ORDERING INFORMATION

Package	TO-247
Lead (Pb)-free	IRFP460LCPbF SiHFP460LC-E3
SnPb	IRFP460LC SiHFP460LC

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	80	
Linear Derating Factor		2.2	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	960	mJ
Repetitive Avalanche Current ^a	I_{AR}	20	A
Repetitive Avalanche Energy ^a	E_{AR}	28	mJ
Maximum Power Dissipation	P_D	280	W
Peak Diode Recovery dV/dt ^c	dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 4.3\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 20\text{ A}$ (see fig. 12).
- $I_{SD} \leq 20\text{ A}$, $dI/dt \leq 160\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.45	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.59	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A ^b	-	-	0.27	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 12 A ^b		12	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	3600	-	pF
Output Capacitance	C _{oss}			-	440	-	
Reverse Transfer Capacitance	C _{rss}			-	39	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 20 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	120	nC
Gate-Source Charge	Q _{gs}			-	-	32	
Gate-Drain Charge	Q _{gd}			-	-	49	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 20 A R _G = 4.3 Ω, R _D = 12 Ω, see fig. 10 ^b		-	18	-	ns
Rise Time	t _r			-	77	-	
Turn-Off Delay Time	t _{d(off)}			-	40	-	
Fall Time	t _f			-	43	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L _S			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	80	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 20 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 20 A, dI/dt = 100 A/μs ^b		-	570	860	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	6.6	9.9	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

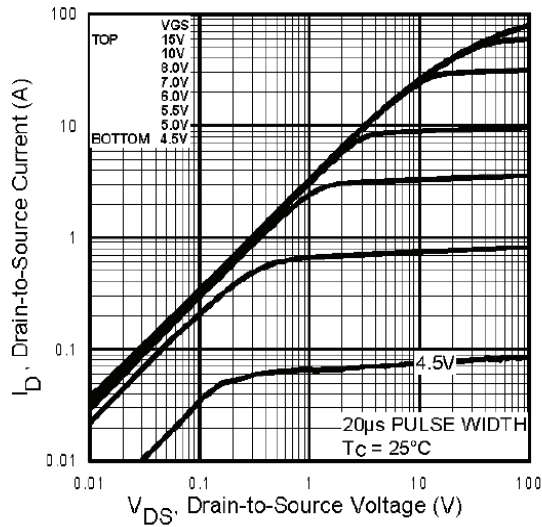


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

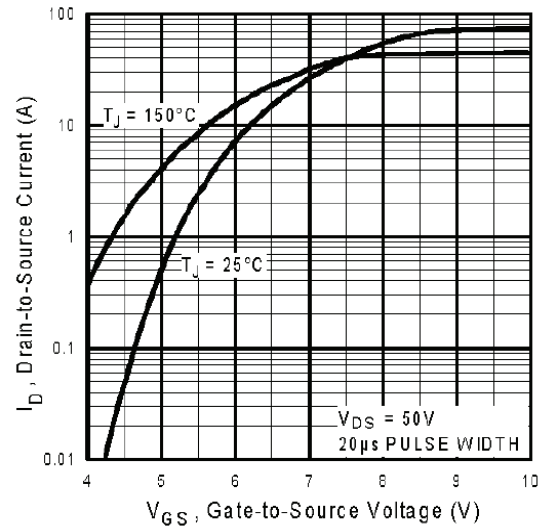


Fig. 3 - Typical Transfer Characteristics

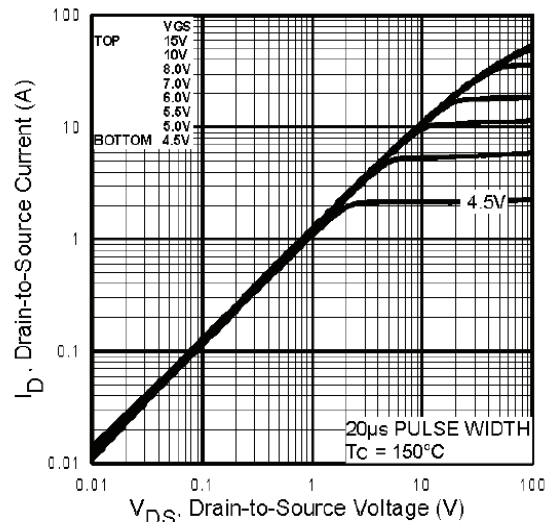


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

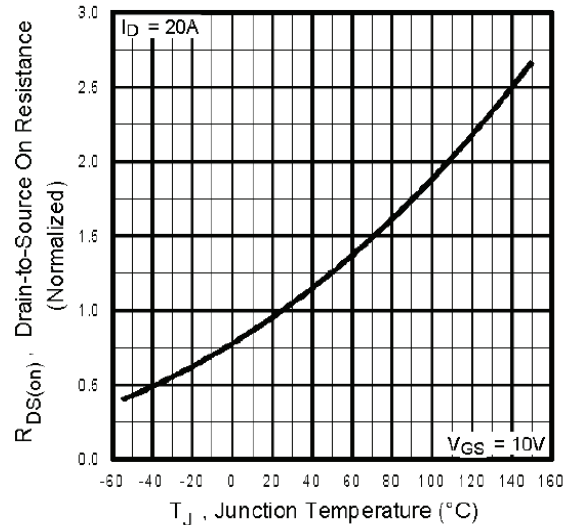


Fig. 4 - Normalized On-Resistance vs. Temperature

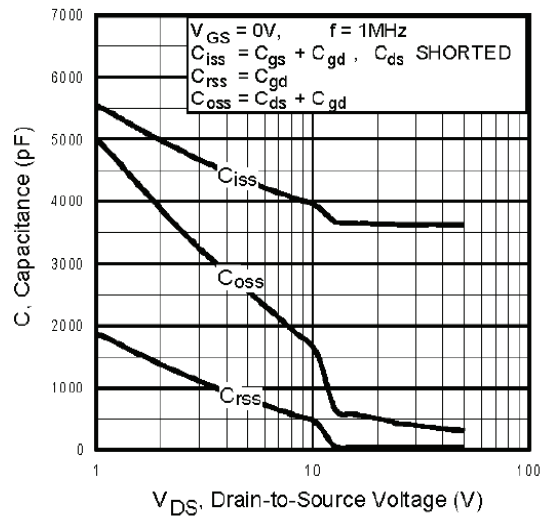


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

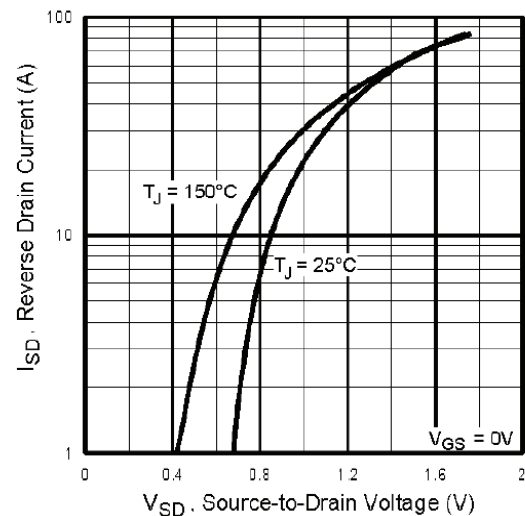


Fig. 7 - Typical Source-Drain Diode Forward Voltage

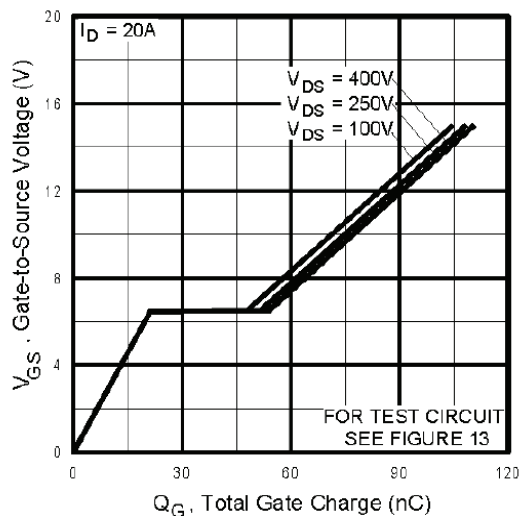


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

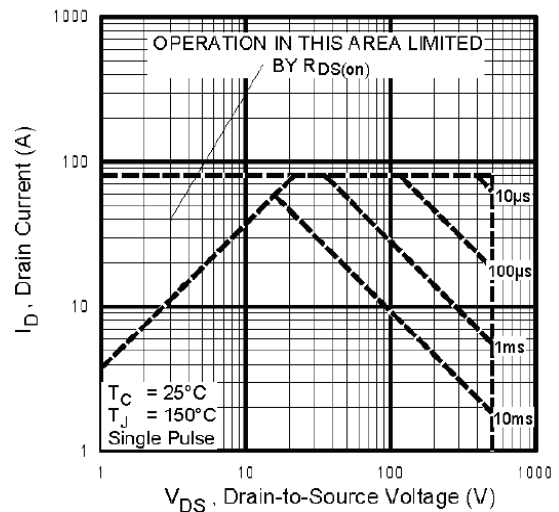


Fig. 8 - Maximum Safe Operating Area

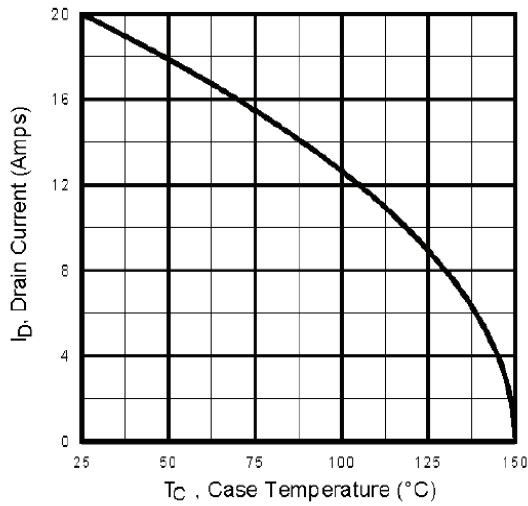


Fig. 9 - Maximum Drain Current vs. Case Temperature

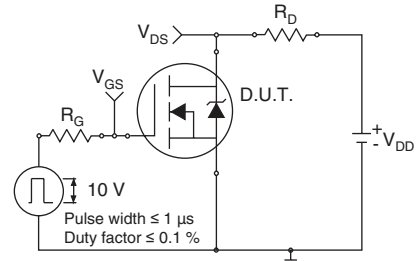


Fig. 10a - Switching Time Test Circuit

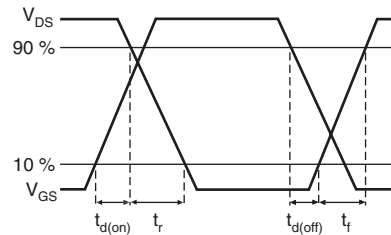


Fig. 10b - Switching Time Waveforms

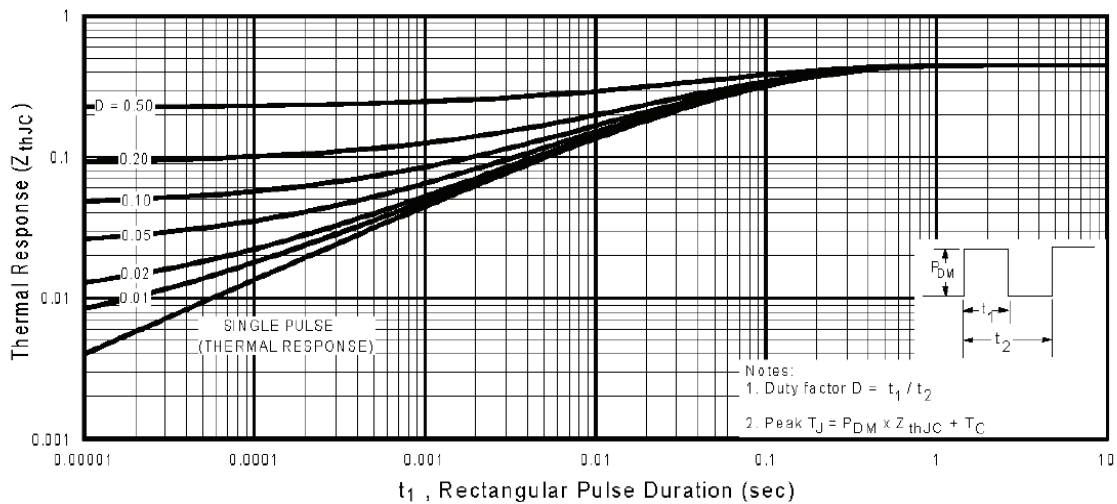


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

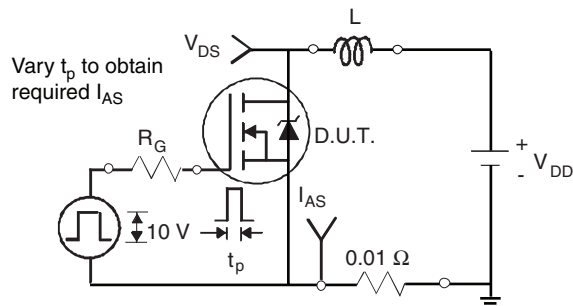


Fig. 12a - Unclamped Inductive Test Circuit

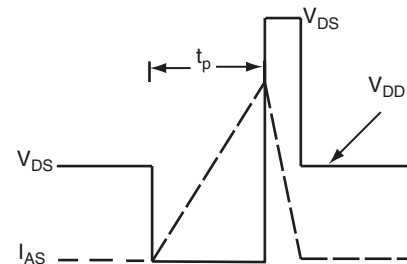


Fig. 12b - Unclamped Inductive Waveforms

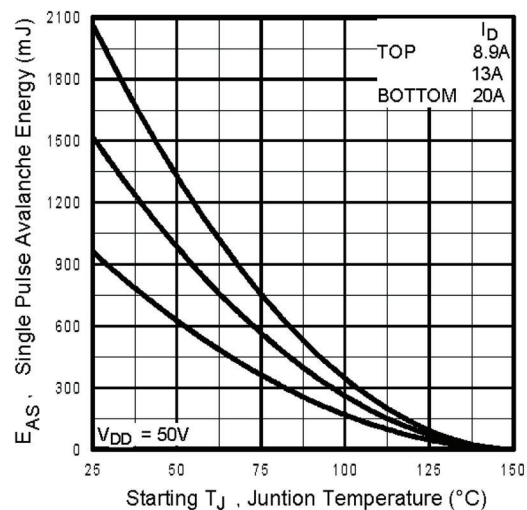


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

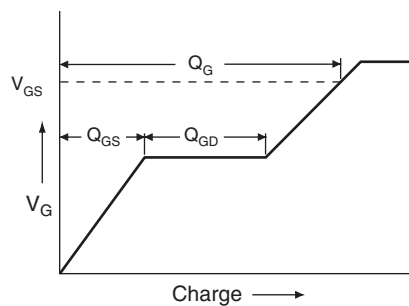


Fig. 13a - Basic Gate Charge Waveform

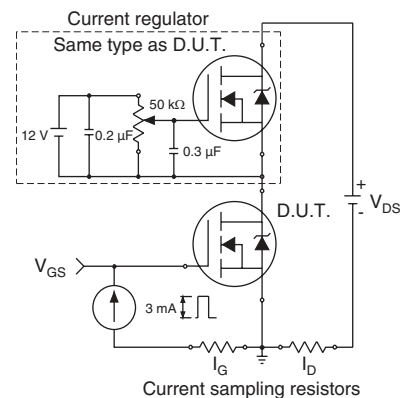


Fig. 13b - Gate Charge Test Circuit

① Driver gate drive

P.W. Period

$D = \frac{\text{P.W.}}{\text{Period}}$

$V_{GS} = 10 \text{ V}^*$

② D.U.T. I_{SD} waveform

Reverse recovery current

Body diode forward current

di/dt

③ D.U.T. V_{DS} waveform

Diode recovery dv/dt

V_{DD}

Body diode forward drop

④ Inductor current

Ripple $\leq 5\%$

I_{SD}

* $V_{GS} = 5 \text{ V}$ for logic level devices

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