

Layout Note:
net "3VPCU" and "RTD_GND"
minimum trace width 12mils.

IT8502

Note 1: Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it's output to external VDDC derived power domain circuit, this signal should be isolated by a diode such as KBR15T6 and QAO2.
(2) If it's input from external VDDC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2:
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

AJ085020PD4

7.25MHz clock lines
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

Figure 10-2. Reset Timing

Internal VSTBY POR# or WRST#

Internal EC Logic Reset#

Hardware Strap Signal

Stabilized PLL Clock

t_{VSTBY_POR}

$t_{EC_RESET\#}$

t_{STRAP}

t_{PLL_S1}

t_{PLL_S2}

Sleep mode

Wakeup from Sleep mode

t_{STRAP}

Symbol	Parameter	Min.	Typ.	Max.	Unit
t _{RSTPW}	Internal EC logic reset after VSTBY POR or WRST#	—	1650	—	Tick (by 32.768 KHz)
t _{STRAP}	Strap sampling time	0	—	—	ns
t _{PLLS1}	PLL stabilization time hardware	—	5	—	ms
t _{PLLS2}	PLL stabilization time after waking up from Sleep mode	—	5	—	ms
t _{PER}	PLL clock period	—	1/Freq _{PLL}	—	ns
Freq _{PLL}	PLL clock frequency if PLLFREQ = 0011b	—	32.3	—	MHz
	PLL clock frequency if PLLFREQ = 0101b	—	46.0	—	MHz
	PLL clock frequency if PLLFREQ = 0111b	—	64.5	—	MHz
Freq _{EC}	EC clock frequency if PLLFREQ = 0111b	—	9.2	—	MHz

Figure 10-3. Warm Reset Timing

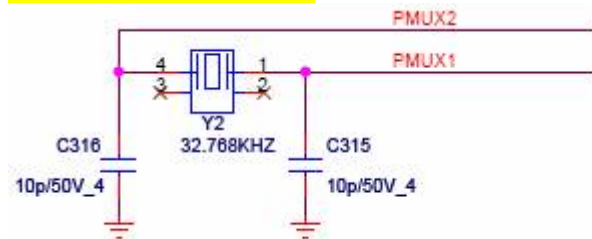


Table 10-3. Warm Reset AC Table

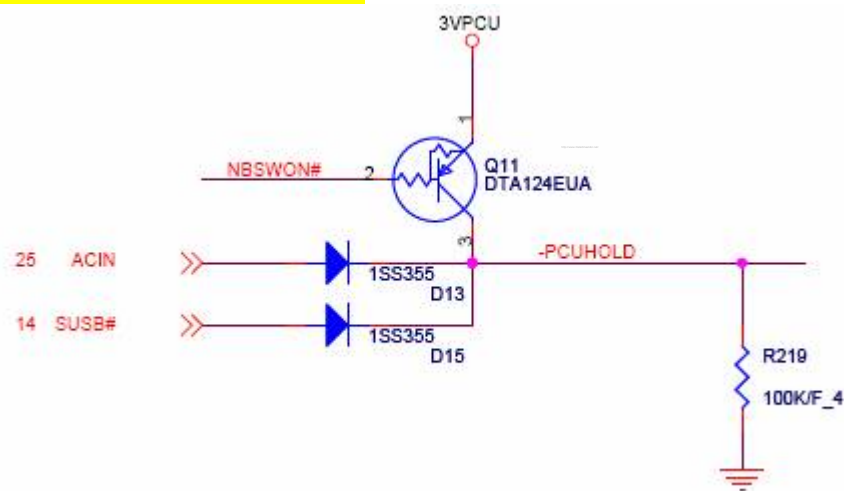
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	μs

EC 不动先确认一下几个地方：

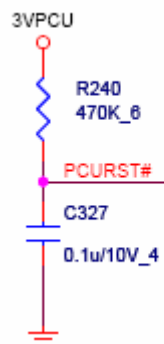
1.Y2 开机后是否有起振？



2. -PCUHOLD 是否为高电平？

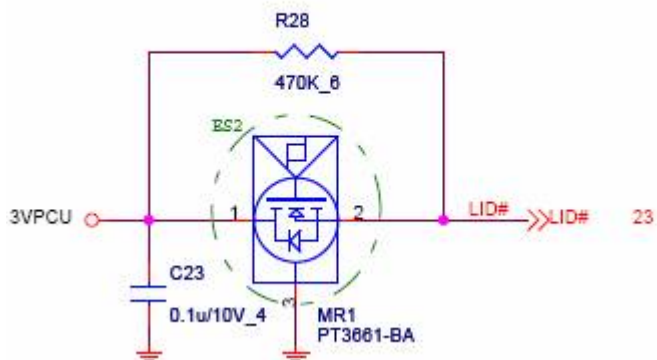


3. PCURST#信号是否为高电平？

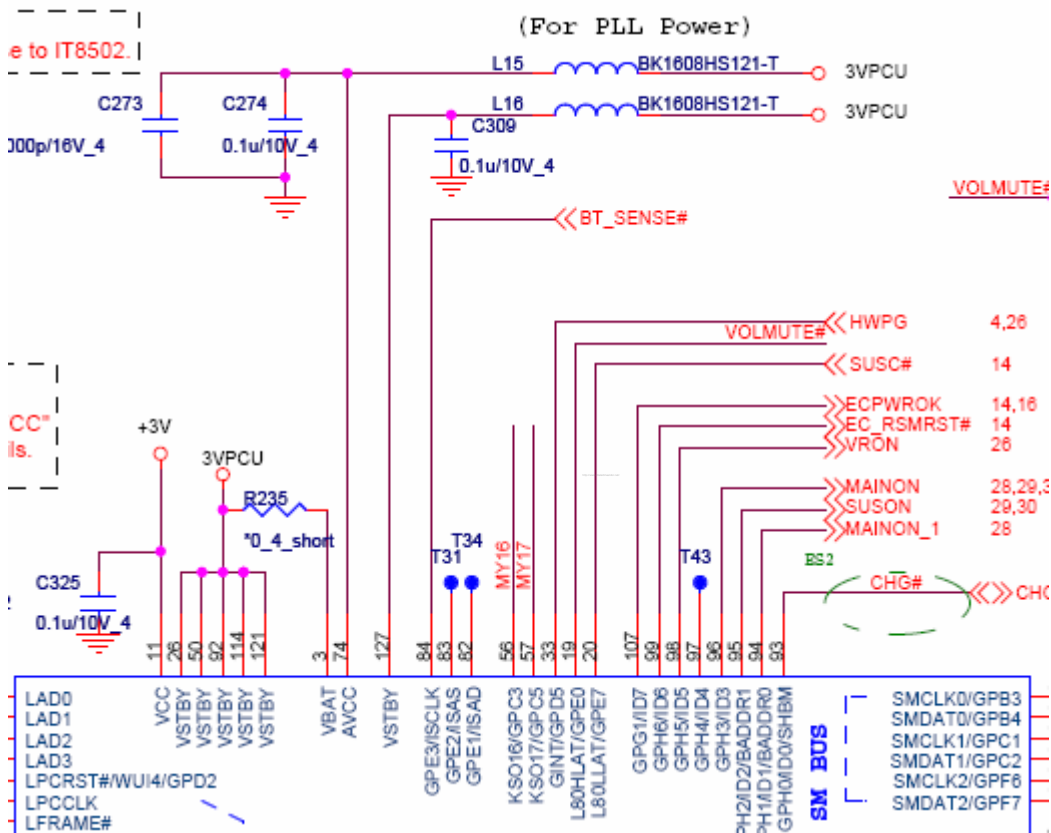


4. LID#信号是否为高电平？

HALL SENSOR



5. 3VPCU 是否正常供给 EC?



6. NBSWON#信号波形是否正常?

7. LFRAME#信号是否有动起来?