



# **JM20330**

## **Serial ATA Bridge Chip**

### **Datasheet**

*Rev. 2.3*



## Table of Contents

|                                           |    |                                              |    |
|-------------------------------------------|----|----------------------------------------------|----|
| 0. Revision History .....                 | 3  | 6.1 PIO Data-in Commands .....               | 22 |
| 1. General Description .....              | 5  | 6.2 PIO Data-Out Commands .....              | 22 |
| 2. Features .....                         | 6  | 6.3 DMA Data-In Commands .....               | 23 |
| 2.1 General .....                         | 6  | 6.4 DMA Data-Out Commands .....              | 23 |
| 2.2 Host Bridge .....                     | 6  | 6.5 Queued DMA Commands .....                | 23 |
| 2.3 Device Bridge .....                   | 6  | 6.6 PACKET/DIAG Commands .....               | 24 |
| 3. Block Diagram .....                    | 7  | 6.7 Non-Data Commands .....                  | 24 |
| 3.1 Physical Layer .....                  | 7  | 6.8 ATAPI PACKET Commands .....              | 26 |
| 3.2 Link Layer .....                      | 8  | 6.9 Vender Specific Command .....            | 29 |
| 3.3 Transport Layer .....                 | 8  | 6.10 Ultra DMA Transfer Rate .....           | 33 |
| 3.4 Application Layer .....               | 8  | 6.11 Device Mode Master-Only Operation ..... | 34 |
| 4. Package .....                          | 9  | 7. UART Interface Operation .....            | 35 |
| 4.1 Package Dimensions .....              | 9  | 7.1 UART Interface .....                     | 35 |
| 4.1.1 TQFP 64 .....                       | 9  | 7.2 SCR and Control Register Map .....       | 37 |
| 4.1.2 QFN 64 .....                        | 10 | 7.3 Register Description .....               | 39 |
| 4.2 Package Pin-Out .....                 | 12 | 8. Electrical Characteristics .....          | 43 |
| 4.3 Pin List Table .....                  | 13 | 8.1 Power Requirements .....                 | 43 |
| 5. Pin Description .....                  | 14 | 8.2 Absolute Maximum Ratings .....           | 43 |
| 5.1 Pin Type Definition .....             | 14 | 8.3 Typical Operation Conditions .....       | 43 |
| 5.2 Serial ATA Interface .....            | 15 | 8.4 DC Characteristics .....                 | 44 |
| 5.3 Parallel ATA Interface .....          | 16 | 8.5 ATA I/O DC Characteristics .....         | 44 |
| 5.4 Power Supply .....                    | 18 | 8.6 ATA I/O AC Characteristics .....         | 44 |
| 5.5 Configuration Interface .....         | 19 | 9. Power-on Reset Sequence .....             | 45 |
| 5.6 Parallel ATA Reverse Order .....      | 21 |                                              |    |
| 6. Supported ATA/ATAPI Command List ..... | 22 |                                              |    |



## 0. Revision History

| Version       | Date       | Revision Description                                                                                                                                                                                                                                                   |
|---------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preliminary   | 2004-08-05 | 1. Initial B2 version                                                                                                                                                                                                                                                  |
| Preliminary 1 | 2004-08-27 | 1. Provide internal weak pull-low (Typical 31 K $\Omega$ ) & internal weak pull-high (Typical 31 K $\Omega$ ).                                                                                                                                                         |
| 2.0           | 2005-01-20 | 1. Support Multiple-Word DMA.<br>2. Modify the description of signals HSTROBE and DSTROBE.<br>3. Modify the 6-10 Ultra DMA Transfer Rate to only support 150Mhz operation.<br>4. Extend the ACTL from 20 bits to 40 bits.                                              |
| 2.1           | 2005-03-10 | 1. Modify Absolute Maximum Ratings voltage and current.                                                                                                                                                                                                                |
| 2.2           | 2006-01-11 | 1. Add description of crystal Oscillator in page 14<br>2. Add industry spec. description in section 8.3                                                                                                                                                                |
| 2.3           | 2006-07-20 | 1. Add power on sequence.<br>2. Modify Absolute Maximum Ratings voltage and current.<br>3. Change the minimum commercial ambient operation temperature from -10 to 0.<br>4. Revised REXT 12K $\Omega$ 1%<br>5. Add 6.11 section for device mode master-only operation. |
|               |            |                                                                                                                                                                                                                                                                        |



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Printed in Taiwan 2003

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## **1. General Description**

The Serial ATA Bridge is a single chip solution for serial and parallel ATA translation. It includes the Serial ATA PHY, Link, Transport, and parallel ATA (application layer) controller. The main applications are for legacy IDE storage devices connecting to newer chipset supporting serial ATA, such as the iCH5 south bridge of Intel chipset, and serial ATA IDE storage devices connecting to traditional IDE south bridge.

The Serial ATA physical, link, and transport layer are compliance to Serial ATA Generation 1, which supports a 1.5Gbps data rate. The application layer supports both the ATA register command set and PACKET command set, which could drive both the Hard Disk Drive and ATAPI Optical Storage such as CR-ROM, CD-RW, DVD-ROM, DVD-RW, etc. The serial ATA and application layer support both device and host operation and could be configured by a simple HOST/DEVICE pin.

This chip is designed by 0.18um CMOS technology and 64-pin TQFP or QFN package.



## **2. Features**

### **2.1 General**

- 0.18um CMOS technology.
- Serial ATA 1.5Gbps (Gen. 1) PHY.
- Spread-Spectrum Clock (SSC) technology.
- 1.8V and 3.3V power system.
- 25MHz external reference clock.
- 64-pin TQFP and QFN packages.

### **2.2 Host Bridge**

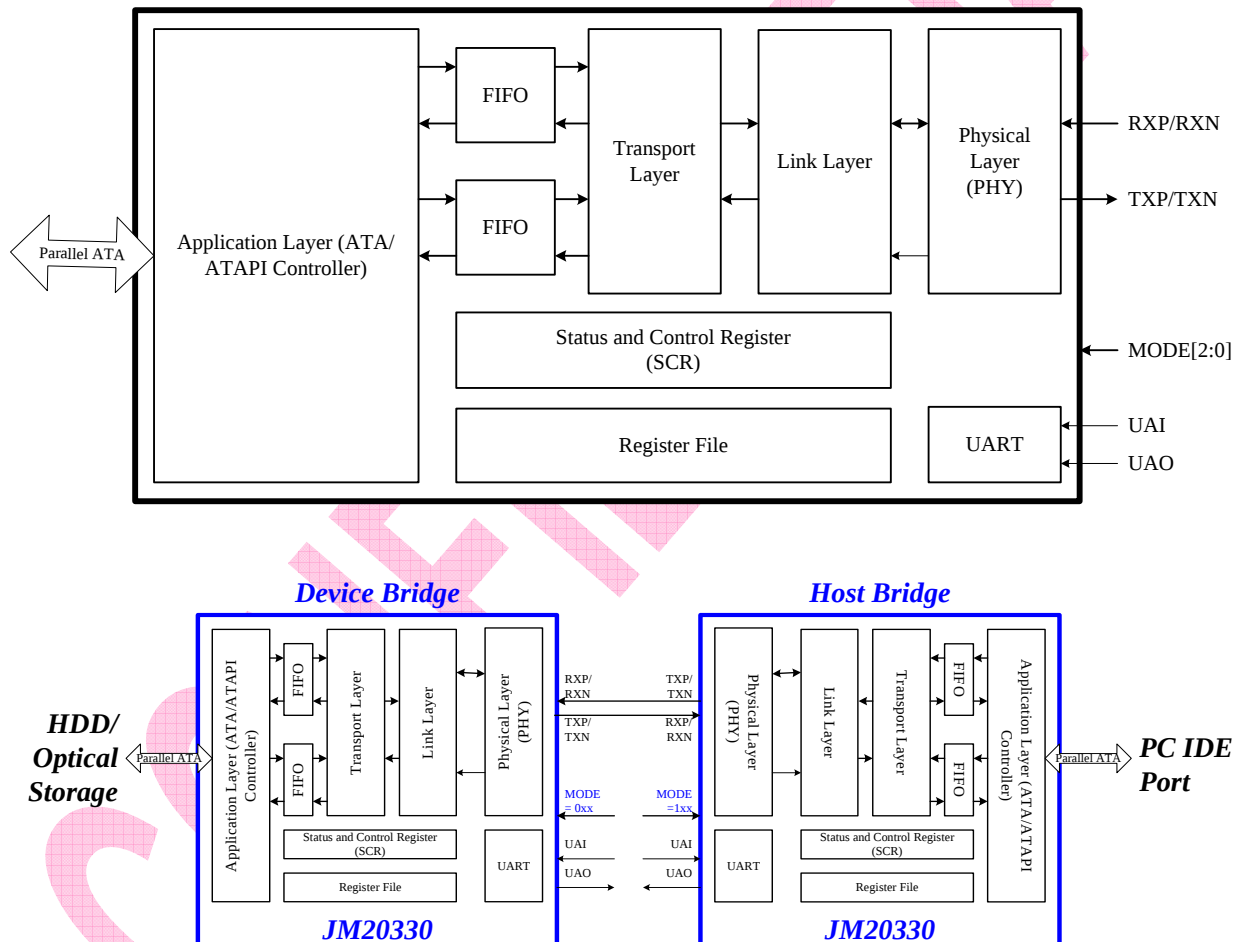
- ATA/ATAPI PIO mode 0 to 4.
- ATA/ATAPI Multiple-Word DMA 0 to 2.
- ATA/ATAPI Ultra DMA of transfer rate 16.7, 25, 33, 48, 66, 100, 133, and 150MB/s.
- ATA/ATAPI master/slave emulation.
- ATA/ATAPI PACKET command feature set.
- ATA/ATAPI-7 Force Unit Access feature set.
- ATA/ATAPI-7 Streaming feature set.
- ATA/ATAPI LBA48 addressing mode associated with 2-byte sector count.
- Serial ATA power saving modes.
- Serial ATA BIST operation.
- Serial ATA hot-plug.
- SATA II Asynchronous Signal Recovery support.

### **2.3 Device Bridge**

- ATA/ATAPI PIO mode 0 to 4.
- ATA/ATAPI Multiple-Word DMA 0 to 2.
- ATA/ATAPI Ultra DMA of transfer rate 16.7, 25, 33, 48, 66, 100, 133, and 150MB/s.
- ATA/ATAPI PACKET command feature set.
- ATA/ATAPI-7 Force Unit Access feature set.
- ATA/ATAPI-7 Streaming feature set.
- ATA/ATAPI LBA48 addressing mode associated with 2-byte sector count.

- Serial ATA power saving modes.
- Serial ATA BIST operation.
- Serial ATA hot-plug.
- SATA II Asynchronous Signal Recovery support.

### 3. Block Diagram



#### 3.1 Physical Layer

The physical layer provides serialization/de-serialization transformation between serial data bus and link layer. It also includes an OOB block to detect COMRESET/COMINIT and COMWAKE for serial bus power on initialization and hot-plug.



### **3.2 Link Layer**

The link layer performs frame envelope encoding and decoding. It receives the frame instruction from transport layer, and generates the necessary primitive for serial link flow control. While receiving data, it detects the primitive and performs the front-end operation to extract the useful frame data for transport layer. It also generates CRC for serial link error handling, and provides 8b/10b data scramble for data transfer.

### **3.3 Transport Layer**

The transfer layer performs frame information structure assembly and decomposition. It also includes FIFO to adjust the speed mismatch between application layer and serial link.

### **3.4 Application Layer**

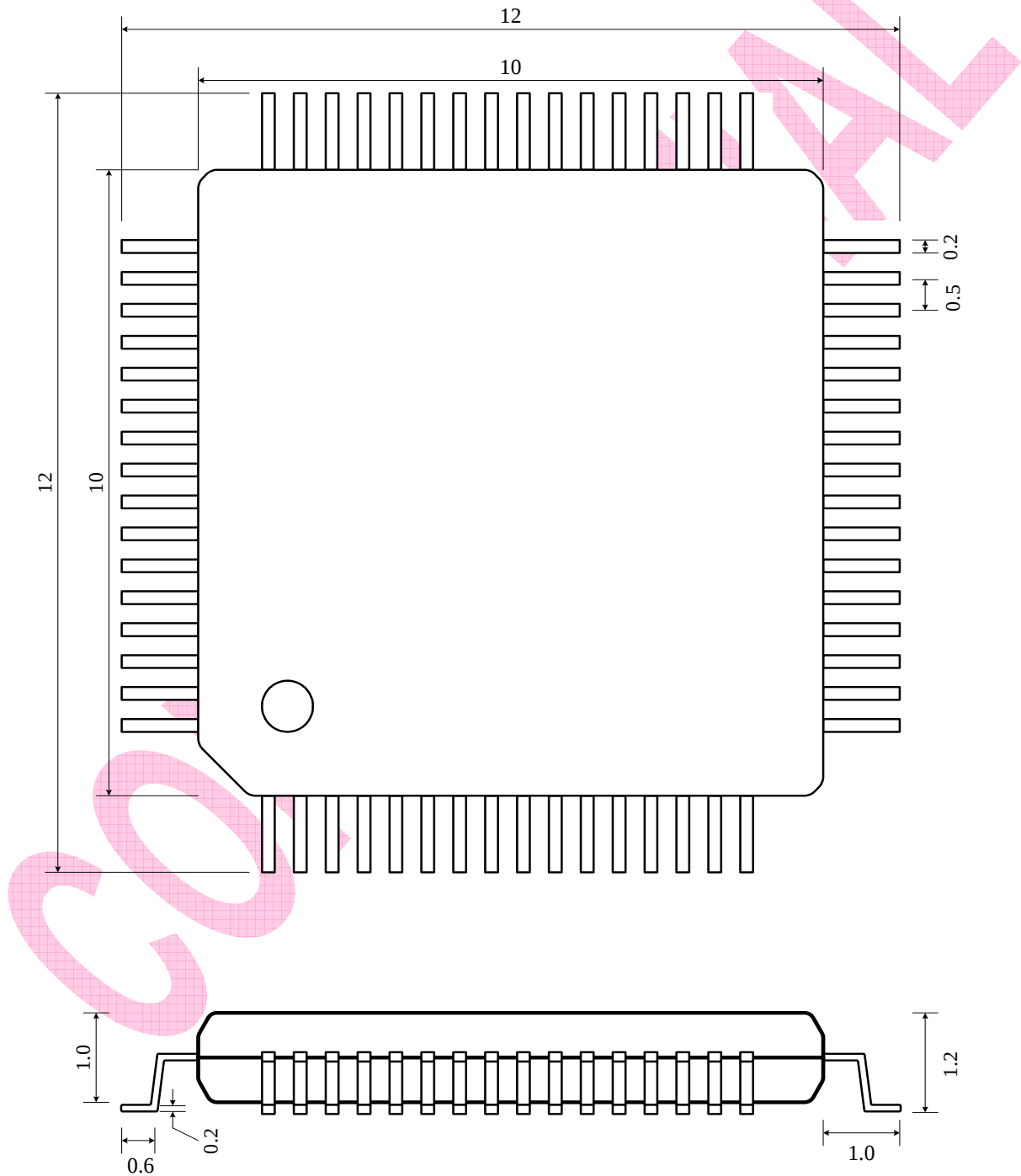
The application layer is essentially an ATA/ATAPI protocol engine, which complies with ATA/ATAPI-7. It performs the protocol and timing control for parallel ATA and ATAPI command set.



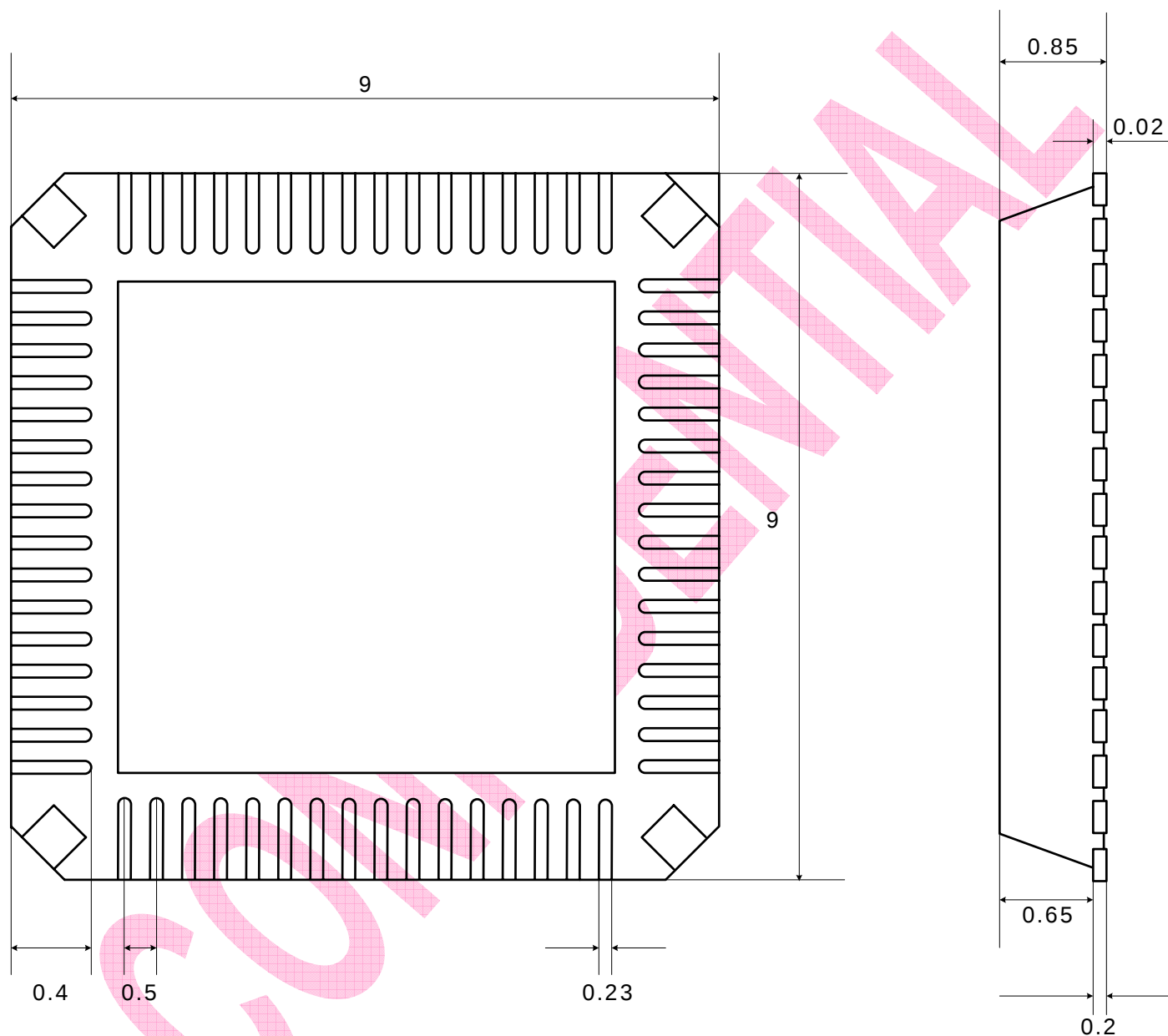
## 4. Package

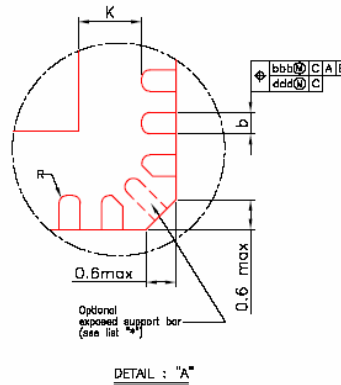
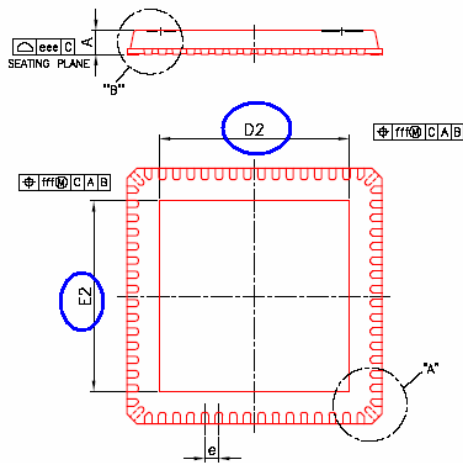
### 4.1 Package Dimensions

#### 4.1.1 TQFP 64



### 4.1.2 QFN 64





NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

| L/F | Exposed Pad Size |      |      |              |       |       | * |
|-----|------------------|------|------|--------------|-------|-------|---|
|     | D2/E2 (mm)       |      |      | D2/E2 (inch) |       |       |   |
|     | MIN              | NOM  | MAX  | MIN          | NOM   | MAX   |   |
| ①   | 6.90             | 7.05 | 7.20 | 0.272        | 0.278 | 0.283 | Y |
| ②   | 6.70             | 6.85 | 7.00 | 0.264        | 0.270 | 0.276 | N |
| ③   | 3.64             | 3.79 | 3.94 | 0.143        | 0.149 | 0.155 | N |
| ④   | 5.49             | 5.64 | 5.79 | 0.216        | 0.222 | 0.228 | N |
| ⑤   | 6.75             | 6.90 | 7.05 | 0.266        | 0.272 | 0.278 | N |

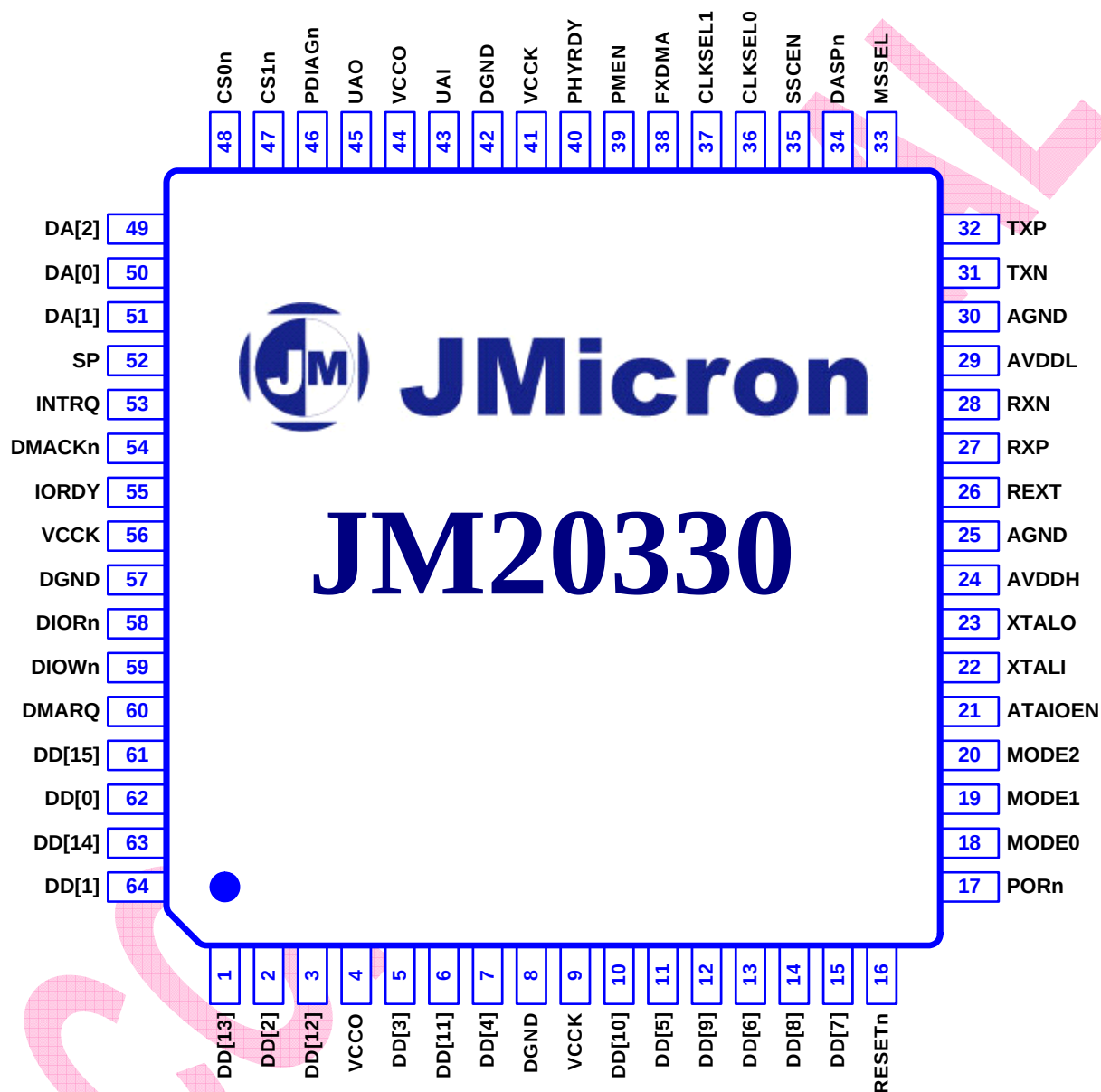
TITLE : 64LD QFN (9X9 mm) PACKAGE OUTLINE

L/F MATERIAL : A194 FH

|       |                          |         |                  |
|-------|--------------------------|---------|------------------|
| APPR. | F.D.Tang                 | DWG NO. | CE064-SW1        |
| ENG.  | Albert Lee<br>Terry Tsai | REV NO. | D                |
| QM.   | STI Inc                  | PRODUCT | CE0643A, CE0641B |



## 4.2 Package Pin-Out





### 4.3 Pin List Table

| No. | Pin Name | No. | Pin Name | No. | Pin Name | No. | Pin Name |
|-----|----------|-----|----------|-----|----------|-----|----------|
| 1   | DD13     | 17  | PORn     | 33  | MSSEL    | 49  | DA2      |
| 2   | DD2      | 18  | MODE0    | 34  | DASPN    | 50  | DA0      |
| 3   | DD12     | 19  | MODE1    | 35  | SSCEN    | 51  | DA1      |
| 4   | VCCO     | 20  | MODE2    | 36  | CLKSEL0  | 52  | SP       |
| 5   | DD3      | 21  | ATAIOEN  | 37  | CLKSEL1  | 53  | INTRQ    |
| 6   | DD11     | 22  | XTALI    | 38  | FXDMA    | 54  | DMACKn   |
| 7   | DD4      | 23  | XTALO    | 39  | PMEN     | 55  | IORDY    |
| 8   | DGND     | 24  | AVDDH    | 40  | PHYRDY   | 56  | VCCK     |
| 9   | VCCK     | 25  | AGND     | 41  | VCCK     | 57  | DGND     |
| 10  | DD10     | 26  | REXT     | 42  | DGND     | 58  | DIORn    |
| 11  | DD5      | 27  | RXP      | 43  | UAI      | 59  | DIOWn    |
| 12  | DD9      | 28  | RXN      | 44  | VCCO     | 60  | DMARQ    |
| 13  | DD6      | 29  | AVDDL    | 45  | UAO      | 61  | DD15     |
| 14  | DD8      | 30  | AGND     | 46  | PDIAGn   | 62  | DD0      |
| 15  | DD7      | 31  | TXN      | 47  | CS1n     | 63  | DD14     |
| 16  | RESETn   | 32  | TXP      | 48  | CS0n     | 64  | DD1      |



## 5. Pin Description

### 5.1 Pin Type Definition

| Pin Type | Definition                                       |
|----------|--------------------------------------------------|
| A        | Analog                                           |
| D        | Digital                                          |
| I        | Input                                            |
| O        | Output                                           |
| IO       | Bi-directional                                   |
| L        | Internal weak pull-low (Typical 31 K $\Omega$ )  |
| H        | Internal weak pull-high (Typical 31 K $\Omega$ ) |



## 5.2 Serial ATA Interface

| Signal Name | Pin Number | Type | Description                                                                                                                                             |
|-------------|------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| XTALI/OSCI  | 22         | AI   | <b>Crystal Input/Oscillator Input.</b> It is connected to an external 1.8V/3.3V crystal/oscillator. The clock rate is 25MHz.<br>Freq tolerance +-100ppm |
| XTALO       | 23         | AO   | <b>Crystal Output.</b> It is connected to an external crystal.                                                                                          |
| REXT        | 26         | AI   | <b>External Reference Resistance.</b> An external 12K $\Omega$ 1% resistor should be connected and bypass to the analog ground.                         |
| RXP         | 27         | AI   | <b>Serial Data Receiver.</b> It receives positive input of differential signal.                                                                         |
| RXN         | 28         | AI   | <b>Serial Data Receiver.</b> It receives negative input of differential signal.                                                                         |
| TXP         | 32         | AO   | <b>Serial Data Transmitter.</b> It transmits positive output of differential signal.                                                                    |
| TXN         | 31         | AO   | <b>Serial Data Transmitter.</b> It transmits negative output of differential signal.                                                                    |



### 5.3 Parallel ATA Interface

| Signal Name                             | Pin Number                                        | Type       | Description                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------------------|---------------------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DD[15:0]</b>                         | 61,63,1,3,6,10,12,<br>14,15,13,11,7,5,2,<br>64,62 | DIO<br>8mA | <b>Data Bus.</b> This is a bi-directional data bus for a host and a device to transfer data, command, and status.                                                                                                                                                                                                                                                                    |
| <b>CSn[1:0]</b>                         | 47,48                                             | DIO<br>8mA | <b>Chip Select.</b> Active-low signals from a host to select a Command Block or Control Block register of a device.                                                                                                                                                                                                                                                                  |
| <b>DA[2:0]</b>                          | 49, 51,50                                         | DIO<br>4mA | <b>Device Address.</b> Address signals from a host to access a register or data port of the device.                                                                                                                                                                                                                                                                                  |
| <b>DIORn/<br/>HDMARDYn/<br/>HSTROBE</b> | 58                                                | DIO<br>8mA | <b>IO Read/Ultra DMA Ready/Ultra DMA Data Strobe.</b><br><b>DIORn:</b> Active-low signal from a host to read a register or data port of a device.<br><b>HDMARDYn:</b> Active-low signal from a host to indicate its ready to receive Ultra DMA data-in burst from a device.<br><b>HSTROBE:</b> Signal from a host to latch data into a device at Ultra DMA data-out operation.       |
| <b>DIOWn/<br/>STOP</b>                  | 59                                                | DIO<br>8mA | <b>IO Write/Stop Ultra DMA Burst.</b><br><b>DIOWn:</b> Active-low signal from a host to write a register or data port of a device.<br><b>STOP:</b> Active-high signal from a host to terminate an Ultra DMA transfer.                                                                                                                                                                |
| <b>DMACKn</b>                           | 54                                                | DIO<br>8mA | <b>DMA Acknowledge.</b> Active-low signal from a host to acknowledge the DMA request from a device.                                                                                                                                                                                                                                                                                  |
| <b>DMARQ</b>                            | 60                                                | DIO<br>8mA | <b>DMA Request.</b> Active-high signal from a device to request a DMA transfer.                                                                                                                                                                                                                                                                                                      |
| <b>INTRQ</b>                            | 53                                                | DIO<br>8mA | <b>Device Interrupt.</b> Active-high signal from a device to interrupt a host.                                                                                                                                                                                                                                                                                                       |
| <b>IORDY/<br/>DDMARDYn/<br/>DSTROBE</b> | 55                                                | DIO<br>8mA | <b>IO Ready/Ultra DMA Ready/Ultra DMA Data Strobe.</b><br><b>IORDY:</b> Active-high signal from a device to extend the host cycle time for operation at PIO mode 3 and above.<br><b>DDMARDYn:</b> Active-low signal from a device used to indicate its ready to receive Ultra DMA data-out burst from a host.<br><b>DSTROBE:</b> Signal from a device used to latch data into a host |



| Signal Name               | Pin Number | Type        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           |            |             | at Ultra DMA data-in operation.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>PDIAGn/<br/>PATAOR</b> | 46         | DIOH<br>8mA | <b>Diagnostic Signal.</b><br>In Host Bridge mode: <b>PDIAGn</b> provides the diagnostic signals from device 1 to device 0 to indicate the device 1 diagnosis is complete.<br>In Device mode: <b>PATAOR</b> defines the pin order of parallel ATA interface. (see 5.6)<br>0: ATA interface signals in Normal Order mode.<br>1: ATA interface signals in Reverse Order mode.                                                                                           |
| <b>RESETn</b>             | 16         | DIO<br>8mA  | <b>Hardware Reset.</b> Active-low signal from a host to reset a device.                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>DASPN/GPIO0</b>        | 34         | DIOH<br>8mA | <b>Slave Device Present.</b> Active-low signal from Device 1 to Device 0 in Host Bridge mode to indicate the presence of slave device. In Device 0 configuration, this pin is an input. In Device 1 configuration, it is an output. This pin is used as slave present indicator at ATA power on device diagnostics phase, and used as device activity at command or data transfer. In Device Bridge mode, the pin will output bit3 of parallel ATA control register. |
| <b>SP/GPIO2</b>           | 52         | DIOL<br>4mA | <b>Slave Device Present.</b> Active-high signal from Device 1 to Device 0 in Host Bridge mode to indicate the presence of slave device. In Device 0 configuration, this pin is an input. In Device 1 configuration, it is an output. In Device Bridge mode, the pin will output bit5 of parallel ATA control register.                                                                                                                                               |



## 5.4 Power Supply

| Signal | Pin Number | Type | Description                                                                                                   |
|--------|------------|------|---------------------------------------------------------------------------------------------------------------|
| AVDDH  | 24         | AI   | <b>Analog Power.</b> Analog 3.3V power supply. It should be bypassed to ground by a 0.1uF capacitance.        |
| AVDDL  | 29         | AI   | <b>Analog Power.</b> Analog 1.8V power supply. It should be bypassed to ground by a 0.1uF capacitance.        |
| AGND   | 25,30      | AI   | <b>Analog Ground.</b>                                                                                         |
| VCCO   | 4,44       | DI   | <b>Digital IO Power.</b> Digital 3.3V power supply. It should be bypassed to ground by a 0.1uF capacitance.   |
| VCKK   | 9,41,56    | DI   | <b>Digital Core Power.</b> Digital 1.8V power supply. It should be bypassed to ground by a 0.1uF capacitance. |
| DGND   | 8,42,57    | DI   | <b>Digital ground.</b>                                                                                        |



## 5.5 Configuration Interface

| Signal Name     | Pin Number | Type                     | Description                                                                                                                                                                                                                                                                                |
|-----------------|------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PORn            | 17         | DIH<br>4mA               | <b>Power On Reset.</b> Low-active global reset. It should be connected to an external RC to build the power on initialization.                                                                                                                                                             |
| SSCEN           | 35         | DIL<br>4mA               | <b>Spread Spectrum Clock Enable.</b><br>0: Disable SATA spread spectrum clocking. (default)<br>1: Enable SATA spread spectrum clocking.                                                                                                                                                    |
| CLKSEL[1:0]     | 37,<br>36  | DIL<br>DIH<br>4mA        | <b>Reference Clock Selection.</b><br>01: 25MHz external reference clock.<br>others: reserved.                                                                                                                                                                                              |
| PHYRDY          | 40         | DO<br>4mA                | <b>Physical Layer Ready.</b><br>0: Serial ATA physical layer communication is not established.<br>1: Serial ATA physical layer communication is established.                                                                                                                               |
| MODE[2:0]       | 20,19,18   | DIL<br>DIH<br>DIL<br>4mA | <b>Operation Mode.</b> Set host/device and Ultra DMA operation mode.<br>000: Device Mode 100MB/s.<br>001: Device Mode 133MB/s.<br>010: Device Mode 150MB/s. (default)<br>011: Reserved.<br>100: Host Mode 100MB/s.<br>101: Host Mode 133MB/s.<br>110: Host Mode 150MB/s.<br>111: Reserved. |
| MSSEL/<br>GPIO1 | 33         | DIOL<br>4mA              | <b>Master/Slave Selection.</b><br>In Host Bridge mode:<br>0: Device 0 configuration. (default)<br>1: Device 1 configuration.<br>In Device Bridge mode, the pin will output bit4 of parallel ATA control register.                                                                          |
| FXDMA           | 38         | DIL<br>4mA               | <b>Fixed UDMA Data Rate.</b><br>0: Adjustable Ultra DMA data rate according to Set Feature command.                                                                                                                                                                                        |



| Signal Name    | Pin Number | Type       | Description                                                                                                                                                                                                                                        |
|----------------|------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                |            |            | 1: Negate Set Feature command, and fix Ultra DMA data rate specified by <b>MODE[1:0]</b> setting.                                                                                                                                                  |
| <b>ATAIOEN</b> | 21         | DIH<br>4mA | <b>ATA IO Interface Enable.</b><br>0: Disable the ATA output pins.<br>1: Enable the ATA output pins.                                                                                                                                               |
| <b>PMEN</b>    | 39         | DIH<br>4mA | <b>Power Management Command Enable.</b><br>0: Disable translating ATA Power Management feature command to Serial ATA Partial or Slumber mode.<br>1: Enable translating ATA Power Management feature command to Serial ATA Partial or Slumber mode. |
| <b>UAI</b>     | 43         | DIH<br>4mA | <b>On-chip UART input.</b>                                                                                                                                                                                                                         |
| <b>UAO</b>     | 45         | DOH<br>4mA | <b>On-chip UART output.</b>                                                                                                                                                                                                                        |



## 5.6 Parallel ATA Reverse Order

The parallel ATA pin order is determined by **PDIAGn/PATAOR** in device bridge mode. The pin-out in reverse order is shown below.

| Pin | Normal Order | Reverse Order | Pin | Normal Order | Reverse Order |
|-----|--------------|---------------|-----|--------------|---------------|
| 1   | DD13         | DD0           | 48  | CS0n         | DD7           |
| 2   | DD2          | DD15          | 49  | DA2          | DD8           |
| 3   | DD12         | DMARQ         | 50  | DA0          | DD6           |
| 5   | DD3          | DIOWn         | 51  | DA1          | DD9           |
| 6   | DD11         | DIORn         | 52  | SP           | DD5           |
| 7   | DD4          | DMACKn        | 53  | INTRQ        | DD10          |
| 10  | DD10         | INTRQ         | 54  | DMACKn       | DD4           |
| 11  | DD5          | SP            | 55  | IORDY        | IORDY         |
| 12  | DD9          | DA1           | 58  | DIORn        | DD11          |
| 13  | DD6          | DA0           | 59  | DIOWn        | DD3           |
| 14  | DD8          | DA2           | 60  | DMARQ        | DD12          |
| 15  | DD7          | CS0n          | 61  | DD15         | DD2           |
| 16  | RESETn       | CS1n          | 62  | DD0          | DD13          |
| 34  | DASPn        | DASPn         | 63  | DD14         | DD1           |
| 47  | CS1n         | RESETn        | 64  | DD1          | DD14          |



## 6. Supported ATA/ATAPI Command List

### 6.1 PIO Data-in Commands

| Command                         | Code     | Support |
|---------------------------------|----------|---------|
| CFA TRANSLATE SECTOR            | 87h      | NO      |
| DEVICE CONFIGURATION IDENTIFY   | B1h(C2h) | YES     |
| IDENTIFY DEVICE                 | ECh      | YES     |
| IDENTIFY COMPONENT              | D0h      | YES     |
| IDENTIFY PACKET DEVICE          | A1h      | YES     |
| READ BUFFER                     | E4h      | YES     |
| READ LOG EXT                    | 2Fh      | YES     |
| READ MULTIPLE                   | C4h      | YES     |
| READ MULTIPLE EXT               | 29h      | YES     |
| READ SECTOR(S)                  | 20h/21h  | YES     |
| READ SECTOR(S) EXT              | 24h      | YES     |
| READ LONG                       | 22h/23h  | YES     |
| SMART READ DATA                 | B0h(D0h) | YES     |
| SMART READ ATTRIBUTE THRESHOLDS | B0h(D1h) | YES     |
| SMART READ LOG                  | B0h(D5h) | YES     |

### 6.2 PIO Data-Out Commands

| Command                          | Code     | Support |
|----------------------------------|----------|---------|
| CFA WRITE MULTIPLE WITHOUT ERASE | CDh      | NO      |
| CFA WRITE SECTORS WITHOUT ERASE  | 38h      | NO      |
| DEVICE CONFIGURATION SET         | B1h(C3h) | YES     |
| DOWNLOAD MICROCODE               | 92h      | YES     |
| SECURITY DISABLE PASSWORD        | F6h      | YES     |
| SECURITY ERASE UNIT              | F4h      | YES     |
| SECURITY SET PASSWORD            | F1h      | YES     |
| SECURITY UNLOCK                  | F2h      | YES     |
| SET MAX PASSWORD                 | F9h(01h) | YES     |
| SET MAX UNLOCK                   | F9h(03h) | YES     |
| SET MAX PASSWORD EXT             | 37h(01h) | YES     |



| Command                          | Code     | Support |
|----------------------------------|----------|---------|
| SET MAX UNLOCK EXT               | 37h(03h) | YES     |
| SMART WRITE LOG                  | B0h(D6h) | YES     |
| SMART WRITE ATTRIBUTE THRESHOLDS | B0h(D7h) | YES     |
| WRITE BUFFER                     | E8h      | YES     |
| WRITE LOG EXT                    | 3Fh      | YES     |
| WRITE MULTIPLE                   | C5h      | YES     |
| WRITE MULTIPLE EXT               | 39h      | YES     |
| WRITE SECTOR(S)                  | 30h/31h  | YES     |
| WRITE SECTOR(S) EXT              | 34h      | YES     |
| WRITE LONG                       | 32h/33h  | YES     |
| WRITE VERIFY SECTOR(S)           | 3Ch      | YES     |

### 6.3 DMA Data-In Commands

| Command             | Code    | Support |
|---------------------|---------|---------|
| READ DMA            | C8h/C9h | YES     |
| IDENTIFY DEVICE DMA | EEh     | YES     |
| READ DMA EXT        | 25h     | YES     |

### 6.4 DMA Data-Out Commands

| Command       | Code    | Support |
|---------------|---------|---------|
| WRITE DMA     | Cah/CBh | YES     |
| WRITE DMA EXT | 35h     | YES     |

### 6.5 Queued DMA Commands

| Command              | Code | Support |
|----------------------|------|---------|
| READ DMA QUEUED      | C7h  | NO      |
| READ DMA QUEUED EXT  | 26h  | NO      |
| WRITE DMA QUEUED     | CCh  | NO      |
| WRITE DMA QUEUED EXT | 36h  | NO      |
| SERVICE              | A2h  | NO      |



## 6.6 PACKET/DIAG Commands

| Command                   | Code | Support |
|---------------------------|------|---------|
| PACKET                    | A0h  | YES     |
| DEVICE RESET              | 08h  | YES     |
| EXECUTE DEVICE DIAGNOSTIC | 90h  | YES     |
| IDENTIFY PACKET DEVICE    | A1h  | YES     |

## 6.7 Non-Data Commands

| Command                          | Code     | Support |
|----------------------------------|----------|---------|
| CFA ERASE SECTORS                | C0h      | NO      |
| CFA REQUEST EXTENDED ERROR       | 03h      | NO      |
| CHECK MEDIA CARD TYPE            | D1h      | YES     |
| CHECK POWER MODE                 | E5h/98h  | YES     |
| DEVICE CONFIGURATION FREEZE LOCK | B1h(C1h) | YES     |
| DEVICE CONFIGURATION RESTORE     | B1h(C0h) | YES     |
| FLUSH CACHE                      | E7h      | YES     |
| FLUSH CACHE EXT                  | EAh      | YES     |
| FORMAT TRACK                     | 50h      | YES     |
| GET MEDIA STATUS                 | DAh      | YES     |
| IDLE                             | E3h/97h  | YES     |
| IDLE IMMEDIATE                   | E1h/95h  | YES     |
| INITIALIZE DEVICE PARAMETERS     | 91h      | YES     |
| MEDIA EJECT                      | EDh      | YES     |
| MEDIA LOCK                       | DEh      | YES     |
| MEDIA UNLOCK                     | DFh      | YES     |
| NOP                              | 00h      | YES     |
| RECALIBRATE                      | 1xh      | YES     |
| READ NATIVE MAX ADDRESS          | F8h      | YES     |
| READ NATIVE MAX ADDRESS EXT      | 27h      | YES     |
| READ VERIFY SECTOR(S)            | 40h/41h  | YES     |
| READ VERIFY SECTOR(S) EXT        | 42h      | YES     |
| SECURITY ERASE PREPARE           | F3h      | YES     |
| SECURITY FREEZE LOCK             | F5h      | YES     |



| Command                           | Code     | Support |
|-----------------------------------|----------|---------|
| SEEK                              | 70h      | YES     |
| SET FEATURES                      | EFh      | YES     |
| SET MAX ADDRESS                   | F9h      | YES     |
| SET MAX LOCK                      | F9h(02h) | YES     |
| SET MAX FREEZELOCK                | F9h(04h) | YES     |
| SET MAX ADDRESS EXT               | 37h      | YES     |
| SET MAX LOCK EXT                  | 37h(02h) | YES     |
| SET MAX FREEZE LOCK EXT           | 37h(04h) | YES     |
| SET MULTIPLE MODE                 | C6h      | YES     |
| SLEEP                             | E6h/99h  | YES     |
| SMART DISABLE OPERATIONS          | B0h(D9h) | YES     |
| SMART ENABLE OPERATIONS           | B0h(D8h) | YES     |
| SMART ENABLE/DISABLE AUTOSAVE     | B0h(D2h) | YES     |
| SMART SAVE ATTRIBUTE VALUES       | B0h(D3h) | YES     |
| SMART EXECUTE OFF_LINE IMMEDIATE  | B0h(D4h) | YES     |
| SMART RETURN STATUS               | B0h(DAh) | YES     |
| SMART ENABLE/DISABLE AUTO OFFLINE | B0h(DBh) | YES     |
| STANDBY                           | E2h/96h  | YES     |
| STANDBY IMMEDIATE                 | E0h/94h  | YES     |

**6.8 ATAPI PACKET Commands**

| Command                          | Code | Support |
|----------------------------------|------|---------|
| FORMAT UNIT                      | 04h  | YES     |
| MODE SELECT(6)                   | 15h  | YES     |
| MODE SELECT(10)                  | 55h  | YES     |
| MEDIUM SCAN                      | 38h  | YES     |
| SEND CUE SHEET                   | 5Dh  | YES     |
| SEND DVD STRUCTURE               | BFh  | YES     |
| SEND DIAGNOSTIC                  | 1Dh  | YES     |
| SEND EVENT                       | A2h  | YES     |
| SEND KEY                         | A3h  | YES     |
| SEND OPC INFORMATION             | 54h  | YES     |
| WRITE                            | 0Ah  | YES     |
| WRITE(10)                        | 2Ah  | YES     |
| WRITE(12)                        | AAh  | YES     |
| WRITE AND VERIFY(10)             | 2Eh  | YES     |
| WRITE AND VERIFY(12)             | A Eh | YES     |
| WRITE BUFFER COMMAND             | 3Bh  | YES     |
| BLANK                            | A1h  | YES     |
| CLOSE TRACK/RZONE/SESSION/BORDER | 5Bh  | YES     |
| ERASE                            | 19h  | YES     |
| GET CONFIGURATION                | 46h  | YES     |
| GET EVENT/STATUS NOTIFICATION    | 4Ah  | YES     |
| GET PERFORMANCE                  | ACh  | YES     |
| INQUIRY                          | 12h  | YES     |
| LOAD/UNLOAD MEDIUM               | A6h  | YES     |
| MECHANISM STATUS                 | BDh  | YES     |
| MODE SENSE(6)                    | 1Ah  | YES     |
| MODE SENSE(10)                   | 5Ah  | YES     |
| PAUSE/RESUME                     | 4Bh  | YES     |
| PLAY AUDIO(10)                   | 45h  | YES     |
| PLAY AUDIO(12)                   | A5h  | YES     |
| PLAY AUDIO MSF                   | 47h  | YES     |



| Command                      | Code | Support |
|------------------------------|------|---------|
| PLAY CD                      | BCh  | YES     |
| PREVENT/ALLOW MEDIUM REMOVAL | 1Eh  | YES     |
| READ(6)                      | 08h  | YES     |
| READ(10)                     | 28h  | YES     |
| READ(12)                     | A8h  | YES     |
| READ BLOCK LIMITS            | 05h  | YES     |
| READ CAPACITY COMMAND        | 25h  | YES     |
| READ CD                      | BEh  | YES     |
| READ CD MSF                  | B9h  | YES     |
| READ DISC INFORMATION        | 51h  | YES     |
| READ DVD STRUCTURE           | ADh  | YES     |
| READ FORMAT CAPACITIES       | 23h  | YES     |
| READ HEADER                  | 44h  | YES     |
| READ MASTER CUE              | 59h  | YES     |
| READ POSITION                | 34h  | YES     |
| READ REVERSE                 | 0Fh  | YES     |
| READ SUBCHANNEL              | 42h  | YES     |
| READ TOC/PMA/ATIP            | 43h  | YES     |
| READ TRACK/RZONE INFORMATION | 52h  | YES     |
| RECEIVE DIAGNOSTICS          | 1Ch  | YES     |
| RECOVER BUFFERED DATA        | 14h  | YES     |
| RELEASE                      | 17h  | YES     |
| REPAIR RZONE                 | 58h  | YES     |
| REPORT DENSITY SUPPORT       | 44h  | YES     |
| REPORT KEY                   | A4h  | YES     |
| RESERVE                      | 16h  | YES     |
| REQUEST SENSE                | 03h  | YES     |
| RESERVE TRACK/RZONE          | 53h  | YES     |
| REWIND                       | 01h  | YES     |
| SCAN                         | BAh  | YES     |
| SEEK                         | 2Bh  | YES     |
| SET CD SPEED                 | BBh  | YES     |
| SET READ AHEAD               | A7h  | YES     |



| Command                      | Code | Support |
|------------------------------|------|---------|
| SPACE                        | 11h  | YES     |
| START/STOP UNIT              | 1Bh  | YES     |
| STOP PLAY/SCAN               | 4Eh  | YES     |
| SYNCHRONIZE CACHE            | 35h  | YES     |
| TEST UNIT READY              | 00h  | YES     |
| VERIFY                       | 13h  | YES     |
| VERIFY(10)                   | 2Fh  | YES     |
| VERIFY(12)                   | AFh  | YES     |
| READ BUFFER COMMAND          | 3Ch  | YES     |
| READ BUFFER CAPACITY COMMAND | 5Ch  | YES     |
| WRITE FILEMARKS              | 10h  | YES     |



## 6.9 Vender Specific Command

In Serial ATA host adapter, the SCR register access act as an important role to perform device attached/detached detection, Partial/Slumber power saving mode configuration. However, the bridge function does not have any standard ATA/ATAPI command could use to access the SCR. Therefore, JM20330 provides a vender specific ATA command that the host software have this way to access the SCR of the Serial ATA host through ATA interface. This JMicron specified command also provides a Serial ATA BIST initiator, and user specified physical packet size of a PACKET command as described in this chapter.

| Command                            | Code | Support |
|------------------------------------|------|---------|
| Vender Specific: SCR & PACKET SIZE | FCh  | YES     |

The register-delivered contents and description are shown as below.

| Register      | 7   | 6 | 5   | 4   | 3           | 2 | 1 | 0 |
|---------------|-----|---|-----|-----|-------------|---|---|---|
| Features      | FCh |   |     |     |             |   |   |   |
| Sector count  | na  |   | PKT | SCR | SCR address |   |   |   |
| Sector number | 4Ah |   |     |     |             |   |   |   |
| Cylinder low  | 4Dh |   |     |     |             |   |   |   |
| Cylinder high | 43h |   |     |     |             |   |   |   |
| Device/head   | na  |   |     | DEV | na          |   |   |   |
| Command       | FCh |   |     |     |             |   |   |   |

**SCR address:** to address one of the 16 SCR registers, this field is valid if the SCR is set to 1.

**SCR:** when this bit is set to 1, the host bridge will enter SCR access mode.

**PKT:** when this bit is set to 1, the host bridge will be ready to receive the data size of packet command that operates in DMA mode.

The data size just for one packet command after the FCh command.

The command code 0xFAh—0xFFh are vender specific. We choose 0xFCh as JMicron specific. To avoid other vendors also choose 0xFCh, we put pattern "JMC" into SN, CL and CH registers. The JMC corresponding ASCII codes are '0x4Ah', '0x4Dh' and '0x43h'. The host bridge will decode command, SN, CL and CH registers to determine if enter JMicron special function mode. In JMicron special function mode, the host bridge will not send Reg-FIS to SATA device and will decode sector count register for mode selection.

### SCR access:



If the SCR bit is set to 1, the software will access the SCR based on the SCR address. The following is the software sequence of SCR access:

- a. Write Device register to select device.
- b. Write features register with 0xFCh.
- c. Write Sector count with setting SCR and SCR address.
- d. Write Sector number with 0x4Ah.
- e. Write Cylinder low with 0x4Dh.
- f. Write Cylinder high with 0x43h.
- g. Write command register with 0xFCh.
- h. The host bridge will enter SCR access mode.
- i. Read/Write data port to get/put from/into the addressed SCR register word 0.
- j. Read/Write data port to get/put from/into the addressed SCR register word 1.
- k. Hardware will exit JM micron special function mode automatically if features, SN, CL, CH and command don't match any of the above special values.

#### **Get Packet command size:**

If this bit is set to 1 by Jmicron special function mode, the host bridge will save the following 2-word data from PATA data port as data size of packet command. The size is **Double Word (32-bit)-based** only. When the host bridge is not in this mode, the transfer size depends on the OP code and command packet.

The following is the software programming sequence:

- a. Write Device register to select device.
- b. Write features register with 0xFCh.
- c. Write Sector number with 0x4Ah.
- d. Write Cylinder low with 0x4Dh.
- e. Write Cylinder high with 0x43h.
- f. Write features register with 0xFCh.
- g. The host bridge will enter Get Packet command size mode.
- h. Write Sector count with setting PKT bit to 1.
- i. Write data port to put into the data size counter word 0. (MSB)
- j. Write data port to put into the data size counter word 1. (LSB)



- k. Hardware will exit JM micron special function mode automatically if features, SN, CL, CH and command don't match any of the above special values.

The following is the software programming sequence to exit Get Packet command size mode:

- a. Write Device register to select device.
- b. Write features register with 0xFCh.
- c. Write Sector number with 0x4Ah.
- d. Write Cylinder low with 0x4Dh.
- e. Write Cylinder high with 0x43h.
- f. Write features register with 0xFCh.
- g. The host bridge will enter Get Packet command size mode.
- h. Write Sector count with setting PKT bit to 0.
- i. Hardware will exit JM micron special function mode automatically if features, SN, CL, CH and command don't match any of the above special values.



The register map for this command is as the followed table. The description of each register, please refer to 7.3.

| Addr | Name     | 31                   | 30            | 29         | 28         | 27          | 26 | 25 | 24         | 23           | 22           | 21       | 20        | 19           | 18 | 17 | 16       | 15           | 14        | 13 | 12 | 11     | 10          | 9      | 8 | 7            | 6             | 5          | 4 | 3        | 2 | 1            | 0 |                    |  |             |  |              |  |              |  |      |  |
|------|----------|----------------------|---------------|------------|------------|-------------|----|----|------------|--------------|--------------|----------|-----------|--------------|----|----|----------|--------------|-----------|----|----|--------|-------------|--------|---|--------------|---------------|------------|---|----------|---|--------------|---|--------------------|--|-------------|--|--------------|--|--------------|--|------|--|
| 00h  | SStatus  | Reserved (0)         |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    | IPM    |             |        |   | SPD          |               |            |   | DET      |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 01h  | SError   | DIAG                 |               |            |            |             |    |    |            |              |              |          |           | ERR          |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 02h  | SControl | Reserved (0)         |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    | IPM    |             |        |   | SPD          |               |            |   | DET      |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 03h  | BIST_DW0 | Reserved (0)         |               |            |            |             |    |    |            | T            | 0            | S        | L         | Reserved (0) |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 04h  | BIST_DW1 | BIST Pattern DWord 0 |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 05h  | BIST_DW2 | BIST Pattern DWord 1 |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 06h  | SYSCTRL  | Reserved (0)         |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   | BIST_JM_sram |               | BIST_JM_en |   | degap_en |   | Plug_irq     |   | Transmit only mode |  | CONT_DISAB  |  | R_SCRM DISAB |  | SND BIST     |  |      |  |
| 07h  | Debug 0  | ff_a2t_err           | empty_t2a_37  | emptu_a2t  | link_state |             |    |    | ff_t2a_err | full_t2a     | full_a2t_37  | tp_state |           |              |    | 0  | ctrl_err | err_queue    | cmd_state |    |    |        | pdiag_state |        |   |              | fis_con_state |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 08h  | Debug 1  | 0                    | empty_t2a0_37 | empty0_a2t | 0          | dma_state_h |    |    |            | 0            | full_t2a0_37 | 0        | app_state |              |    |    | 0        | pio_state    |           |    |    | 0      | dma_state   |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 09h  | PHYCTRL  | ACTL[39:32]          |               |            |            |             |    |    |            | Reserved (0) |              |          |           |              |    |    |          |              |           |    |    | MS_SSC |             | MS_OOB |   |              |               |            |   |          |   | PHYout_mode2 |   | PHYout_model1      |  | TXAMP [3:0] |  | Force3G      |  | Force PHYRDY |  | TXEN |  |
| 0Ah  | ACTL     | ACTL[31:0]           |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 0bh  | BIST DW3 | BIST data Dword 2    |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 0ch  | BIST DW4 | BIST data Dword 3    |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 0dh  | BIST DW5 | BIST data Dword 4    |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 0eh  | BIST DW6 | BIST data Dword 5    |               |            |            |             |    |    |            |              |              |          |           |              |    |    |          |              |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |
| 0fh  | PM Sup   |                      |               |            |            |             |    |    |            |              |              |          |           | PM port[3:0] |    |    |          | Notify[15:0] |           |    |    |        |             |        |   |              |               |            |   |          |   |              |   |                    |  |             |  |              |  |              |  |      |  |



## 6.10 Ultra DMA Transfer Rate

| Operation Mode<br>(MODE[2:0] setting) | Ultra DMA Mode<br>(Set Feature command) | Data Rate (MB/s) |
|---------------------------------------|-----------------------------------------|------------------|
| 150MHz                                | 0                                       | 16.7             |
|                                       | 1                                       | 25               |
|                                       | 2                                       | 33               |
|                                       | 3                                       | 44               |
|                                       | 4                                       | 66               |
|                                       | 5                                       | 100              |
|                                       | 6                                       | 120              |
|                                       | 7                                       | 150              |



## **6.11 Device Mode Master-Only Operation**

In legacy IDE framework, we can attach two IDE drives on the IDE cable. The two drives are master and slave correspondingly. But in SATA framework, we can only attach one SATA drive on the SATA port. From the SATA Host's viewpoint, the attached SATA drive is master. In order to meet the SATA framework, if we use JM20330 to bridge the SATA Host and IDE drive the jumper selection of the attached IDE drive must be master.

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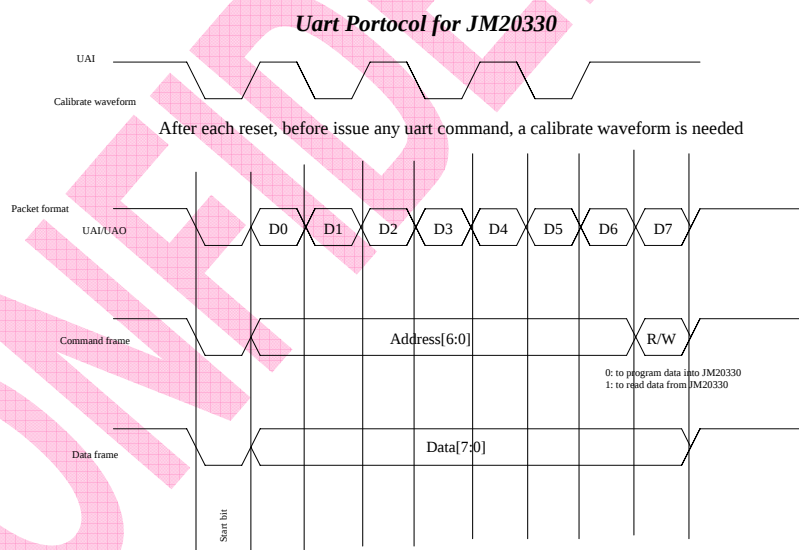


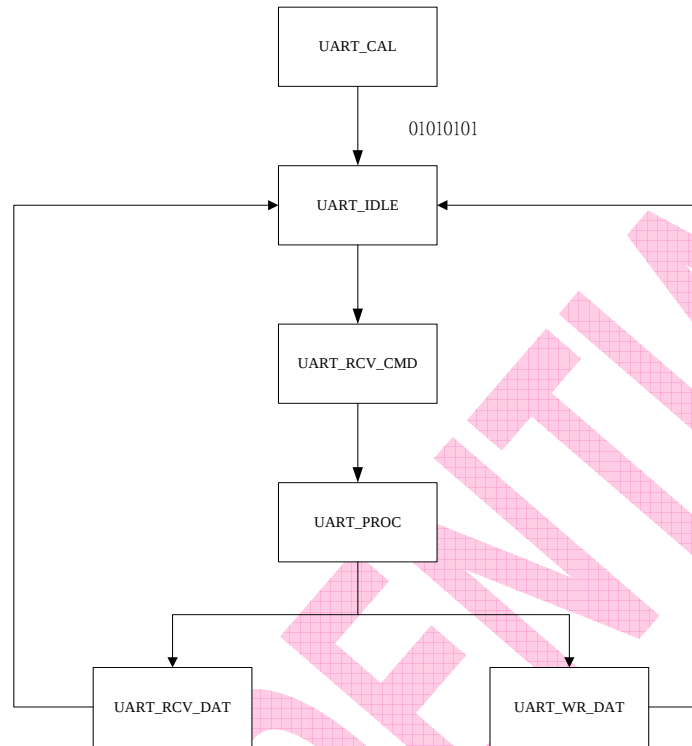
## 7. UART Interface Operation

The on-chip UART is an optional interface that user could use to access the SCR registers, fine tuning the serial link parameters of physical layer. Except of SCR, most registers had their power-on default values and are reserved for system troubleshooting only. Never change these registers in normal operation. Else, it may damage the file system in the storage system.

### 7.1 UART Interface

The on-chip UART interface is a user configurable baud rate full duplex serial interface. The software utility or firmware program should sent a 0xAAh preamble for on-chip UART core for baud rate identification, then followed by accessing Command + Data frame for internal register access. The Command frame data structure is that first data bit is a read/write control bit, and the others are address bits of the register. The bit ordering of both Command and Data are MSB to LSB. The max and min pulse width shall be 420us and 532ns. The time restriction between calibration, command, and data frame shall be 500ns.







## 7.2 SCR and Control Register Map

The internal register is 8-bit format. To access a SCR register, it requires to assert four Command + Data frame. The following shows the register map in DWord format.

| Addr   | Name     | 31                   | 30 | 29            | 28 | 27         | 26 | 25         | 24 | 23          | 22 | 21         | 20 | 19           | 18 | 17           | 16 | 15       | 14 | 13        | 12 | 11     | 10 | 9       | 8 | 7            | 6 | 5          | 4 | 3        | 2 | 1           | 0 |                    |  |               |  |              |  |          |  |              |  |      |  |
|--------|----------|----------------------|----|---------------|----|------------|----|------------|----|-------------|----|------------|----|--------------|----|--------------|----|----------|----|-----------|----|--------|----|---------|---|--------------|---|------------|---|----------|---|-------------|---|--------------------|--|---------------|--|--------------|--|----------|--|--------------|--|------|--|
| 00-03h | SStatus  | Reserved (0)         |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    | IPM    |    |         |   | SPD          |   |            |   | DET      |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 04-07h | SError   | DIAG                 |    |               |    |            |    |            |    |             |    |            |    | ERR          |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 08-0Bh | SControl | Reserved (0)         |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    | IPM    |    |         |   | SPD          |   |            |   | DET      |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 0C-0Fh | BIST_DW0 | Reserved (0)         |    |               |    |            |    |            |    | T           | 0  | S          | L  | Reserved (0) |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 10-13h | BIST_DW1 | BIST Pattern DWord 0 |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 14-17h | BIST_DW2 | BIST Pattern DWord 1 |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 18-1Bh | SYSCTRL  | Reserved (0)         |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   | BIST_JM_sram |   | BIST_JM_en |   | degap_en |   | Plug_irq    |   | Transmit only mode |  | CONT DISAB    |  | R_SCRM DISAB |  | SND BIST |  |              |  |      |  |
| 1C-1Fh | Debug 0  | ff_a2t_err           |    | empty_t2a_37  |    | emptu_a2t  |    | link_state |    |             |    | ff_t2a_err |    | full_t2a     |    | full_a2t_37  |    | tp_state |    |           |    | 0      |    | crc_err |   | err_queue    |   | cmd_state  |   |          |   | pdiag_state |   |                    |  | fis_con_state |  |              |  |          |  |              |  |      |  |
| 20-23h | Debug 1  | 0                    |    | empty_t2a0_37 |    | empty0_a2t |    | 0          |    | dma_state_h |    |            |    | 0            |    | full_t2a0_37 |    | 0        |    | app_state |    |        |    | 0       |   | pio_state    |   |            |   | 0        |   |             |   | dma_state          |  |               |  |              |  |          |  |              |  |      |  |
| 24-27h | PHYCTRL  | ACTL[39:32]          |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    | MS_SSC |    | MS_OOB  |   |              |   |            |   |          |   |             |   | PHYOut_mode2       |  | PHYOut_mode1  |  | TXAMP [3:0]  |  | Force3G  |  | Force PHYRDY |  | TXEN |  |
| 28-2Bh | ACTL     | ACTL[31:0]           |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 2C-2Fh | BIST DW3 | BIST data Dword 2    |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 30-33h | BIST DW4 | BIST data Dword 3    |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 34-37h | BIST DW5 | BIST data Dword 4    |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |
| 38-3Bh | BIST DW6 | BIST data Dword 5    |    |               |    |            |    |            |    |             |    |            |    |              |    |              |    |          |    |           |    |        |    |         |   |              |   |            |   |          |   |             |   |                    |  |               |  |              |  |          |  |              |  |      |  |



|        |               |  |  |  |                 |              |
|--------|---------------|--|--|--|-----------------|--------------|
| 3C-3Fh | <b>PM Sup</b> |  |  |  | PM<br>Port[3:0] | Notify[15:0] |
|--------|---------------|--|--|--|-----------------|--------------|

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### 7.3 Register Description

| Register Name | ATA Address | UART Address | Description                               |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------|-------------|--------------|-------------------------------------------|------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SStatus       | 00h         | 00-03h       | The Serial ATA interface Status register. |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|               |             |              | <i>bit</i>                                | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                                                                                                                                                                                              |
|               |             |              | 3:0                                       | R          | 0000         | <b>DET.</b> The DET value indicates the interface device detection and physical layer state.<br>0000 No device detected and Phy communication not established<br>0001 Device presence detected but Phy communication not established<br>0011 Device presence detected and Phy communication established<br>0100 Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode<br>All other values reserved |
|               |             |              | 7:4                                       | R          | 0001         | <b>SPD.</b> The SPD value indicates the negotiated interface communication speed established<br>0000 No negotiated speed (device not present or communication not established)<br>0001 Generation 1 communication rate negotiated<br>All other values reserved                                                                                                                                                                                  |
|               |             |              | 11:8                                      | R          | 0000         | <b>IPM.</b> The IPM value indicates the current interface power management state<br>0000 Device not present or communication not established<br>0001 Interface in active state<br>0010 Interface in PARTIAL power management state<br>0110 Interface in SLUMBER power management state<br>All other values reserved                                                                                                                             |
|               |             |              | Others                                    | R          | 0            | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| SError        | 01h         | 04-07h       | The Serial ATA interface Error register.  |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|               |             |              | <i>bit</i>                                | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                                                                                                                                                                                              |
|               |             |              | 0                                         | R/WC       | 0            | <b>I.</b> Recovered data integrity error                                                                                                                                                                                                                                                                                                                                                                                                        |
|               |             |              | 1                                         | R/WC       | 0            | <b>M.</b> Recovered communications error                                                                                                                                                                                                                                                                                                                                                                                                        |
|               |             |              | 8                                         | R/WC       | 0            | <b>T.</b> Non-recovered transient data integrity error                                                                                                                                                                                                                                                                                                                                                                                          |
|               |             |              | 9                                         | R/WC       | 0            | <b>C.</b> Non-recovered persistent communication or data integrity error                                                                                                                                                                                                                                                                                                                                                                        |
|               |             |              | 10                                        | R/WC       | 0            | <b>P.</b> Protocol error                                                                                                                                                                                                                                                                                                                                                                                                                        |
|               |             |              | 11                                        | R/WC       | 0            | <b>E.</b> Internal error                                                                                                                                                                                                                                                                                                                                                                                                                        |
|               |             |              | 16                                        | R/WC       | 0            | <b>N.</b> PhyRdy change                                                                                                                                                                                                                                                                                                                                                                                                                         |
|               |             |              | 17                                        | R/W        | 0            | <b>I.</b> Phy Internal Error                                                                                                                                                                                                                                                                                                                                                                                                                    |
|               |             |              | 18                                        | R/WC       | 0            | <b>W.</b> Comm Wake                                                                                                                                                                                                                                                                                                                                                                                                                             |
|               |             |              | 19                                        | R/WC       | 0            | <b>B.</b> 10b to 8b Decode error                                                                                                                                                                                                                                                                                                                                                                                                                |
|               |             |              | 20                                        | R/WC       | 0            | <b>D.</b> Disparity Error                                                                                                                                                                                                                                                                                                                                                                                                                       |
|               |             |              | 21                                        | R/WC       | 0            | <b>C.</b> CRC Error                                                                                                                                                                                                                                                                                                                                                                                                                             |
|               |             |              | 22                                        | R/WC       | 0            | <b>H.</b> Handshake error                                                                                                                                                                                                                                                                                                                                                                                                                       |
|               |             |              | 23                                        | R/WC       | 0            | <b>S.</b> Link Sequence Error                                                                                                                                                                                                                                                                                                                                                                                                                   |
|               |             |              | 24                                        | R/WC       | 0            | <b>T.</b> Transport state transition error                                                                                                                                                                                                                                                                                                                                                                                                      |
|               |             |              | 25                                        | R/WC       | 0            | <b>F.</b> Unrecognized FIS type                                                                                                                                                                                                                                                                                                                                                                                                                 |



| Register Name | ATA Address | UART Address | Description                                |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------|-------------|--------------|--------------------------------------------|------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|               |             |              | Others                                     | R          | 0            | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| SControl      | 02h         | 08-0Bh       | The Serial ATA interface Control register. |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|               |             |              | <i>bit</i>                                 | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|               |             |              | 3:0                                        | R/W        | 0000         | <b>DET.</b> The DET field controls the host adapter device detection and interface initialization.<br>0000 No device detection or initialization action requested<br>0001 Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. Upon a write to the SControl register that sets the LSB of the DET field to one, the host shall transition to the HP1:HR Reset state and shall remain in that state until the LSB of the DET field is cleared to zero by a subsequent write to the SControl register.<br>0100 Disable the Serial ATA interface and put Phy in offline mode.<br>All other values reserved |
|               |             |              | 7:4                                        | R/W        | 0001         | <b>SPD.</b> The SPD field represents the highest allowed communication speed the interface is allowed to negotiate when interface communication speed is established<br>0000 No speed negotiation restrictions<br>0001 Limit speed negotiation to a rate not greater than Generation 1 communication rate<br>All other values reserved                                                                                                                                                                                                                                                                                                                                                                                                                            |
|               |             |              | 11:8                                       | R/W        | 0000         | <b>IPM.</b> The IPM field represents the enabled interface power management states that can be invoked via the Serial ATA interface power management capabilities<br>0000 No interface power management state restrictions<br>0001 Transitions to the PARTIAL power management state disabled<br>0010 Transitions to the SLUMBER power management state disabled<br>0011 Transitions to both the PARTIAL and SLUMBER power management states disabled<br>All other values reserved                                                                                                                                                                                                                                                                                |
|               |             |              | Others                                     | R/W        | 0            | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| BIST_DW0      | 03h         | 0C-0Fh       | <b>BIST Control Register.</b>              |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|               |             |              | <i>bit</i>                                 | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|               |             |              | 20                                         | RW         | 0            | <b>L.</b> Far-end retimed loopback mode.<br>0: Disable.<br>1: Enable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|               |             |              | 21                                         | RW         | 0            | <b>S.</b> Scrambler enable of transmitter.<br>0: Disable.<br>1: Enable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|               |             |              | 23                                         | RW         | 0            | <b>T.</b> Enable transmitting-only.<br>0: Disable.<br>1: Enable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|               |             |              | others                                     | R          | 0            | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| BIST_DW1      | 04h         | 10-13h       | <b>BIST Pattern Doubled-Word 1.</b>        |            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|               |             |              | <i>bit</i>                                 | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|               |             |              | 31:0                                       | RW         | 0            | BIST Pattern.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |



| Register Name | ATA Address | UART Address | Description                             |            |              |                                                                                                                                                                                                                                                                      |
|---------------|-------------|--------------|-----------------------------------------|------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BIST_DW2      | 05h         | 14-17h       | <b>BIST Pattern Doubled-Word 2.</b>     |            |              |                                                                                                                                                                                                                                                                      |
|               |             |              | <i>bit</i>                              | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                   |
|               |             |              | 31:0                                    | RW         | 0            | BIST Pattern.                                                                                                                                                                                                                                                        |
| SYSCTRL       | 06h         | 18-1Bh       | <b>System Control Register.</b>         |            |              |                                                                                                                                                                                                                                                                      |
|               |             |              | <i>bit</i>                              | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                   |
|               |             |              | 0                                       | RW         | 0            | <b>SEND_BIST.</b> Send BIST FIS.<br>0: Normal operation.<br>1: Start to send BIST FIS.<br>When this bit is set, the JM20330 will send a BIST FIS with the L, S, T field and data pattern specified in <b>BIST_DW0</b> , <b>BIST_DW1</b> , <b>BIST_DW2</b> registers. |
|               |             |              | 1                                       | RW         | 0            | <b>RxSCRMDis.</b> Receiver scrambler Disable.<br>0: Enable receiver scrambler.<br>1: Disable receiver scrambler.                                                                                                                                                     |
|               |             |              | 2                                       | RW         | 0            | <b>CONT_Disable.</b> CONT primitive Enable.<br>0: Enable CONT primitive.<br>1: Disable CONT primitive.                                                                                                                                                               |
|               |             |              | 3                                       | RW         | 0            | <b>Tx_only_en.</b> Force the transmitter to send the BIST pattern. <b>ForcePHYRDY</b> bit must be set before enabling this function.                                                                                                                                 |
|               |             |              | 4                                       | RW         | 0            | <b>Plug_irq.</b> Reserved.                                                                                                                                                                                                                                           |
|               |             |              | 5                                       | RW         | 0            | <b>Degap_en.</b> Reserved.                                                                                                                                                                                                                                           |
|               |             |              | 6                                       | RW         | 0            | <b>BIST_JM_en.</b> 1:JM bist enable, 0:JM bist disable                                                                                                                                                                                                               |
|               |             |              | 7                                       | RW         | 0            | <b>BIST_JM_scram.</b> 1: scramble enable, 0:scramble disable                                                                                                                                                                                                         |
|               |             |              | others                                  | R          | 0            | Reserved.                                                                                                                                                                                                                                                            |
| DEBUG_0       | 07h         | 1C-1FH       | <b>System Debug Port 0.</b>             |            |              |                                                                                                                                                                                                                                                                      |
| DEBUG_1       | 08h         | 20-23H       | <b>System Debug Port 1.</b>             |            |              |                                                                                                                                                                                                                                                                      |
| PHYCTRL       | 09h         | 24-27h       | <b>Physical Layer Control Register.</b> |            |              |                                                                                                                                                                                                                                                                      |
|               |             |              | <i>bit</i>                              | <i>R/W</i> | <i>Reset</i> | <i>Description</i>                                                                                                                                                                                                                                                   |
|               |             |              | 0                                       | RW         | 1            | <b>TXEN.</b> Transmitter enable.<br>0: Disable.<br>1: Enable. (Normal operation)                                                                                                                                                                                     |
|               |             |              | 1                                       | RW         | 0            | <b>FORCEPHYRDY.</b> Forced PHY ready.<br>0: Normal operation.<br>1: Forced PHY ready regardless OOB power on initialization.                                                                                                                                         |
|               |             |              | 2                                       | RW         | 0            | <b>FRCE3G.</b> This bit is valid only for 3G PHY.                                                                                                                                                                                                                    |
|               |             |              | 6:3                                     | RW         | 000          | <b>TXAMP.</b> Transmitter amplitude control.                                                                                                                                                                                                                         |



| Register Name | ATA Address | UART Address | Description                       |     |       |                                        |
|---------------|-------------|--------------|-----------------------------------|-----|-------|----------------------------------------|
|               |             |              | 11:7                              | R   | R     | Reserved.                              |
|               |             |              | 12                                | RW  | 0     | MS_OOB. Reserved.                      |
|               |             |              | 13                                | RW  | 0     | MS_SSC. Reserved.                      |
|               |             |              | others                            | R   | 0     | Reserved.                              |
|               |             |              |                                   |     |       |                                        |
| ACTL          | 0Ah         | 28-2Bh       | PHY Analog Control Register.      |     |       |                                        |
|               |             |              | bit                               | R/W | Reset | Description                            |
|               |             |              | 31:0                              | RW  | AB155 | Reserved for analog parameter control. |
| BIST_DW3      | 0Bh         | 2C-2Fh       | BIST Pattern Doubled-Word 3.      |     |       |                                        |
|               |             |              | bit                               | R/W | Reset | Description                            |
|               |             |              | 31:0                              | RW  | 0     | BIST Pattern.                          |
| BIST_DW4      | 0Ch         | 30-33h       | BIST Pattern Doubled-Word 4.      |     |       |                                        |
|               |             |              | bit                               | R/W | Reset | Description                            |
|               |             |              | 31:0                              | RW  | 0     | BIST Pattern.                          |
| BIST_DW5      | 0Dh         | 34-37h       | BIST Pattern Doubled-Word 5.      |     |       |                                        |
|               |             |              | bit                               | R/W | Reset | Description                            |
|               |             |              | 31:0                              | RW  | 0     | BIST Pattern.                          |
| BIST_DW6      | 0Eh         | 38-3Bh       | BIST Pattern Doubled-Word 6.      |     |       |                                        |
|               |             |              | bit                               | R/W | Reset | Description                            |
|               |             |              | 31:0                              | RW  | 0     | BIST Pattern.                          |
| PM Sup        | 0Fh         | 3C-2Fh       | PM and Async notification support |     |       |                                        |
|               |             |              | bit                               | R/W | Reset | Description                            |
|               |             |              | 15:0                              | RW  | 0     | Notify register                        |
|               |             |              | 19:16                             | RW  | 0     | PM port register                       |



## 8. Electrical Characteristics

### 8.1 Power Requirements

| Parameter                    | Symbol                 | Condition | Min   | Typical | Max   | Unit |
|------------------------------|------------------------|-----------|-------|---------|-------|------|
| Digital I/O pad power supply |                        |           | 9.43  | 9.50    | 9.57  | mA   |
| Digital core power supply    |                        |           | 44.8  | 47.5    | 49.2  | mA   |
| Analog power supply          | AVDDH <sub>(ABS)</sub> |           | 17.90 | 17.92   | 17.93 | mA   |
| Analog power supply          | AVDDL <sub>(ABS)</sub> |           | 54.5  | 55.0    | 55.2  | mA   |

### 8.2 Absolute Maximum Ratings

| Parameter                          | Symbol                 | Condition | Min  | Typical | Max      | Unit |
|------------------------------------|------------------------|-----------|------|---------|----------|------|
| Absolute digital I/O power supply  | VCCO <sub>(ABS)</sub>  |           | 2.4  | 3.3     | 4.4      | V    |
|                                    |                        |           | 3.9  | 9.1     | 13       | mA   |
| Absolute digital core power supply | VCKK <sub>(ABS)</sub>  |           | 1.4  | 1.8     | 3.2      | V    |
|                                    |                        |           | 36   | 46      | 70       | mA   |
| Absolute analog power supply       | AVDDH <sub>(ABS)</sub> |           | 2.6  | 3.3     | 4.4      | V    |
|                                    |                        |           | 17   | 18      | 27       | mA   |
| Absolute analog power supply       | AVDDL <sub>(ABS)</sub> |           | 1.4  | 1.8     | 3.2      | V    |
|                                    |                        |           | 45   | 55      | 110      | mA   |
| Absolute Input Voltage             |                        |           | -0.4 |         | VCCO+0.4 | V    |
| Absolute Storage Temperature       |                        |           | -55  |         | +85      | °C   |
| Absolute Junction Temperature      |                        |           | -35  |         | +125     | °C   |

### 8.3 Typical Operation Conditions

| Parameter                           | Symbol | Condition             | Min  | Typical | Max  | Unit |
|-------------------------------------|--------|-----------------------|------|---------|------|------|
| Ambient operation temperature       |        | For commercial spec.  | 0    |         | 70   | °C   |
| Ambient operation temperature       |        | For industry spec. ** | -40  |         | 85   | °C   |
| Junction Temperature                |        |                       | 0    |         | 125  | °C   |
| Operation digital I/O power supply  | VCCO   |                       | 3.0  | 3.3     | 3.6  | V    |
| Operation digital core power supply | VCKK   |                       | 1.62 | 1.8     | 1.98 | V    |
| Operation analog power supply       | AVDDH  |                       | 3.0  | 3.3     | 3.6  | V    |
| Operation analog power supply       | AVDDL  |                       | 1.62 | 1.8     | 1.98 | V    |



## 8.4 DC Characteristics

| Parameter           | Symbol   | Condition | Min | Typical | Max | Unit |
|---------------------|----------|-----------|-----|---------|-----|------|
| Input low voltage   | $V_{IL}$ |           | 0   |         | 0.8 | V    |
| Input high voltage  | $V_{IH}$ |           | 2.0 |         |     | V    |
| Output low voltage  | $V_{OL}$ |           | 0   |         | 0.4 | V    |
| Output high voltage | $V_{OH}$ |           | 2.6 |         | 3.6 | V    |

## 8.5 ATA I/O DC Characteristics

| Parameter                | Symbol   | Condition | Min | Typical | Max | Unit    |
|--------------------------|----------|-----------|-----|---------|-----|---------|
| DC sink current          | $I_{OL}$ |           | 8   |         |     | mA      |
| Internal pull-up current |          |           | 40  |         | 160 | $\mu$ A |
| Input low-voltage        | $V_{IL}$ |           |     |         | 0.8 | V       |
| Input high-voltage       | $V_{IH}$ |           | 2.0 |         | 5.0 | V       |
| Output low-voltage       | $V_{OL}$ |           | 0   |         | 0.4 | V       |
| Output high-voltage      | $V_{OH}$ |           | 2.6 |         | 3.6 | V       |

## 8.6 ATA I/O AC Characteristics

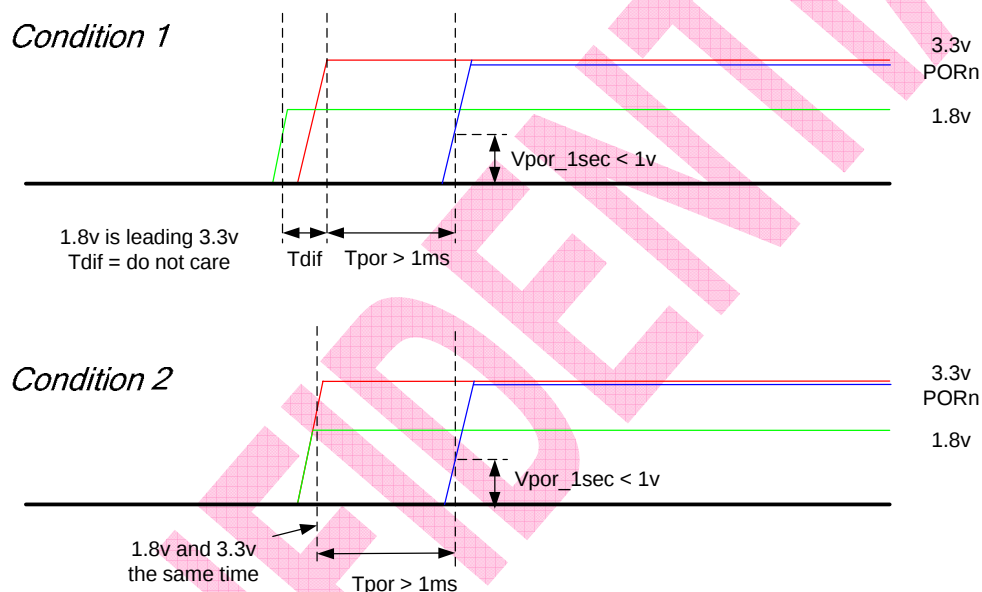
| Parameter          | Symbol   | Condition | Min | Typical | Max | Unit |
|--------------------|----------|-----------|-----|---------|-----|------|
| Rising slew-rate   |          |           | 0.4 | 0.7     | 1.0 | V/ns |
| Falling slew-rate  |          |           | 0.4 | 0.7     | 1.0 | V/ns |
| Device Capacitance | C device |           |     |         | 27  | pF   |



## 9. Power-on Reset Sequence

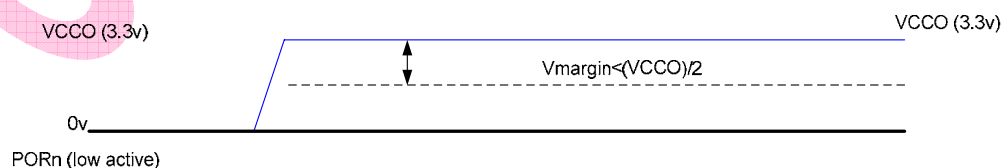
The JM20330 is a UMC 0.18 process chip solution. Which need 2 power supply e.g. 1.8 v and 3.3 v. When power on, keep 1.8v leading 3.3v. If it can not be achieved, the 3.3v and 1.8v should come at the same time.

The external RC power on reset circuit is built in the system board, the PORn signal in pin 17 shall be still low( asserted ) till 1 ms second after both 1.8 v and 3.3 v power supply are stable ( as shown in condtion2 and contion3).



Ether condition 1, or condition 2 is ok.

After the power on reset, the JM20330 enter into normal operation mode. During the normal operation mode, the PORn signal in pin 17 must always kept in high, and the noise margin shall be always keep less than  $V_{CCO}/2$ , as shown is the following diagram.



Noise margin of PORn