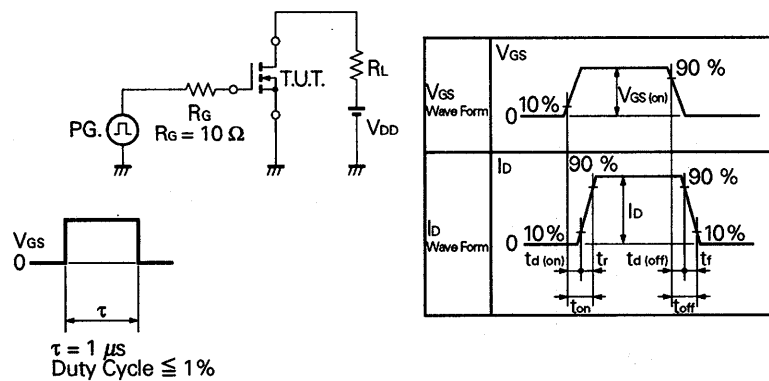


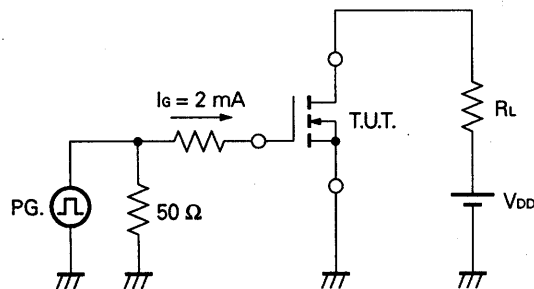
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		42	50	$\text{m}\Omega$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		50	70	$\text{m}\Omega$	$V_{GS} = 4.0\text{ V}, I_D = 20\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	12			S	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$
Drain Leakage Current	I_{DSS}			10	μA	$V_{DS} = 100\text{ V}, V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$
Input Capacitance	C_{iss}		3300		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		800		pF	
Reverse Transfer Capacitance	C_{res}		200		pF	
Turn-On Delay Time	$t_{d(on)}$		40		ns	$V_{GS(on)} = 10\text{ V}$ $V_{DD} = 50\text{ V}$ $I_D = 20\text{ A}, R_G = 10\ \Omega$ $R_L = 2.5\ \Omega$
Rise Time	t_r		210		ns	
Turn-Off Delay Time	$t_{d(off)}$		210		ns	
Fall Time	t_f		155		ns	
Total Gate Charge	Q_G		80		nC	$V_{GS} = 10\text{ V}$ $I_D = 40\text{ A}$ $V_{DD} = 80\text{ V}$
Gate to Source Charge	Q_{GS}		10		nC	
Gate to Drain Charge	Q_{GD}		30		nC	
Diode Forward Voltage	V_{SD}		1.2		V	$I_{SD} = 40\text{ A}, V_{GS} = 0$
Reverse Recovery Time	t_{rr}		210		ns	$I_F = 40\text{ A}, V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		600		nC	

Test Circuit 1: Switching Time

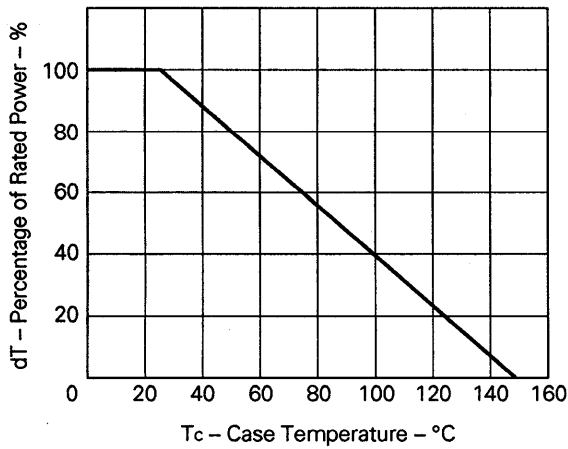


Test Circuit 2: Gate Charge

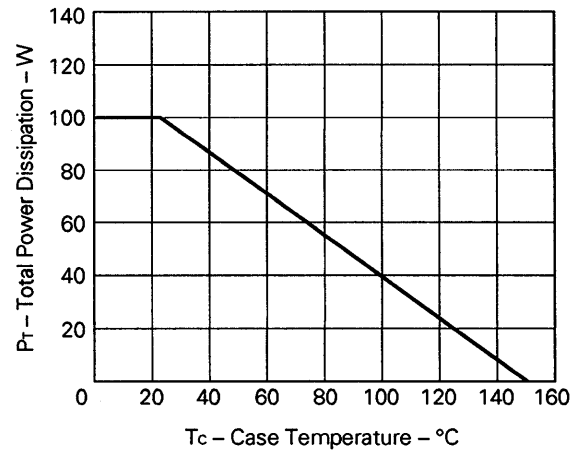


TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

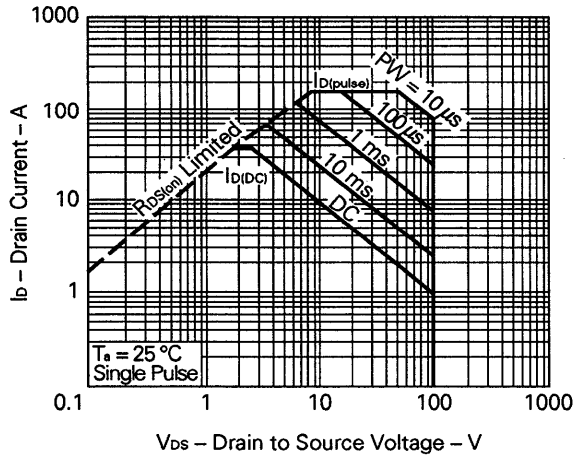
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



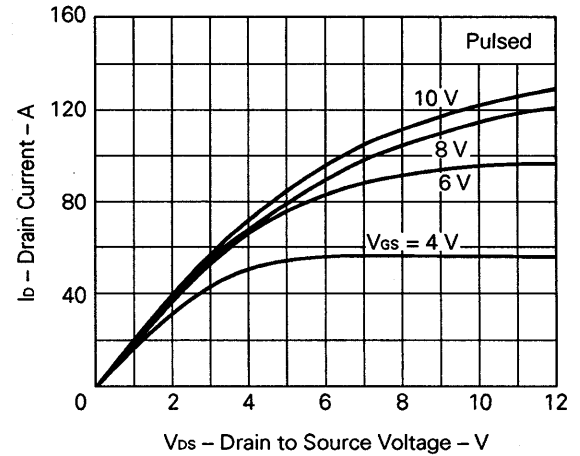
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



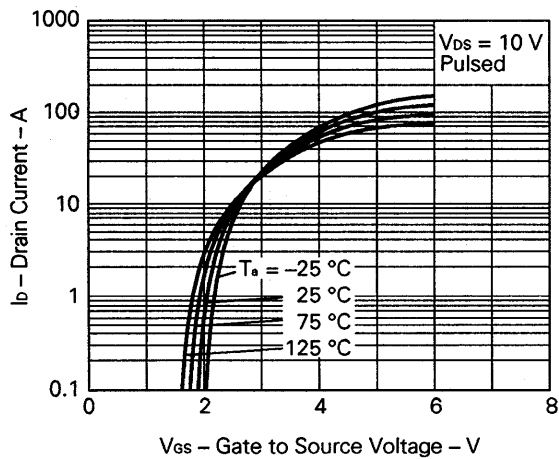
FORWARD BIAS SAFE OPERATING AREA

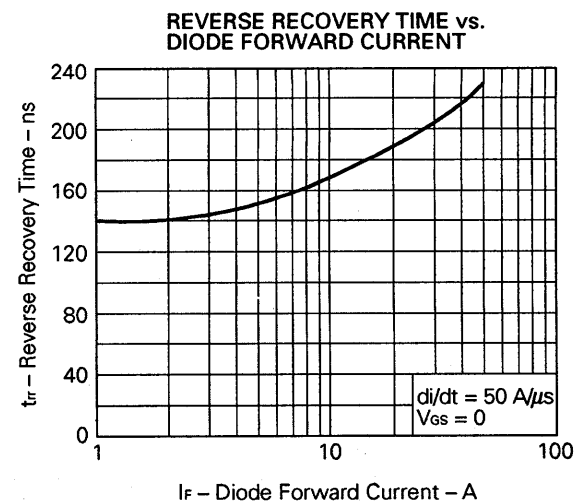
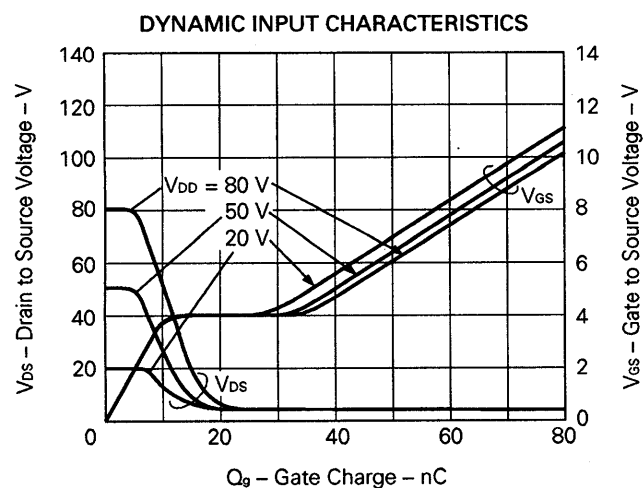
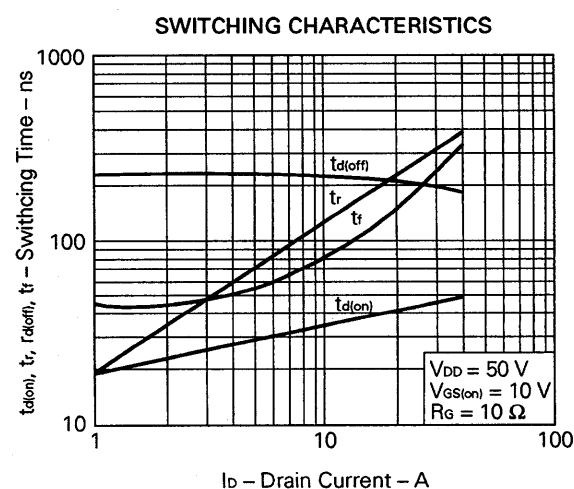
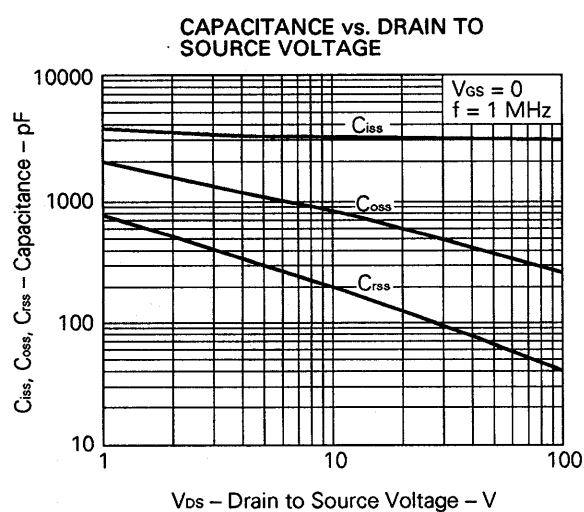
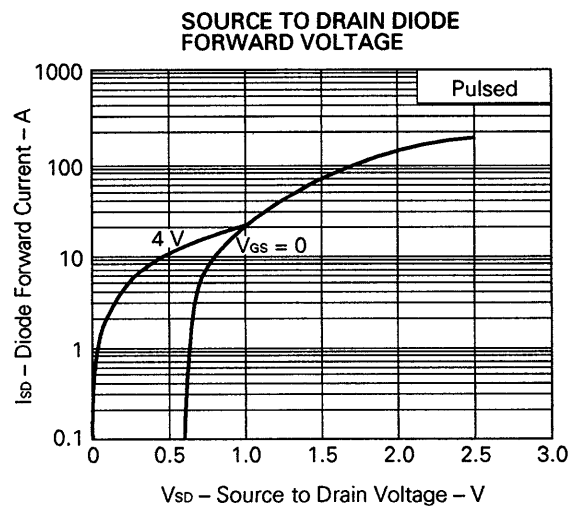
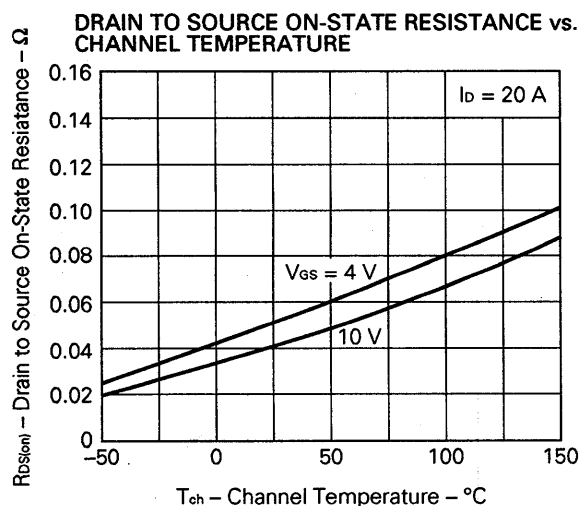


DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

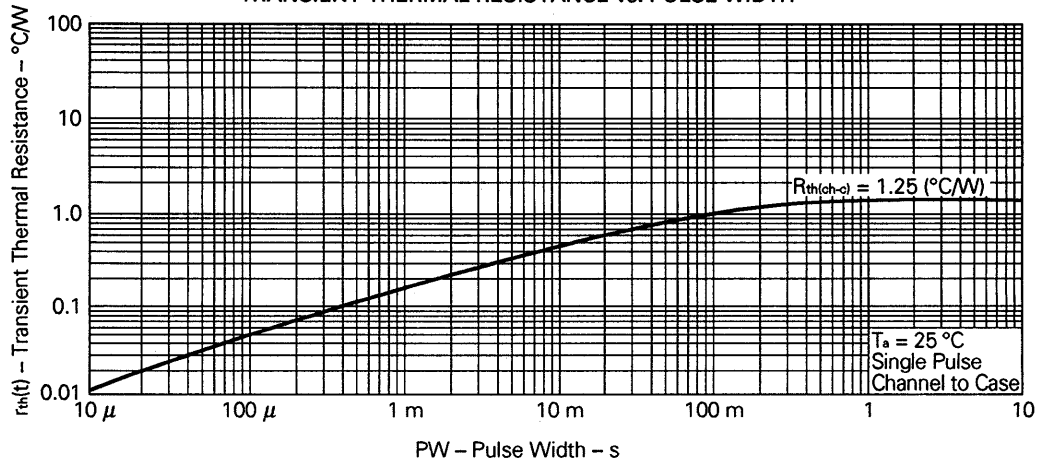


TRANSFER CHARACTERISTICS

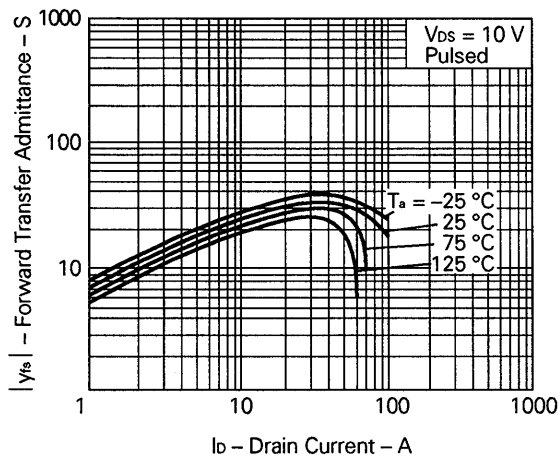




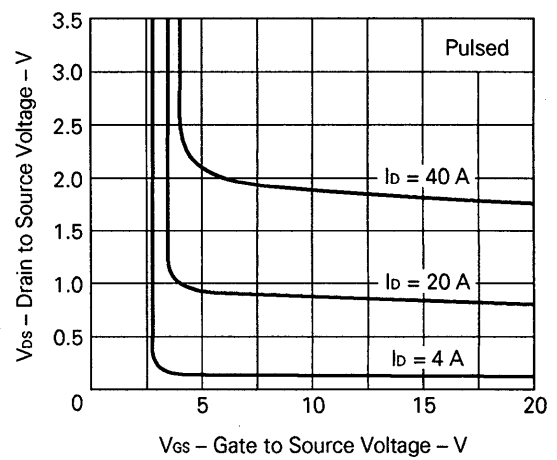
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



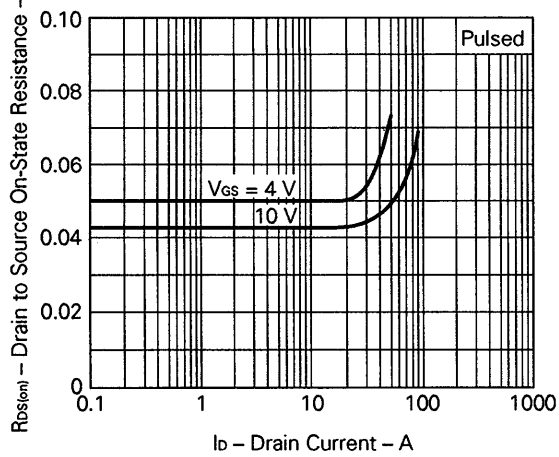
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



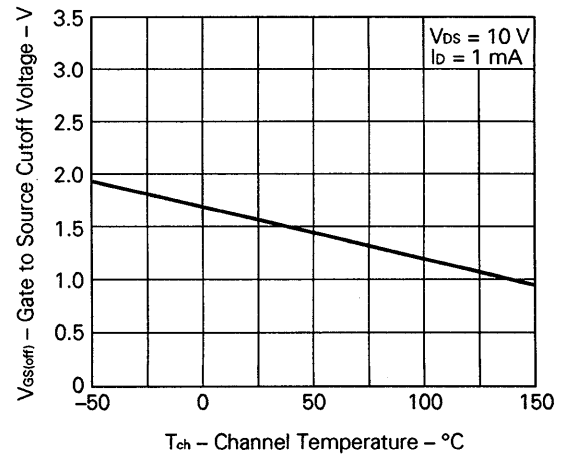
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



REFERENCE

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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