2SK2373

Silicon N-Channel MOS FET

HITACHI

ADE-208-268
1st. Edition

Application

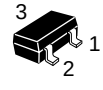
Low frequency power switching

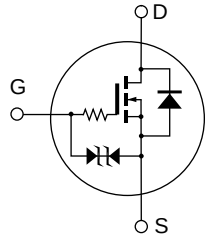
Features

- Low on-resistance
- Small package
- Low drive current
- 4 V gate drive device can be driven from 5 V source.
- Suitable for low signal load switch

Outline

MPAK





1. Source
2. Gate
3. Drain

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}$*[1]	0.4	A
Body to drain diode reverse drain current	I_{DR}	0.2	A
Channel dissipation	Pch*[2]	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

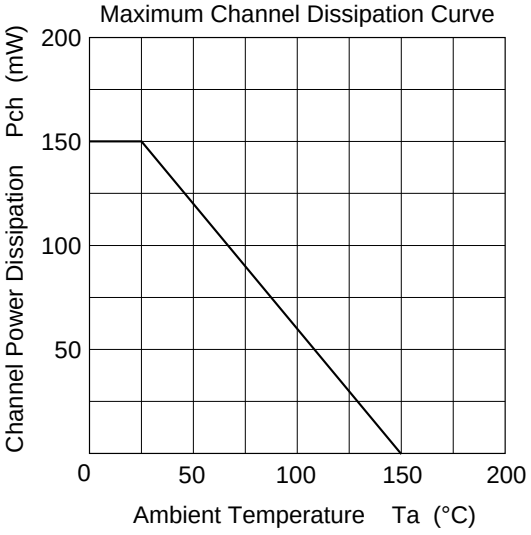
Notes 1. PW ≤ 100 µs, duty cycle ≤ 10 %
2. Marking is “ZE–”.

Electrical Characteristics (Ta = 25°C)

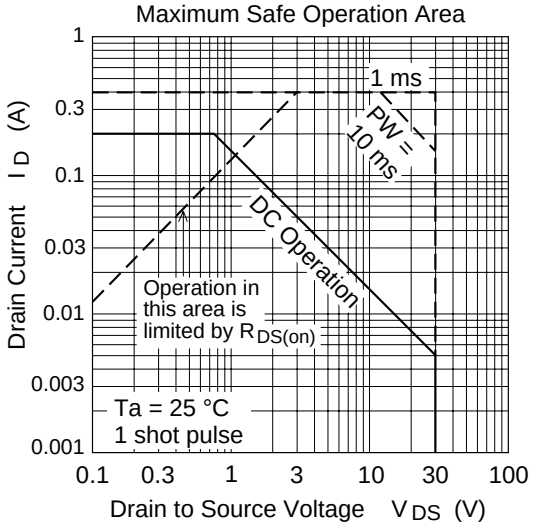
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±2	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 10 µA, V_{DS} = 5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.4	2.5	Ω	I_D = 20 mA V_{GS} = 4 V*[1]
		—	1.0	1.4	Ω	I_D = 10 mA V_{GS} = 10 V*[1]
Input capacitance	Ciss	—	17.8	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	25.4	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3.7	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	50	—	ns	I_D = 0.1 A
Rise time	t_r	—	125	—	ns	V_{GS} = 10 V
Turn-off delay time	$t_{d(off)}$	—	660	—	ns	R_L = 100 Ω
Fall time	t_f	—	400	—	ns	PW = 2 µs

Note 1. Pulse Test

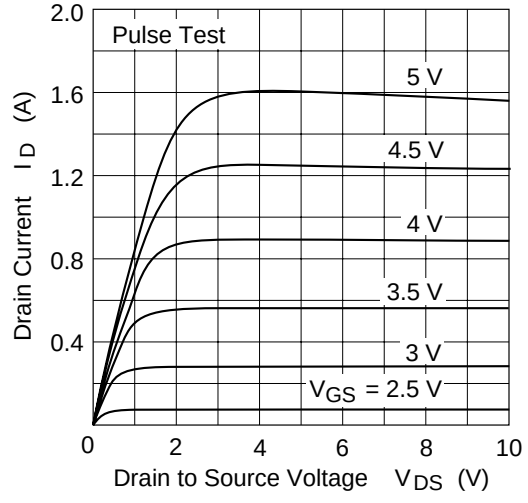
Maximum Channel Dissipation Curve



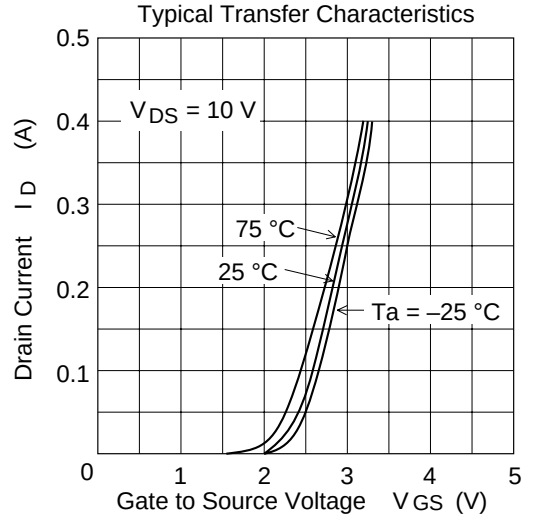
Maximum Safe Operation Area



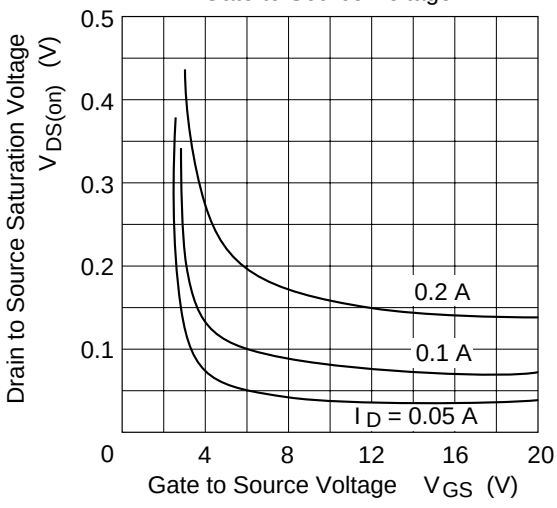
Typical Output Characteristics



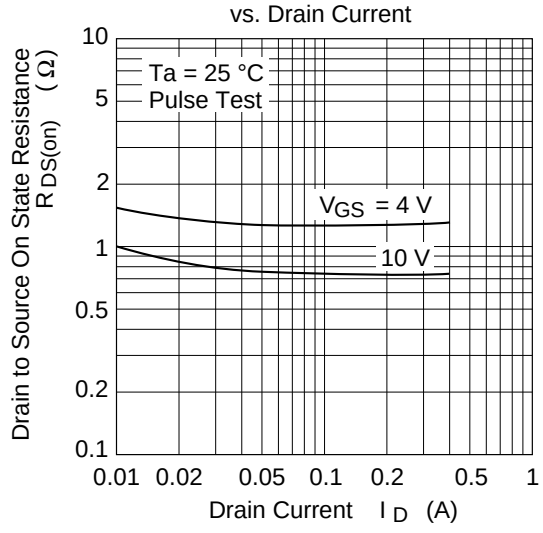
Typical Transfer Characteristics



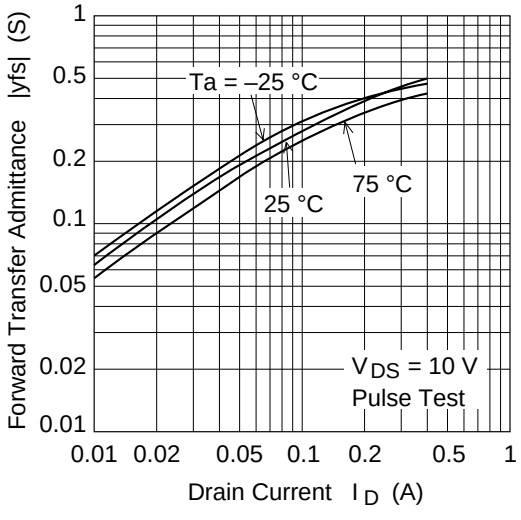
Drain to Source Saturation Voltage vs. Gate to Source Voltage



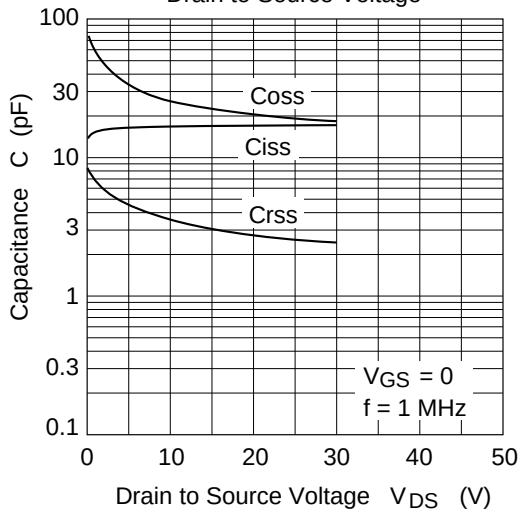
Static Drain to Source on State Resistance vs. Drain Current

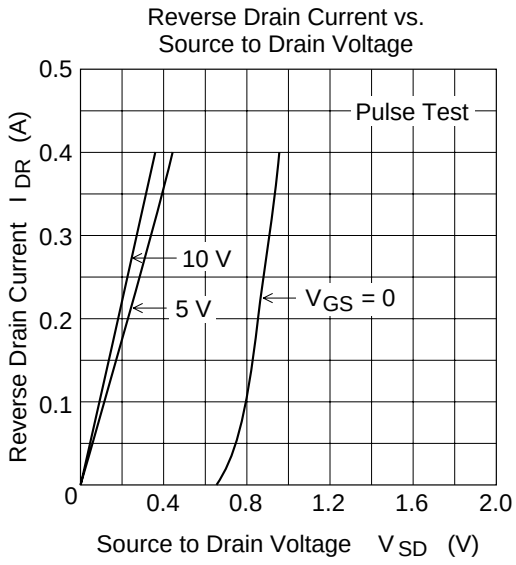


Forward Transfer Admittance vs. Drain Current

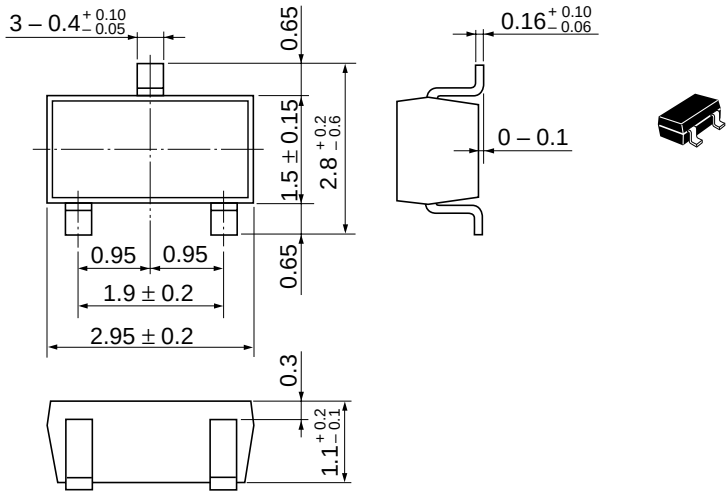


Typical Capacitance vs. Drain to Source Voltage




Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
V_{GS} = 0
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0.5
0.4
0.3
0.2
0.1
0
0.4
0.8
1.2
1.6
2.0

Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.011 g

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