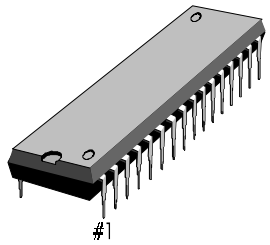
INTRODUCTION

The KB22688E is a monolithic integrated circuit designed for demodulating two carrier TV-MPX broadcast.

32–SDIP–400



FEATURES

- 1st & 2nd Sound IF
- Double-PLL FM Detection
- AGC for CCA part
- Matrix for Multi-Sound Broadcasts
- Pilot Detector
- External Control Interface
- ID Indicators (Stereo, Bilingual)
- Available for Korea standard
- Non-clipping Output up to 400% modulation with AGC
- Available in DC control, Normal microcontroler control or IIC bus control systems
- ID output: Direct LED drive or IIC serial data output
- Non-adjust

ORDERING INFORMATION

Device	Package	Operating Temperature
KB22688E	32–SDIP–400	–10 to + 70 °C

BLOCK DIAGRAM

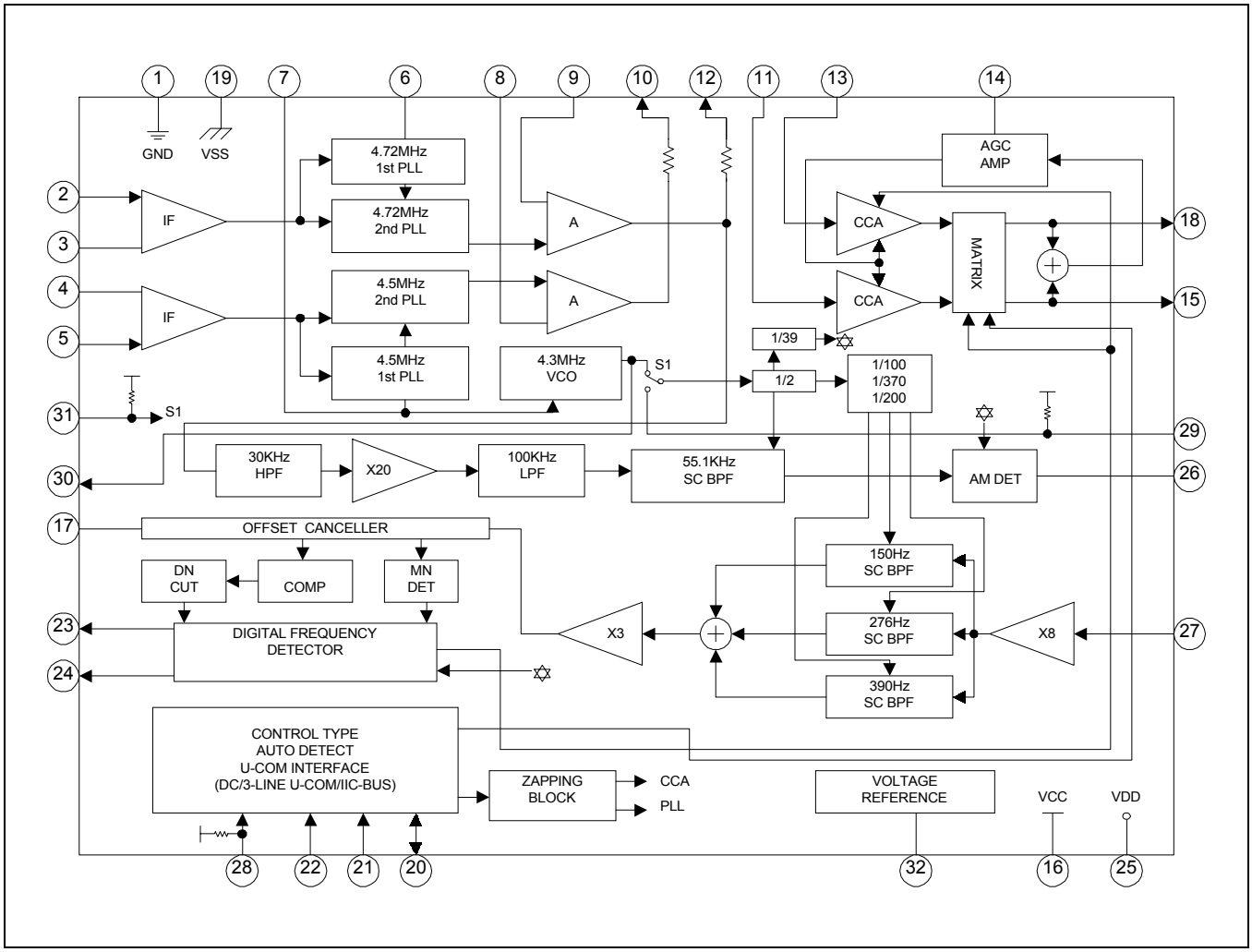


Figure 1.

PIN CONFIGURATION

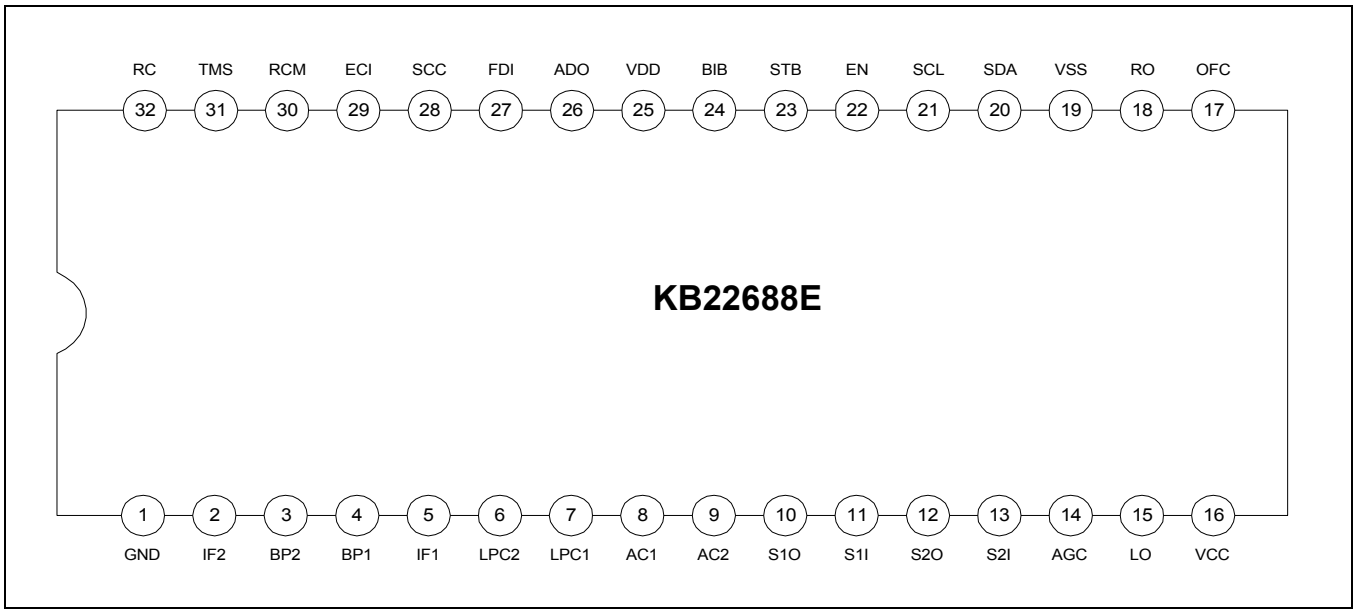


Figure 2.

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	Analog GND	17	ID Filter Offset Canceling Cap.
2	SIF 2 Input	18	R Output
3	SIF 2 Bypass	19	Digital VSS
4	SIF 1 Bypass	20	Data Input / Output (SDA)
5	SIF 1 Input	21	Clock Input (SCL)
6	SIF 2 LPF Capacitor	22	Enable Input (EN)
7	SIF 1 LPF Capacitor	23	ID Indicator (Stereo)
8	SIF 1 Amplifier Capacitor	24	ID Indicator (Bilingual)
9	SIF 2 Amplifier Capacitor	25	Digital VDD
10	SIF 1 DET Output	26	AM DET Output
11	SIF 1 CCA Input	27	Frequency DET Input
12	SIF 2 DET Output	28	Slave Custom Code
13	SIF 2 CCA Input	29	External Clock In
14	AGC Detect Capacitor	30	Reference Clock Monitor
15	L output	31	Test Mode Switch
16	Analog VCC	32	Voltage Reference Capacitor

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Supply voltage	VCC_{max}	Ta = 25 °C V_I = 0	–	–	6	V
Power Dissipation	P_D		–	–	1000	mW
Operating temperature	T_{OPR}		– 10	–	70	°C
Storage temperature	T_{STG}		– 40	–	125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{OPR}	–	4.7	5	5.5	V

ELECTRICAL CHARACTERISTICS

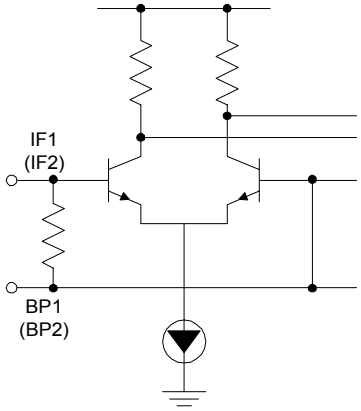
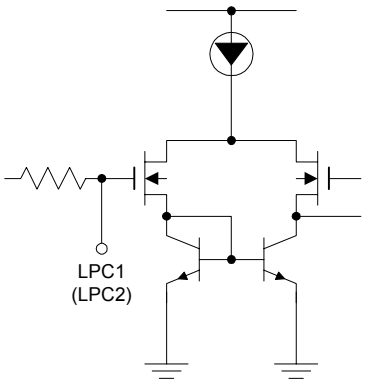
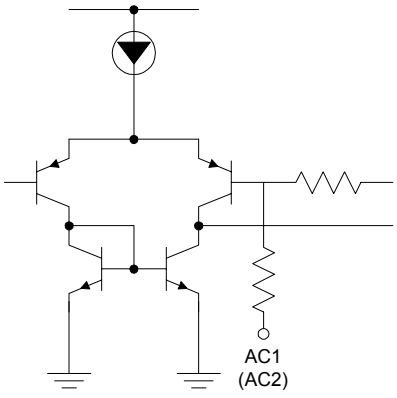
DC Electrical Characteristics

(Ta = 25°C, VCC = VDD = 5V, fm = 1kHz, V_I = 80dBμ, Δf = ± 25kHz, unless otherwise specified)

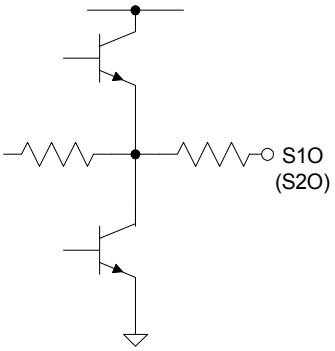
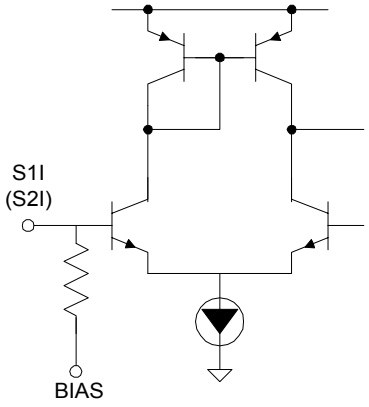
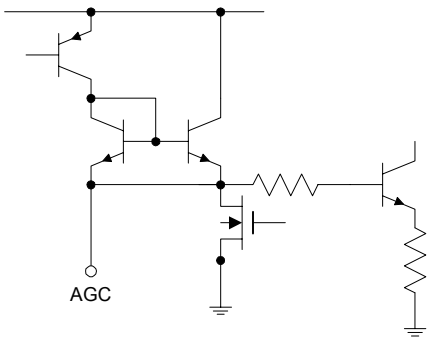
	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		ICC	Vi = 0	35	60	85	mA
		IDD	Vi = 0	–	–	2.0	mA
SIF	Input Limiting Voltage	Vlim	–	–	–	50	dBμ
	AM Rejection Ratio	AMRR	AM 30% Mod	40	55	–	dB
	Input Impedance	Zin	–	–	1	–	Kohm
PILOT *	Pilot Input Sensitivity	Vps	–	–	–	50	dBμ
	ID ON time	Ton	MONO → ST, BI	–	1.0	1.5	SEC
	ID OFF time	Toff	ST, BI → MONO	–	–	0.3	SEC
	Output level	Vo	–	380	450	520	mVrms
Matrix	Matrix THD	THDm1	–	–	0.2	1.0	%
		THDm2	Δ f = ± 100kHz	–	0.5	5.0	%
	Noise Output (RF off)	Voff	Carrier OFF	–	–	400	mVrms
	Output Impedance	Zout	–	–	–	50	ohm
	Separation Ratio	SEPtyp	non-adjust	25	–	–	dB
		SEPadj	IIC Bus adjust	40	45	–	dB
	Cross Talk	CT	Δ f = ± 25kHz	50	55	–	dB
	Matrix S/N Ratio	S/N	Δ f = ± 25kHz	55	60	–	dB
		S/N(st)	Δ f = ± 25kHz (ST)	50	55	–	dB
	MUTE Attenuation Ratio	Amute	Δ f = ± 25kHz	–	–66	–55	dB

* : Pilot signal FM deviation is ± 2.5kHz after 50% AM modulation.

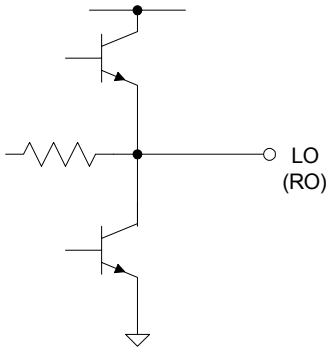
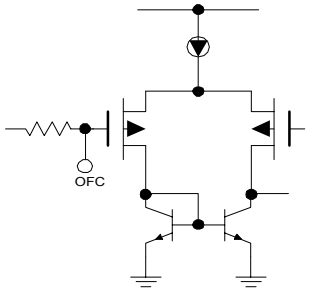
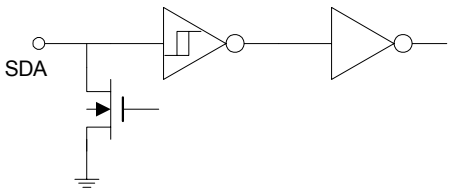
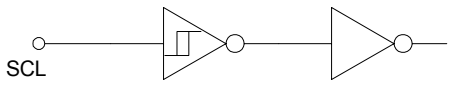
PIN DESCRIPTION

Pin No.	Symbol	Pin Name	Description	Internal Equivalence Circuit
1	GND	Analog ground	–	–
2, 5	SIF2, SIF1	SIF input pin	SIF signal input through a SIF filter	
3, 4	BP2, BP1	IF bypass pin	IF Bypass pin is grounded with a capacitor	
6, 7	LPC2, LPC1	PLL LPF pin	The external capacitor extracts DC level from the 1st PLL output of FM DET.	
8, 9	AC1, AC2	DET AMP NF pin	Negative feedback pin of FM DET amplifier Grounded with a capacitor	

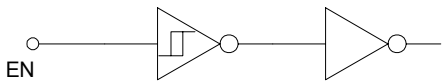
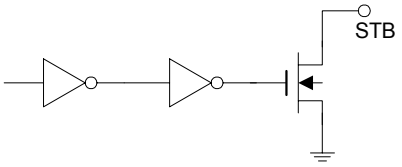
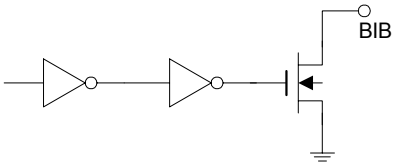
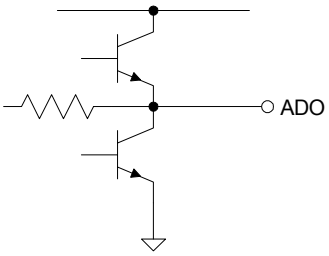
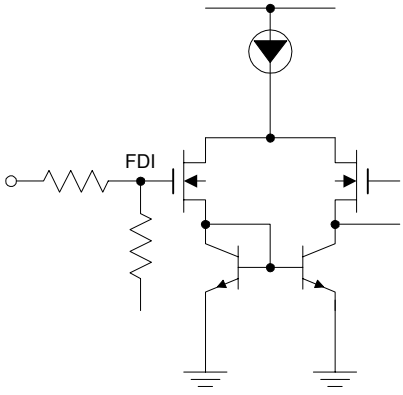
PIN DESCRIPTION (Continued)

Pin No.	Symbol	Pin Name	Description	Internal Equivalence Circuit
10, 12	S1O, S2O	FM DET output	FM DET output pin connected with a de-emphasis circuit	
11, 13	S1I, S2I	FM detected signal input pin	Input pin of current control amplifier (CCA). FM detected output signal is added to this pin.	
14	AGC	AGC DET pin	AGC detect pin is grounded through a capacitor. If the signal level is over the predetermined value, this terminal voltage will be raised. AGC function can be deactivated by connect this terminal to GND.	

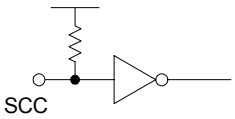
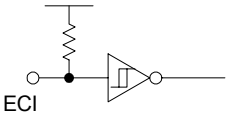
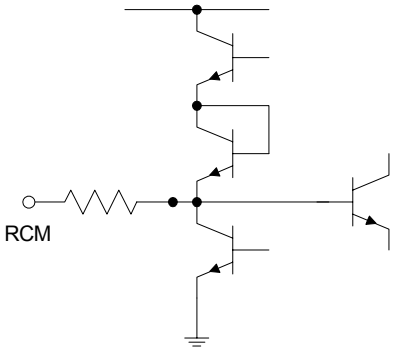
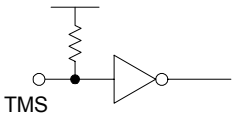
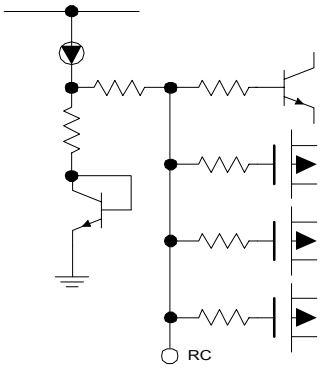
PIN DESCRIPTION (Continued)

Pin No.	Symbol	Pin Name	Description	Internal Equivalence Circuit
15, 18	LO, RO	Matrix output pin	Audio output signal is provided from this pin.	
16	VCC	Analog power	–	–
17	OFC	ID BPF offset cancel pin	The external capacitor is used to eliminate offset of ID filter	
19	VSS	Digital ground	–	–
20	SDA	Serial data input and output	It is the data communication line of IIC bus used to exchange the MICOM data and IC internal data.	
21	SCL	Clock signal	CLOCK line of IIC bus.	

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Pin Name	Description	Internal Equivalence Circuit
22	EN	Enable select pin	It is always “H” in DC control system, always “L” in IIC bus system, and used as strobe port in normal MICOM system.	
23	STB	Stereo indicator pin	When ID is detected as STEREO, this pin will remain “L” (OPEN DRAIN).	
24	BIB	Bilingual indicator pin	When ID is detected as Bilingual, this pin will remain “L” (OPEN DRAIN).	
25	VDD	Power supply (Digital)	–	–
26	ADO	AM DET output pin	AM detected signal will output from this terminal.	
27	FDI	Frequency DET input pin	AM detected signal goes into this terminal coupled with a capacitor to remove DC offset.	

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Pin Name	Description	Internal Equivalence Circuit
28	SCC	Slave custom code	When Open: Slave Address = 84H (Write), 85 (Read) When connect to VSS: Slave Address = 86H (Write), 87 (Read)	
29	ECI	External clock input pin	Normal is open. It can be used as high speed test for IC maker.	
30	RCM	Reference clock monitor	Internal Reference Clock Monitor IC maker test option	
31	TMS	Test mode Switch	Normal State: Open Test State: VSS IC maker test option	
32	RC	Voltage Reference Capacitor pin	Connect to capacitor to stabilize the reference voltage	

OPERATION DESCRIPTION

SYSTEM

KB22688E consists of IF AMP, FM DET, AGC, MATRIX, U-COM Control INTERFACE and ID DET blocks. All blocks are operable and available without adjust for Korea standard broadcast system.

IF AMP BLOCK

This block amplifies the provided IF signal to a detectable level of FM DET. Total gain is over 60dB and bandwidth is about 3 ~ 10MHz.

FM DET

KB22688E adopts non-adjust double-PLL type FM detection circuits. First PLL has a role of chasing FM carrier frequency with wide holding range (for example, hold range is 2MHz) and second PLL does actual FM detection with narrow holding range (about 300kHz), The free running frequency of 2nd PLL is same as the lock frequency of 1 st. PLL, and free running frequency of 1 st. PLL is determined by internal Resistor and Capacitor. The free running frequency can be varied by the variation of resistor and capacitor.

AGC

The AGC block comprises AGC detector part and CCA part (Current control Amplifier). The MATRIX output signal level is set to 400mVrms when applied 100% modulated FM signal and supply voltage is 5V. As the gain of CCA is about 6 dB and the gain of matrix is 6dB, so the output signal level of CCA is 200 mVrms and the matrix output is 400 mVrms. If over- modulated (over 200%) FM signal is added to KB22688E input port, the output will be clipped by supply voltage dynamic limitation range (The linear amplify range is limited lower than 800 mVrms).

To prevent this problem, In KB22688E we use AGC circuit to reduce the gain of CCA part when the over- modulated FM signal has been applied, AGC circuit is deactivated until the modulation is over 200%. If AGC is activated, the THD and separation characteristics of output signal would be deteriorated because the gain of CCA is varied according to modulation ratio.

MATRIX

MATRIX part separates provided FM detected signal into MONO, STEREO, BILINGUAL, and SUB according to broadcast status and end users setting, it mainly consists of analog switches and operational amplifiers. The input and output signal format of MATRIX is shown as follows.

Broadcast Mode	Input		
	S1	S2	Remark
Stereo	L+R	L–R	–
Bilingual	Main	Sub	–
Mono	Main	None *	* can be main

User Select / Broadcast Mode	Output							
	Stereo		Bilingual		Sub		Mono	
	LOUT	ROUT	LOUT	ROUT	LOUT	ROUT	LOUT	ROUT
Stereo	2L	2R	L+R	L+R	L+R	L+R	L+R	L+R
Bilingual	Main	Main	Main	Sub	Sub	Sub	Main	Main
Mono	Main	Main	Main	Main	Main	Main	Main	Main

ID DET

ID signal is FM modulated to second carrier (SIF2) with a 2.5kHz FM modulation after AM modulated to 55kHz PILOT sub-carrier with a 50% AM modulation. ID DET part consists of 3 blocks: that is filter block for extracting pilot carrier, AM detector block for AM detection of ID signal and digital block for detecting the frequency of provided ID signal logically. In the filter block, audio signal is removed by HPF and pilot signal is extracted by the automatically adjusted switch - capacitor BPF (band pass filter) with a center frequency of 55kHz. ID signal is extracted from the pilot carrier in the AM detector block, then Digital block detects the frequency of ID signal, The ID signal can be detected in the range shown as follow:

ID	Low Off	Low On	High On	High Off
Stereo (150 Hz)	125 Hz	140 Hz	160 Hz	176 Hz
Bilingual (276 Hz)	237 Hz	255 Hz	300 Hz	312 Hz

This block's circuit is configured to reduce the blinking of the ID, and consequently has the following characteristics: typ 1 sec and Max 1.5 sec delay when converting from Mono to Stereo, or to Bilingual. 0.3 sec delay when converting from Stereo or Bilingual to Mono. Therefore, when changing the channels on your TV set, a minimum of 1.5 sec is needed for ID Detect Time.

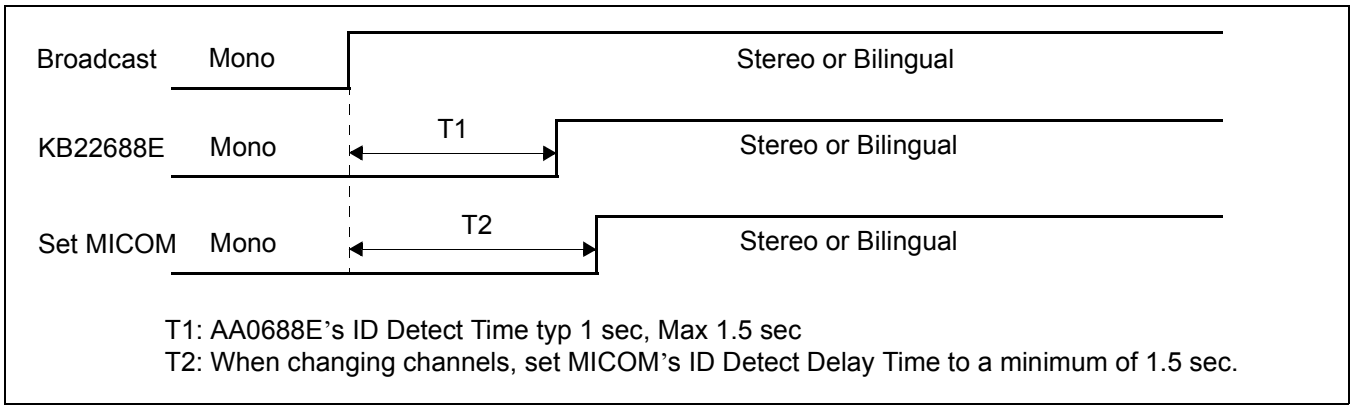


Figure 3. Timing Diagram for Changing Channels from Mono to stereo or Bilingual

The ID Detect Block of the KB22688E can momentarily malfunction if the signal is weak. Hence, we recommend that you delay for at least 1 sec at Set MICOM before detecting the ID, if the ID changes at a fixed channel.

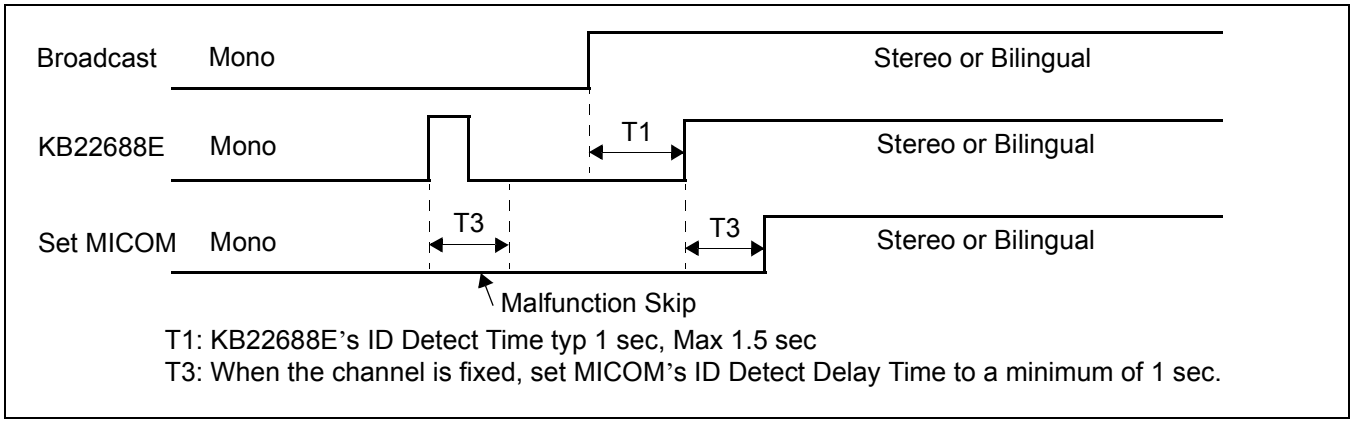


Figure 4. Timing Diagram when Channel is Fixed

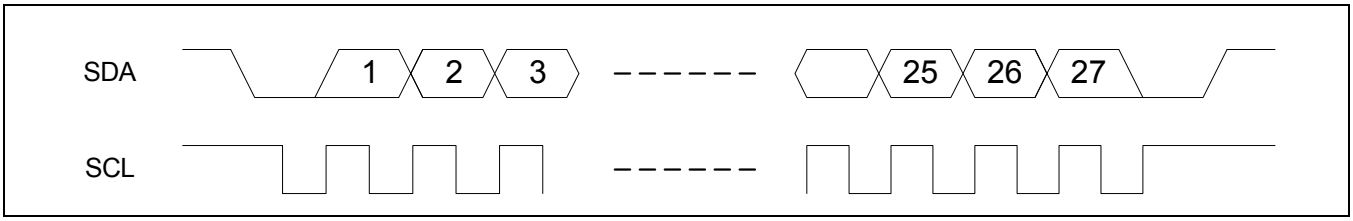
MICOM

KB22688E is available in DC control, normal microcontroller control, and IIC BUS microcontroller control system, and it can distinguish the control type automatically by monitoring PIN 22 (EN) status. The relation of control source type and PIN 22 status is shown as follows.

	IIC Bus	Normal MICOM	DC Control
EN (Pin 22)	always “L”	MICOM strobe	always “H”

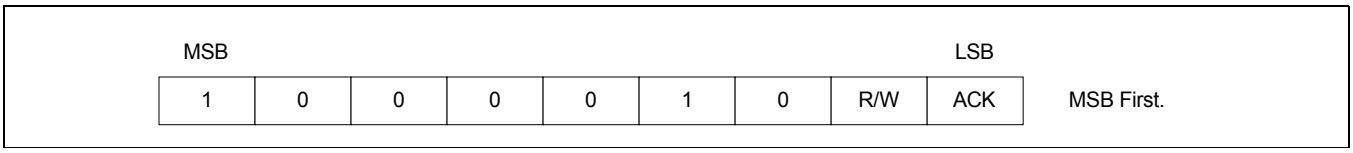
Protocol of IIC BUS microcontroller control (PIN 22: L)

The KB22688E can be controlled via the 2-line IIC BUS by the microcontroller. The two lines (SDA-serial data. SCL-serial clock) exchange information between the devices connected to the IIC bus. SDA is bidirectional line which is connected to a positive supply voltage via a pull up resistor. When the bus is free both lined are HIGH. The data on the SDA line must be stable during the High-powered of the clock. The HIGH or LOW data can only change when the clock signal line is LOW. A HIGH -to -LOW transition of the SDA line while SCL is HIGH is defined as a start condition. A LOW- to -HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition. The bus receiver will be reset by the reception of a start condition and is considered to be busy after the start condition. After a stop condition the bus is considered as free again.

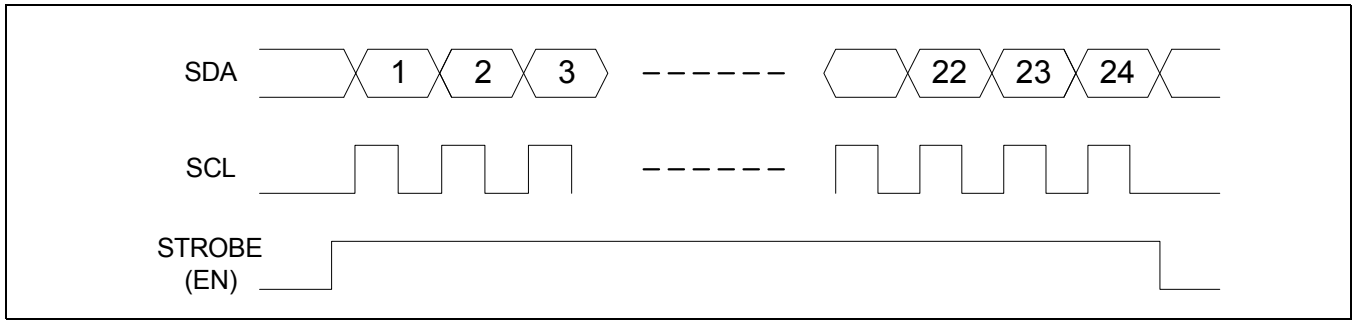


1st Byte	1 ~ 7th bit	Chip select code (1000010B)
	8th bit	R/W
	9th, 18th, 27th bit	Acknowledge
2nd Byte	10th ~ 17th bit	SUB address (function)
3rd Byte	197th ~ 26th bit	Data (D1 ~ D8)

Data transmitted to the KB22688E starts with the module address as follows:



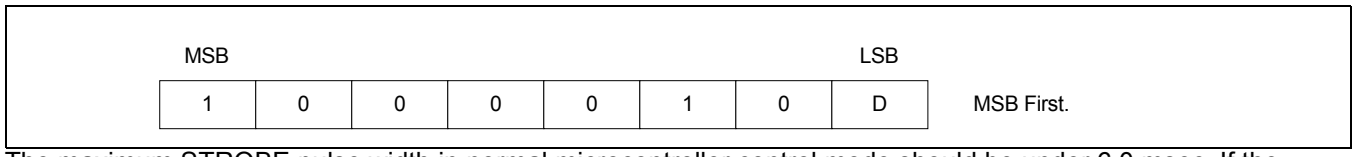
Protocol of normal microcontroller control (PIN 22: STROBE)



1st Byte	1 ~ 7th bit	Chip select code (1000010B)
	8th bit	Not use (don't care)
2nd Type	9th ~ 16th bit	Function assignment
3rd Type	17th ~ 24th bit	Data (D1 ~ D8)

The module address of KB22688E in normal microcontroller control mode is as follows:

.



The maximum STROBE pulse width in normal microcontroller control mode should be under 6.0 msec. If the STROBE pulse width excess the limit, KB22688E will be changed to DC control mode.

Control Item in Each Control Mode

In each control mode, control items is limited as follows:

Control	Mode Change	Mute	Preset	Pre-adjust set	Data Transmission	Receive Acknowledge
IIC Bus	O	O	O	O	O	O
Normal MICOM	O	O	O	×	×	×
DC Control	×	×	×	×	×	×

NOTES:

1. PRE-SET: When power is ON, MICOM initials the status of KB22688E to preset status. (All IC has same preset status data)
2. PRE-ADJUST SET: When power is ON, MICOM initials the status of KB22688E to pre-measured and stored status. (Different each IC)
3. DATA TRANSMISSION: Transmit stored data to MICOM when MICOM requests.
4. RECEIVE ACKNOWLEDGE: Return acknowledge signal to MICOM after DATA receipt.

MICOM control map

In IIC BUS mode, SLAVE Address = WRITE: 84H, READ: 85H
In normal MICOM mode, chip select code = 1000010B

SUB ADDRESS (2nd BYTE) (MSB<->LSB)	DATA (3rd BYTE) MSB							LSB	FUNCTION	REMARK
	D1	D2	D3	D4	D5	D6	D7	D8		
000XXXXX (Mode Control)	0	0	X	X	X	X	X	X	Mono	End user control
	1	0	X	X	X	X	X	X	Stereo	
	0	1	X	X	X	X	X	X	Bilingual	
	1	1	X	X	X	X	X	X	Sub	
001XXXXX (Mute Control)	0	X	X	X	X	X	X	X	Mute Off	
	1	X	X	X	X	X	X	X	Mute	
010XXXXX (Test Mode Control)	0	X	X	X	X	X	X	X	Normal mode	Ic maker test
	1	X	X	X	X	X	X	X	Test mode	
011XXXXX (Free Run Frequency Control)	0	0	X	X	X	X	X	X	Default	
	1	0	X	X	X	X	X	X	Frequency down	
	0	1	X	X	X	X	X	X	Default zap	
	1	1	X	X	X	X	X	X	Frequency down zap	
100XXXXX	D1	D2	D3	D4	D5	X	X	X	Separation adjust (3)	Set maker
101XXXXX	S1U	S1D	S2U	S2D	X	X	X	X	Pin DC cont.	IC maker test
110XXXXX (Test Mode)	0	0	X	X	X	X	X	X	Operating	
	1	0	X	X	X	X	X	X	Slave zap	
	0	1	X	X	X	X	X	X	Master zap	
	1	1	X	X	X	X	X	X	External clock	
111XXXXX	X	X	X	X	X	X	X	X	Not use	

NOTES:

1. MSB first
2. When power is ON, all latch data are “0”, KB22688C is set to MONO OFF, MUTE OFF, SEPARATION ADJUST DEFAULT (00001XXX).
3. Separation Adjust Data

D1	D2	D3	D4	D5			D1	D2	D3	D4	D5			D1	D2	D3	D4	D5	
0	0	0	0	0	(MIN)	<---	1	0	0	0	0	(TYP)	---->	1	1	1	1	1	(MAX)

Control Function Description

- MODE CONTROL: Control the MATRIX structure according to broadcast status and end user's setting. KB22688E has 4 modes (MONO, STEREO, BILINGUAL and SUB)
- MUTE CONTROL: When MUTE CONTROL is on, the audio output of KB22688E is off.
- SEP. ADJUST: The separation characteristic of KB22688E in STEREO mode can be controlled by IIC BUS. This option controls S2 FM demodulated output signal level so as to make the separation characteristic in best status.
- TEST MODE: IC makers test item.

DC Control Map (PIN22: H)

DC (Logic) Input		Function
SCL	SDA	
0	0	Mono
1	0	Stereo
0	1	Bilingual
1	1	Sub

READ Mode in IIC BUS MICOM Control Mode

KB22688E can transmit the data which is registered inside IC to the MICOM in IIC BUS control system.
If the 8th bit of module address is 'H', it means MICOM requests the data stored in the IC and KB22688Eenter data transmission mode. During the read mode, KB22688E ignores the data the data of 2nd type (SUB address) and transmits the internal data within the period of 3rd byte. The SDA line of MICOM should be maintain H to accept transmitted data from IC. The format of read data is as follows.no

Bit of 3rd Byte	1	2	3	4	Read Mode	5	6	7	8
Transmit Data	BI	ST	$\overline{BI}$	$\overline{ST}$		ZC	$\overline{ZC}$	0	1
	0	0	1	1	Mono	Option for IC maker (ZC: IC test option)			
	1	0	0	1	Bilingual				
	0	1	1	0	Stereo				
	Others				Transmission error				

Others

In IIC BUS control system, if the SLAVE address is correct, the acknowledge signal will be generated by KB22688E no matter the sub address is right or wrong, When sub address is wrong IC will do nothing.

NOTES:

1. The characteristic of SIF Filter should be suitable to MPX sound system.
   We suggest to use MURATA Co. products: SFSH4.5MCB and SFSH4.72MCB.
2. If you need to use two chip in one set (e.g. TVCR), You should separate the chips by select pin 28 voltage.
   When it is high or open, Write =84H, Read = 85H.
   When pin 28 is connected to ground, Write =86H, Read = 87H.
3. Program control method:
   1. Under window 95 environment, extract kb22688b.zip
   2. Install: setup.exe
   3. Run kb22688b.exe
4. PC parallel port pin description:

PIN	1	2	3	19
SIGNAL	SDA	SCL	EN	GND

TEST CIRCUIT

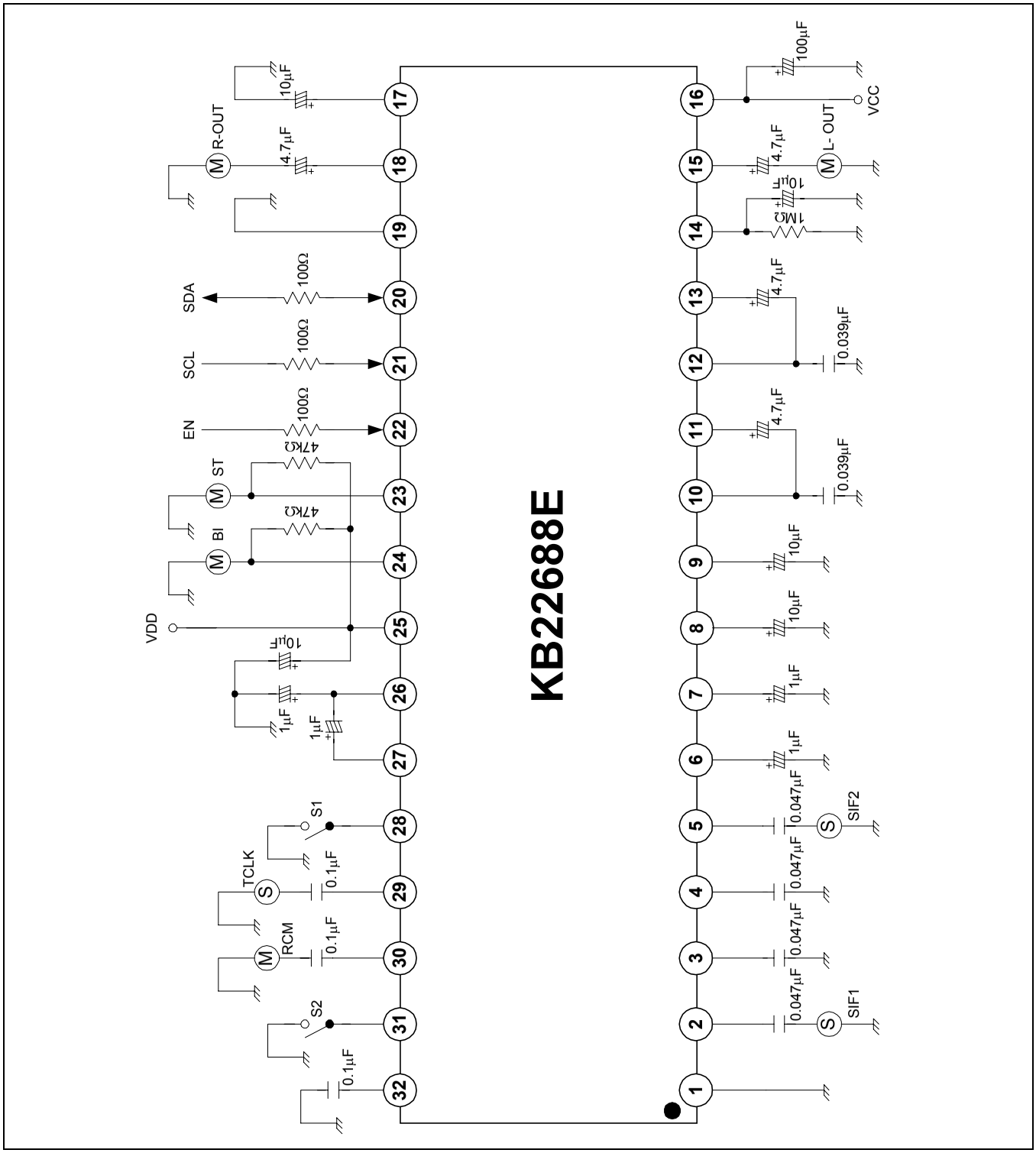


Figure 5.

APPLICATION CIRCUIT

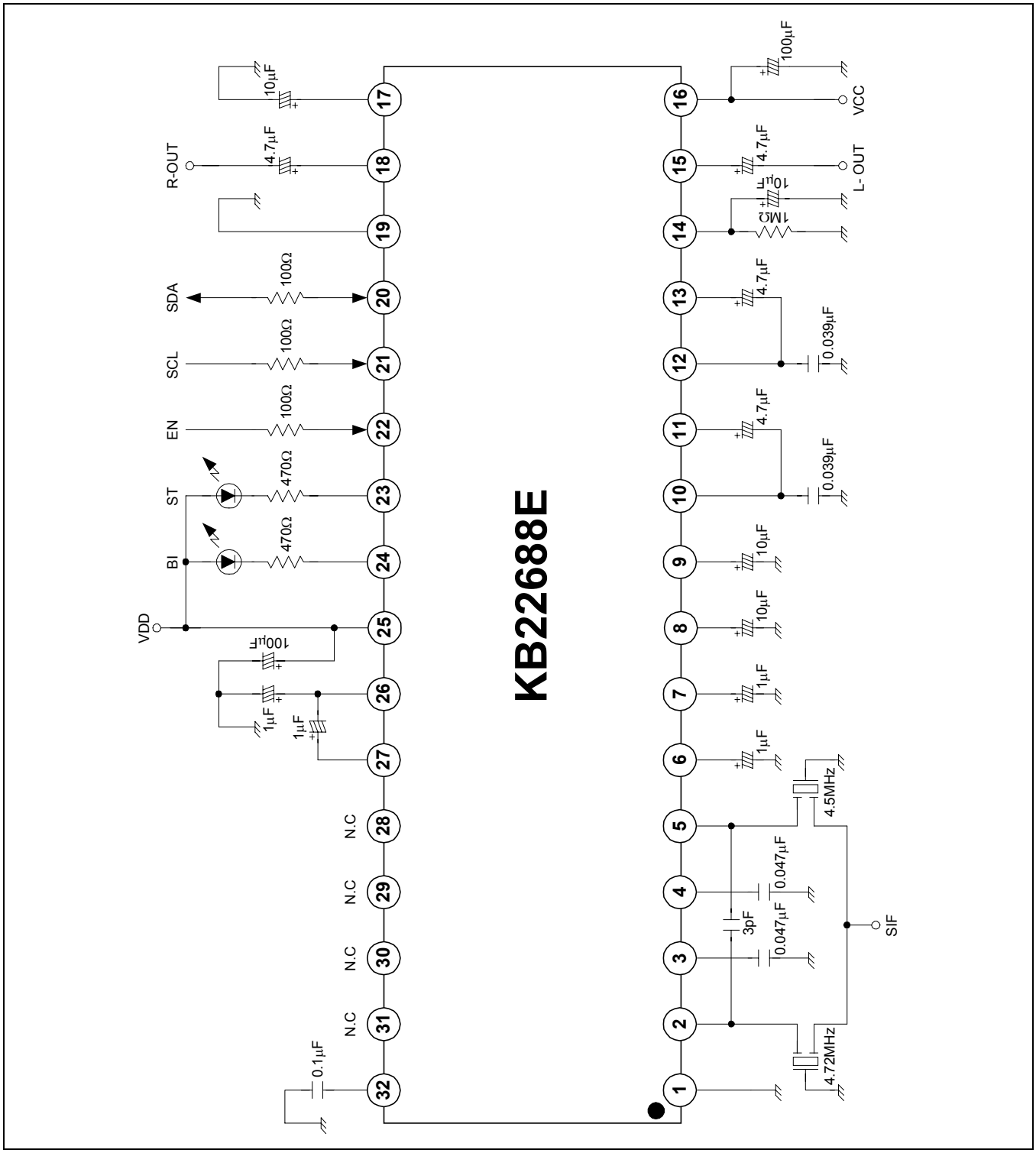


Figure 6.