Ordering number : ENA0253

SANYO Semiconductors
DATA SHEET

LA76814 — Monolithic Linear IC For NTSC Color Television Sets VIF/SIF/Y/C/Deflection Implemented in a Single Chip

Overview

LA76814 is VIF/SIF/Y/C/Deflection implemented in a single chip for NTSC color television sets.

Functions

- VIF/SIF/Y/C/Deflection implemented in a single chip.
- I^2C bus control.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_8 max		7.0	V
	V_{43} max		7.0	V
Maximum supply current	I_{18} max		25	mA
	I_{25} max		35	mA
Allowable power dissipation	Pd max	Ta ≤ 65°C *	1.5	W
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-55 to +150	°C

*: When mounted on a 114.3×76.1×1.6 mm^3 glass epoxy board

Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_8		5.0	V
	V_{43}		5.0	V
Recommended supply current	I_{18}		19	mA
	I_{25}		27	mA
Operating supply voltage range	V_8 op		4.7 to 5.3	V
	V_{43} op		4.7 to 5.3	V
Operating supply current range	I_{18} op		17 to 21	mA
	I_{25} op		24 to 30	mA

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Electrical Characteristics Ta = 25°C, V_{CC} = V_8 = V_{43} = 5.0V, I_{CC} = I_{18} = 19mA, I_{CC} = I_{25} = 27mA

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit voltage, current						
IF supply current	I_8	V_8 = 5V, V_3 = 2.5V		61.0		mA
RGB supply voltage	V_{18}	I_{18} = 19mA		8.0		V
Horizontal supply voltage	V_{25}	I_{25} = 27mA		5.0		V
Video supply current	I_{43}	I_{43} = 5V		94.0		mA
VIF block						
Maximum RFAGC voltage	VRFH	CW = 80dBμ, DAC = 0	8.5	9.0		Vdc
Minimum RFAGC voltage	VRFL	CW = 80dBμ, DAC = 63	0.0	0.3	0.7	Vdc
RF AGC Delay Pt (@DAC = 0)	RFAGC0	DAC = 0	85			dBμ
RF AGC Delay Pt (@DAC = 63)	RFAGC63	DAC = 63			75	dBμ
Input sensitivity	Vi	Output-3db		43	46	dBμ
No-signal video output voltage	VOn	No signal	3.3	3.7	4.1	Vdc
Sync signal tip level	VOtip	CW = 80dBμ	1.1	1.4	1.7	Vdc
Video output amplitude	VO	80dBμ, AM = 78%, fm = 15kHz	1.9	2.0	2.1	Vp-p
Video S/N	S/N	CW = 80dBμ	45	49		dB
C-S beat level	IC-S	V3.58MHz/V920kHz	40	45		dB
Differential gain	DG	80dBμ, 87.5% Video MOD		5.0	10.0	%
Differential phase	DP	80dBμ, 87.5% Video MOD		2.0	10.0	deg
Maximum AFT output voltage	VAFTH	CW = 80dBμ, frequency variations	4.3	4.7	5.0	Vdc
Minimum AFT output voltage	VAFTL	CW = 80dBμ, frequency variations	0.0	0.2	0.7	Vdc
AFT detection sensitivity	VAFTS	CW = 80dBμ, frequency variations	18.0	28.0	38.0	mV/kHz
APC pull-in range (U)	fPU		1.0			MHz
APC pull-in range (L)	fPL		1.0			MHz
SIF block						
FM detection output voltage	SOADJ			620		mVrms
FM limiting sensitivity	SLS	Output -3dB		47	55	dBμ
FM detection output f characteristics	SF	fm = 100kHz	-0.5		3.0	dB
FM detection output distortion	STHD	FM = ±25kHz			1.0	%
AM rejection ratio	SAMR	AM = 30%	40			dB
SIF S/N	SSN	DIN.Andio	57	61		dB
de-emph time constant	SNTC		2.0	3.0	4.0	dB
BPF band characteristics	SBW			1.5		dB
AUDIO block						
Maximum gain	AGMAX	1kHz	-2.5	0.0	2.5	dB
Variable range	ARANGE		60	65		dB
Frequency characteristics	AF	20kHz	-3.0	0.0	3.0	dB
Mute	AMUTE		70	75		dB
Distortion	ATHD	1kHz, 400mVrms, Vol: MAX			0.5	%
S/N	ASN	DIN.Audio	65	70		dB
Crosstalk	ACT		70	75		dB
Chroma block						
ACC amplitude characteristics 1	ACCM1_N	Input: +6dB/0dB 0dB = 40IRE	0.8	1.0	1.2	deg
ACC amplitude characteristics 2	ACCM2_N	Input: -14dB/0dB	0.7	1.0	1.1	deg
B-Y/Y amplitude ratio	CLRBY		80	100	150	%
Color control characteristics 1	CLRMN	Color MAX/CEN	1.6	1.8	2.2	deg
Color control characteristics 2	CLRMM	Color MAX/MIN	30	45	70	dB
Color control sensitivity	CLRSE		1	1.4	4	%/bit
Tint center	TINCEN		-10	0	10	deg
Tint variable range (+)	TINT+		35			deg
Tint variable range (-)	TINT-				-35	deg

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Demodulation output ratio R-Y/B-Y	RB_N	R-Y/B-Y_Angle_DAC	0.80	0.90	1.00	deg
Demodulation output ratio G-Y/B-Y	GB_N	R-Y/B-Y_Angle_DAC	0.24	0.30	0.36	deg
Demodulation angle R-Y/B-Y	ANGRB_N	R-Y/B-Y_Angle_DAC = Center	95	105	115	deg
Demodulation angle G-Y/B-Y	ANGGB_N	R-Y/B-Y_Angle_DAC = Center	-130	-118	-100	deg
Killer operating point	KILL_N	0dB = 40IRE	-41	-35	-29	dB
APC pull-in range (+)	PULIN+_N		350			Hz
APC pull-in range (-)	PULIN-_N				-350	Hz
Residual higher harmonic level B	E_CAR_B				300	mVp-p
Residual higher harmonic level R	E_CAR_R				300	mVp-p
Residual higher harmonic level G	E_CAR_G				300	mVp-p
OSD block						
OSD Fast SW threshold	FSTH		1.7	2	2.5	V
Red RGB output level	$R_{OSD}C$			100		IRE
Green RGB output level	$G_{OSD}C$			100		IRE
Blue RGB output level	$B_{OSD}C$			100		IRE
Analog OSD R output amplitude gain match	R_{RGB}		0.8	1	1.2	Ratio
Analog OSD G output amplitude gain match	G_{RGB}		0.8	1	1.2	Ratio
Analog OSD B output amplitude gain match	B_{RGB}		0.8	1.0	1.2	Ratio
RGB output (cutoff drive) block						
Brightness control — Normal	BRT63		1.8	2.15	2.5	V
Brightness control — Hi brightness (max)	BRT127		15	20	25	IRE
Brightness control — Low brightness (min)	BRT0		-25	-20	-15	IRE
Cutoff control (min)	Vbias0		1.8	2.2	2.6	V
(Bias control) (max)	Vbias255		2.8	3.2	3.6	V
Resolution	Vbiassns			4		mV/Bit
Sub-bias control Resolution	Vsbiassns			8		mV/Bit
Drive adjustment Maximum output (R, B)	RBout127			2.5		Vp-p
Drive adjustment Maximum output (G)	Gout15			2.15		Vp-p
Output attenuation (R, B)	RBout0		7	9	11	dB
Output attenuation (G)	Gout0		3	5	7	dB
Gamma correction	RGBγ		78	85	92	IRE
Video SW block						
Video signal input 1DC voltage	VIN1DC		2.2	2.5	2.8	V
Video signal input 1AC voltage	VIN1AC			1		Vp-p
Video signal input 2DC voltage	VIN2DC		2.2	2.5	2.8	V
Video signal input 2AC voltage	VIN2AC			1		Vp-p
SVO terminal DC voltage	SVODC		1.7	2	2.3	V
SVO terminal AC voltage	SVOAC		1.7	2	2.3	Vp-p

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Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Filter block							
Chroma trap amount NTSC		Ctrap	SHARPNESS = 0	-36.0	-26.0	-22.0	dB
C-BPF1A (3.08MHz)		CBP308	Reference: 3.58MHz	-5.0	-1.5	0.0	dB
C-BPF1B (3.88/3.28MHz)		CBP03	Reference: 3.28MHz	-2.0	0.0	2.0	dB
C-BPF1C (4.08/3.08MHz)		CBP05	Reference: 3.08MHz	-3.0	0.0	3.0	dB
Y-DL TIME1 S-VHS		TdY1	FILTER SYS = 100	300.0	350.0	400.0	ns
Y-DL TIME3 NTSC		TdY3	FILTER SYS = 000	530.0	580.0	630.0	ns
Video block							
Video overall gain (Contrast max)		CONT127		9.0	11.0	13.0	dB
Contrast adjustment Characteristics	Normal/max	CONT63		-7.5	-6.0	-4.5	dB
	Min/max	CONT0		-15.0	-12.0	-9.0	dB
Sharpness variability range	Normal	Sharp16	F = 2.2MHz, FILTER SYS = 0000	5.0	8.0	11.0	dB
	Max	Sharp31	F = 2.2MHz, FILTER SYS = 0000	9.0	12.0	14.0	dB
	Min	Sharp0	F = 2.2MHz, FILTER SYS = 0000	-4.0	-1.0	2.0	dB
Maximum black stretch gain		BKSTmax		20.0	25.0	30.0	IRE
Black stretch threshold (60IRE Δblack)		BKSTTH		-5.0	0.0	5.0	IRE
DC transmission amount		ClampG		95.0	100.0	105.0	%
Horizontal/vertical blanking output level		RGBBLK		0.1	0.4	0.7	V
Video frequency characteristics 1 S-VHS		BW1	7.0MHz/100kHz	-6.0	-3.0	-1.0	dB
Video frequency characteristics 3 NTSC		BW3	2.6MHz/100kHz	-6.0	-3.0	-1.0	dB
Deflection block							
Horizontal free-running frequency		fH		15600	15734	15850	Hz
Horizontal pull-in range		fH PULL		±400			Hz
Horizontal output pulse width		Hduty		36.1	37.6	39.1	μs
Horizontal output pulse saturation voltage		V Hsat		0	0.2	0.4	V
Vertical free-running frequency 60		VFR60		262.0	262.5	263.0	H
Horizontal output pulse phase		HPHCEN		9.5	10.5	11.5	μs
Horizontal position adjustment range		HPHrange	5bit		±2.2		μs
Horizontal position adjustment maximum variability width		HPHstep				200.0	ns
POR circuit operating voltage		VPOR		3.70	4.00	4.30	V
Horizontal blanking	Left @0	BLKL0	BLKL: 000	7500	8300	9100	ns
	Left @7	BLKL7	BLKL: 111	10800	11600	12400	ns
	Right @0	BLKR0	BLKR: 000	1800	2600	3400	ns
	Right @7	BLKR7	BLKR: 111	-1100	-300	500	ns
Sand castle	Pulse crest value H	SANDH		5.3	5.6	5.9	V
	Pulse crest value M1	SANDM1		3.7	4.0	4.3	V
	Pulse crest value L	SANDL		0.1	0.4	0.7	V
Burst gate pulse	Width	BGPWD		3.5	4.0	4.5	μs
	Phase	BGPPH		4.9	5.4	5.9	μs
X-ray protection circuit operating voltage		VXRAY		0.59	0.69	0.79	V

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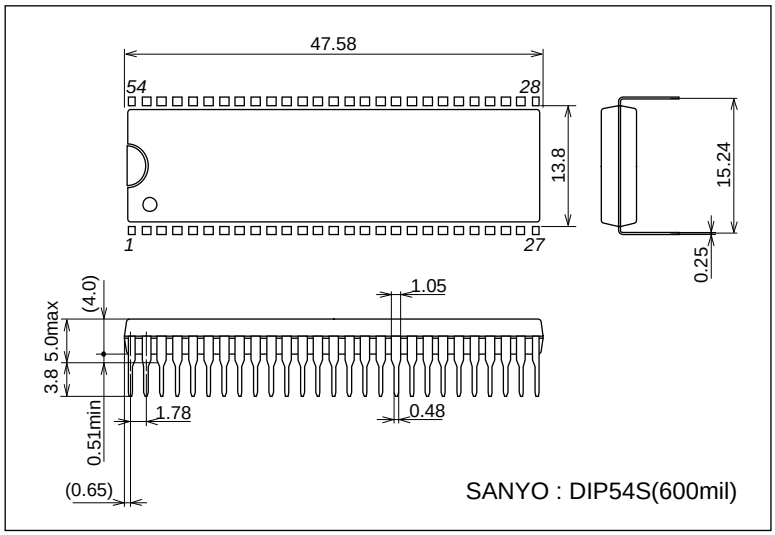
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Vertical screen size compensation							
Vertical ramp output amplitude	NTSC@64	Vsnt64	VSIZE: 1000000	0.75	0.85	0.95	Vp-p
	NTSC@0	Vsnt0	VSIZE: 0000000	0.40	0.50	0.60	Vp-p
	NTSC@127	Vsnt127	VSIZE: 1111111	1.05	1.20	1.35	Vp-p
High-voltage dependent vertical size correction							
Vertical size correction @0		Vsizecomp	VCOMP: 000	0.83	0.88	0.93	ratio
Vertical screen position adjustment							
Vertical ramp DC voltage	NTSC@32	Vdcnt32	VDC: 100000	2.25	2.40	2.55	Vdc
	NTSC@0	Vdcnt0	VDC: 000000	1.85	2.00	2.15	Vdc
	NTSC@63	Vdcnt63	VDC: 111111	2.65	2.80	2.95	Vdc
Vertical linearity	@16	Vlin16	VLIN: 10000	0.85	1.00	1.15	ratio
	@0	Vlin0	VLIN: 00000	1.17	1.32	1.47	ratio
	@31	Vlin31	VLIN: 11111	0.57	0.72	0.87	ratio
Vertical S-shaped correction	@16	VScor16	VSC: 10000	0.55	0.70	0.85	ratio
	@0	VScor0	VSC: 00000	0.85	1.00	1.15	ratio
	@31	VScor31	VSC: 11110	0.36	0.51	0.66	ratio
AKB							
AKB DC threshold		AKBDC		2.2	2.5	2.8	V

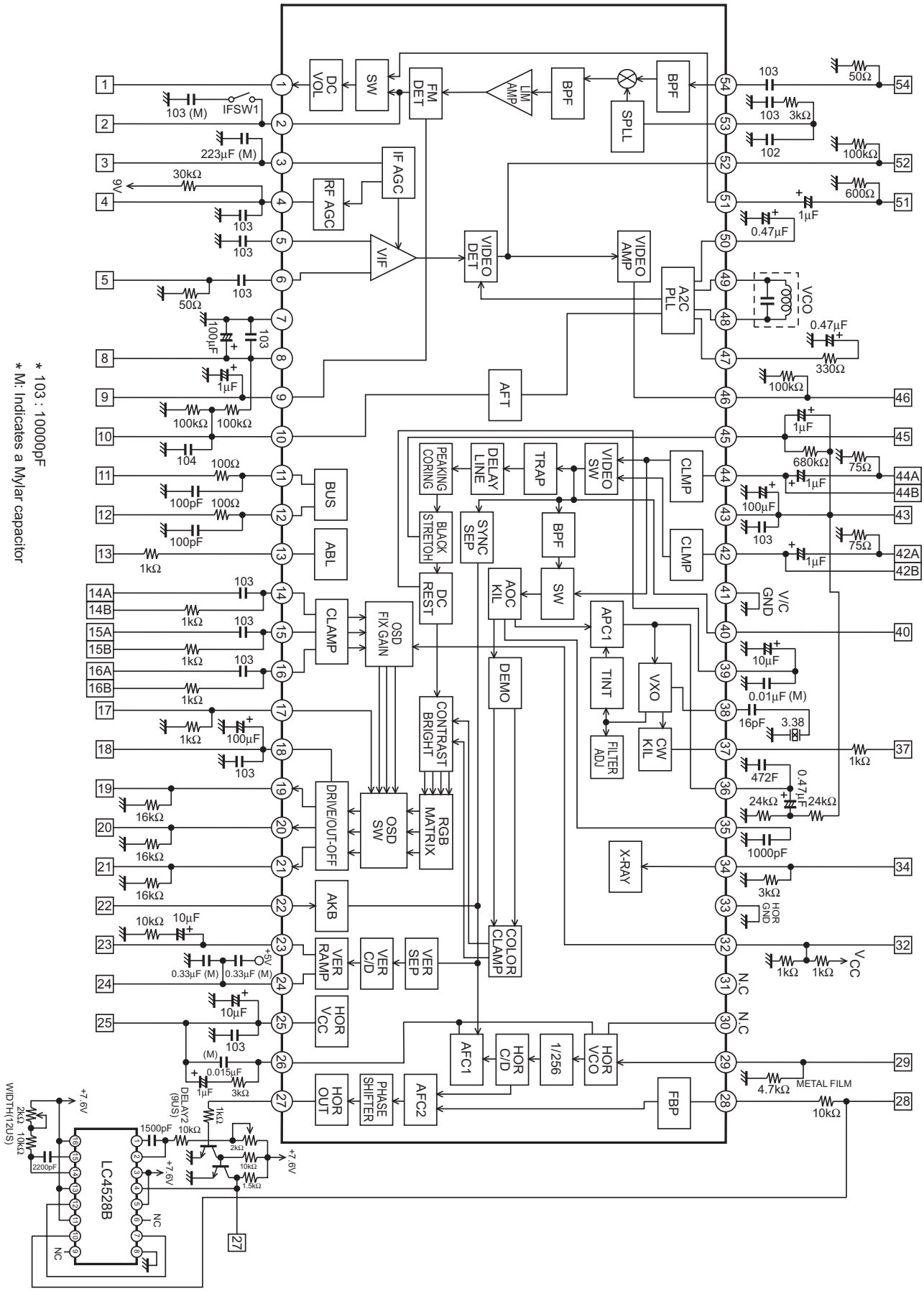
Package Dimensions

unit : mm

3273



Block Diagram and Test Circuit



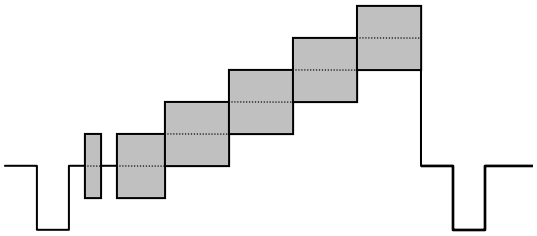
Test Conditions Ta = 25°C, V_{CC} = V_8 = V_{43} = 5.0V, I_{CC} = I_{25} = 27mA.

Circuit voltage, current

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal supply voltage	HV_{CC}	25		Apply a current of 27mA to pin 25 and measure the voltage at pin 25.	Initial
IF supply current	I_8	8	No signal	Apply a voltage of 5.0V to pin 43 and measure the incoming DC current [mA].	Initial
Video/vertical supply current	I_{43}	43		Apply a voltage of 5.0V to pin 43 and measure the incoming DC current [mA].	Initial

VIF Block Input Signals and Test Conditions

1. Input signals must all be input to the PIF IN (pin 6) in the Test Circuit.
2. All input signal voltage values are the levels at the VIF IN (pin 6) in the Test Circuit.
3. Signal contents and signal levels.

Input signal	Waveform	Conditions
SG1		45.75MHz
SG2		42.17MHz
SG3		41.25MHz
SG4		Frequency variable
SG5		45.75MHz 87.5% Video Mod. 10-stairstep wave (Subcarrier: 3.58MHz)
SG6		45.75MHz fm = 15kHz, AM = 78%

4. Before measurement, adjust the DAC as follows.

Parameter	Test point	Input signal	Adjustment
Video Level DAC	46	SG6, 80dBμ	Set the output level at pin 46 as close to 2.0Vp-p as possible.

VIF Block Test Conditions

Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Maximum RF AGC voltage		VRFH	4	SG1 80dBμ	Measure the DC voltage at pin 4.	RF.AGC = "000000"
Minimum RF AGC voltage		VRFL	4	SG1 80dBμ	Measure the DC voltage at pin 4.	RF.AGC = "111111"
RF AGC Delay Pt	(@DAC = 0)	RFAGC0	4	SG1	Obtain the input level at which the DC voltage at pin 4 becomes 4.5V.	RF.AGC = "000000"
	(@DAC = 63)	RFAGC63	4	SG1	Obtain the input level at which the DC voltage at pin 4 becomes 4.5V.	RF.AGC = "111111"
Input sensitivity		Vi	46	SG6	Using an oscilloscope, observe the level at pin 46 and obtain the input level at which the waveform's p-p value becomes 1.4Vp-p.	
No-signal video output voltage		VOn	46	No signal	Set IF AGC = "1" and measure the DC voltage at pin 46.	IF.AGC = "1"
Sync signal tip level		VOtip	46	SG1 80dBμ	Measure the DC voltage at pin 46.	
Video output amplitude		VO	46	SG6 80dBμ	Using an oscilloscope, observe the level at pin 46 and measure the waveform's p-p value.	
Video S/N		S/N	46	SG1 80dBμ	Measure the noise voltage at pin 46 with an RMS voltmeter through a 10kHz to 4.2MHz band-pass filter. ····Vsn 20Log (1.0/Vsn).	
C-S beat level		IC-S	46	SG1 SG2 SG3	Input a 80dBμ SG1 signal and measure the DC voltage (V3) at pin 3. Mix SG1 = 74dBμ, SG2 = 69dBμ, and SG3 = 49dBμ to enter the mixture in the VIF IN. Apply V3 to pin 3 from an external DC power supply. Using a spectrum analyzer, measure the difference between pin 46's 3.58MHz component and 920kHz component.	
Differential gain		DG	46	SG5 80dBμ	Using a vector scope, measure the level at pin 46.	
Differential phase		DP	46	SG5 80dBμ	Using a vector scope, measure the level at pin 46.	
Maximum AFT output voltage		VAFTH	10	SG4 80dBμ	Set and input the SG4 frequency to 44.75MHz. Measure the DC voltage at pin 10 at that moment.	
Minimum AFT output voltage		VAFTL	10	SG4 80dBμz	Set and input the SG4 frequency to 46.75MHz. Measure the DC voltage at pin 10 at that moment.	
AFT detection sensitivity		VAFTS	10	SG4 80dBμz	Adjust the SG4 frequency and measure frequency deviation Δf when the DC voltage at pin 10 changes from 1.5V to 3.5V. VAFTS = 2000/Δf [mV/kHz]	
APC pull-in range (U), (L)		fPU, fPL	46	SG4 80dBμ	Connect an oscilloscope to pin 46 and adjust the SG4 frequency to a frequency higher than 45.75MHz to bring the PLL into unlocked mode. (A beat signal appears.) Lower the SG4 frequency and measure the frequency at which the PLL locks again. In the same manner, adjust the SG4 frequency to a lower frequency to bring the PLL into unlocked mode. Lower the SG4 frequency and measure the frequency at which the PLL locks again.	

SIF Block (FM block) Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. Bus control condition: IF.AGC. = "1"
2. IFSW1 = "ON"
3. Input signals are input to pin 54 and the carrier frequency is 4.5MHz.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
FM detection output voltage	SOADJ	2	90dBμ, fm = 400Hz, FM = ±25kHz	Adjust the DAC (FM.LEVEL) to 7 and measure the 400Hz component of the FM detection output at pin 2. ···· SV1[mVrms]	FM.LEVEL = 7
FM limiting sensitivity	SLS	2	fm = 400Hz, FM = ±25kHz	Measure the input level (dBμ) at which the 400Hz component of the FM detection output at pin 2 becomes -3dB relative to SV1.	FM.LEVEL = 7
FM detection output f characteristics (fm = 100kHz)	SF	2	90dBμ, fm = 100kHz FM = ±25kHz	Set IFSW1 = "OFF". Measure the FM detection output of pin 2. ···· SV2[mVrms] SF = 20Log (SV1/SV2) [dB]	FM.LEVEL = 7
FM detection output distortion	STHD	2	90dBμ, fm = 400Hz, FM = ±25kHz	Measure the distortion factor of the 400Hz component of the FM detection output at pin 2.	FM.LEVEL = 7
AM rejection ratio	SAMR	2	90dBμ, fm = 400Hz, AM = 30%	Measure the 400Hz component of the FM detection output at pin 2. Assign the measured value to SV3. ···· SV3[mVrms] SAMR = 20Log (SV1/SV2) [dB]	FM.LEVEL = 7
SIF.S/N	SSN	2	90dBμ, CW	Measure the noise level (DIN AUDIO) at pin 2. ···· SV4[mVrms] SSN = 20Log (SV1/SV4) [dB]	FM.LEVEL = 7
NT de-emph time constant	SNTC	2	90dBμ, fm = 2.12kHz FM = ±25kHz	Measure the 2.12kHz component of the FM detection output at pin 2. ···· SV5[mVrms] SNTC = 20Log (SV1/SV5) [dB]	FM.LEVEL = 7
BPF band characteristics	SBW	2	90dBμ, CW	Set SW: IF1 = "OFF". PIN 9 = 5V Measure the 646kHz component at pin 2. ···· SV6[mVrms] Set the input frequency to 4.65MHz to the input frequency and measure the 496kHz component at pin 2. ···· SV7[mVrms] SBW = 20Log (SV6/SV7) [dB]	FM.LEVEL = 7

Audio Block Input Signals and Test Conditions

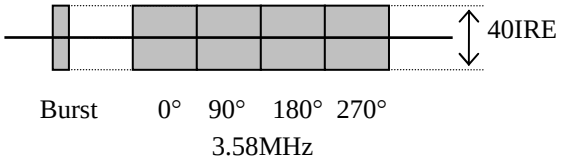
Unless otherwise specified, the following conditions apply when each measurement is made.

1. Bus control condition:
   AUDIO.MUTE = "0", AUDIO.SW = "1", VOL.FIL = "0", IF.AGC. = "1"
2. Input 4.5MHz, 90dBμ and CW at pin 54.
3. Enter an input signal from pin 51.

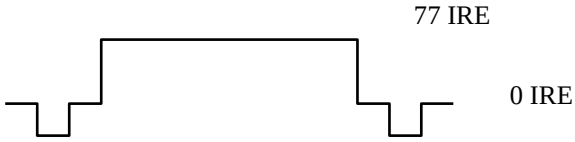
Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Maximum gain	AGMAX	1	1kHz, CW 400mVrms	Measure the 1kHz component at the pin 1. ···· V1[mVrms] AGMAX = 20Log (V1/400) [dB]	VOLUME = "1111111"
Variable range	ARANGE	1	1kHz, CW 400mVrms	Measure the 1kHz component at the pin 1. ···· V2[mVrms] ARANGE = 20Log (V1/V2) [dB]	VOLUME = "0000000"
Frequency characteristics	AF	1	20kHz, CW 400mVrms	Measure the 20kHz component at the pin 1. ···· V3[mVrms] AF = 20Log (V3/V1) [dB]	VOLUME = "1111111"
Mute	AMUTE	1	1kHz, CW 400mVrms	Measure the 20kHz component at the pin 1. ···· V4[mVrms] AMUTE = 20Log (V1/V4) [dB]	VOLUME = "1111111" AUDIO.MUTE = ”1”
Distortion	ATHD	1	1kHz, CW 400mVrms	Measure the distortion of the 1kHz component at the pin 1.	VOLUME = "1111111"
S/N	ASN	1	No signal	Measure the noise level (DIN AUDIO) at the pin 1. ···· V5[mVrms] ASN = 20Log (V1/V5) [dB]	VOLUME = "1111111"
Crosstalk	ACT	1	1kHz, CW 400mVrms	Measure the 1kHz component at the pin 1. ···· V6[mVrms] ACT = 20Log (V1/V6) [dB]	VOLUME = "1111111" AUDIO.SW = "0"

Chroma input signal:

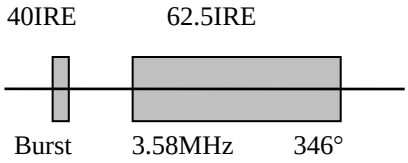
C-1



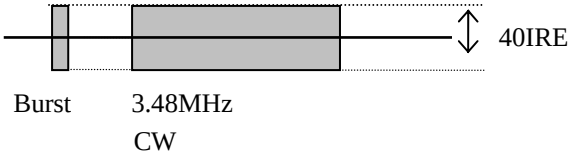
77IRE signal (L-77)



C-2

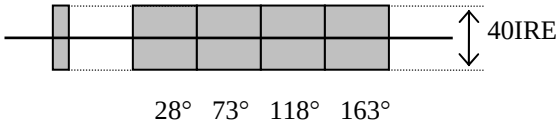


C-3

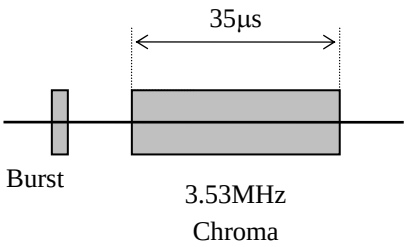


(If a frequency is specified, use the specified frequency.)

C-4



C-5



Chroma Block Test Conditions

Parameter		Symbol	Test point	Input signal	Test method	Bus conditions
ACC amplitude	Charac-teristics 1	ACCM1	Bout 21	C-1 0dB +6dB	Measure the output when 0dB is applied to the chroma input and the output amplitude when +6dB is applied to the chroma input and calculate the ratio between them. ACCM1 = 20Log (+6dBdata/0dBdata)	
	Charac-teristics 2	ACCM2	Bout 21	C-1 -14dB	Measure the output when 0dB is applied to the chroma input and the output amplitude when -14dB is applied to the chroma input and calculate the ratio between them.. ACCM2 = 20Log (-14dBdata/0dBdata)	
B-Y/Y amplitude ratio		CLRBY	21	YIN: L77 C-1:No signal	Measure the Y system's output level. ···· V1	
				C-2	Input a signal to the CIN (only sync signal to the YIN) and measure the output level to calculate as follows: CLRBY = 100×(V2/V1)+15%	
Color control	Charac-teristics 1	CLRMN	21	C-3	Measure the output amplitude V1 at color control MAX mode and output amplitude V2 at color control NOM mode. CLRMN = V1/V2	Color: 1111111 (Max) Color: 1000000 (NOM)
	Charac-teristics 2	CLRMM	21	C-3	Measure the output amplitude V3 at color control MIN mode. CLRMM = 20Log (V1/V3)	Color: 0000000 (Min)
Color control sensitivity		CLRSE	21	C-3	Measure the output amplitude V4 at color control 90 mode and output amplitude V5 at color control 38 mode to calculate as follows: CLRSE = 100×(V4-V5)/(V2×52)	Color: 1011010 Color: 0100110
Tint center		TINCEN	21	C-1	Measure each part of the output waveform and calculate the B-Y axis angle.	TINT: 1000000
Tint control	MAX	TINMAX	21	C-1	Measure each part of the output waveform and calculate the B-Y axis angle as follows: TINMAX = B-Y axis angle-TINCEN	TINT: 1111111
	MIN	TINMIN	21	C-1	Measure each part of the output waveform and calculate the B-Y axis angle as follows: TINMIN = B-Y axis angle-TINCEN	TINT: 0000000
Tint control sensitivity		TINSE	21	C-1	Measure the angle A1 at TINT control 85 mode and angle A2 at TINT control 42 mode. TINSE = (A1-A2)/43	TINT: 1010101 TINT: 0101010
Demodulation output ratio R-Y/B-Y		RB	19 20 21	YIN: L77 C-1: No signal YIN: 0 IRE C-3	Input a signal to YIN and adjust DAC in R and B drives so that the Y output levels at pins 17 and 19 become as close to the level at 18 as possible. (*1) After that, input 0 IRE to YIN and C-3 to CIN. Measure BOUT output amplitude Vb and ROUT output amplitude Vr and calculate RB=Vr/Vb.	Color: 1000000 Adjustment value in B and R drives: *1
Demodulation output ratio G-Y/B-Y		GB	20	C-3	Measure GOUT output amplitude Vg and calculate GB = Vg/Vb. For the R/B Drive, the adjustment value: *1 applies.	Color: 1000000 Adjustment value in B and R drives: *1
Demodulation angle R-Y/B-Y		ANGRB	21 19	C-1	Measure each output level of the BOUT and ROUT and calculate the angles of the B-Y axis and R-Y axis. ANGBR = (R-Y angle)-(B-Y angle)	

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Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Demodulation angle G-Y/B-Y	ANGGB	20	C-1	Measure each output level of the GOUT and calculate the angle of the G-Y axis. ANGBG = (G-Y angle)-(B-Y angle)	
Killer operating point	KILL	21	C-3	Reduce the input signal until the output level becomes 50mVp-p or less. Measure the input level at that moment.	
Chroma VCO free-running frequency	CVCOF	35	CIN: No signal	Measure oscillation frequency f. CVCOF = f-3579545 (Hz)	
fsc output amplitude	C_FSC	21	C-1	Measure 3.58MHz CW output amplitude at pin 37.	

Chroma BPF Block Test Conditions

Parameter		Symbol	Test point	Input signal	Test method	Bus conditions
Band-pass amplitude character-istic	3.08MHz	CBP308	21	C-3	Measure V5 output amplitude. Set the chroma frequency (CW) to 3.08MHz and measure V6 output amplitude. CBE308 = 20Log (V6/V5)	FILTER.SYS: 1 C.BYPASS: 0
	3.88/3.28 MHz	CBP03	21	C-3	Measure V7 output amplitude when the chroma frequency (CW) is 3.28MHz and V8 output amplitude when it (CW) is 3.88 MHz. CBE = 20Log (V8/V7)	FILTER.SYS: 1 C.BYPASS :0
	4.08/3.08 MHz	CBP05	21	C-3	Set the chroma frequency (CW) to 4.08MHz and measure V9 output amplitude. CBE05 = 20Log (V9/V6)	FILTER.SYS: 1 C.BYPASS: 0

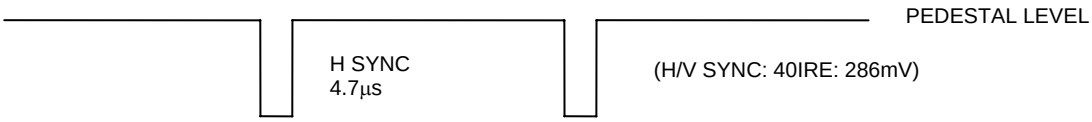
Video Block Input Signals and Test Conditions

Chroma input signal* chroma or burst signal: 40 IRE

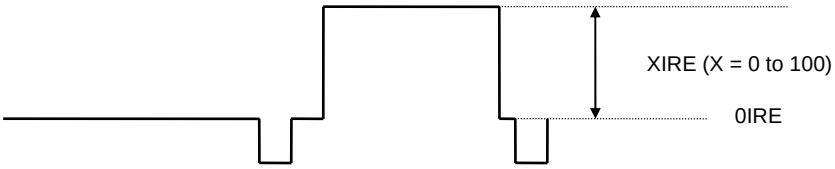
Y input signal: 1001RE (714mV)

Bus control bit conditions: Initial state

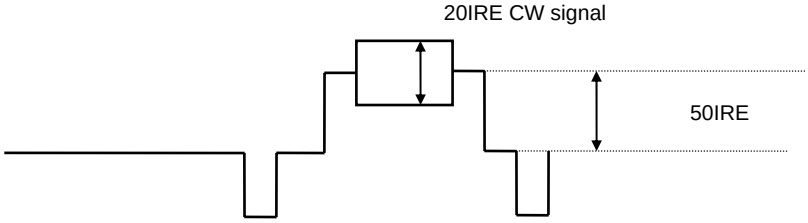
0IRE signal (L-0): NTSC standard signal



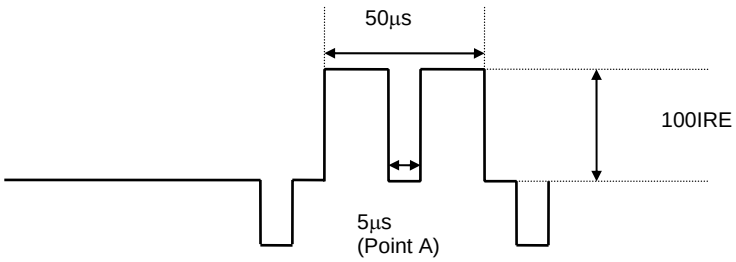
XIRE signal (L-X)



CW signal (L-CW)

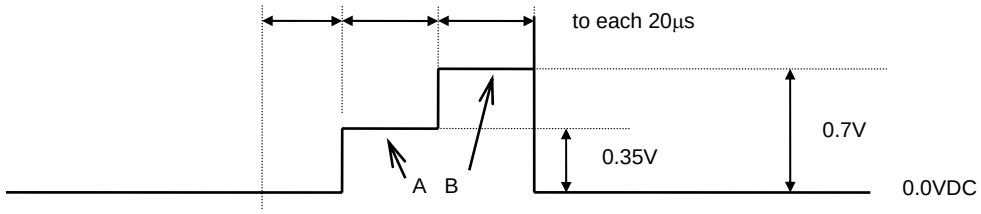


BLACK STRETCH 0IRE signal (L-BK)

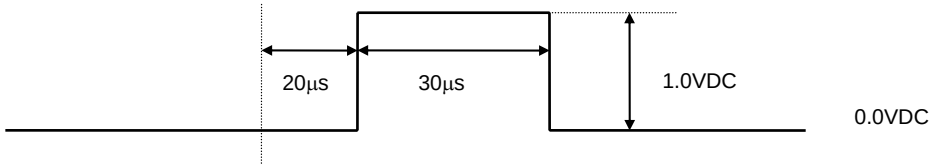


R/G/B IN Input signal

RGB Input signal 1 (0-1)



RGB Input signal 2 (0-2)



First conditions: Pin 13: 5V, Pin 14: GND, Pin 15: GND, Pin 16: GND, Pin 17: GND.

Video Block Test Conditions

Parameter		Symbol	Test point	Input signal	Test method	Bus conditions
Video overall gain (Contrast max)		CONT127	21	L-50	Measure the output signal's 50IRE amplitude. ···· CNTHB[Vp-p] CONT127 = 20Log (CNTHB/0.357).	CONTRAST: 1111111
Contrast adjustment characteristics	Normal /max	CONT63	21	L-50	Measure the output signal's 50IRE amplitude. ···· CNTCB[Vp-p] CONT63 = 20Log (CNTCB/0.357).	CONTRAST: 0111111
	Min/ max	CONT0	21	L-50	Measure the output signal's 50IRE amplitude. ···· CNTLB[Vp-p] CONT0 = 20Log (CNTLB/0.357).	CONTRAST: 0000000
Video frequency Characteristics	SVHS	BW1	21	L-CW	With the input signal's continuous wave = 100kHz, measure the output signal's continuous wave amplitude. ···· PEAKDC[Vp-p] With the input signal's continuous wave = 7MHz, measure the output signal's continuous wave amplitude. ···· CW7[Vp-p] BW1 = 20Log (CW7/PEAKDC)	FILTER SYS: 100 SHARPNESS: 000000
	NTSC	BW3	21	L-CW	With the input signal's continuous wave = 2.5MHz, measure the output signal's continuous wave amplitude. ···· CW2.5[Vp-p] BW3 = 20Log (CW2.5/PEAKDC)	FILTER SYS: 0000 SHARPNESS: 000000
Chroma trap amount		Ctrap	21	L-CW	With the input signal's continuous wave = 3.58MHz, measure the output signal's continuous wave amplitude. ···· F00[Vp-p] Ctrap = 20Log (F00/PEAKDC)	FILTER SYS: 000 SHARPNESS: 000000
DC transmission amount		ClampG	21	L-0	Measure the output signal's 0IRE DC level. ···· BRTPL[V]	Brightness: 0000000 CONTRAST: 1111111
				L-100	Measure the output signal's 0IRE DC level: DRVPH[V] and 100IRE amplitude: DRVH[Vp-p]. ClampG = 100 × (1+(DRVPH-BRTPL)/DRVH).	Brightness: 0000000 Contrast: 1111111
Y-DL TIME	SVHS	TdY1	21	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	FILTER SYS: 100
	NTSC	TdY3	21	L-50	Obtain the time difference (the delay time) from when the rise of the input signal's 50IRE amplitude to the output signal's 50IRE amplitude.	FILTER SYS: 000
Maximum black stretch gain		BKSTmax	21	L-BK	Measure the 0IRE DC level at point A of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode. ···· BKST1[V] Measure the 0IRE DC level at point A of the output signal in the Black Stretch ON mode. ···· BKST2[V] BKSTmax = 2×50× (BKST1-BKST2)/CNTHB	Blk Str DEF: 0
Black stretch threshold Δblack (60IRE Δblack)		BKSTTHΔ	21	L-40	Measure the 40IRE DC level of the output signal in the Black Stretch Defeat ON mode. ···· BKST3[V] Measure the 60IRE DC level of the output signal in the Black Stretch Defeat (Black Stretch OFF) mode. ···· BKST4[V] BKSTTHΔ = 50× (BKST4-BKST3)/CNTHB	Blk Str DEF: 0

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Parameter		Symbol	Test point	Input signal	Test method	Bus conditions
Sharpness variability characteristics	Normal	Sharp16	21	L-CW	With the input signal's continuous wave = 2.2MHz, measure the output signal's continuous wave amplitude. ···· F00S16 [Vp-p] Calculate Sharp16 = 20Log (F00S16/PEAKDC).	FILTER SYS: 000 Sharpness: 10000
	Max	Sharp31		L-CW	With the input signal's continuous wave = 2.2MHz, measure the output signal's continuous wave amplitude. ···· F00S31 [Vp-p] Calculate Sharp31 = 20Log (F00S31/PEAKDC).	Sharpness: 11111
	Min	Sharp0		L-CW	With the input signal's continuous wave=2.2MHz, measure the output signal's continuous wave amplitude. ···· F00S0 [Vp-p] Calculate Sharp0 = 20Log (F00S0/PEAKDC).	Sharpness: 00000
Horizontal/vertical blanking output level		RGBBLK	21	L-100	Measure the DC level (RGBBLK V) for the output signal's blanking period.	

OSD Block Test Conditions

When measuring the OSD block, set the bus bit to 63(0111111) for Contrast, 63(0111111) for Brightness.

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
OSD Fast SW threshold	FSTH	21	L-0 O-2	Apply voltage to pin 17 and measure the voltage at pin 17 at the point where the output signal switches to the OSD signal.	Pin 14A: O-2 applied
Red RGB output level	ROSDC	19	L-50 L-0 O-2	Measure the output signal's 50IRE amplitude. ···· CNTCR [Vp-p] Measure the OSD output amplitude. ···· OSDHR [Vp-p] ROSDH = 50×(ROSDH /CNTCR)	 Pin 17: 3.5V Pin 14A: O-2 applied
Green RGB output level	GOSDC	21	L-50 L-0 O-2	Measure the output signal's 50IRE amplitude. ···· CNTCG [Vp-p] Measure the OSD output amplitude. ···· OSDHG [Vp-p] GOSDC = 50×(OSDHG/CNTCG)	 Pin 17: 3.5V Pin 15A: O-2 applied
Blue RGB output level	BOSDC	21	L-50 L-0 O-2	Measure the output signal's 50IRE amplitude. ···· CNTCB [Vp-p] Measure the OSD output amplitude. ···· OSDHB [Vp-p] BOSDC = 50 × (OSDHB/CNTCB)	 Pin 17: 3.5V Pin 16A: O-2 applied
Analog OSD R output level		19	L-0 O-1	Measure the amplitudes at point A (0.35V portion of the input signal 0-1) and point B (0.7V portion of the input signal 0-1) of the output signal. Assign the measured values to RGBLR Vp-p and RGBHR Vp-p, respectively.	Pin 17 : 3.5V Pin 14A : O-1 applied
Gain match	RRGB			RRGB = RGBLR/CNTCR.	
Linearity	LRRGB			LRRGB = 100×(RGBLR/RGBHR).	
Analog OSD G output level		20	L-0 O-1	Measure the amplitudes at point A (0.35V portion of the input signal 0-1) and point B (0.7V portion of the input signal 0-1) of the output signal. Assign the measured values to RGBLG Vp-p and RGBHG Vp-p, respectively.	Pin 17: 3.5V Pin 15A: O-1 applied
Gain match	GRGB			GRGB = RGBLG/CNTCG.	
linearity	LGRGB			LGRGB = 100×(RGBLG/RGBHG).	

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Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
Analog OSD B output level		21	L-0 O-1	Measure the amplitudes at point A (0.35V portion of the input signal 0-1) and point B (0.7V portion of the input signal 0-1) of the output signal. Assign the measured values to RGBLB Vp-p and RGBHB Vp-p, respectively.	Pin 17: 3.5V Pin 16A: O-1 applied
Gain match	BRGB			BRGB = RGBLB/CNTCB.	
Linearity	LBRGB			LBRGB = 100×(RGBLB/RGBHB).	

RGB Output Block (Cutoff, drive block) Test Conditions

When measuring the RGB block, set the bus bit to 127(01111111) for Contrast.

Parameter		Symbol	Test point	Input signal	Test method	Bus conditions
Brightness control	Normal	BRT63	19 20 21	L-0	Measure the 0IRE DC levels of the RGB output signals. R output (pin 19) ···· BRTPCR [V] G output (pin 20) ···· BRTPCG [V] B output (pin 21) ···· BRTPCB [V] BRT63 = (BRTPCR+BRTPCG+BRTPCB)/3.	Brightness: 01111111
	Max	BRT127	21		Measure the 0IRE DC level of the output signal of B output (21). ···· BRTPHB [V] BRT127 = 50×(BRTPHB-BRTPCB)/CNTHB.	Brightness: 1111111
	Min	BRT0			Measure the 0IRE DC level of the output signal of B output (21). ···· BRTPHB [V] BRT0 = 50×(BRTPLB-BRTPCB)/CNTHB.	Brightness: 0000000
Bias (cutoff) control	Min	Vbias0	19 20 21	L-50	Measure the 0IRE DC levels of the RGB output signals. R output (pin 19) ···· Vbias0R [V] G output (pin 20) ···· Vbias0G [V] B output (pin 21) ···· Vbias0B [V]	Sub-Brightness: 0000000
	Max	Vbias255			Measure the 0IRE DC levels of the RGB output signals. R output (pin 19) ···· Vbias255R [V] G output (pin 20) ···· Vbias255G [V] B output (pin 21) ···· Vbias255B [V]	Sub-Brightness: 1111111 Red/Green/Blue Bias: 11111111
Bias (cutoff) control resolution		Vbiassns			Measure the 0IRE DC levels of the RGB output signals. R output (pin 19) ···· BAS80R [V] G output (pin 20) ···· BAS80G [V] B output (pin 21) ···· BAS80B [V]	Red/Green/Blue Bias:01010000
					Measure the 0IRE DC levels of the RGB output signals. R output (pin 19) ···· BAS48R [V] G output (pin 20) ···· BAS48G [V] B output (pin 21) ···· BAS48B [V]	Red/Green/Blue Bias: 00110000
					Vbiassns* = (BAS80*-BAS48*)/32 *: R, G, B	
Sub-bias control resolution		Vsbiassns		L-50	Measure the 0IRE DC levels of the RGB output signals. R output (pin 19) ···· SBTPMR [V] G output (pin 20) ···· SBTPMG [V] B output (pin 21) ···· SBTPMB [V] Vsbiassns* = (BRTPC*-SBTPM*) *: R, G, B	Sub-Brightness: 0101010 Contrast: 0111111

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Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Drive adjustment maximum output	RBout127 Gout15	19 20 21	L-100	Measure the 100IRE amplitude of the R, B output signals. R output (pin 19) ···· DRVHR [Vp-p] B output (pin 21) ···· DRVHB [Vp-p] Measure the 0IRE DC levels of the G output signals. G output (pin 20) ···· DRVHG [Vp-p]	Brightness: 0000000
Output attenuation	RBout0 Gout0			Measure the 100IRE amplitude of the R, B output signals. R output (pin 19) ···· DRVLR [Vp-p] B output (pin 21) ···· DRVLB [Vp-p] Measure the 0IRE DC levels of the G output signals. G output (pin 20) ···· DRVHG [Vp-p] RBout0* = 20Log (DRVH*/DRVL*) Gout0* = 20Log (DRVH*/DRVL*)	Brightness: 0000000 Red/Blue Drive: 0000000
Gamma correction	Rγ Gγ Bγ	19 20 21	L-100	Measure the 100IRE amplitude of the RGB output signals with Gamma Def being ON and OFF. ···· *A, *B [Vp-p]	Gamma Def: Off, On B Gamma sel: 11, 00
				γ = 100(*A/*B) * : R, G, B	

VIDEO SW Block Test Conditions

When measuring the VIDEO SW block, set the bus bit to 63(0111111) for Contrast, 63(0111111) for Brightness.

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Video signal input 1DC voltage	V_{IN}1DC	42	L-100	Input signals to pin 42 and measure the voltage of the pedestal.	VIDEO SW: 1
Video signal input 2DC voltage	SVODC	44	L-100	Input signals to pin 44 and measure the voltage of the pedestal.	VIDEO SW: 0
SVO terminal DC voltage	SVODC	40	L-100	Input signals to pin 42 and measure the voltage of the pedestal at pin 40.	VIDEO SW: 1
SVO terminal AC voltage	SVOAC	40	L-100	Input signals to pin 42 and measure the voltage of the pedestal at pin 40.	VIDE0 SW: 1

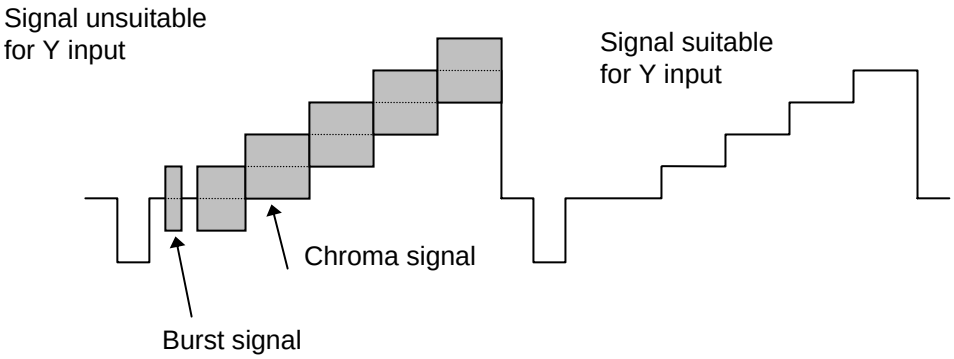
Deflection Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. VIF, SIF blocks: No signal
2. C input: No. signal
3. Sync input: A horizontal/vertical composite sync signal

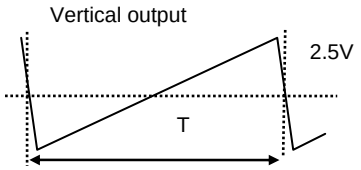
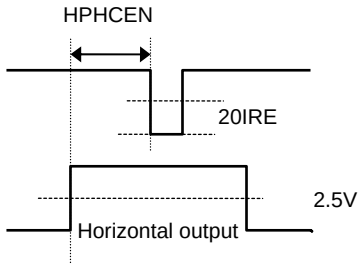
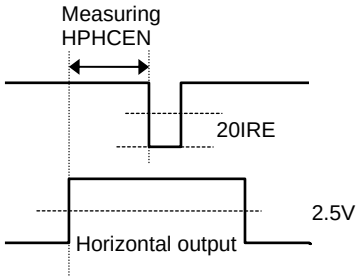
NTSC:40IRE, horizontal sync signal (15.734264kHz) and vertical sync signal (59.94kHz)

Note: No burst signal, chroma signal shall exist below the pedestal level.



4. Bus control conditions: Initial conditions unless otherwise specified.
5. The delay time from the rise of the horizontal output (pin 27 output) to the fall of the FBP IN (pin 28 input) is 9μs.
6. Pin 13 (ABL input, vertical size correction circuit input terminal) is connected to V_{CC} (5.0V).

Deflection Block Test Conditions

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal free-running frequency	fH	27	Y IN: No signal	Connect a frequency counter to the output of pin 27 (H out) and measure the horizontal free-running frequency.	
Horizontal pull-in range	fH PULL	42	YIN: Horizontal/ vertical sync signal	Using an oscilloscope, monitor the horizontal sync signal which is input to the Y IN (pin 42) and the pin 27 output (H out) and vary the horizontal signal frequency to measure the pull-in range.	
Horizontal output pulse length	Hduty	27	Y IN: Horizontal/ vertical sync signal	Measure the voltage for the pin 27 horizontal output pulse's low-level period.	
Horizontal output pulse saturation voltage	V Hsat	27	Y IN: Horizontal/ vertical sync signal	Measure the voltage for the pin 27 horizontal output pulse's low-level period.	
Vertical free-running period 60 (NTSC)	VFR60	23	Y IN: No signal	Measure the vertical output period T at pin 23 T×15.734kHz 	CDMODE: 0
Horizontal output pulse	HPHCEN	27 42	Y IN: Horizontal/ vertical sync signal	Measure the delay time from to the rise of the pin 27 horizontal output pulse to the fall of the Y IN horizontal sync signal. 	
Horizontal position adjustment range	HPHrange	27 42	Y IN: Horizontal/ vertical sync signal	With H PHASE: 0 and 31, measure the delay time from the rise of the pin 27 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the difference from H PHCEN. 	H PHASE: 00000 H PHASE: 11111

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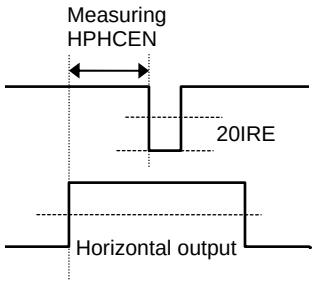
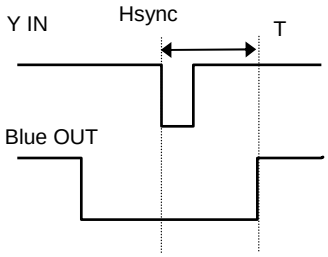
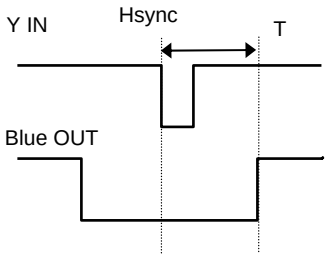
Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal position adjustment maximum variable width		HPHstep	27 42	Y IN: Horizontal/ vertical sync signal	With H PHASE: 0 to 31 varied, measure the delay time from to the rise of the pin 27 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the variation at each step. Retrieve data for maximum variation. 	H PHASE: 00000 to H PHASE: 11111
POR circuit operating voltage		VPOR	25	Y IN: Horizontal/ vertical sync signal	Connect a DC power supply in place of the current source to pin 25 and gradually decrease the voltage from 5.0V until the BUS READ TATUS [POR][STATUS1 (DA01) becomes "1". Measure the DC voltage at pin 28 at the moment.	
Horizontal blanking left variable range	@0	BLKL0	21 42	Y IN: Horizontal/ vertical sync signal	Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKL = 000. 	BLKL: 000
	@7	BLKL7			Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKL = 111. 	BLKL: 111

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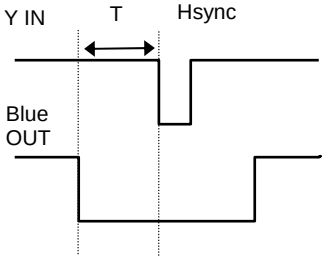
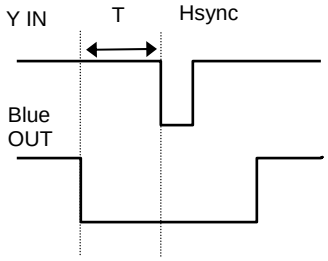
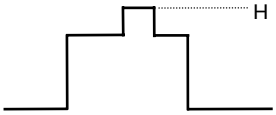
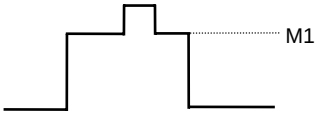
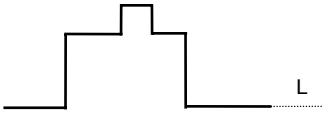
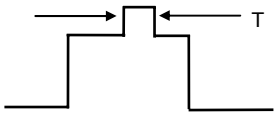
Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal blanking right variable range	@0	BLKR0	21 42	Y IN: Horizontal/ vertical sync signal	Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKR = 000. 	BLKR: 000
	@7	BLKR7			Measure the time T from the left end of Hsync at pin 42 Y IN to the left end of blanking at pin 21 BlueOUT with BLKR = 111. 	BLKR: 111
Sand castle pulse crest value	H	SANDH	28	Y IN: Horizontal/ vertical sync signal	Measure the supply voltage at point H of the pin 28 FBP IN wave form for Hsync period. 	
	M1	SANDM1			Measure the supply voltage at point M1 of the pin 28 FBP IN wave form for Hsync period. 	
	L	SANDL			Measure the supply voltage at point L of the pin 28 FBP IN wave form for Hsync period. 	
Burst gate pulse length		BGPWD	28	Y IN: Horizontal/ vertical sync signal	Measure the BGP width T of the pin 28 FBP IN wave form for Hsync period. 	

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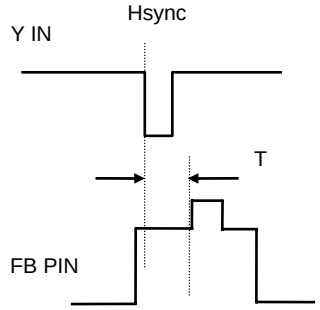
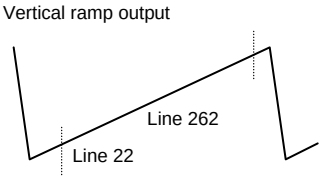
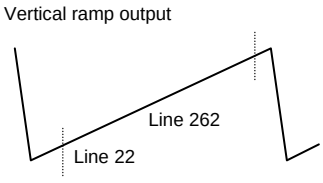
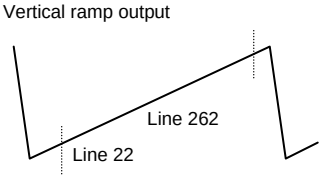
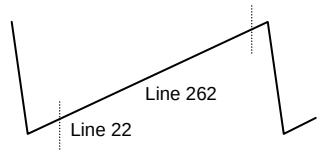
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Burst gate pulse I phase	BGPPH	28 42	Y IN: Horizontal/ vertical sync signal	Measure the time from the left end of Hsync at pin 42 Y IN to the left end of the pin 28 FBP IN wave form for Hsync period.  	
X-ray protection circuit operating voltage	VXRAY	27 34	Y IN: Horizontal/ vertical sync signal	Connect a DC power supply to pin 34 and gradually increase the voltage from 0V until the pin 27 horizontal output pulse ceases. Measure the DC voltage at pin 34 at that moment.	

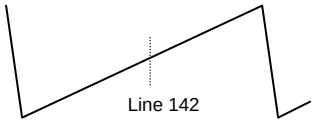
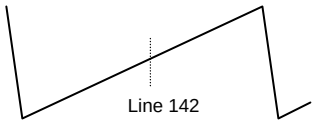
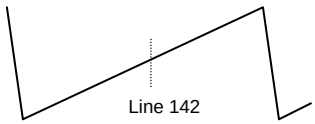
Vertical Screen Size Correction

Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Vertical ramp output Amplitude	@64	Vsnt64	23	Y IN: Horizontal/ vertical sync signal	Monitor the pin 23 vertical ramp output and measure the voltage at line 22 and line 262. Calculate as follows: Vspal64 = Vline262-Vline22  	
	@0	Vsnt0			Monitor the pin 23 vertical ramp output and measure the voltage at line 22 and line 262 Calculate as follows: Vspal64 = Vline262-Vline22  	VSIZE: 0000000
	@127	Vsnt127			Monitor the pin 23 vertical ramp output and measure the voltage at line 22 and line 262 Calculate as follows: Vspal64 = Vline262-Vline22  	VSIZE: 1111111

High-voltage Dependent Vertical Size Correction

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical size correction @0	Vsizecomp	23	Y IN: Horizontal/ vertical sync signal	Monitor the pin 23 vertical ramp output and measure the voltage at the line 22 and line 262 with VCOMP = 000. Calculate as follows: Va = Vline262-Vline22 Apply 4.0V to pin 11 and measure the voltage at the line 22 and line 262 again. Calculate as follows: Va = Vline262-Vline22 Calculate as follows: Vsizecomp = Vb/Va Vertical ramp output  	VCOMP: 000

Vertical screen position adjustment

Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Vertical ramp DC voltage	@32	Vdcnt32	23	Y IN: Horizontal/ vertical sync signal	Monitor the pin 23 vertical ramp output and measure the voltage at line 142. Vertical ramp output  	
	@0	Vdcnt0			Monitor the pin 23 vertical ramp output and measure the voltage at line 142. Vertical ramp output  	VDC: 000000
	@63	Vdcnt63			Monitor the pin 23 vertical ramp output and measure the voltage at line 142. Vertical ramp output  	VDC: 111111

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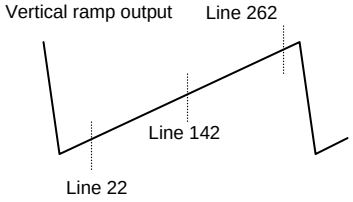
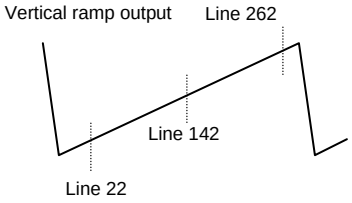
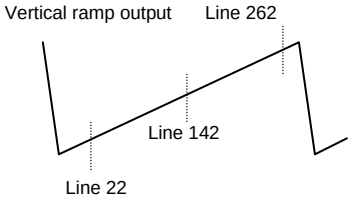
Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Vertical linearity	@16	Vlin16	23	Y IN: Horizontal/ vertical sync signal	Monitor the pin 23 vertical ramp output and measure the voltage at line 22, line 142 and 262. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin16 = (Vb-Va)/(Vc-Vb)  	
	@0	Vlin0			Monitor the pin 23 vertical ramp output and measure the voltage at line 22, line 142 and 262. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin0 = (Vb-Va)/(Vc-Vb)  	VLIN: 00000
	@31	Vlin31			Monitor the pin 23 vertical ramp output and measure the voltage at line 22, line 142 and 262 with vLIN = 11111. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin31 = (Vb-Va)/(Vc-Vb)  	VLIN: 11111

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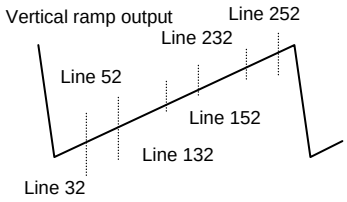
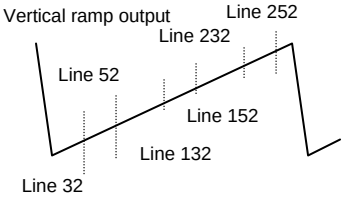
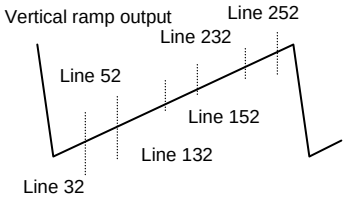
Input signal		Symbol	Test point	Input signal	Test method	Bus conditions
Vertical S-shaped correction	@16	VScor16	23	Y IN: Horizontal/ vertical sync signal	Monitor the pin 23 vertical ramp output and measure the voltage at line 32, line 52, line 132, line 152, line 232 and 252. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows: VScor16 = 0.5((Vb-Va)+(Vf-Ve))/(Vd-Vc) 	VS: 10000
	@0	VScor0			Monitor the pin 23 vertical ramp output and measure the voltage at the line 32, line 52, line 132, line 152, line 232 and line 252 with VSC = 000. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows: VScor0 = 0.5((Vb-Va)+(Vf-Ve))/(Vd-Vc) 	
	@31	VScor31			Monitor the pin 23 vertical ramp output and measure the voltage at line 32, line 52, line 132, line 152, line 232 and line 252 with VSC = 000. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows: Vscor31 = 0.5((Vb-Va)+(Vf-Ve))/(Vd-Vc) 	VSC: 11111
AKB DC threshold		AKBDC	22	Y IN: Horizontal/ vertical sync signal PAL or NTSC	Increase the DC voltage applied at pin 22 from 2.0V to 3.0V gradually and measure the DC voltage at pin 22 when BUS READ STATUS, [AKB (R, G, B)] and [STATUS2 (DA01, DA02, DA03)] become (1, 1, 1).	

Control Register Bit Allocation Map

Control Register Bit Allocations								
Sub Address	MSB			DATA BITS				LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
00000000	ON/OFF	AFC gain&gate	H.FREQ					
	1	0	1	1	1	1	1	1
00001	H BLK SW	Audio.Mute	Video.Mute	H.PAHSE				
	0	0	0	1	0	0	0	0
00010	Sync.Kill	V.SIZE						
	0	1	0	0	0	0	0	0
00011	VSEPUP	V.KILL	V.POSI					
	0	0	1	0	0	0	0	0
00100	Gray Mode	Cross B/W		V.LIN				
	0	0	0	1	0	0	0	0
00101	H BLK R&L			V.SC				
	1	0	0	0	0	0	0	0
00110	V.TEST		V.COMP			COUNT.DOWN.MODE	*	*
	0	0	1	1	1	0	(0)	(0)
00111	R.BIAS							
	0	0	0	0	0	0	0	0
01000	G.BIAS							
	0	0	0	0	0	0	0	0
01001	B.BIAS							
	0	0	0	0	0	0	0	0
01010	*	R.DRIVE						
	(0)	1	1	1	1	1	1	1
01011	Drive.Test	B γ Select		RG γ Def	G.DRIVE			
	0	0	0	1	1	0	0	0
01100	*	B.DRIVE						
	(0)	1	1	1	1	1	1	1
01101	Blank.Def	Sub.Bright						
	0	1	0	0	0	0	0	0
01110	*	Bright						
	(0)	1	0	0	0	0	0	0
01111	*	Contrast						
	(0)	1	0	0	0	0	0	0
10000	OSD Cnt.Test	*	*	*	*	*	OSD Contrast	
	0	(0)	(0)	(0)	(0)	(0)	0	0
10001	Blk.Str.Deff	Coring	Sharpness					
	1	1	0	0	0	0	0	0
10010	Tint.Test	Tint						
	0	1	0	0	0	0	0	0
10011	Color.Test	Color						
	0	1	0	0	0	0	0	0
10100	Video SW	Trap.Test			*	Filter.Sys		
	0	1	0	0	(0)	0	*	0
10101	AKB B/W	AKB Def	C.Temp.R					
	0	0	1	0	0	0	0	0
10110	*	FBPBLK.SW	C.TEMP.G					
	(0)	1	1	0	0	0	0	0
10111	AKB Test		C.TEMP.B					
	0	0	1	0	0	0	0	0

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Sub Address	MSB				DATA BITS			LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
00011000	*	C.Ext	C.Bypass	C_Kill ON	C_Kill OFF	*	*	*
	0	0	1	0	0	(0)	(0)	(0)
11001	Cont.Test	Digital OSD	Brt.Abl.Def	Mid.Stp.Def	Emg.Abl.Def	Bright.Abl.Threshold		
	0	0	0	0	0	1	0	0
11010	*	*	*	*	R-Y/B-Y Angle			
	(0)	(0)	(0)	(0)	1	0	0	0
11010	*	*	*	*	*	*	*	*
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11100	Audio SW	Volume						
	0	0	0	0	0	0	0	0
11101	FM.Test	VOL.FIL	RF.AGC					
	0	0	1	0	0	0	0	0
11110	FM.Mute	*	*	VIF.Sys.SW	*	*	*	IF.AGC
	0	(0)	(0)	0	(0)	(0)	(0)	0
11111	VIDEO.LEVEL			FM.LEVEL				
	1	0	0	1	0	0	0	0

Status Register Bit Allocations

	MSB				DATA BITS			LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
2nd Byte	X.Ray	POR	*	RF.AGC	IF.LOCK	V.TRI	*	ST/NONST
	*	*	(0)	*	*	*	(0)	*
3rd Byte	H.Lock	AKB			*	*	*	*
	*	R	G	B	(0)	(0)	(0)	(0)

Control Register Truth Table

Register Name	0 HEX	1 HEX	2 HEX	3 HEX
ON/OFF (T.Disable)	OFF (Tset Enable)	ON (Test Disable)		
AFC gain&gate	Auto (Gain)	Gain: Fast		
	Auto (Gate)	Non-Gate		
H BLK SW	Right Control	Left Control		
Audio.Mute	Active	Mute		
Video.Mute	Active	Mute		
Sync.Kill	Sync active	Sync killed		
Vsepup	normal	Vsepup		
V.KILL	Vrt active	Vrt killed		
Gray Mode	Normal	Gray OSD		
Cross B/W	Normal	Black	White	Cross
Vertical Test	Normal	Vrt S Corr	Vrt Lin	Vrt Size
Count down mode	Auto Mode	non standard		
Drive.Test	Normal	Test Mode		
B Gamma Select	B Gamma on 85% (same as R, G)	B Gamma on 90%	B Gamma on 95%	B Gamma off
R/G Gamma. Def	RG Gamma on	RG Gamma off		
Blank.Def	Blanking	No Blank		
OSD Cnt.Test	Normal	Test Mode		
Blk.Str.Deff	Blk Str On	Blk Str Off		
Coring	Core Off	Core On		
Tint.Test	Normal	Test Mode		
Color.Test	Normal	Test Mode		
Video.SW	Internal Mode	External Mode		
AKB B/W	AKB Black	AKB White		
AKB Def	AKB On	AKB Off		
FBPBLK.SW	FBP not or	FBP or		
AKB Test	Normal	Test Mode1	Test Mode2	Test Mode3
C.Ext	Internal Mode	External Mode		
C.Bypass	Bypass OFF	Bypass ON		
C_Kill ON	Auto Mode	Killer ON		
C_Kill OFF	Auto Mode	Killer OFF		
Cont.Test	Normal	Test Mode		
Digital OSD	Analogue	Digital		
Emg.Abl.Def	Emg On	Emg Off		
Brt.Abl.Def	Brt ABL On	Brt ABL Off		
Mid.Stp.Def	Mid Stp On	Mid Stp Off		
Audio.SW	Internal Mode	External Mode		
FM.Test	Normal	Test Mode		
VOL.FIL	Normal	Filte OFF		
FM.Mute	Active	Mute		
VIF.Sys.SW	45.75MHz	58.75MHz		
IF.AGC	AGC active	AGC defeat		

Filter System

	Y Filter	Chroma Filter
0 HEX	3.58MHz Trap	Peaked 3.58MHz BPF
1 HEX	3.58MHz Trap	Symmetrical 3.58MHz BPF
2 HEX	3.58MHz Trap	Peaked 3.58MHz BPF
3 HEX	3.58MHz Trap	Symmetrical 3.58MHz BPF
4 HEX	No Trap (Wide Band mode)	Peaked 3.58MHz BPF
5 HEX	No Trap (Wide Band mode)	Symmetrical 3.58MHz BPF
6 HEX	No Trap (Wide Band mode)	Peaked 3.58MHz BPF
7 HEX	No Trap (Wide Band mode)	Symmetrical 3.58MHz BPF

Status Byte Truth Table

Register	0 HEX	1 HEX
X.RAY	Undetected	Detected
POR	Undetected	Detected
RF.AGC	RF.AGC.OUT = "L"	RF.AGC.OUT = "H"
IF.LOCK	Lock	Unlock
V.TRI	V.Triger Undetected	V.Triger Detected
ST/NONST	Non-Standard	Standard
H.LOCK	Horiz Unlocked	Horiz Locked
AKB R	R Beam Current Low	R Beam Current High
AKB G	G Beam Current Low	G Beam Current High
AKB B	B Beam Current Low	B Beam Current High

Initial Conditions

Initial Test Conditions	
Register	
ON/OFF (T.Disable)	1 HEX
AFC gain&gate	0 HEX
H.FREQ	3F HEX
H BLK SW	0 HEX
Audio.Mute	0 HEX
Video.Mute	0 HEX
H.PHASE	10 HEX
Sync.Kill	0 HEX
V.SIZE	40 HEX
VSEPUP	0 HEX
V.KILL	0 HEX
V.POSI	20 HEX
Gray Mode	0 HEX
Cross B/W	0 HEX
V.LIN	10 HEX
H BLK R&L	4 HEX
V.SC	00 HEX
V.TEST	0 HEX
V.COMP	7 HEX
COUNT.DOWN.MODE	0 HEX
R.BIAS	00 HEX
G.BIAS	00 HEX
B.BIAS	00 HEX
R.DRIVE	7F HEX
Drive.Test	0 HEX
B Gamma Select	0 HEX
R/G Gamma.Def	1 HEX
G.DRIVE	8 HEX
B.DRIVE	7F HEX
Blank.Def	0 HEX
Sub.Bright	40 HEX
Bright	40 HEX
Contrast	40 HEX

Initial Test Conditions (continued)	
Register	
OSD Cnt.Test	0 HEX
OSD Contrast	0 HEX
Blk.Str.Deff	1 HEX
Coring	1 HEX
Sharpness	00 HEX
Tint.Test	0 HEX
Tint	40 HEX
Color.Test	0 HEX
Color	40 HEX
Video.SW	0 HEX
Trap.Test	4 HEX
Filter.Sys	0 HEX
AKB B/W	0 HEX
AKB Def	0 HEX
C.Temp.R	20 HEX
FBPBLK.SW	1 HEX
C.Temp.G	20 HEX
AKB Test	0 HEX
C.Temp.B	20 HEX
C.Ext	0 HEX
C.Bypass	1 HEX
C_Kill ON	0 HEX
C_Kill OFF	0 HEX
Cont.Test	0 HEX
Digitsl OSD	0 HEX
Bright.Abl.Threshold	4 HEX
Emg.Abl.Def	0 HEX
Brt.Abl.Def	0 HEX
Mid.Stp.Def	0 HEX
R-Y/B-Y Angle	8 HEX
Audio.SW	0 HEX
Volume	00 HEX
FM.Test	0 HEX
VOL.FIL	0 HEX
RF.AGC	20 HEX
FM.Mute	0 HEX
VIF.Sys.SW	0 HEX
IF.AGC	0 HEX
VIDEO.LEVEL	4 HEX
FM.LEVEL	10 HEX

Control Register Descriptions

Register Name	Bits	General Description
ON/OFF (T Disable)	1	Enable the horizontal output & Disable the Test SW & enable Audio/Video Mute SW
AFC Gain & gate	1	Select horizontal first loop gain & H-sync gating on/off
H Freq.	6	Align ES Sample horizontal frequency
H.BLK.SW	1	Blanking Control (Right/Left)
Audio Mute	1	Disable audio outputs
Video Mute	1	Disable video outputs
H PHASE	5	Align sync to flyback phase
Sync Kill	1	Force free-run mode
Vertical Size	7	Align vertical amplitude
Vsep.up	1	Select vertical sync. separation sensitivity
Vertical Kill	1	Disable vertical output
V POSI (Vertical DC)	6	Align vertical DC bias
Gray Mode	1	OSD Gray Tone Enable
Cross B/W	2	Service Test Mode (normal/Black/White/Cross)
V LIN (Vertical Linearit)	5	Align vertical linearity
H BLK R&L	3	H-Blanking Control (Width/Phase)
Vertical S-Correction	5	Align vertical S-correction
Vertical Test	2	Select vertical DAC test modes
Vertical Size Compensation	3	Align vertical size compensation
Count Down Mode	1	Select vertical countdown mode
Red Bias	8	Align Red OUT DC level
Green Bias	8	Align Green OUT DC level
Blue Bias	8	Align Blue OUT DC level
Red Drive	7	Align Red OUT AC level
Drive Test	1	Enable Drive control DAC test modes
B Gamma Select	2	Select Blue Gamma Gain
R/G Gamma Defeat	1	Disable R/G Gamma Correction
Green Drive	4	Align Green OUT AC level
Blue Drive	7	Align Blue OUT AC level
Blank Def	1	Disable RGB output blanking
Sub Brightness	7	Align common RGB DC level
Brightness Control	7	Customer brightness control
Contrast Control	7	Customer contrast control
OSD Contrast Test	1	Enable OSD Contrast DAC test mode
OSD Contrast Control	2	Align OSD AC level
Blk Str Def	1	Disable black stretch
Coring Enable	1	Enable luminance coring
Sharpness Control	6	Customer sharpness control
Tint Test	1	Enable tint DAC test mode
Tint Control	7	Customer tint control
Color Test	1	Enable color DAC test mode
Color Control	7	Customer color control
Video SW	1	Select Video source
Trap.Test	3	Trap Test
Filter System	3	Select Y/C Filter mode
AKB B/W	1	Select AKB Black or White
AKB Def	1	Disable AKB circuits
C Temp R	6	Align AKB color temperature
FBPBLK.SW	1	Enable RGB Blanking or FBP
C Temp G	6	Align AKB color temperature
AKB Test	2	Enable AKB C Temp. DAC test mode
C Temp B	6	Align AKB color temperature

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Register Name	Bits	General Description
AutoFlesh	1	Enable AutoFlesh function
C Ext	1	Selected-C In SW on
C Bypass	1	Select Chroma BPF bypass
C Kill On	1	C Kill Mode (1: Enable Killer circuit)
C Kill Off	1	Disable Killer circuit
Cont Test	1	Enable contrast DAC test mode
Bright ABL Threshold	3	Align brightness ABL threshold
Emergency ABL Defeat	1	Disable emergency brightness ABL
Bright ABL Defeat	1	Disable brightness ABL
Bright Mid Stop Defeat	1	Disable brightness mid stop
Digital OSD	1	Select Digital/Analogue OSD
R-Y/B-Y Angle	4	R-Y/B-Y Angle
Audio SW	1	Select Audio source
Volume Control	7	Customer volume control
FM.Test	1	FM.Test
Volume Filter Defeat	1	Disable volume DAC filter
RF AGC Delay	6	Align RF AGC threshold
FM Mute	1	Disable FM outputs
VIF System SW	1	Select 38.9/39.5/38.0/45.75/58.75
IF AGC Defeat	1	Disable IF and RF AGC
Video Level	3	Align IF video level
FM Level	5	Align WBA output level

Pin Assignment

PIN	FUNCTION	PIN	FUNCTION
1	Audio Output	54	SIF Input
2	FM Output	53	SIF APC Filter
3	PIF AGC	52	SIF Output
4	RF AGC Output	51	Ext. Audio Input
5	PIF Input1	50	FLL Filter
6	PIF Input2	49	VCO Coil 1
7	IF Ground	48	VCO Coil 2
8	IF V_{CC}	47	APC Filter
9	FM Filter	46	Video Output
10	AFT Output	45	Black Level Detector
11	Bus Data	44	Internal Video Input (S-C IN)
12	Bus Clock	43	Video/Vertical V_{CC}
13	ABL	42	External Video Input (Y IN)
14	Red Input	41	Video/Vertical/BUS Ground
15	Green Input	40	Selected Video Output
16	Blue Input	39	ACC Filter
17	Fast Blanking Input	38	3.58MHz Crystal
18	RGB V_{CC}	37	fsc (3.58MHz) Output
19	Red Output	36	Chroma APC Filter
20	Green Output	35	KILLER Filter
21	Blue Output	34	XRAY
22	B.AKB Input	33	Horizontal Ground
23	Vertical Output	32	OSD Contrast
24	Ramp ALC Filter	31	NC
25	Horizontal/BUS V_{CC}	30	NC
26	Horizontal AFC Filter	29	VCO IREF
27	Horizontal Output	28	Flyback Pulse Input