

SANYO

No.2290C

LC7582,7582E,7582W

LCD Driver

Overview

The LC7582,7582E,7582W is a general-purpose LCD driver designed for use in electronic tuning frequency display or microcomputer-controlled system applications.

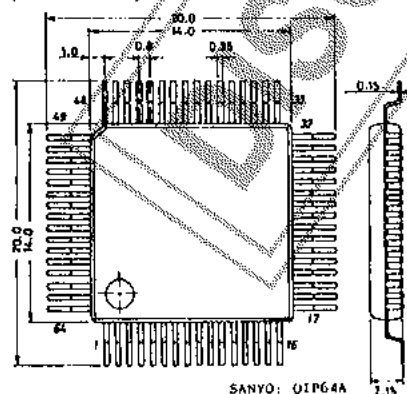
Features

- 53 segments (max.) output (Static display)
- Drive system: 1/1duty (53 segments), 1/2duty (104 segments)
- Data input: 3 serial input pins
- 2 pins for 5-level AD converter (Level meter use, etc.)
- 2 display (DSP) pins for direct display
- INH pin for blanking out display

Absolute Maximum Ratings at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD\max}$	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	V_{LCD}	-0.3 to $V_{DD}+0.3$	V
Input Voltage	$V_{IN(1)}$	CE, CLK, DATA, INH	-0.3 to +7.0	V
	$V_{IN(2)}$	S44 to S47 (Output OFF (Used as AD1, AD2, DSP1, DSP2))	-0.3 to $V_{DD}+0.3$	V
	$V_{IN(3)}$	OSC	-0.3 to $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	OSC	-0.3 to $V_{DD}+0.3$	V
Output Current	$I_{OUT(1)}$	S1 to S53	100	μA
	$I_{OUT(2)}$	COM1,2	1.0	mA
Allowable Power Dissipation	$P_{d\max}$	$T_a=85^{\circ}\text{C}$	100	mW
Operating Temperature	T_{opg}		-30 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-40 to +125	$^{\circ}\text{C}$

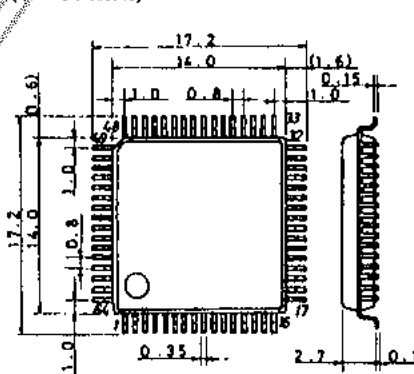
Case Outline 3057 [LC7582]
(unit: mm)



SANYO: QIP64A

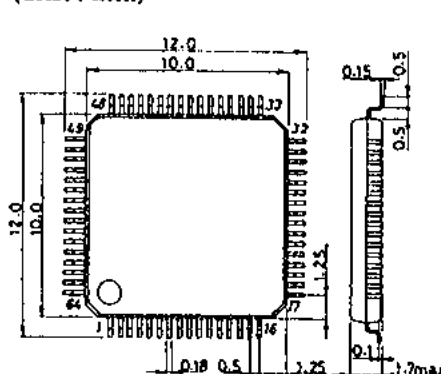
2.15

Case Outline 3159 [LC7582E]
(unit: mm)



SANYO: QIP64E

Case Outline 3190 [LC7582W]
(unit: mm)



SANYO: SQFP64

Specifications and information herein are subject to change without notice.

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Allowable Operating Conditions at Ta=-30 to +85°C, V_{SS}=0V

	Pin	min	typ	max	unit
Supply Voltage	V _{DD}	3.0		6.5	V
	V _{LCD}	3.0		V _{DD}	V
Input "H"-Level Voltage	V _{IH} (1)	0.7V _{DD}		6.5	V
Input "L"-Level Voltage	V _{IL} (1)	0		0.3V _{DD}	V
Input "H"-Level Voltage	V _{IH} (2)	0.7V _{DD}		V _{DD}	V
Input "L"-Level Voltage	V _{IL} (2)	0		0.3V _{DD}	V
Input "H"-Level Voltage	V _{IH} (3)	0.8V _{DD}		6.5	V
Input "L"-Level Voltage	V _{IL} (3)	0		0.2V _{DD}	V
Recommended External Resistance	R		51		kohm
Recommended External Capacitance	C		680		pF
OSC Guaranteed Range	f _{OSC}	25	50	100	kHz
"L"-Level Clock Pulse Width	t _{DL}	0.25			usec
"H"-Level Clock Pulse Width	t _{DH}	0.25			usec
Setup Time	t _{sup}	0.25			usec
Data Hold Time	t _{dh}	0.25			usec
Serial Data Pulse Width	t ₁	1			usec
"	t ₂	1.25			usec
"	t ₃			1	usec
"	t ₄	4			usec

Electrical Characteristics under Allowable Operating Conditions

	Pin	min	typ	max	unit
Input "H"-Level Current	I _{IH} (1)			5	uA
Input "L"-Level Current	I _{IL} (1)			5	uA
Input "H"-Level Current	I _{IH} (2)			10	uA
Input "L"-Level Current	I _{IL} (2)			10	uA
Input "H"-Level Current	I _{IH} (3)			10	uA
Input "L"-Level Current	I _{IL} (3)			10	uA
Output "H"-Level Voltage	V _{OH} (1)	I _O =-10uA	V _{DD} -1.0		V
Output "L"-Level Voltage	V _{OL} (1)	I _O =10uA		1.0	V
Output "H"-Level Voltage	V _{OH} (2)	I _O =-100uA	V _{LCD} -0.6		V
Output "L"-Level Voltage	V _{OL} (2)	I _O =100uA		0.6	V

Continued on next page.

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	Pin	min	typ	max	unit
Center Level Voltage	V_{MID}	$V_{LCD}=6.5V,$ $I_o=100\mu A$	2.65	3.25	3.85 V
"	V_{MID}	$V_{LCD}=3.0V,$ $I_o=100\mu A$	0.9	1.5	2.1 V
1st Step Lighting Voltage	V_{A1}	S45, S47	0.07V _{DD}	0.1V _{DD}	0.13V _{DD} V
2nd	"	V_{A2}	"	"	"
3rd	"	V_{A3}	"	"	"
4th	"	V_{A4}	"	"	"
5th	"	V_{A5}	"	"	"
Step Voltage Diff.	V_{step}	See Fig.1	0.09V _{DD}	0.1V _{DD}	0.11V _{DD} V
OSC Frequency	f_{osc}	osc	R=51kohms, C=680pF	40	50 60 kHz
Supply Current	I_{DD}				1 mA
"	I_{LCD}				2 mA
Hysteresis Voltage	V_H	V_{LCD} CE, CLK, DATA	$V_{DD}=5V$	0.3	V

Pin Assignment

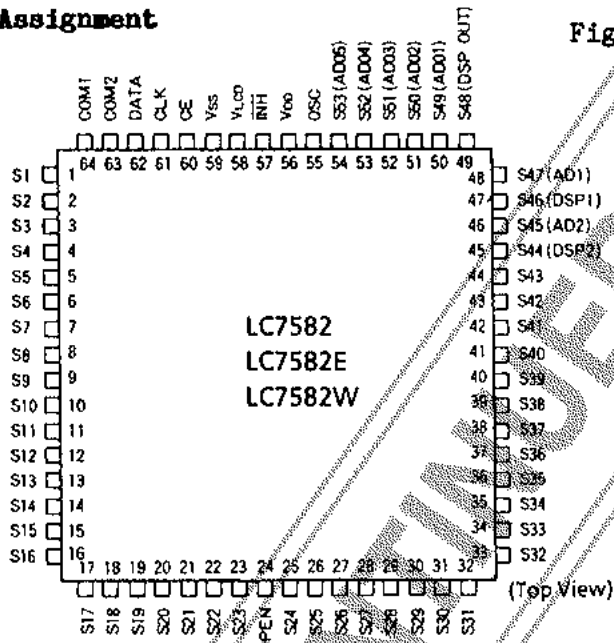
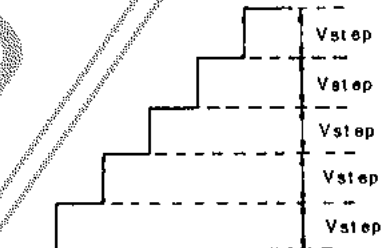
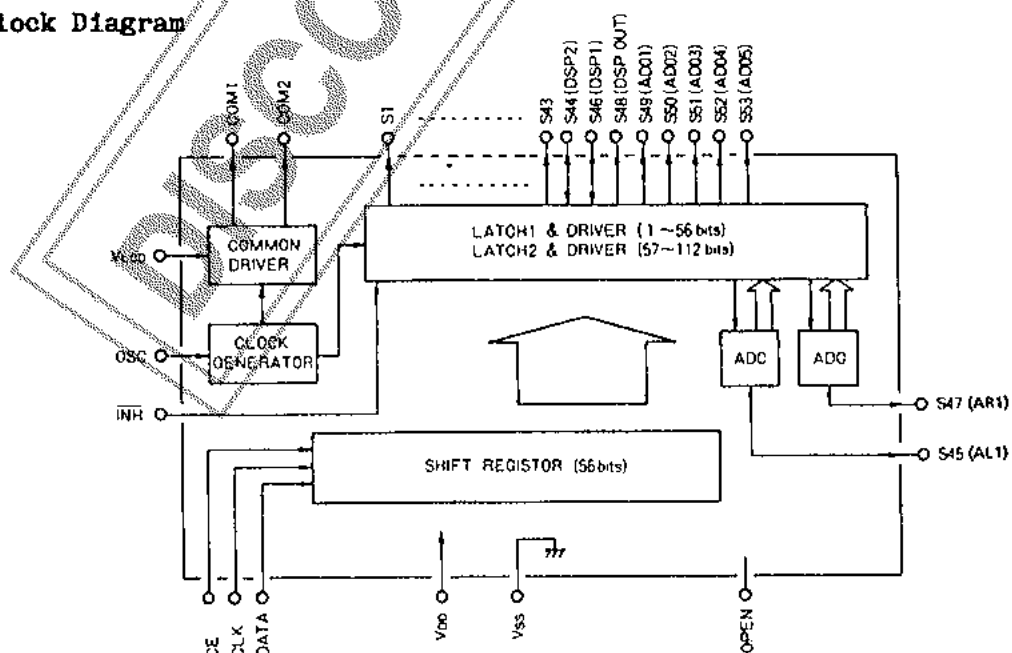


Fig.1 Step Voltage Difference
Input voltage on S45(AD2), S47(AD1)



Block Diagram



Pin Description

- S1 to S43 : Segment output pin
- S46(DSP1), S44(DSP2) : Segment output or DSP input pin
- S47(AD1), S45(AD2) : Segment output or AD input pin
- S48(DSPOUT) : Segment output or DSP output pin
- S49 to S53(AD01to5) : Segment output or AD output pin
- COM1,2 : Common output pin (COM1 only is used for 1/1duty and in this case COM2 is open.)
- V_{LCD} : LCD bias voltage setting pin
- OSC : OSC pin
- CE, CLK, DATA : Input pin for serial data transfer
- V_{SS}, V_{DD} : Power supply pin
- INH : Display blanking input pin (Available for output driver only. Therefore, serial data can be also transferred during unlighting.)
- OPEN : No connection

Data Transfer Mode

- 1/1duty

Transfer direction (56 bits)



- 1/2duty (When the number of display segments does not exceed 52, transfer data is 56 bits long. Transfer mode is the same as for 1/1 duty. Data of D54 to D106 only cannot be changed.)

Transfer direction (112 bits)



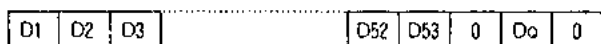
D53, D106: Dummy bit (don't care)

- D₁ to D₅₃ : Display data (1/1duty) Lighted at "1"
- D₁ to D₁₀₆ : Display data (1/2duty) Unlighted at "0"
- (Note) When the AD, DSP functions are selected:
 - 1/1duty : D46 to D53 ----- Dummy bit (don't care)
 - 1/2duty : D88 to D106 ----- Dummy bit (don't care)
- Dp : Drive mode select bit
 - 1/2duty at "1"
 - 1/1duty at "0"
- Dq : AD, DSP function select bit
 - AD, DSP function at "1"
 - Segment output at "0"
- X : Don't care

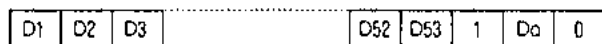
(Note) When the AD, DSP functions selected are not used, fix the AD1, AD2, DSP1, DSP2 pins at V_{DD} or V_{SS} .

Sample Transfers

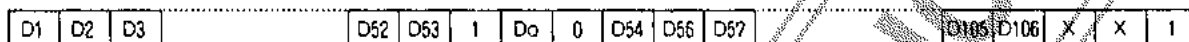
- 1/1 duty



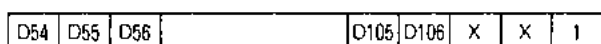
- 1/2 duty and 52 segments or less



- 1/2 duty and 52 segments or more

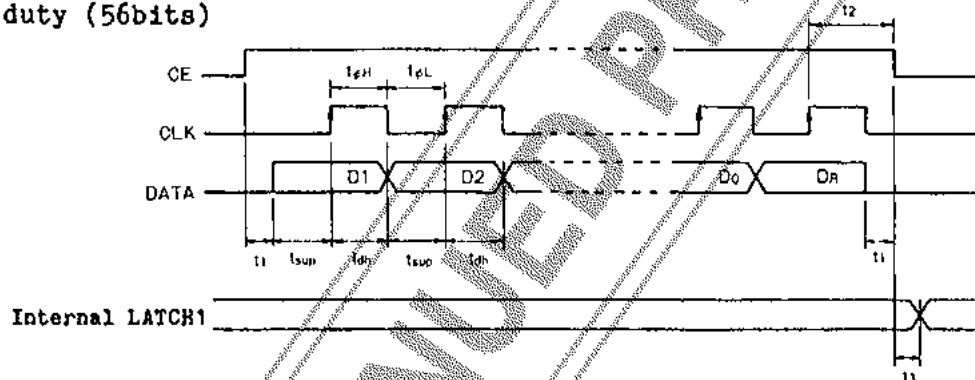


(Note) 1/2 duty and 52 segments or less do not allow transfer shown below.

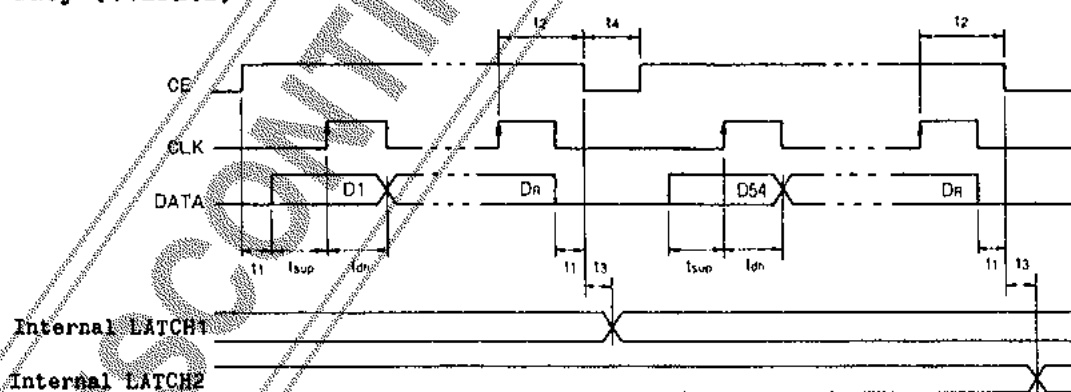


Serial Data

- 1/1 duty (56bits)

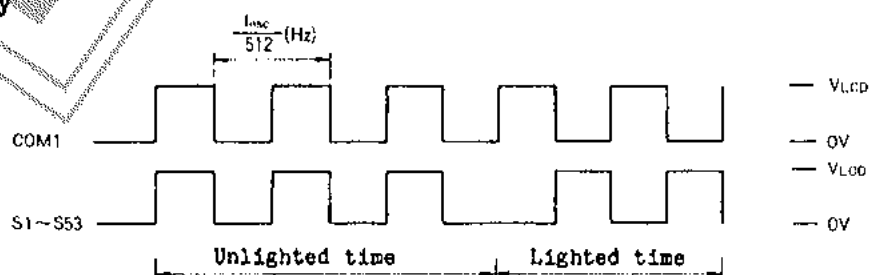


- 1/2 duty (112bits)

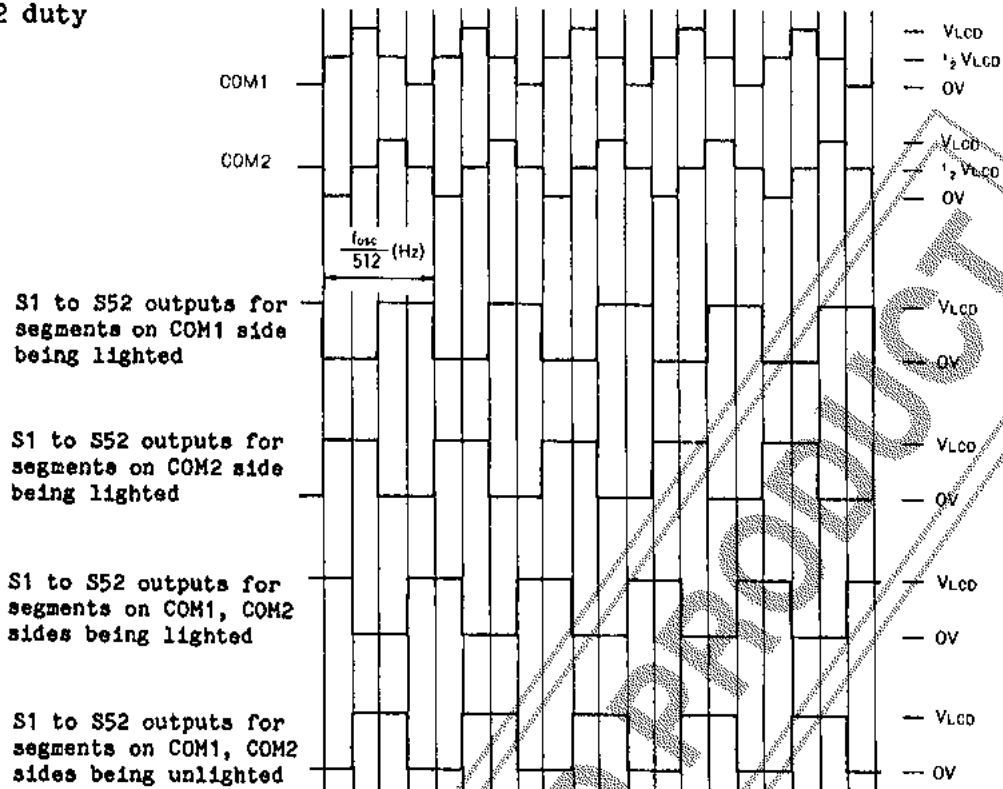


Output Waveforms

- 1/1 duty



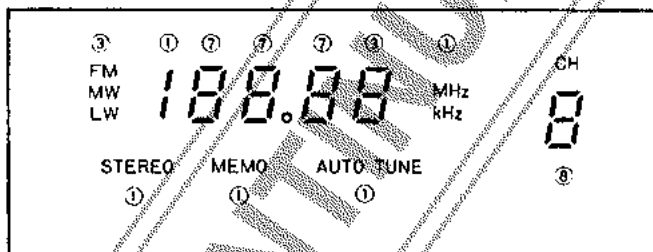
. 1/2 duty



Sample Display

- . Static drive (1/1duty) (AD, DSP pins are not used.)

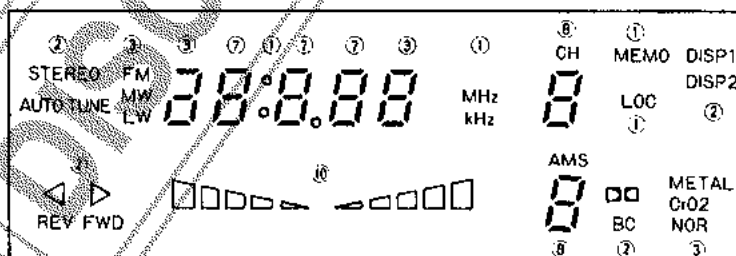
40 segments-used application (Up to 53 segments usable)



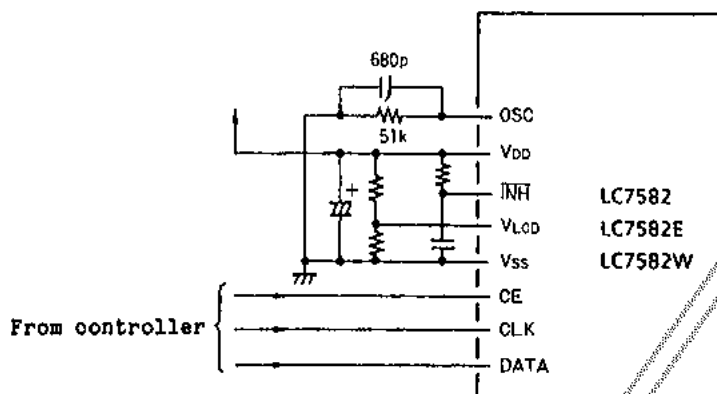
Note: ○ : Number of segments

. 1/2duty drive

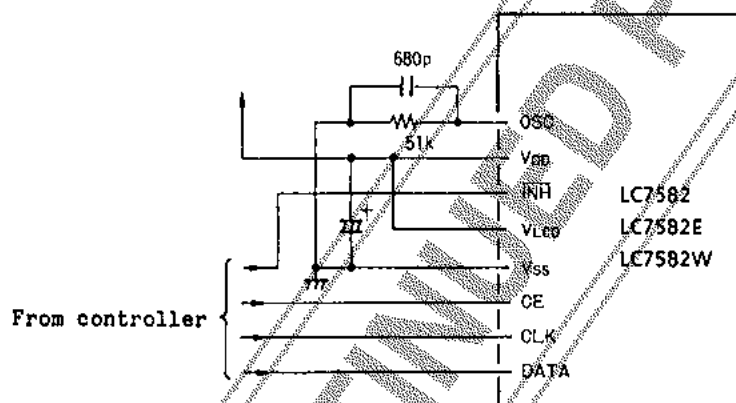
71 segments-used application (Up to 104 segments usable)



Sample Application Circuit 1



Sample Application Circuit 2



Note) The internal display data is indeterminate immediately after V_{DD} rise. If the display is kept lighted as it is, the display will have no meaning. The display is forced to be unlighted when the $\overline{INH}$ is at "L" level. Do not release ("H") until the transfer of display data from the controller is completed.

Correspondence between Transfer (External Input) Data and Output Pin

(Note) COM1 only is used at 1/1 duty.

Output pin	OP	0		1		COM1	COM2
	DQ	0	1	0	1		
	1/1 duty		1/2 duty				
S1	D1	D1	D1	D1	○		
			D2	D2		○	
S2	D2	D2	D3	D3	○		
			D4	D4		○	
S3	D3	D3	D5	D5	○		
			D6	D6		○	
S26	D26	D26	D51	D51	○		
			D52	D52		○	
S27	D27	D27	D54	D54	○		
			D55	D55		○	
S28	D28	D28	D56	D56	○		
			D57	D57		○	
S43	D43	D43	D86	D86	○		
			D87	D87		○	
S44	D44	D44	D88	※DSP 2	○		
			D89			○	
S45	D45	D45	D90	※ALI	○		
			D91			○	
S46	D46	※DSP 1	D92	※DSP 1	○		
			D93			○	
S47	D47	※ARI	D94	※ARI	○		
			D95			○	
S48	D48	※DISPO1	D96	※DSPO1	○		
			D97	※DSPO2		○	
S49	D49	※ARO1	D98	※ARO1	○		
			D99	※ALO1		○	
S50	D50	※ARO2	D100	※ARO2	○		
			D101	※ALO2		○	
S51	D51	※ARO3	D102	※ARO3	○		
			D103	※ALO3		○	
S52	D52	※ARO4	D104	※ARO4	○		
			D105	※ALO4		○	
S53	D53	※ARO5	Always lighting	※ARO5	○		
			Always lighting	※ALO5		○	

Note

- DSP1 : External display input data name. The output is DSP01.
- DSP01 : External display output data name. The input is DSP1.
- DSP2 : External display input data name. The output is DSP02.
- DSP02 : External display output data name. The input is DSP2.
- ARI : AD converter input data name. The output is ARO1 to 5.
- ARO1 to 5 : AD converter output data name. The input is ARI.
- ALI : AD converter input data name. The output is ALO1 to 5.
- ALO1 to 5 : AD converter output data name. The input is ALI.

OSC Frequency

When determining the OSC frequency, see below.

Fig. 1 OSC Frequency at OSC Pin vs. CR

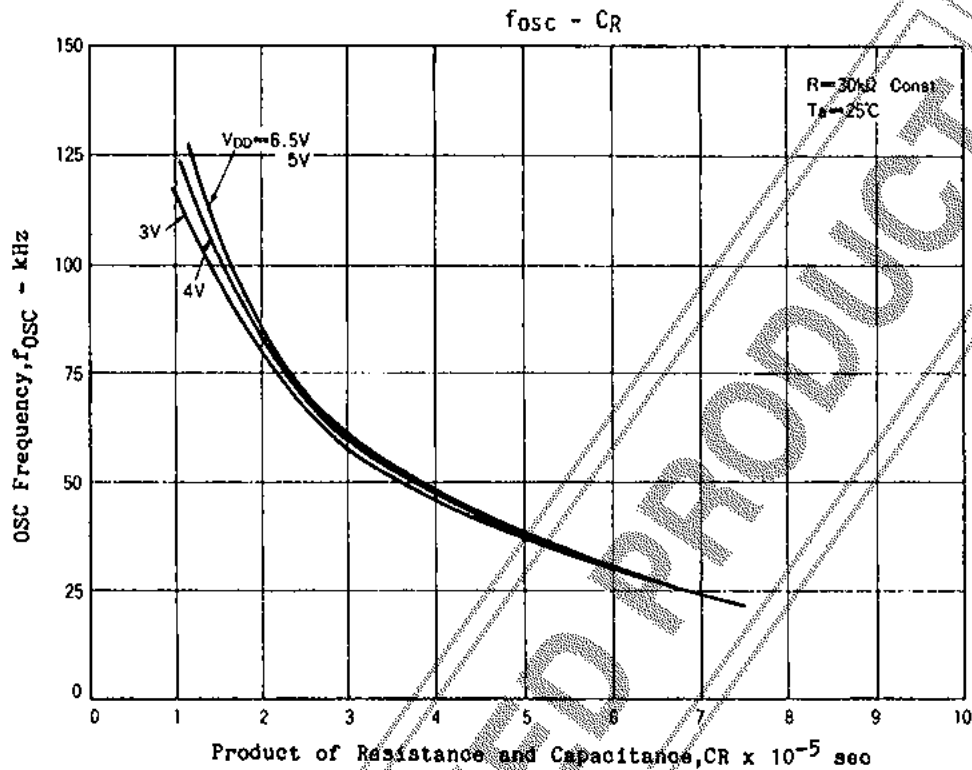
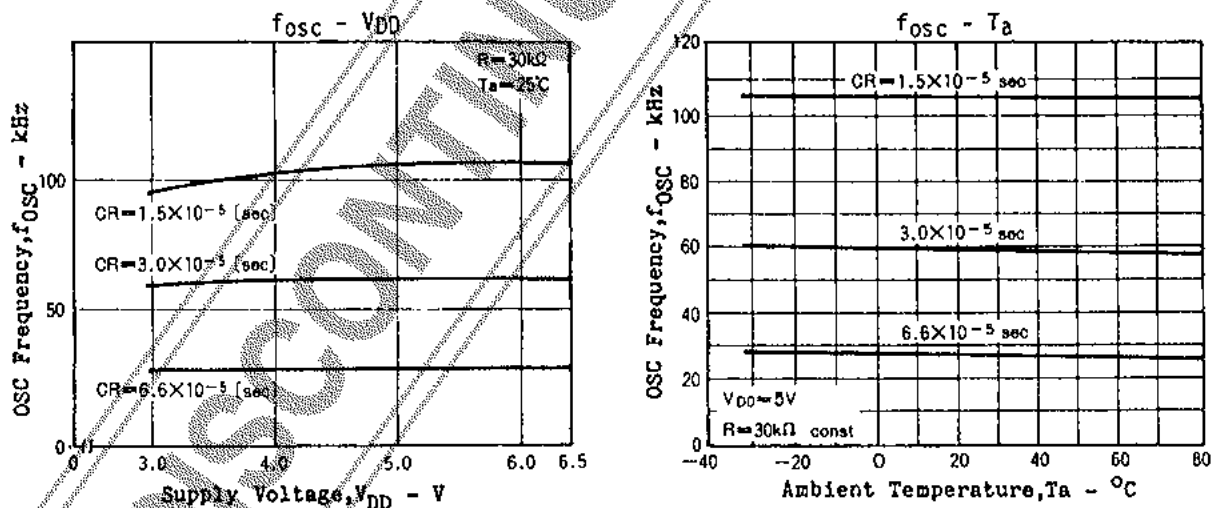


Fig. 2 OSC Frequency at OSC Pin vs. V_{DD}



Recommended external resistor value 10kohms to 100kohms (carbon)

Recommended external capacitor value 330pF to 3300pF

330pF to 820pF (ceramic, temperature coefficient: 0)

1000pF to 3300pF (polyester, temperature coefficient: plus)

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