LPC2141/42/44/46/48

Single-chip 16-bit/32-bit microcontrollers; up to 512 kB flash with ISP/IAP, USB 2.0 full-speed device, 10-bit ADC and DAC

Rev. 5 — 12 August 2011 Product data sheet

1. General description

The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine the microcontroller with embedded high-speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, LPC2141/42/44/46/48 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI, SSP to I^2C-bus and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and medical systems.

2. Features and benefits

2.1 Key features

- 16-bit/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.
- 8 kB to 40 kB of on-chip static RAM and 32 kB to 512 kB of on-chip flash memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip boot loader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software and high-speed tracing of instruction execution.
- USB 2.0 Full-speed compliant device controller with 2 kB of endpoint RAM.

  In addition, the LPC2146/48 provides 8 kB of on-chip RAM accessible to USB by DMA.
- One or two (LPC2141/42 vs. LPC2144/46/48) 10-bit ADCs provide a total of 6/14 analog inputs, with conversion times as low as 2.44 μs per channel.
- Single 10-bit DAC provides variable analog output (LPC2142/44/46/48 only).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-Time Clock (RTC) with independent power and 32 kHz clock input.

- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package.
- Up to 21 external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2141FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2142FBD64			
LPC2144FBD64			
LPC2146FBD64			
LPC2148FBD64			

3.1 Ordering options

Table 2. Ordering options

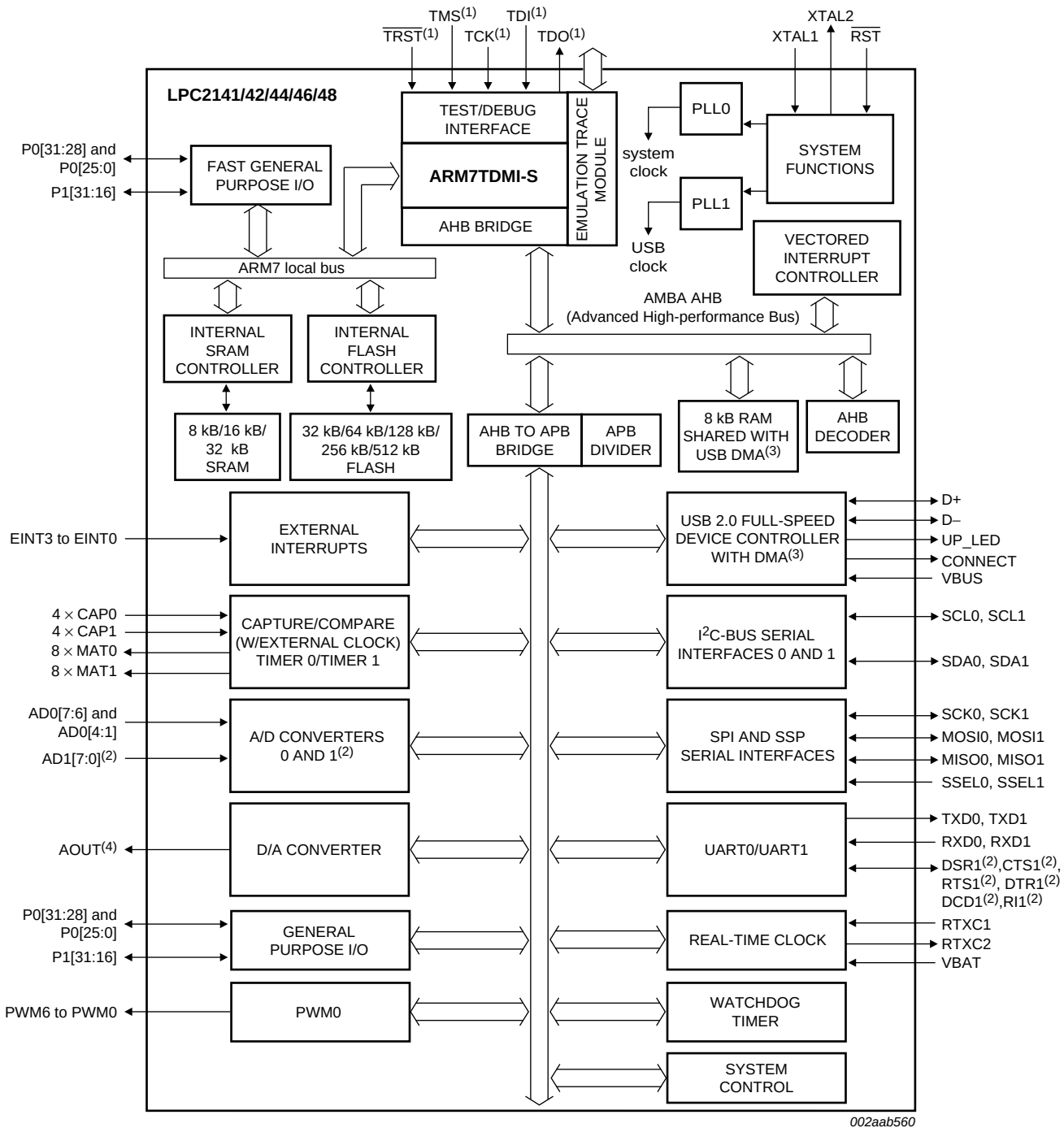
Type number	Flash memory	RAM	Endpoint USB RAM	ADC (channels overall)	DAC	Temperature range
LPC2141FBD64	32 kB	8 kB	2 kB	1 (6 channels)	-	–40 °C to +85 °C
LPC2142FBD64	64 kB	16 kB	2 kB	1 (6 channels)	1	–40 °C to +85 °C
LPC2144FBD64	128 kB	16 kB	2 kB	2 (14 channels)	1	–40 °C to +85 °C
LPC2146FBD64	256 kB	32 kB + 8 kB shared with USB DMA[1]	2 kB	2 (14 channels)	1	–40 °C to +85 °C
LPC2148FBD64	512 kB	32 kB + 8 kB shared with USB DMA[1]	2 kB	2 (14 channels)	1	–40 °C to +85 °C

[1] While the USB DMA is the primary user of the additional 8 kB RAM, this RAM is also accessible at any time by the CPU as a general purpose RAM for data and code storage.

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4. Block diagram



(1) Pins shared with GPIO.

(2) LPC2144/46/48 only.

(3) USB DMA controller with 8 kB of RAM accessible as general purpose RAM and/or DMA is available in LPC2146/48 only.

(4) LPC2142/44/46/48 only.

Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

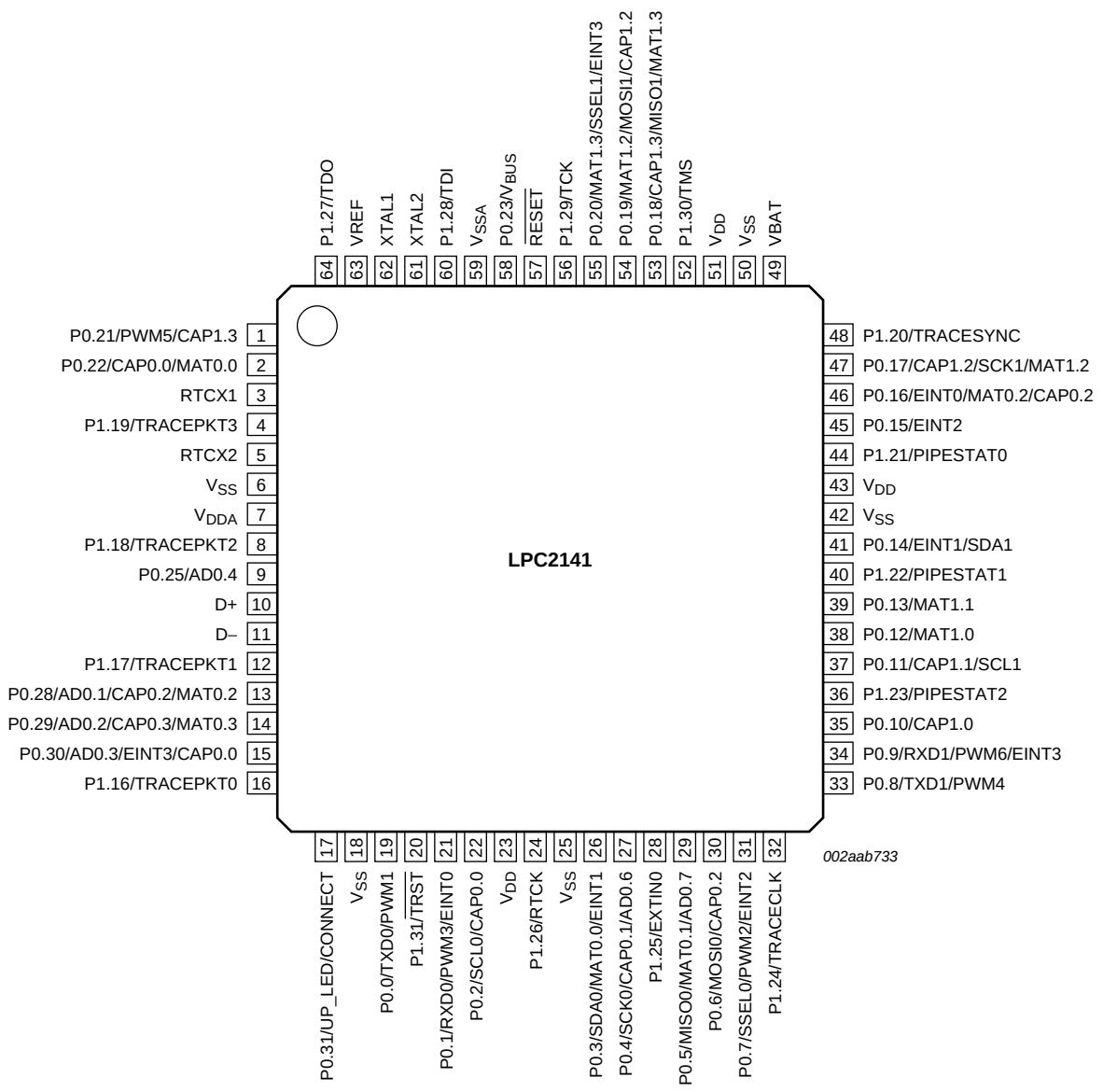


Fig 2. LPC2141 pinning

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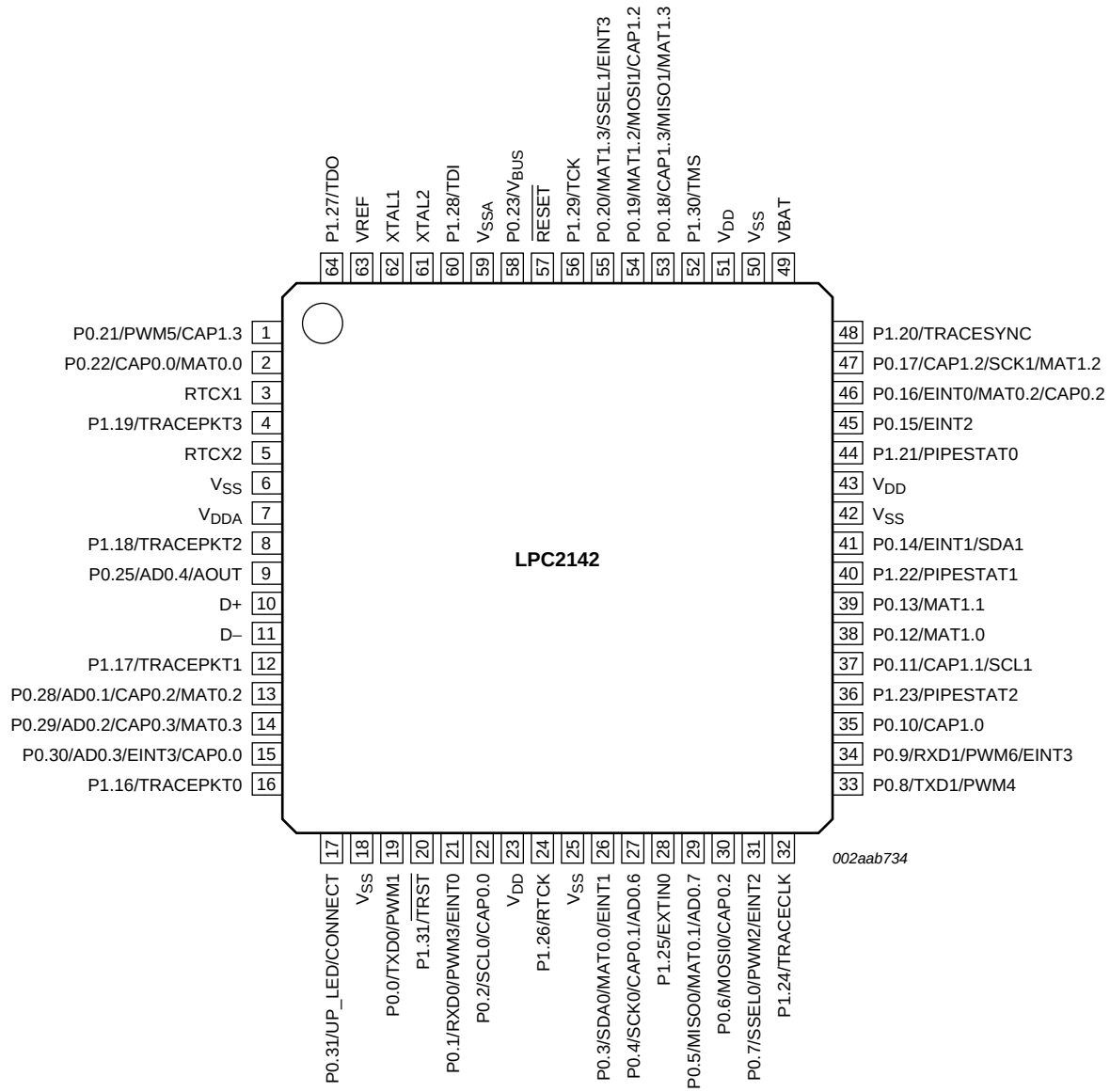


Fig 3. LPC2142 pinning

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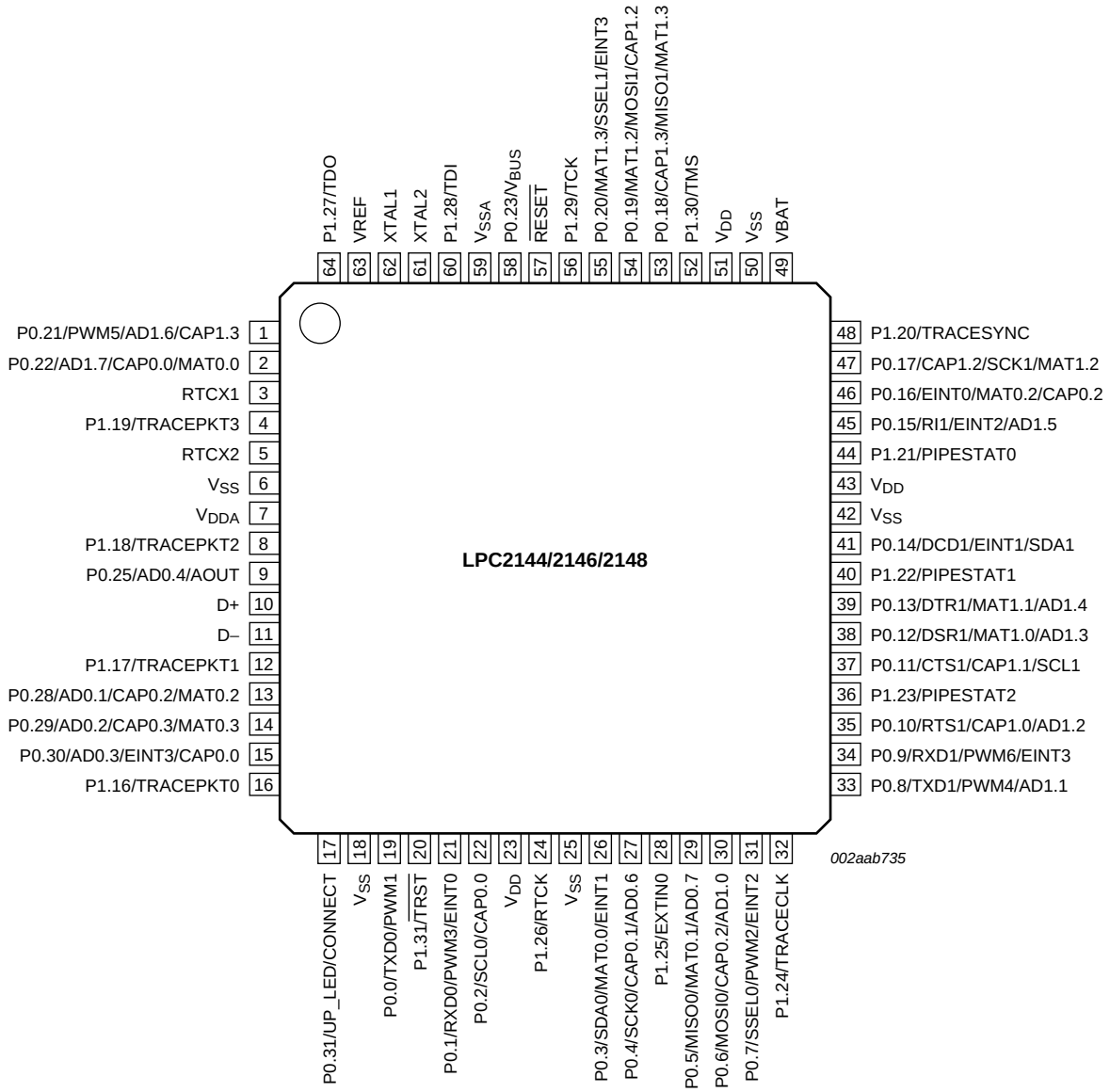


Fig 4. LPC2144/46/48 pinning

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5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins P0.24, P0.26 and P0.27 are not available.
P0.0/TXD0/ PWM1	19[1]	I/O	**P0.0 —** General purpose input/output digital pin (GPIO).
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21[2]	I/O	**P0.1 —** General purpose input/output digital pin (GPIO).
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0.2/SCL0/ CAP0.0	22[3]	I/O	**P0.2 —** General purpose input/output digital pin (GPIO).
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26[3]	I/O	**P0.3 —** General purpose input/output digital pin (GPIO).
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1/AD0.6	27[4]	I/O	**P0.4 —** General purpose input/output digital pin (GPIO).
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		I	**AD0.6 —** ADC 0, input 6.
P0.5/MISO0/ MAT0.1/AD0.7	29[4]	I/O	**P0.5 —** General purpose input/output digital pin (GPIO).
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
		I	**AD0.7 —** ADC 0, input 7.
P0.6/MOSI0/ CAP0.2/AD1.0	30[4]	I/O	**P0.6 —** General purpose input/output digital pin (GPIO).
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		I	**AD1.0 —** ADC 1, input 0. Available in LPC2144/46/48 only.
P0.7/SSEL0/ PWM2/EINT2	31[2]	I/O	**P0.7 —** General purpose input/output digital pin (GPIO).
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.8/TXD1/ PWM4/AD1.1	33[4]	I/O	**P0.8 —** General purpose input/output digital pin (GPIO).
		O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1.1 —** ADC 1, input 1. Available in LPC2144/46/48 only.
P0.9/RXD1/ PWM6/EINT3	34[2]	I/O	**P0.9 —** General purpose input/output digital pin (GPIO).
		I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35[4]	I/O	**P0.10 —** General purpose input/output digital pin (GPIO).
		O	**RTS1 —** Request to Send output for UART1. LPC2144/46/48 only.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD1.2 —** ADC 1, input 2. Available in LPC2144/46/48 only.
P0.11/CTS1/ CAP1.1/SCL1	37[3]	I/O	**P0.11 —** General purpose input/output digital pin (GPIO).
		I	**CTS1 —** Clear to Send input for UART1. Available in LPC2144/46/48 only.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open-drain output (for I^2C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38[4]	I/O	**P0.12 —** General purpose input/output digital pin (GPIO).
		I	**DSR1 —** Data Set Ready input for UART1. Available in LPC2144/46/48 only.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
		I	**AD1.3 —** ADC 1 input 3. Available in LPC2144/46/48 only.
P0.13/DTR1/ MAT1.1/AD1.4	39[4]	I/O	**P0.13 —** General purpose input/output digital pin (GPIO).
		O	**DTR1 —** Data Terminal Ready output for UART1. LPC2144/46/48 only.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
		I	**AD1.4 —** ADC 1 input 4. Available in LPC2144/46/48 only.
P0.14/DCD1/ EINT1/SDA1	41[3]	I/O	**P0.14 —** General purpose input/output digital pin (GPIO).
		I	**DCD1 —** Data Carrier Detect input for UART1. LPC2144/46/48 only.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open-drain output (for I^2C-bus compliance). **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip boot loader to take over control of the part after reset.
P0.15/RI1/ EINT2/AD1.5	45[4]	I/O	**P0.15 —** General purpose input/output digital pin (GPIO).
		I	**RI1 —** Ring Indicator input for UART1. Available in LPC2144/46/48 only.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1.5 —** ADC 1, input 5. Available in LPC2144/46/48 only.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.16/EINT0/ MAT0.2/CAP0.2	46[2]	I/O	**P0.16 —** General purpose input/output digital pin (GPIO).
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47[1]	I/O	**P0.17 —** General purpose input/output digital pin (GPIO).
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53[1]	I/O	**P0.18 —** General purpose input/output digital pin (GPIO).
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54[1]	I/O	**P0.19 —** General purpose input/output digital pin (GPIO).
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55[2]	I/O	**P0.20 —** General purpose input/output digital pin (GPIO).
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1[4]	I/O	**P0.21 —** General purpose input/output digital pin (GPIO).
		O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1.6 —** ADC 1, input 6. Available in LPC2144/46/48 only.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2[4]	I/O	**P0.22 —** General purpose input/output digital pin (GPIO).
		I	**AD1.7 —** ADC 1, input 7. Available in LPC2144/46/48 only.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
P0.23/V_{BUS}	58[1]	I/O	**P0.23 —** General purpose input/output digital pin (GPIO).
		I	**V_{BUS} —** Indicates the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
P0.25/AD0.4/ AOUT	9[5]	I/O	**P0.25 —** General purpose input/output digital pin (GPIO).
		I	**AD0.4 —** ADC 0, input 4.
		O	**AOUT —** DAC output. Available in LPC2142/44/46/48 only.
P0.28/AD0.1/ CAP0.2/MAT0.2	13[4]	I/O	**P0.28 —** General purpose input/output digital pin (GPIO).
		I	**AD0.1 —** ADC 0, input 1.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.29/AD0.2/ CAP0.3/MAT0.3	14[4]	I/O	**P0.29 —** General purpose input/output digital pin (GPIO).
		I	**AD0.2 —** ADC 0, input 2.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15[4]	I/O	**P0.30 —** General purpose input/output digital pin (GPIO).
		I	**AD0.3 —** ADC 0, input 3.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31/UP_LED/ CONNECT	17[6]	O	**P0.31 —** General purpose output only digital pin (GPO).
		O	**UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
		O	**CONNECT —** Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature. **Important:** This is an digital output only pin. This pin MUST NOT be externally pulled LOW when RESET pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16[6]	I/O	**P1.16 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT0 —** Trace Packet, bit 0.
P1.17/ TRACEPKT1	12[6]	I/O	**P1.17 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT1 —** Trace Packet, bit 1.
P1.18/ TRACEPKT2	8[6]	I/O	**P1.18 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P1.19/ TRACEPKT3	4[6]	I/O	**P1.19 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P1.20/ TRACESYNC	48[6]	I/O	**P1.20 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACESYNC —** Trace Synchronization. **Note:** LOW on this pin while RESET is LOW enables pins P1.25:16 to operate as Trace port after reset.
P1.21/ PIPESTAT0	44[6]	I/O	**P1.21 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT0 —** Pipeline Status, bit 0.
P1.22/ PIPESTAT1	40[6]	I/O	**P1.22 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT1 —** Pipeline Status, bit 1.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P1.23/ PIPESTAT2	36[6]	I/O	**P1.23 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT2 —** Pipeline Status, bit 2.
P1.24/ TRACECLK	32[6]	I/O	**P1.24 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACECLK —** Trace Clock.
P1.25/EXTIN0	28[6]	I/O	**P1.25 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		I	**EXTIN0 —** External Trigger Input.
P1.26/RTCK	24[6]	I/O	**P1.26 —** General purpose input/output digital pin (GPIO).
		I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1[31:26] to operate as Debug port after reset.
P1.27/TDO	64[6]	I/O	**P1.27 —** General purpose input/output digital pin (GPIO).
		O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	60[6]	I/O	**P1.28 —** General purpose input/output digital pin (GPIO).
		I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	56[6]	I/O	**P1.29 —** General purpose input/output digital pin (GPIO).
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $^{1}?_{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1.30/TMS	52[6]	I/O	**P1.30 —** General purpose input/output digital pin (GPIO).
		I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{\text{TRST}}$	20[6]	I/O	**P1.31 —** General purpose input/output digital pin (GPIO).
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
D+	10[7]	I/O	USB bidirectional D+ line.
D−	11[7]	I/O	USB bidirectional D− line.
$\overline{\text{RESET}}$	57[8]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62[9]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61[9]	O	Output from the oscillator amplifier.
RTCX1	3[9][10]	I	Input to the RTC oscillator circuit.
RTCX2	5[9][10]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 18, 25, 42, 50	I	**Ground:** 0 V reference.
V_{SSA}	59	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD}	23, 43, 51	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.

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Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
V_{DDA}	7	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is only used to power the on-chip ADC(s) and DAC.
VREF	63	I	**ADC reference voltage:** This should be nominally less than or equal to the V_{DD} voltage but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC.
VBAT	49	I	**RTC power supply voltage:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value typically ranges from 60 kΩ to 300 kΩ.

[7] Pad is designed in accordance with the Universal Serial Bus (USB) specification, revision 2.0 (Full-speed and Low-speed mode only).

[8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[9] Pad provides special analog functionality.

[10] When unused, the RTCX1 pin can be grounded or left floating. For lowest power leave it floating.
The other RTC pin, RTCX2, should be left floating.

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6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt service routines and DSP algorithms) in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30 % over Thumb mode.

6.2 On-chip flash program memory

The LPC2141/42/44/46/48 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip boot loader, flash memory available for user's code on LPC2141/42/44/46/48 is 32 kB, 64 kB, 128 kB, 256 kB and 500 kB respectively.

The LPC2141/42/44/46/48 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data-retention.

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6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2141, LPC2142/44 and LPC2146/48 provide 8 kB, 16 kB and 32 kB of static RAM respectively.

In case of LPC2146/48 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

6.4 Memory map

The LPC2141/42/44/46/48 memory map incorporates several distinct regions, as shown in Figure 5.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.19 “System control”.

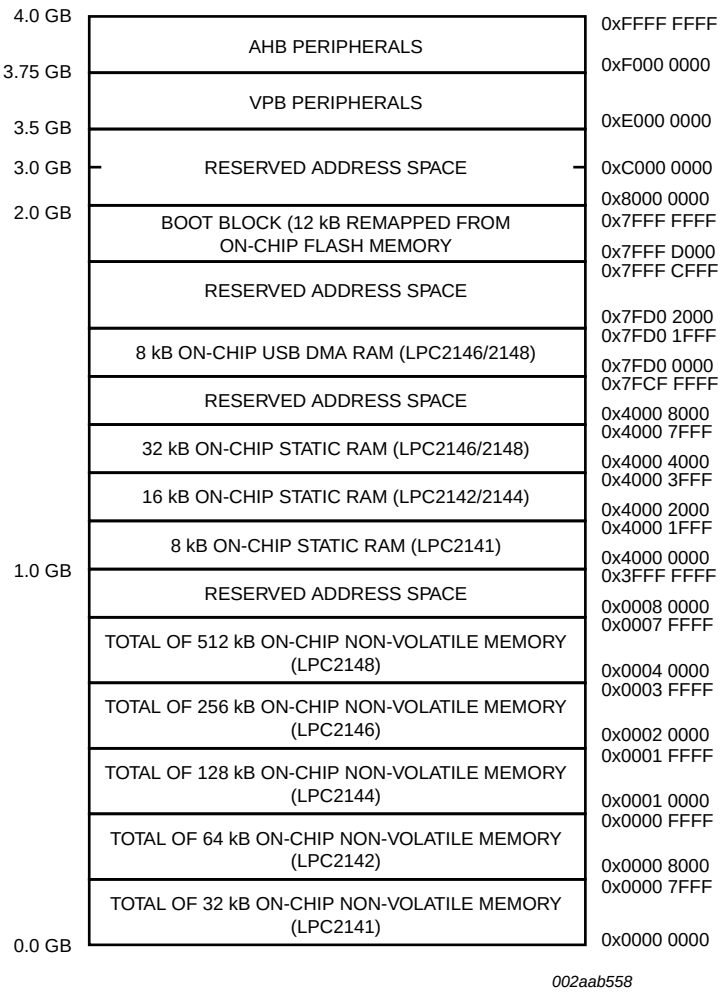


Fig 5. LPC2141/42/44/46/48 memory map

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6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module with its pin select registers defines the functionality of the microcontroller in a given hardware environment.

After reset all pins of Port 0 and Port 1 are configured as input with the following exceptions: If debug is enabled, the JTAG pins will assume their JTAG functionality; if trace is enabled, the Trace pins will assume their trace functionality. The pins associated with the I^2C0 and I^2C1 interface are open drain.

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6.7 Fast general purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2141/42/44/46/48 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2141/42 contain one and the LPC2144/46/48 contain two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. While ADC0 has six channels, ADC1 has eight channels. Therefore, total number of available ADC inputs for LPC2141/42 is 6 and for LPC2144/46/48 is 14.

6.8.1 Features

- 10 bit successive approximation analog to digital converter.
- Measurement range of 0 V to VREF (2.5 V $\leq$ VREF $\leq$ V_{DDA}).
- Each converter capable of performing more than 400000 10-bit samples per second.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters (LPC2142/44/46/48 only).

6.9 10-bit DAC

The DAC enables the LPC2141/42/44/46/48 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

6.9.1 Features

- 10-bit DAC.
- Buffered output.
- Power-down mode available.

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- Selectable speed versus power.

6.10 USB 2.0 device controller

The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC2141/42/44/46/48 is equipped with a USB device controller that enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

A DMA controller (available in LPC2146/48 only) can transfer data between an endpoint buffer and the USB RAM.

6.10.1 Features

- Fully compliant with USB 2.0 Full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports SoftConnect and GoodLink LED indicator. These two functions are sharing one pin.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints (LPC2146/48 only).
- One duplex DMA channel serves all endpoints (LPC2146/48 only).
- Allows dynamic switching between CPU controlled and DMA modes (only in LPC2146/48).
- Double buffer implementation for bulk and isochronous endpoints.

6.11 UARTs

The LPC2141/42/44/46/48 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2144/46/48 UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2141/42/44/46/48 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware (UART1 in LPC2144/46/48 only).

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6.11.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- LPC2144/46/48 UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.12 I^2C-bus serial I/O controller

The LPC2141/42/44/46/48 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2141/42/44/46/48 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

6.12.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2141/42/44/46/48 each contain one SPI controller. The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

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6.13.1 Features

- Compliant with SPI specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.14 SSP serial I/O controller

The LPC2141/42/44/46/48 each contain one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

6.14.1 Features

- Compatible with Motorola's SPI, TI's 4-wire SSI and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.15 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2141/42/44/46/48 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

6.15.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.

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- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable reference clock divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

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6.18 Pulse width modulator

The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2141/42/44/46/48. The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

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- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.19 System control

6.19.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2141/42/44/46/48: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

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The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.19.4 Brownout detector

The LPC2141/42/44/46/48 include 2-stage monitoring of the voltage on the V_{DD} pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the VIC. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low voltage detection asserts reset to inactivate the LPC2141/42/44/46/48 when the voltage on the V_{DD} pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

6.19.5 Code security

This feature of the LPC2141/42/44/46/48 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip boot loader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

6.19.6 External interrupt inputs

The LPC2141/42/44/46/48 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake-up the processor from Power-down mode.

Additionally capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

6.19.7 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

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6.19.8 Power control

The LPC2141/42/44/46/48 supports two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during active and Idle mode.

6.19.9 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $^{1}?_{2}$ to $^{1}?_{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $^{1}?_{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.20 Emulation and debugging

The LPC2141/42/44/46/48 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.20.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

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The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

This clock must be slower than $^{1}?_{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.20.2 Embedded trace

Since the LPC2141/42/44/46/48 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.20.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2141/42/44/46/48 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			–0.5	+3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	–0.5	+6.0	V
		other I/O pins	[2][3]	–0.5	V_{DD} + 0.5	V
I_{DD}	supply current	per supply pin	[4]	-	100	mA
I_{SS}	ground current	per ground pin	[4]	-	100	mA
I_{sink}	sink current	for I^2C-bus; DC; T = 85 °C		-	20	mA
T_{stg}	storage temperature		[5]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[6]			
		all pins		–4000	+4000	V

[1] The following applies to the Limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] Dependent on package type.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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8. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage		[2]	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.3 V pad		3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[3]	2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			2.5	3.3	V_{DDA}	V
Standard port pins, $\overline{RESET}$, P1.26/RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[4][5][6][7]	0	-	5.5	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[8]	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[8]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V	[8]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[8]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[10]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[11]	−15	−50	−85	µA
		$V_{DD} < V_I$ < 5 V	[10]	0	0	0	µA

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Table 5. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(act)}$	active mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash, no active peripherals		-	15	50	
		CCLK = 10 MHz					mA
		CCLK = 60 MHz		-	40	70	mA
		V_{DD} = 3.3 V; T_{amb} = 25 °C; code executed from flash; USB enabled and active; all other peripherals disabled		-	27	70	
		CCLK = 12 MHz					mA
		CCLK = 60 MHz		-	57	90	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C		-	40	100	µA
		V_{DD} = 3.3 V; T_{amb} = 85 °C		-	250	500	µA
I_{BATpd}	Power-down mode battery supply current	RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C	[12]	-	15	30	
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 2.5 V					µA
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	20	40	µA
I_{BATact}	active mode battery supply current	CCLK = 60 MHz; PCLK = 15 MHz; PCLK enabled to RTCK; RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C	[12]	-	78	-	
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V					µA
$I_{BATact(opt)}$	optimized active mode battery supply current	PCLK disabled to RTCK in the PCONP register; RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C; $V_{i(VBAT)}$ = 3.3 V	[12][13]	-	23	-	
		CCLK = 25 MHz					µA
		CCLK = 60 MHz		-	30	-	µA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[8]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD}$	[14]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V

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Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	1.8	1.95	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	1.8	1.95	V
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V		-	-	±10	µA
V_{BUS}	V_{BUS} line input voltage on the USB connector			-	-	5.25	V
V_{DI}	differential input sensitivity	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common-mode range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW output level	R_L of 1.5 kΩ to 3.6 V		-	-	0.3	V
V_{OH}	HIGH output level	R_L of 15 kΩ to GND		2.8	-	3.6	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	steady state drive	[15]	29	-	44	Ω
R_{pu}	pull-up resistance	SoftConnect = ON		1.1	-	1.9	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and external rail.

[3] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD} supply voltages must be present.

[6] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[7] Please also see the errata note mentioned in errata sheet.

[8] Accounts for 100 mV voltage drop in all supply lines.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[10] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[11] Applies to P1.16 to P1.31.

[12] On pin VBAT.

[13] Optimized for low battery consumption.

[14] To V_{SS}.

[15] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

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9. Dynamic characteristics

Table 6. Dynamic characteristics of USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	(t_r/t_f)	90	-	110	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 7	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 7	−2	-	+5	ns
t_{JR1}	receiver jitter to next transition		−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 7 [1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 7 [1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2, P0.3, P0.11, and P0.14)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2, P0.3, P0.11, and P0.14)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$ [3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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9.1 Timing

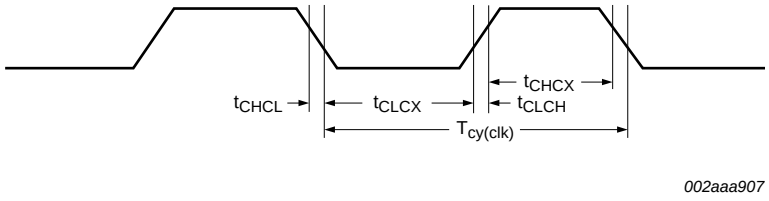


Fig 6. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

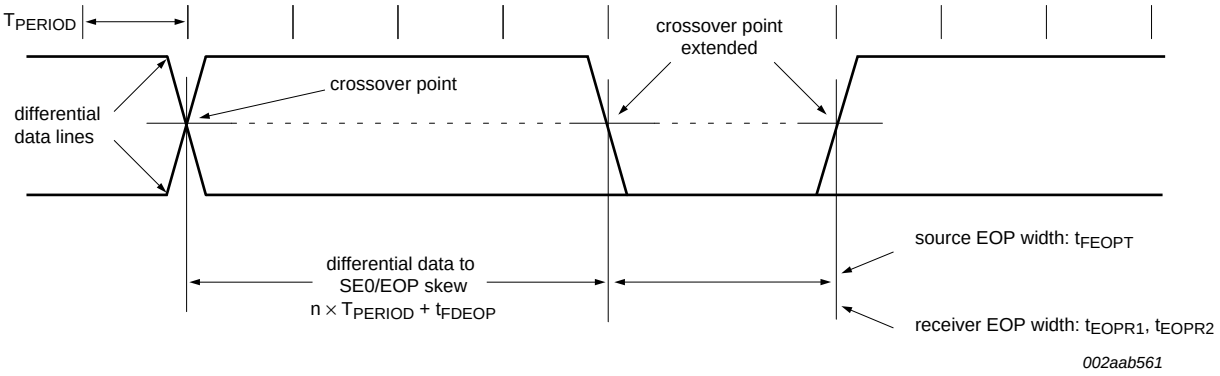


Fig 7. Differential data-to-EOP transition skew and EOP width

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10. ADC electrical characteristics

Table 8. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[3]	-	-	±2	LSB
E_O	offset error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[4]	-	-	±3	LSB
E_G	gain error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[5]	-	-	±0.5	%
E_T	absolute error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[7]	-	-	40	kΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

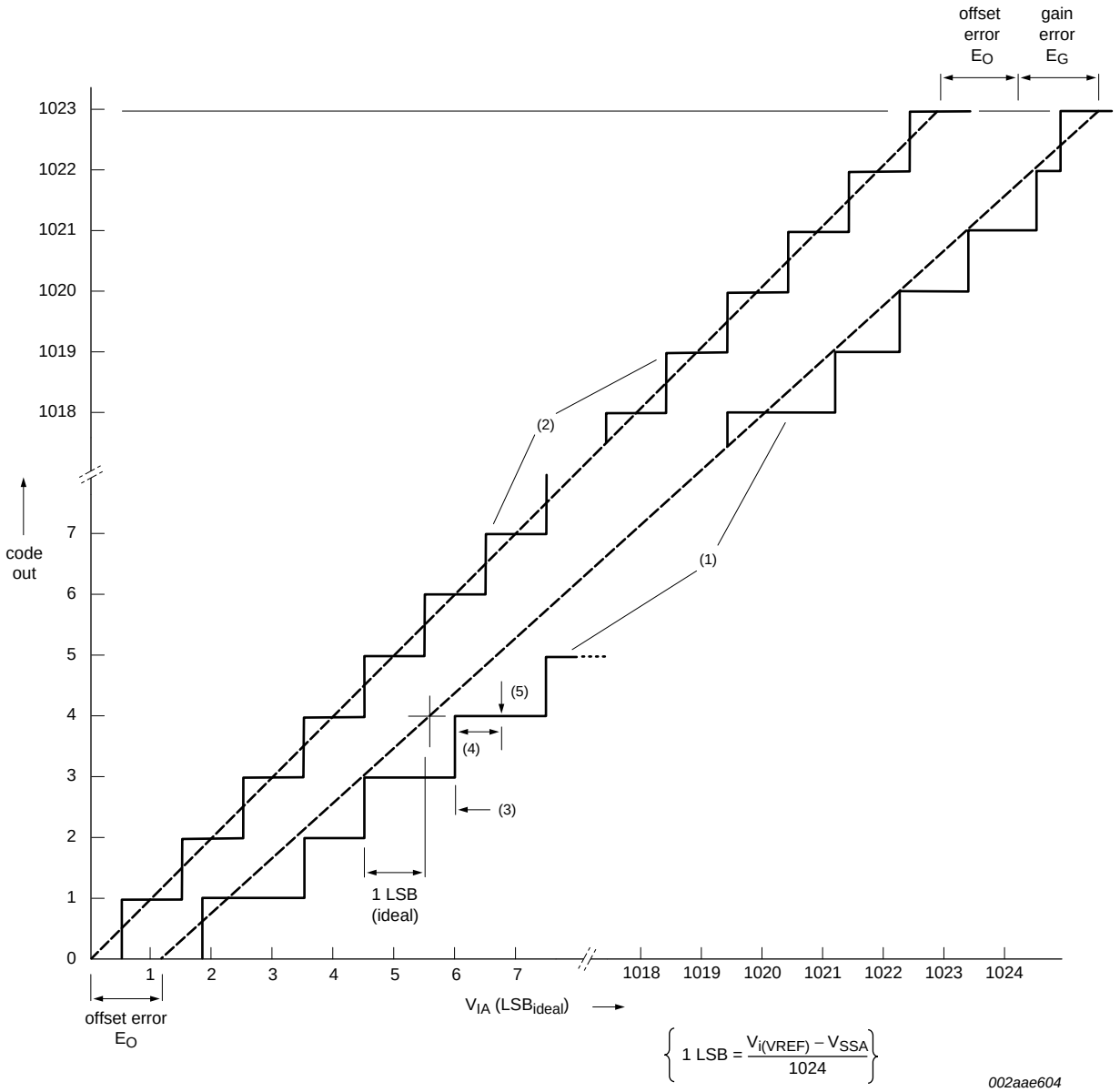
[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7] See Figure 9.

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(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

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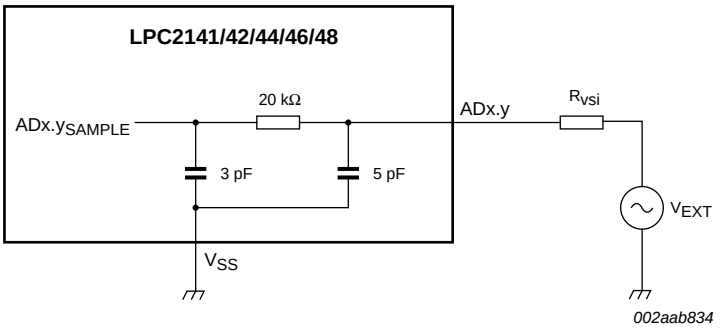


Fig 9. Suggested ADC interface - LPC2141/42/44/46/48 ADx.y pin

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11. DAC electrical characteristics

Table 9. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

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12. Application information

12.1 Suggested USB interface solutions

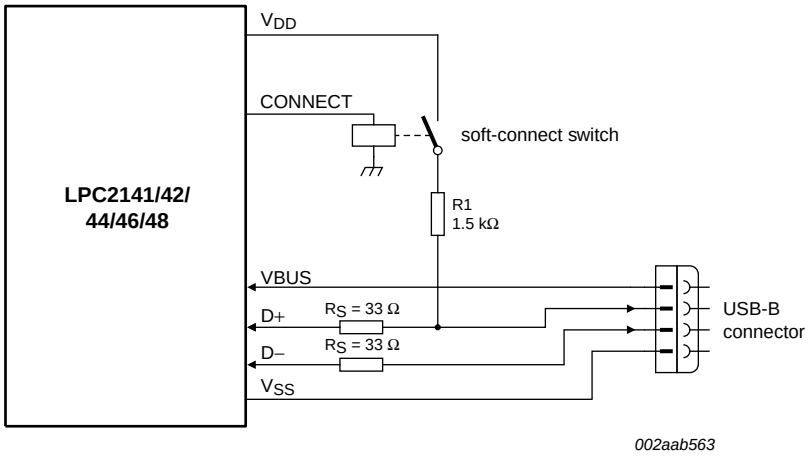


Fig 10. LPC2141/42/44/46/48 USB interface using the CONNECT function on pin 17

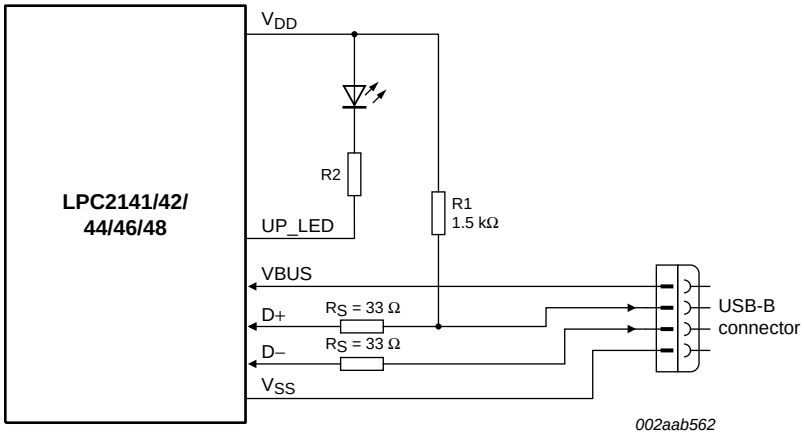


Fig 11. LPC2141/42/44/46/48 USB interface using the UP_LED function on pin 17

12.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor C_i / (C_i + C_g). In slave mode, a minimum of 200 mV (RMS) is needed.

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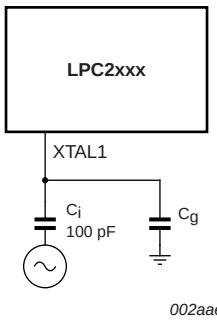


Fig 12. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 12), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTAL2 pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 13 and in Table 10 and Table 11. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 13 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

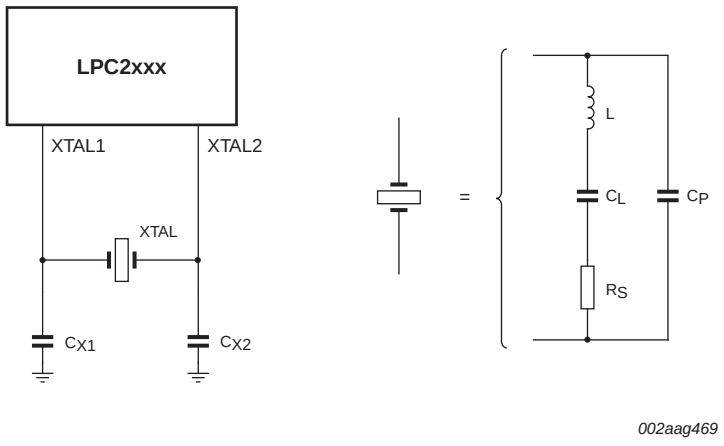


Fig 13. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 10. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF

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Table 10. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 11. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

12.3 RTC 32 kHz oscillator component selection

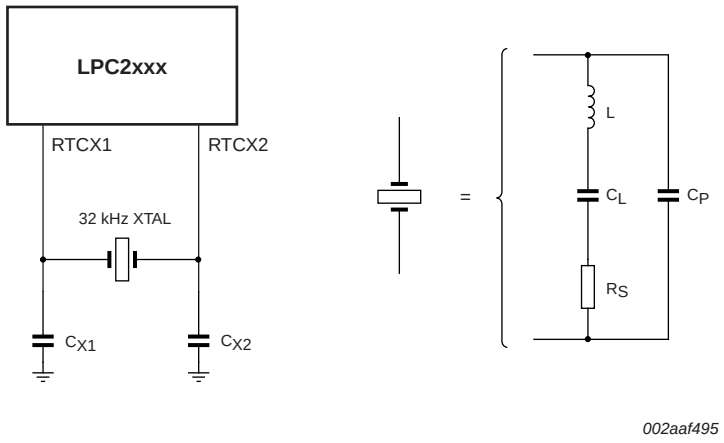


Fig 14. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 14. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 12 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 12

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that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 12. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

12.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

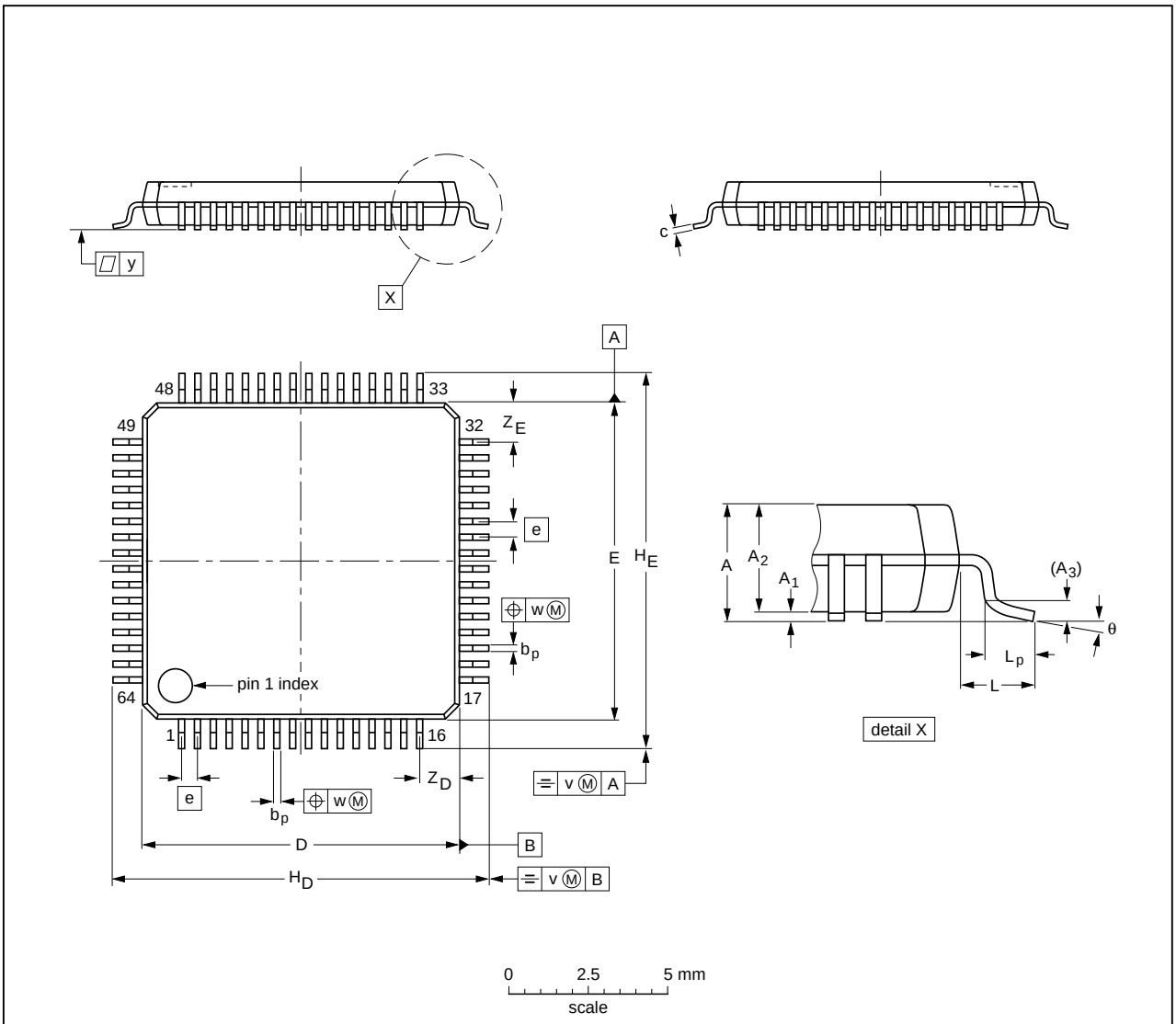
The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

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13. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 15. Package outline SOT314-2 (LQFP64)

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14. Abbreviations

Table 13. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
BOD	Brown-Out Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
DMA	Direct Memory Access
EOP	End Of Packet
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2141_42_44_46_48 v.5	20110812	Product data sheet	-	LPC2141_42_44_46_48 v.4
Modifications:	• Table 3 “Pin description”: Added Table note [10] to RTCX1 and RTCX2 pins. • Table 4 “Limiting values”: Added parameter I_{sink}. • Table 5 “Static characteristics”, I^2C-bus pins: Changed typical hysteresis voltage from $0.5V_{DD}$ to $0.05V_{DD}$. • Table 5 “Static characteristics”: Updated min, typical and max values for oscillator pins $V_{i(XTAL1)}$, $V_{o(XTAL2)}$, $V_{i(RTCX1)}$, and $V_{o(RTCX2)}$. • Table 5 “Static characteristics”: Updated Table note [15]. • Added Section 11 “DAC electrical characteristics”. • Added Section 12.2 “Crystal oscillator XTAL input and component selection”. • Added Section 12.3 “RTC 32 kHz oscillator component selection”. • Added Section 12.4 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Updated Figure 8 “ADC characteristics”.			
LPC2141_42_44_46_48 v.4	20081117	Product data sheet	-	LPC2141_42_44_46_48 v.3
Modifications:	• Replaced all occurrences of VPB with APB. • Table 3: clarified which pins do/don’t have internal pull-ups. • Table 4: changed storage temperature range from −40 °C/125 °C to −65 °C/150 °C. • Table 5: added Table note 7 to input voltage spec. • Table 5: modified Table note 9. • Table 5: moved hysteresis voltage (0.4 V) from typ to min column. • Figure 8: updated figure and figure title, removed note			
LPC2141_42_44_46_48 v.3	20071019	Product data sheet	-	LPC2141_42_44_46_48 v.2
LPC2141_42_44_46_48 v.2	20060828	Product data sheet	-	LPC2141_42_44_46_48 v.1
LPC2141_42_44_46_48 v.1	20051003	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

1 General description 1
2 Features and benefits 1
2.1 Key features 1
3 Ordering information 2
3.1 Ordering options 2
4 Block diagram 3
5 Pinning information 4
5.1 Pinning 4
5.2 Pin description 7
6 Functional description 13
6.1 Architectural overview 13
6.2 On-chip flash program memory 13
6.3 On-chip static RAM 14
6.4 Memory map 14
6.5 Interrupt controller 15
6.5.1 Interrupt sources 15
6.6 Pin connect block 15
6.7 Fast general purpose parallel I/O (GPIO) 16
6.7.1 Features 16
6.8 10-bit ADC 16
6.8.1 Features 16
6.9 10-bit DAC 16
6.9.1 Features 16
6.10 USB 2.0 device controller 17
6.10.1 Features 17
6.11 UARTs 17
6.11.1 Features 18
6.12 I^2C-bus serial I/O controller 18
6.12.1 Features 18
6.13 SPI serial I/O controller 18
6.13.1 Features 19
6.14 SSP serial I/O controller 19
6.14.1 Features 19
6.15 General purpose timers/external event counters 19
6.15.1 Features 19
6.16 Watchdog timer 20
6.16.1 Features 20
6.17 Real-time clock 20
6.17.1 Features 20
6.18 Pulse width modulator 21
6.18.1 Features 21
6.19 System control 22
6.19.1 Crystal oscillator 22
6.19.2 PLL 22
6.19.3 Reset and wake-up timer 22
6.19.4 Brownout detector 23
6.19.5 Code security 23
6.19.6 External interrupt inputs 23
6.19.7 Memory mapping control 23
6.19.8 Power control 24
6.19.9 APB bus 24
6.20 Emulation and debugging 24
6.20.1 EmbeddedICE 24
6.20.2 Embedded trace 25
6.20.3 RealMonitor 25
7 Limiting values 26
8 Static characteristics 27
9 Dynamic characteristics 30
9.1 Timing 31
10 ADC electrical characteristics 32
11 DAC electrical characteristics 35
12 Application information 36
12.1 Suggested USB interface solutions 36
12.2 Crystal oscillator XTAL input and component selection 36
12.3 RTC 32 kHz oscillator component selection . 38
12.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines 39
13 Package outline 40
14 Abbreviations 41
15 Revision history 42
16 Legal information 43
16.1 Data sheet status 43
16.2 Definitions 43
16.3 Disclaimers 43
16.4 Trademarks 44
17 Contact information 44
18 Contents 45

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