3886 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3886 group is the 8-bit microcomputer based on the 740 family core technology.

The 3886 group is designed for controlling systems that require analog signal processing and include two serial I/O functions, A-D converters, D-A converters, system data bus interface function, watchdog timer, and comparator circuit.

The multi-master I^2C bus interface can be added by option.

FEATURES

<Microcomputer mode>

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.4 µs
  (at 10 MHz oscillation frequency)
- Memory size
  ROM ..... 32K to 60K bytes
  RAM ..... 1024 to 2048 bytes
- Programmable input/output ports 72
- Software pull-up resistors ..... Built-in
- Interrupts ..... 21 sources, 16 vectors
  (Included key input interrupt)
- Timers ..... 8-bit × 4
- Serial I/O1 ..... 8-bit × 1(UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit × 1(Clock-synchronized)
- PWM output circuit ..... 14-bit × 2
- Bus interface ..... 2 bytes
- I^2C bus interface (option) ..... 1 channel
- A-D converter ..... 10-bit × 8 channels
- D-A converter ..... 8-bit × 2 channels
- Comparator circuit ..... 8 channels
- Watchdog timer ..... 16-bit × 1
- Clock generating circuit ..... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode ..... 4.0 to 5.5 V
  (at 10 MHz oscillation frequency)
  In middle-speed mode ..... 2.7 to 5.5 V(*)
  (at 10 MHz oscillation frequency)
  In low-speed mode ..... 2.7 to 5.5 V (*)
  (at 32 kHz oscillation frequency)
  (*: 4.0 to 5.5 V for Flash memory version)
- Power dissipation
  In high-speed mode ..... 40 mW
  (at 10 MHz oscillation frequency, at 5 V power source voltage)
  In low-speed mode ..... 60 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Memory expansion possible (only for M38867M8A/E8A)
- Operating temperature range ..... –20 to 85°C

<Flash memory mode>

- Supply voltage ..... V_{CC} = 5 V ± 10 %
- Program/Erase voltage ..... V_{PP} = 11.7 to 12.6 V
- Programming method ..... Programming in unit of byte
- Erasing method
  Batch erasing ..... Parallel/Serial I/O mode
  Block erasing ..... CPU reprogramming mode
- Program/Erase control by software command
- Number of times for programming/erasing 100
- Operating temperature range (at programming/erasing)
  ..... Normal temperature

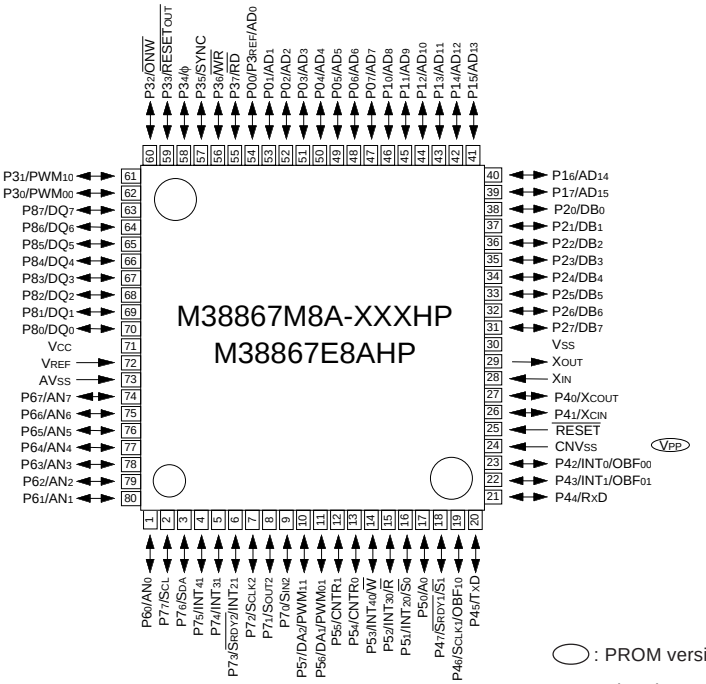
■Notes

1. The flash memory version cannot be used for application embedded in the MCU card.
2. Power source voltage Vcc of the flash memory version is 4.0 to 5.5 V.

APPLICATION

Household product, consumer electronics, communications, note book PC, etc.

PIN CONFIGURATION (TOP VIEW)

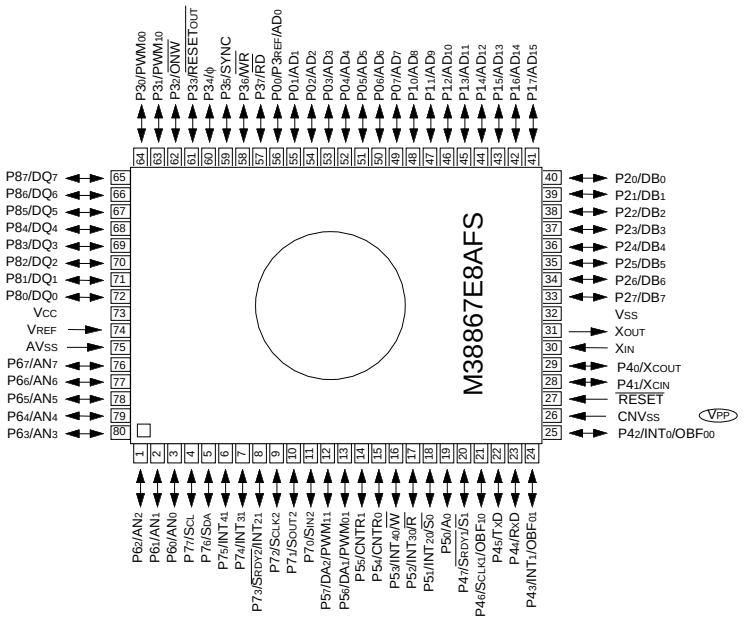


Note: The pin number and the position of the function pin may change by the kind of package.

Package type : 80P6Q-A

Fig. 1 M38867M8A-XXXHP, M38867E8AHP pin configuration

PIN CONFIGURATION (TOP VIEW)

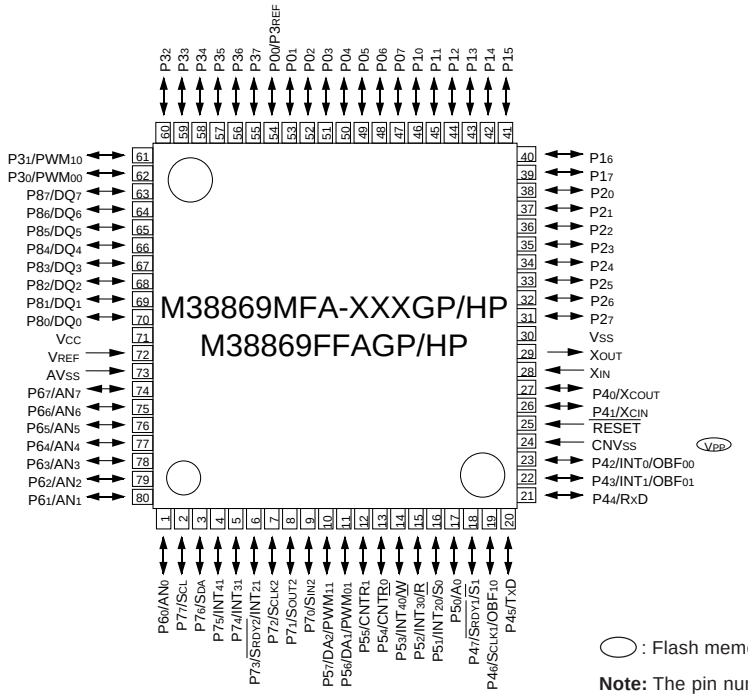


Note: The pin number and the position of the function pin may change by the kind of package.

Package type : 80D0

Fig. 2 M38867E8AFS pin configuration

PIN CONFIGURATION (TOP VIEW)



: Flash memory version

Note: The pin number and the position of the function pin may change by the kind of package.

Package type : 80P6S-A/80P6Q-A

Fig. 3 M38869MFA-XXXGP/HP, M38869FFAGP/HP pin configuration

FUNCTIONAL BLOCK

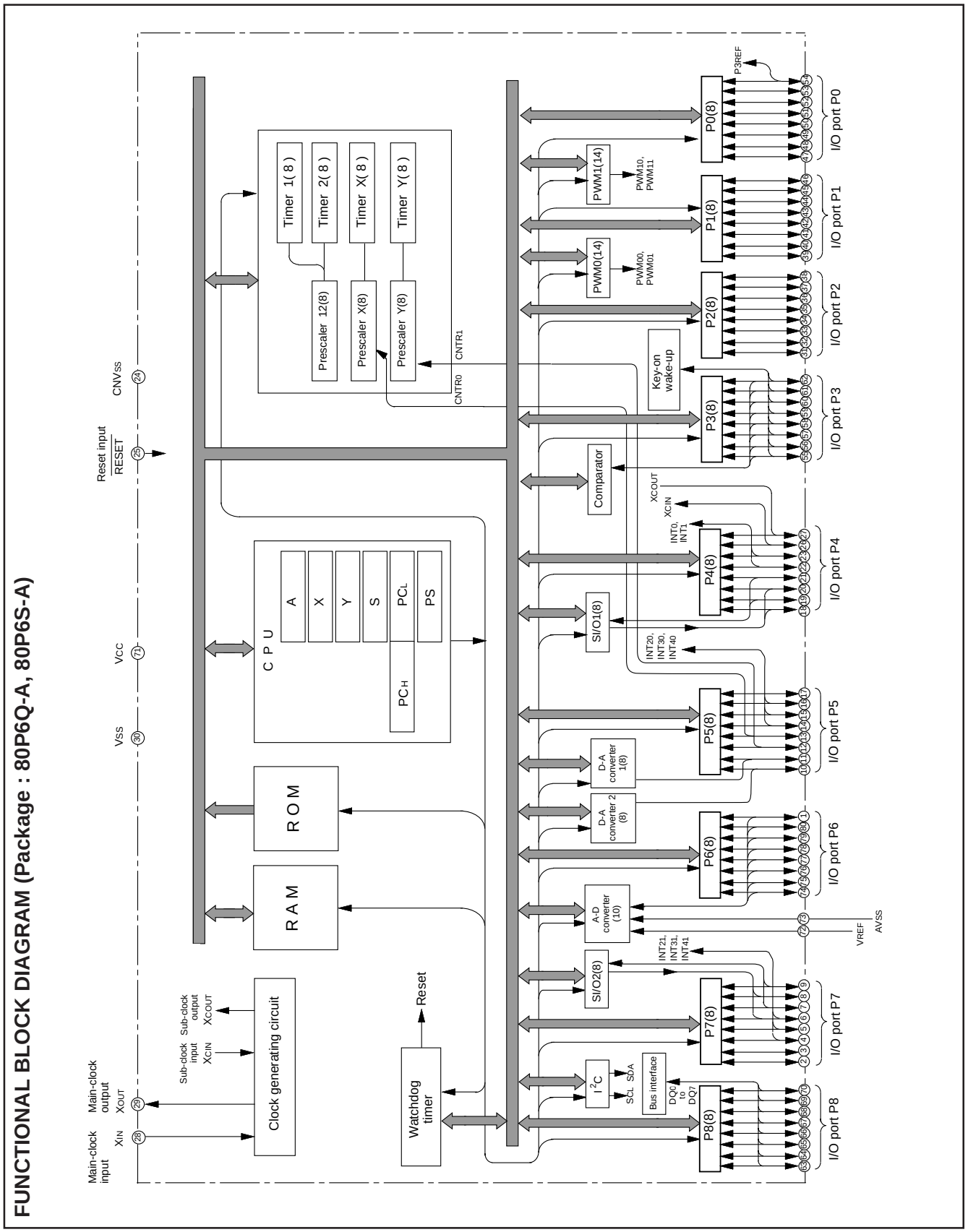


Fig. 4 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss. •In the flash memory version, apply voltage of 4.0 V – 5.5 V to Vcc, and 0 V to Vss	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to VSS. •If this pin is connected to Vcc, the internal ROM is inhibited and an external memory is accessed. •In the flash memory version, connected to VSS. •In the EPROM version or the flash memory version, this pin functions as the VPP power source input pin.	
VREF	Reference voltage	•Reference voltage input pin for A-D and D-A converters.	
AVSS	Analog power source	•Analog power source input pin for A-D and D-A converters. •Connect to VSS.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active “L”.	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/P3REF	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output.	•Comparator reference power source input pin
P01–P07		•When the external memory is used, these pins are used as the address bus. •CMOS compatible input level. •CMOS 3-state output structure or N-channel open-drain output structure.	
P10–P17	I/O port P1	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •When the external memory is used, these pins are used as the address bus. •CMOS compatible input level. •CMOS 3-state output structure or N-channel open-drain output structure.	
P20–P27	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •When the external memory is used, these pins are used as the data bus. •CMOS compatible input level. •CMOS 3-state output structure. •P24 to P27 (4 bits) are enabled to output large current for LED drive (only in single-chip mode).	
P30/PWM00 P31/PWM10	I/O port P3	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •When the external memory is used, these pins are used as the control bus.	•Key-on wake-up input pin •Comparator input pin •PWM output pin
P32–P37		•CMOS compatible input level. •CMOS 3-state output structure. •These pins function as key-on wake-up and comparator input. •These pins are enabled to control pull-up.	•Key-on wake-up input pin •Comparator input pin

Table 2 Pin description (2)

Pin	Name	Functions	Function except a port function
P40/XCOUT P41/XCIN	I/O port P4	•8-bit I/O port with the same function as port P0. <Input level> P40, P41 : CMOS input level P42–P46 : CMOS compatible input level or TTL input level P47 : CMOS compatible input level or TTL input level in the bus interface function <Output structure> P40, P41, P47 : CMOS 3-state output structure P42–P46 : CMOS 3-state output structure or N-channel open-drain output structure •Regardless of input or output port, P42 to P46 can be input every pin level. •When P42 and P43 are used as output port, the function which makes P42 and P43 clear to "0" when the host CPU reads the output data bus buffer 0 can be added.	•Sub-clock generating circuit I/O pins (Connect a resonator.)
P42/INT0 /OBF00 P43/INT1 /OBF01			•Interrupt input pins •Bus interface function pins
P44/RxD P45/TxD			•Serial I/O1 function pins
P46/SCLK1 /OBF10 P47/$\overline{\text{SRDY1}}$ /$\overline{\text{S1}}$			•Serial I/O1 function pins •Bus interface function pins
P50/A0	I/O port P5	•8-bit I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure. •P50 to P53 can be switched between CMOS compatible input level or TTL input level in the bus interface function.	•Bus interface function pins
P51/INT20 /$\overline{\text{S0}}$ P52/INT30 /$\overline{\text{R}}$ P53/INT40 /$\overline{\text{W}}$			•Interrupt input pins •Bus interface function pins
P54/CNTR0 P55/CNTR1			•Timer X, timer Y function pins
P56/DA1 /PWM01 P57/DA2 /PWM11			•D-A converter output pin •PWM output pin
P60/AN0– P67/AN7	I/O port P6	•8-bit I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	•A-D converter output pin
P70/SIN2 P71/SOUT2 P72/SCLK2	I/O port P7	•8-bit I/O port with the same function as port P0. P70–P75 : CMOS compatible input level or TTL input level P76, P77 : CMOS compatible input level or SMBUS input level in the I^2C-BUS interface function, N-channel open-drain output structure •Regardless of input or output port, P70 to P75 can be input every pin level.	•Serial I/O2 function pin
P73/$\overline{\text{SRDY2}}$ /INT21			•Serial I/O2 function pin •Interrupt input pin
P74/INT31 P75/INT41			•Interrupt input pin
P76/SDA P77/SCL			•I^2C-BUS interface function pin
P80/DQ0– P87/DQ7	I/O port P8	•8-bit I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure. •CMOS compatible input level or TTL input level in the bus interface function.	•Bus interface function pin

PART NUMBERING

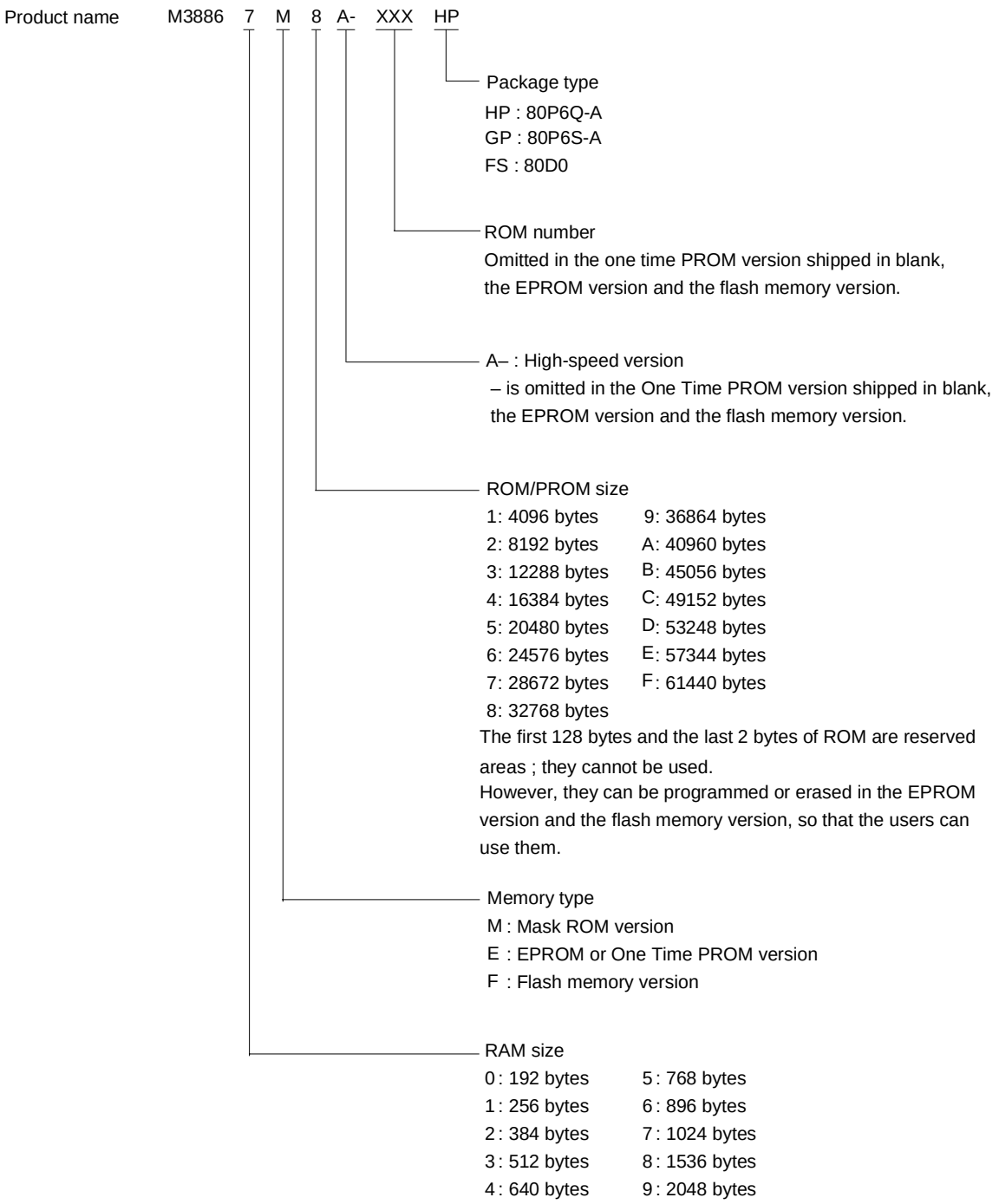


Fig. 5 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3886 group as follows.

Memory Type

Support for mask ROM, One Time PROM, EPROM and flash memory version.

Memory Size

ROM size ..... 32 K to 60 K bytes
RAM size ..... 1024 to 2048 bytes

Packages

80P6Q-A ..... 0.5 mm-pitch plastic molded LQFP
80P6S-A ..... 0.65mm pitch plastic molded QFP
80D0 ..... 0.8 mm-pitch ceramic LCC (EPROM version)

The pin number and the position of the function pin may change by the kind of package.

Memory Expansion

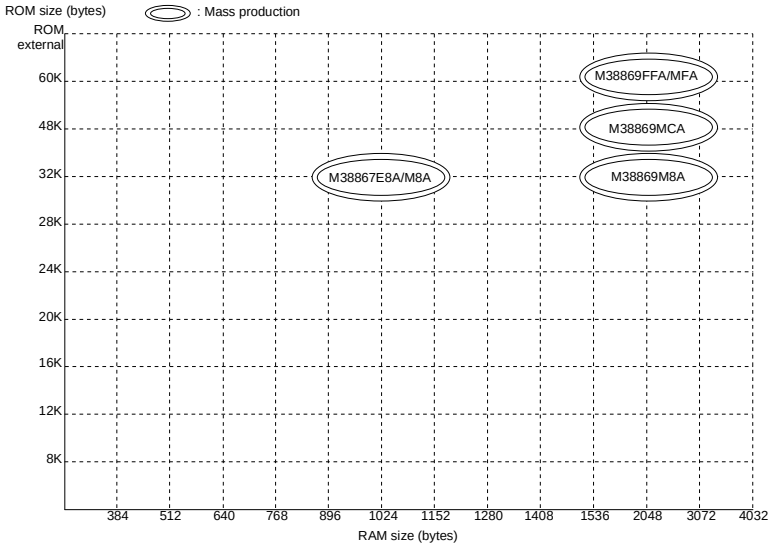


Fig. 6 Memory expansion plan

Currently products are listed below.

Table 3 Support products **As of Jan. 2000**

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38867M8A-XXXHP	32768 (32638)	1024	80P6Q-A	Mask ROM version
M38867E8A-XXXHP				One Time PROM version
M38867E8AHP				One Time PROM version (blank)
M38867E8AFS			80D0	EPROM version
M38869M8A-XXXHP		2048	80P6Q-A	Mask ROM version
M38869M8A-XXXGP			80P6S-A	
M38869MCA-XXXHP	49152 (19022)		80P6Q-A	
M38869MCA-XXXGP			80P6S-A	
M38869MFA-XXXHP	61440 (61310)		80P6Q-A	
M38869MFA-XXXGP			80P6S-A	
M38869FFAHP			80P6Q-A	Flash memory version
M38869FFAGP			80P6S-A	

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3886 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, the processor mode bits specifying the chip operation mode, etc.

The CPU mode register is allocated at address 003B16.

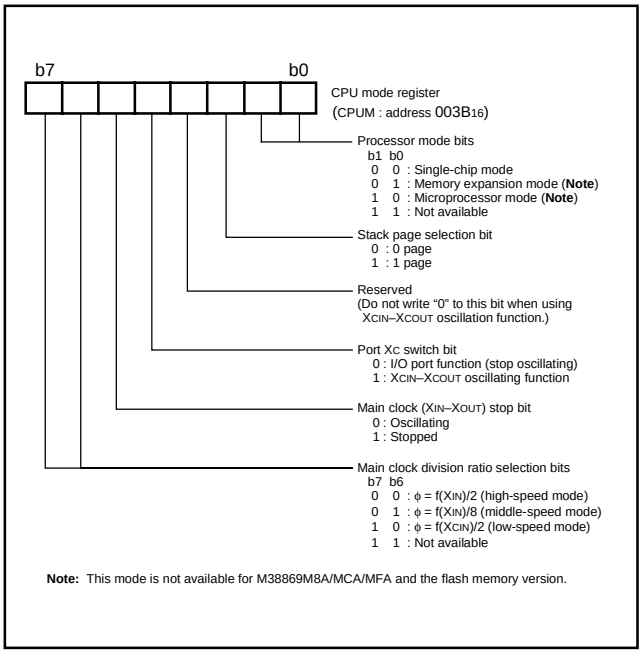


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs. Program/Erase of the reserved ROM area is possible in the EPROM version and the flash memory version

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

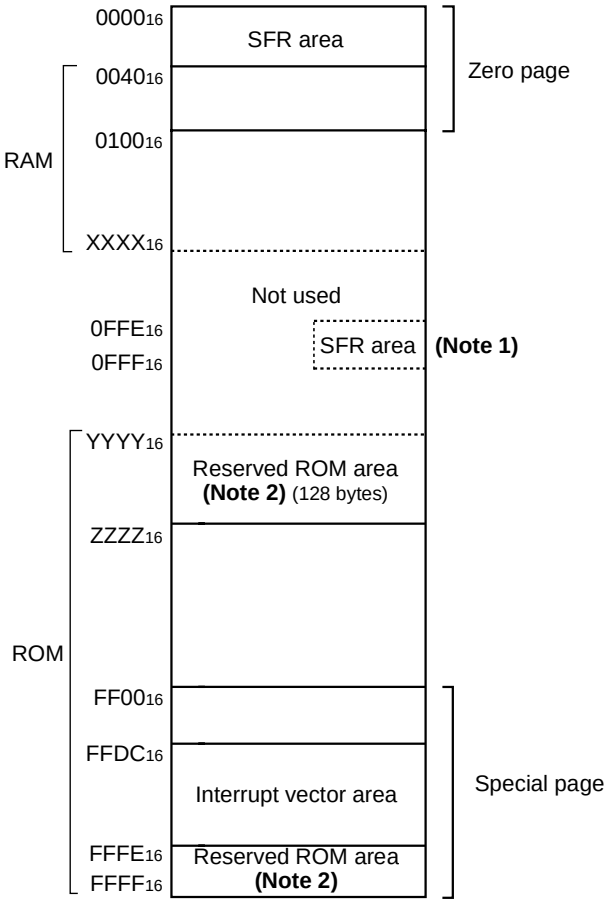
Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016



Notes 1: This area is SFR in M38869FFA.
This area is Reserved in M38869MFA/MCA/M8A.
This area is not used in M38867M8A/E8A.
2: This area is usable in EPROM version and flash memory version.

Fig. 8 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	Port P7 (P7)
$000F_{16}$	Port P7 direction register (P7D)
0010_{16}	Port P8 (P8)/Port P4 input register (P4I)
0011_{16}	Port P8 direction register (P8D)/Port P7 input register (P7I)
0012_{16}	I^2C data shift register (S0)
0013_{16}	I^2C address register (S0D)
0014_{16}	I^2C status register (S1)
0015_{16}	I^2C control register (S1D)
0016_{16}	I^2C clock control register (S2)
0017_{16}	I^2C start/stop condition control register (S2D)
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O1 status register (SIO1STS)
$001A_{16}$	Serial I/O1 control register (SIO1CON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	Serial I/O2 control register (SIO2CON)
$001E_{16}$	Watchdog timer control register (WDTCON)
$001F_{16}$	Serial I/O2 register (SIO2)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Data bas buffer register 0 (DBB0)
0029_{16}	Data bas buffer status register 0 (DBBSTS0)
$002A_{16}$	Data bas buffer control register (DBBCON)
$002B_{16}$	Data bas buffer register 1 (DBB1)
$002C_{16}$	Data bas buffer status register 1 (DBBSTS1)
$002D_{16}$	Comparator data register (CMPD)
$002E_{16}$	Port control register 1 (PCTL1)
$002F_{16}$	Port control register 2 (PCTL2)
0030_{16}	PWM0H register (PWM0H)
0031_{16}	PWM0L register (PWM0L)
0032_{16}	PWM1H register (PWM1H)
0033_{16}	PWM1L register (PWM1L)
0034_{16}	AD/DA control register (ADCON)
0035_{16}	A-D conversion register 1 (AD1)
0036_{16}	D-A1 conversion register (DA1)
0037_{16}	D-A2 conversion register (DA2)
0038_{16}	A-D conversion register 2 (AD2)
0039_{16}	Interrupt source selection register (INTSEL)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

$0FFE_{16}$	Flash memory control register (FCON)	**(Note)**
$0FFF_{16}$	Flash command register (FCMD)	**(Note)**

Note: Flash memory version only

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

When the P8 function select bit of the port control register 2 (address $002F_{16}$) is set to "1", read from address 0010_{16} becomes the port P4 input register, and read from address 0011_{16} becomes the port P7 input register.

As the particular function, value of $P4_2$ to $P4_6$ pins and $P7_0$ to $P7_5$ pins can be read regardless of setting direction registers, by reading the port P4 input register (address 0010_{16}) or the port P7 input register (address 0011_{16}) respectively.

Table 4 I/O port function (1)

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
$P0_0$/$P3_{REF}$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output or N-channel open-drain output	Address low-order byte output Analog comparator power source input pin	CPU mode register Port control register 1 Serial I/O2 control register	(1)
$P0_1$–$P0_7$				Address low-order byte output	CPU mode register Port control register 1	(2)
$P1_0$–$P1_7$	Port P1			Address high-order byte output		
$P2_0$–$P2_7$	Port P2		CMOS compatible input level CMOS 3-state output	Data bus I/O	CPU mode register	(3)
$P3_0$/PWM_{00} $P3_1$/PWM_{10}	Port P3			Control signal I/O PWM output Key-on wake up input Comparator input	CPU mode register Port control register 1 AD/DA control register	(4) (5)
$P3_2$–$P3_7$				Control signal I/O Key-on wake up input Comparator input	CPU mode register Port control register 1	(6)
$P4_0$/X_{COUT} $P4_1$/X_{CIN}	Port P4			Sub-clock generating circuit	CPU mode register	(7) (8)
$P4_2$/INT_0/ OBF_{00} $P4_3$/INT_1/ OBF_{01}			CMOS compatible input level or TTL input level CMOS 3-state output or N-channel open-drain output	External interrupt input Bus interface function I/O	Interrupt edge selection register Port control register 2	(9) (10)
$P4_4$/RxD				Serial I/O1 function input	Serial I/O1 control register Port control register 2	(11)
$P4_5$/TxD				Serial I/O1 function output	Serial I/O1 control register UART control register Port control register 2	(12)
$P4_6$/S_{CLK1} /OBF_{10}				Serial I/O1 function I/O Bus interface function output	Serial I/O1 control register Data bus buffer control register Port control register 2	(13)
$P4_7$/$\overline{S_{RDY1}}$ /$\overline{S_1}$			CMOS compatible input level CMOS 3-state output (when selecting bus interface function) CMOS compatible input level or TTL input level	Serial I/O1 function output Bus interface function input	Serial I/O1 control register Data bus buffer control register	(14)

Table 5 I/O port function (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P5$_0$/A$_0$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output (when selecting bus interface function) CMOS compatible input level or TTL input level	Bus interface function input	Data bus buffer control register	(15)
P5$_1$/INT$_{20}$ /$\overline{S_0}$ P5$_2$/INT$_{30}$ /$\overline{R}$ P5$_3$/INT$_{40}$ /$\overline{W}$				External interrupt input Bus interface function input	Interrupt edge selection register Data bus buffer control register	(16)
P5$_4$/CNTR$_0$ P5$_5$/CNTR$_1$			CMOS compatible input level CMOS 3-state output	Timer X, timer Y function I/O	Timer XY mode register	(17)
P5$_6$/DA$_1$/ PWM$_{01}$ P5$_7$/DA$_2$/ PWM$_{11}$				D-A converter output PWM output	AD/DA control register UART control register	(18) (19)
P6$_0$/AN$_0$– P6$_7$/AN$_7$	Port P6			A-D converter input	AD/DA control register	(20)
P7$_0$/SIN$_2$ P7$_1$/SOUT$_2$ P7$_2$/SCLK$_2$	Port P7		CMOS compatible input level or TTL input level N-channel open-drain output	Serial I/O2 function I/O	Serial I/O2 control register Port control register 2	(21) (22) (23)
P7$_3$/$\overline{SRDY_2}$/ INT$_{21}$				Serial I/O2 function output Bus interface function input	Serial I/O2 control register Port control register 2	(24)
P7$_4$/INT$_{31}$ P7$_5$/INT$_{41}$				External interrupt input	Interrupt edge selection register Port control register 2	(25)
P7$_6$/SDA P7$_7$/SCL			CMOS compatible input level N-channel open-drain output (when selecting I^{2}C-BUS interface function) CMOS compatible input level or SMBUS input level	I^{2}C-BUS interface function I/O	I^{2}C control register	(26) (27)
P8$_0$/DQ$_0$– P8$_7$/DQ$_7$	Port P8		CMOS compatible input level CMOS 3-state output (when selecting bus interface function) CMOS compatible input level or TTL input level	Bus interface function I/O	Data bus buffer control register	(28)

Notes1: For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, refer to the applicable sections.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

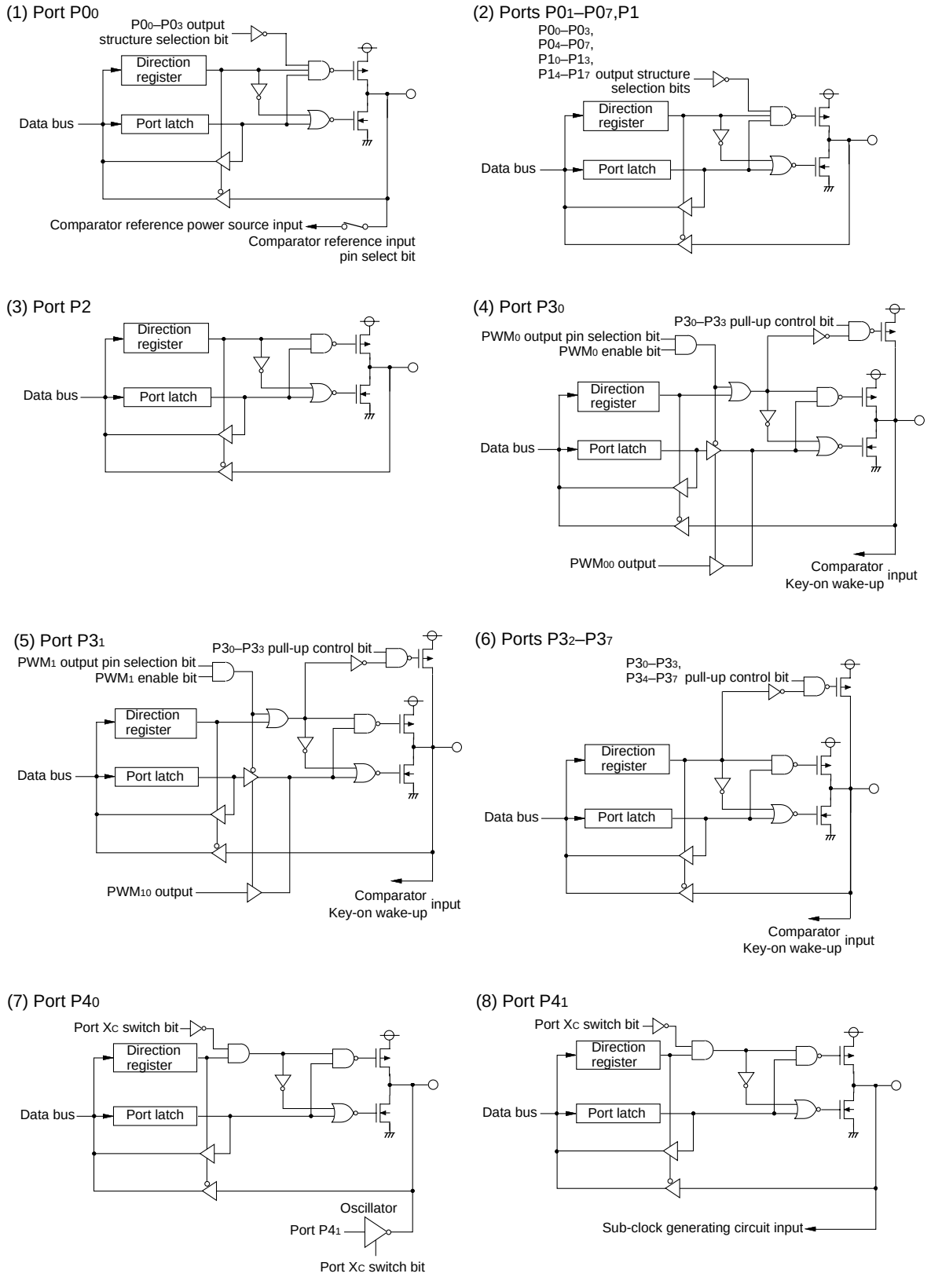
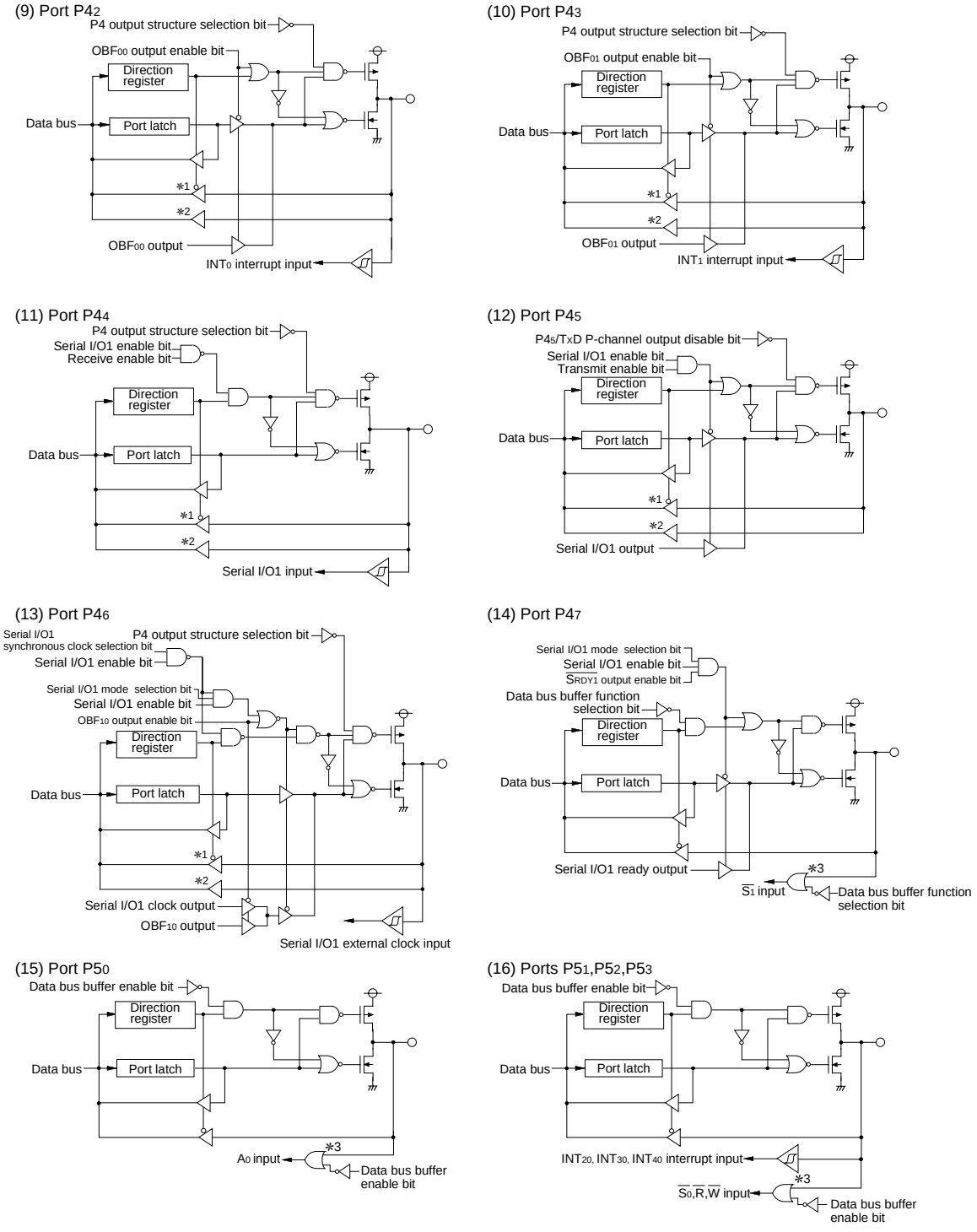
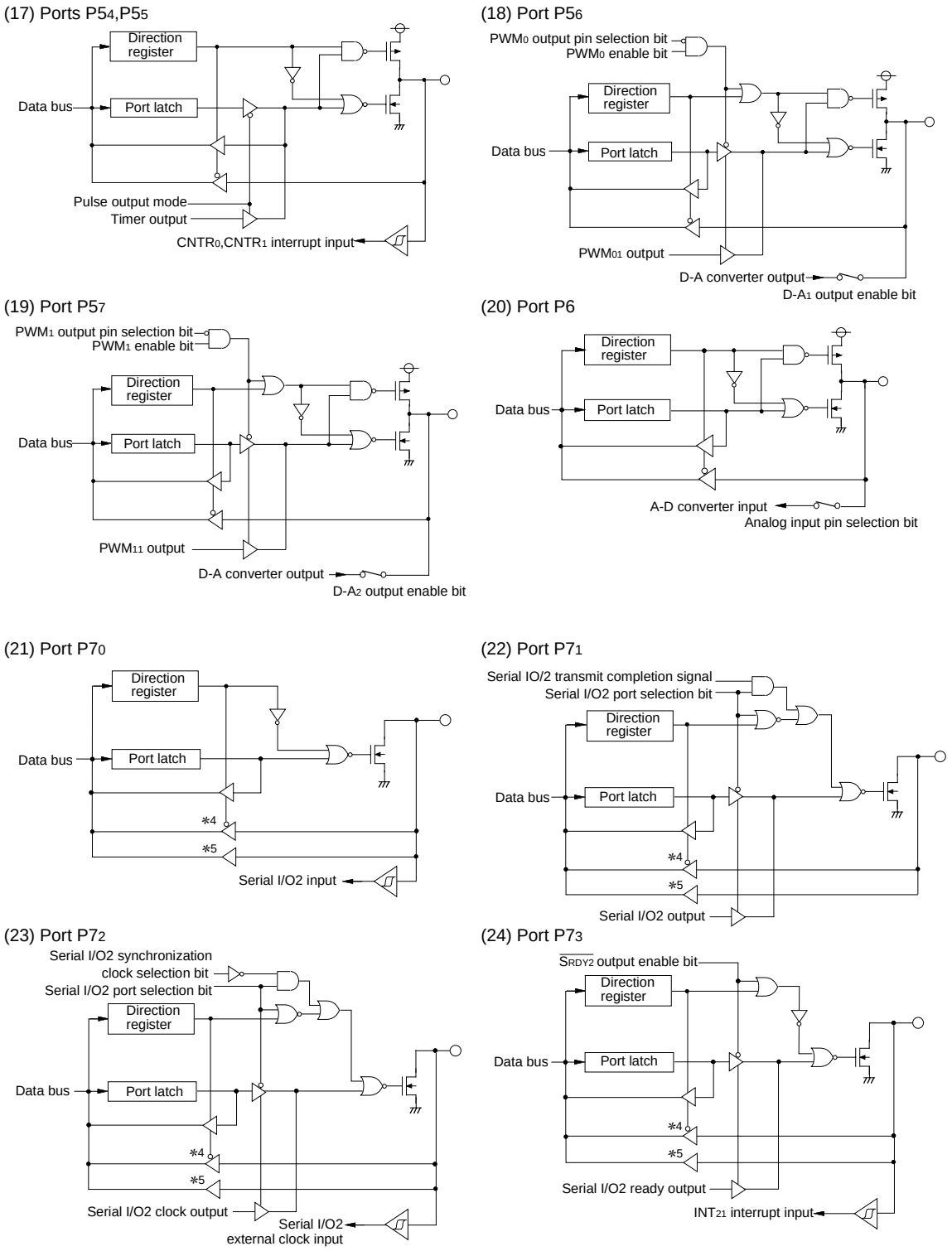


Fig. 10 Port block diagram (1)



∗1. The input level can be switched between CMOS compatible input level and TTL level by the P4 input level selection bit of the port control register 2 (address 002F16).
∗2. The input level can be switched between CMOS compatible input level and TTL level by the P4 input level selection bit of the port control register 2 (address 002F16).
The port P8 and port P4 input register can be switched by the P8 function selection bit of the port control register 2 (address 002F16).
∗3. The input level can be switched between CMOS compatible input level and TTL level by the input level selection bit of the data bus buffer control register (address 002A16).

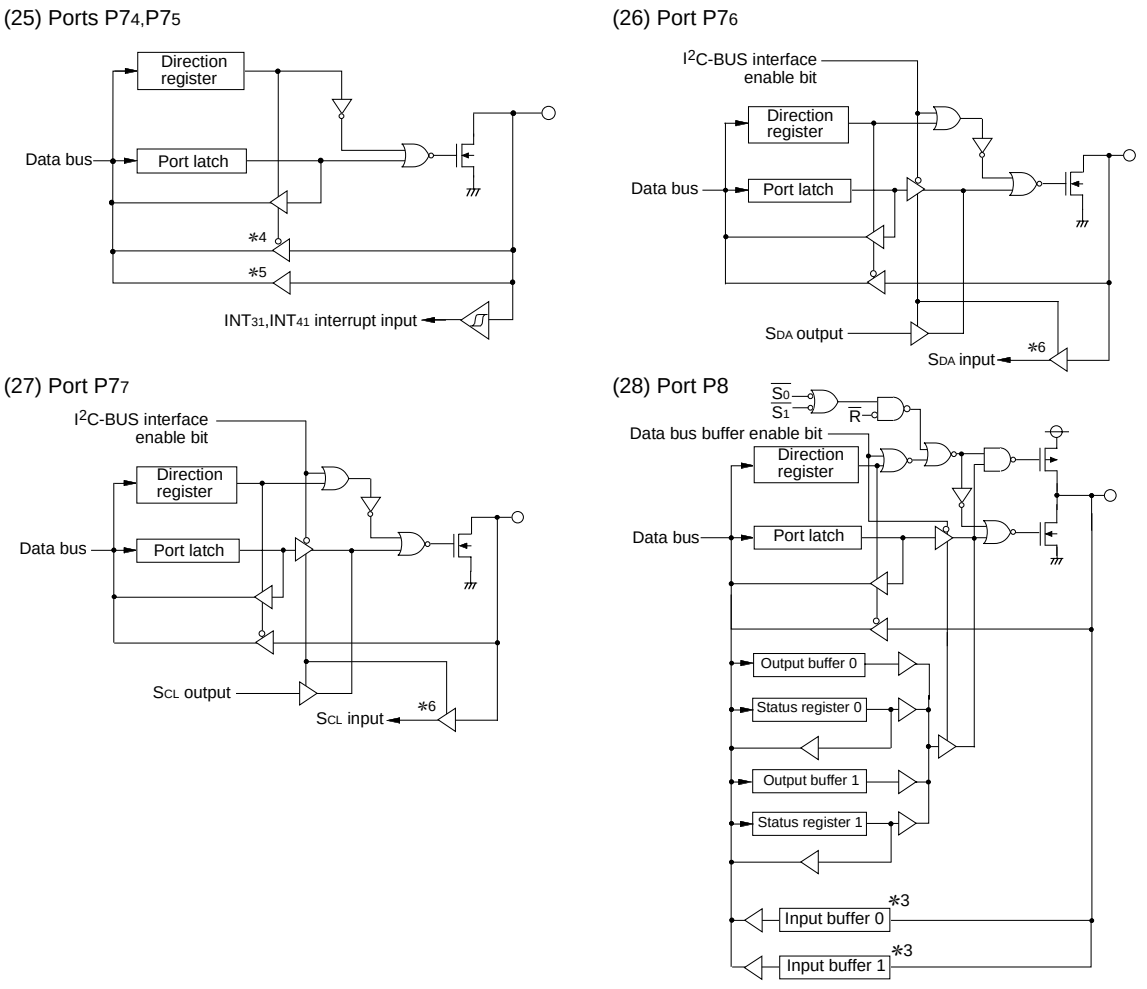
Fig. 11 Port block diagram (2)



*4. The input level can be switched between CMOS compatible input level and TTL level by the P7 input level selection bit of the port control register 2 (address 002F16).

*5. The input level can be switched between CMOS compatible input level and TTL level by the P7 input level selection bit of the port control register 2 (address 002F16).
The port P8 direction register and port P7 input register can be switched by the P8 function selection bit of the port control register 2 (address 002F16).

Fig. 12 Port block diagram (3)



*6. The input level can be switched between CMOS compatible input level and SMBUS level by the I2C-BUS interface pin input selection bit of the I2C control register (address 001516).

Fig. 13 Port block diagram (4)

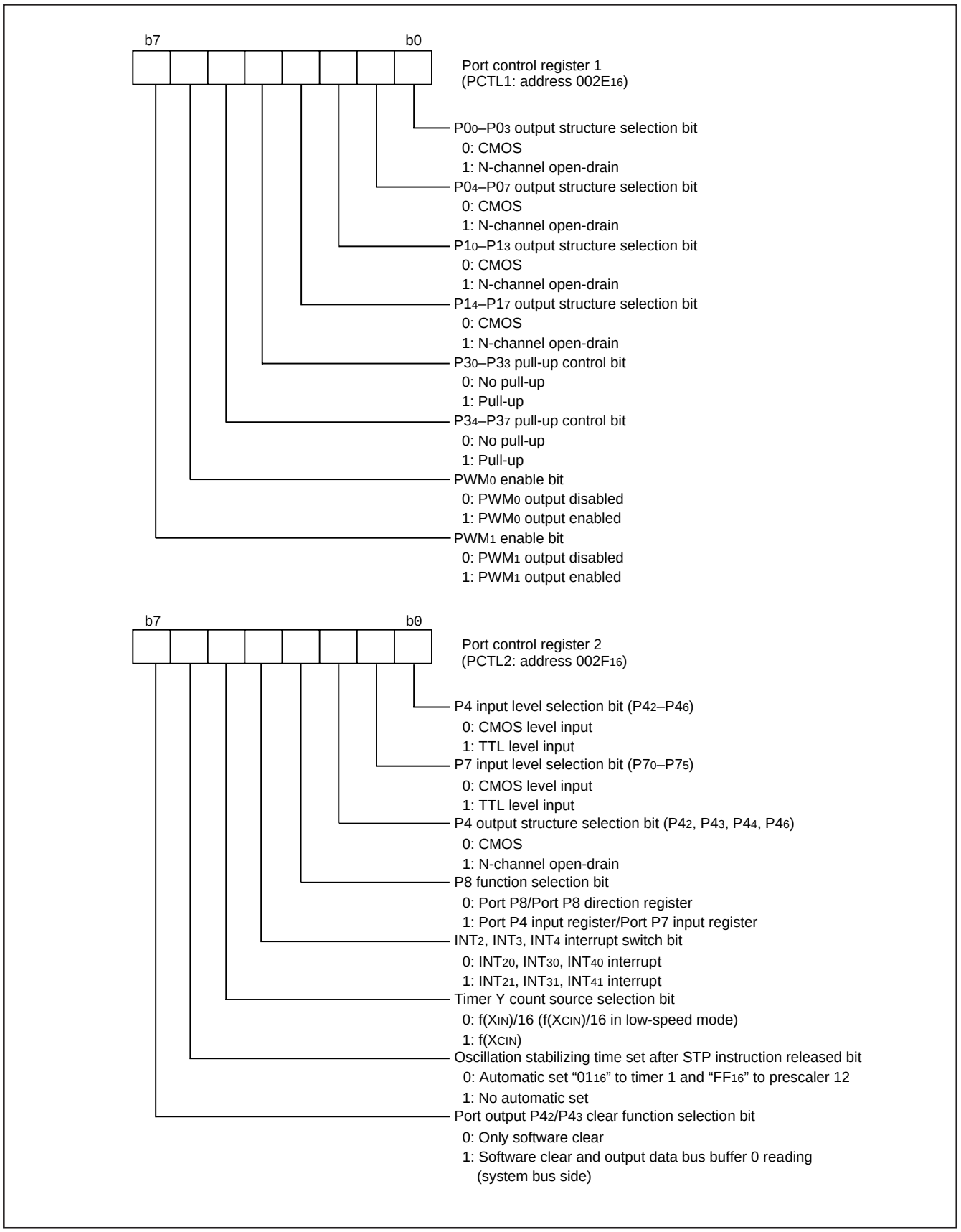


Fig. 14 Structure of port I/O related register

INTERRUPTS

Interrupts occur by 16 sources among 21 sources: nine external, eleven internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Interrupt Source Selection

Any of the following interrupt sources can be selected by the interrupt source selection register (address 0039_{16}).

1. INT_0 or Input buffer full
2. INT_1 or Output buffer empty
3. Serial I/O1 transmission or SCL_{SDA}
4. $CNTR_0$ or SCL_{SDA}
5. Serial I/O2 or I^2C
6. INT_2 or I^2C
7. $CNTR_1$ or Key-on wake-up
8. A-D conversion or Key-on wake-up

External Interrupt Pin Selection

The occurrence sources of the external interrupt INT_2, INT_3, and INT_4 can be selected from either input from INT_{20}, INT_{30}, INT_{40} pin, or input from INT_{21}, INT_{31}, INT_{41} pin by the INT_2, INT_3, INT_4 interrupt switch bit (bit 4 of address $002F_{16}$).

■ Notes

When setting of the following register or bit is changed, the interrupt request bit may be set to "1."

- Interrupt edge selection register (address $003A_{16}$)
- Interrupt source selection register (address 0039_{16})
- INT_2, INT_3, INT_4 interrupt switch bit of Port control register 2 (bit 4 of address $002F_{16}$)

Accept the interrupt after clearing the interrupt request bit to "0" after interrupt is disabled and the above register or bit is set.

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Input buffer full (IBF)				At input data bus buffer writing	
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Output buffer empty (OBE)				At output data bus buffer reading	
Serial I/O1 reception	4	FFF716	FFF616	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF516	FFF416	At completion of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
SCL, SDA				At detection of either rising or falling edge of SCL or SDA	External interrupt (active edge selectable)
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 1	8	FFEF16	FFEE16	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED16	FFEC16	At timer 2 underflow	
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
SCL, SDA				At detection of either rising or falling edge of SCL or SDA	External interrupt (active edge selectable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Key-on wake-up				At falling of port P3 (at input) input logical level AND	External interrupt (falling valid)
Serial I/O2	12	FFE716	FFE616	At completion of serial I/O2 data transfer	Valid when serial I/O2 is selected
I^2C				At completion of data transfer	
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
I^2C				At completion of data transfer	
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	15	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable)
A-D converter	16	FFDF16	FFDE16	At completion of A-D conversion	
Key-on wake-up				At falling of port P3 (at input) input logical level AND	External interrupt (falling valid)
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

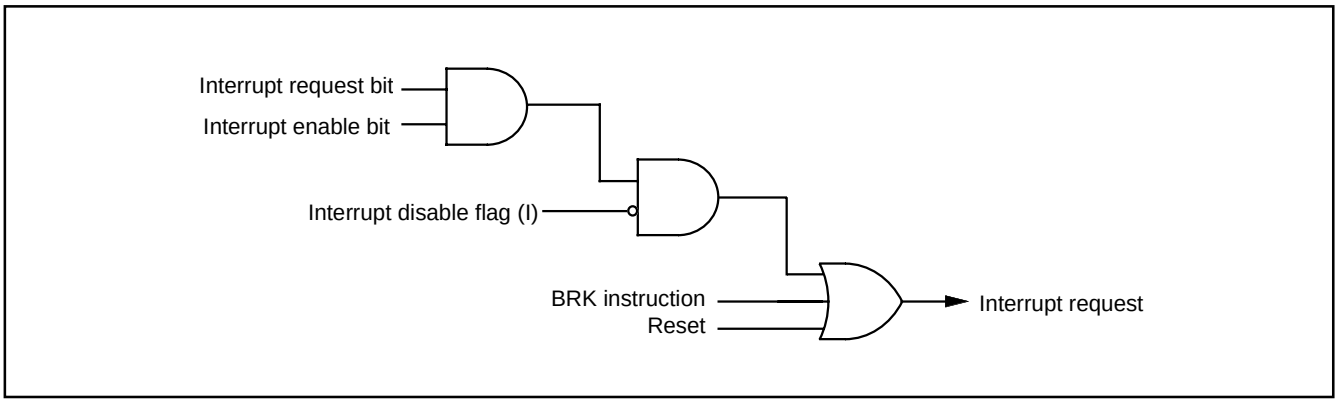


Fig. 15 Interrupt control

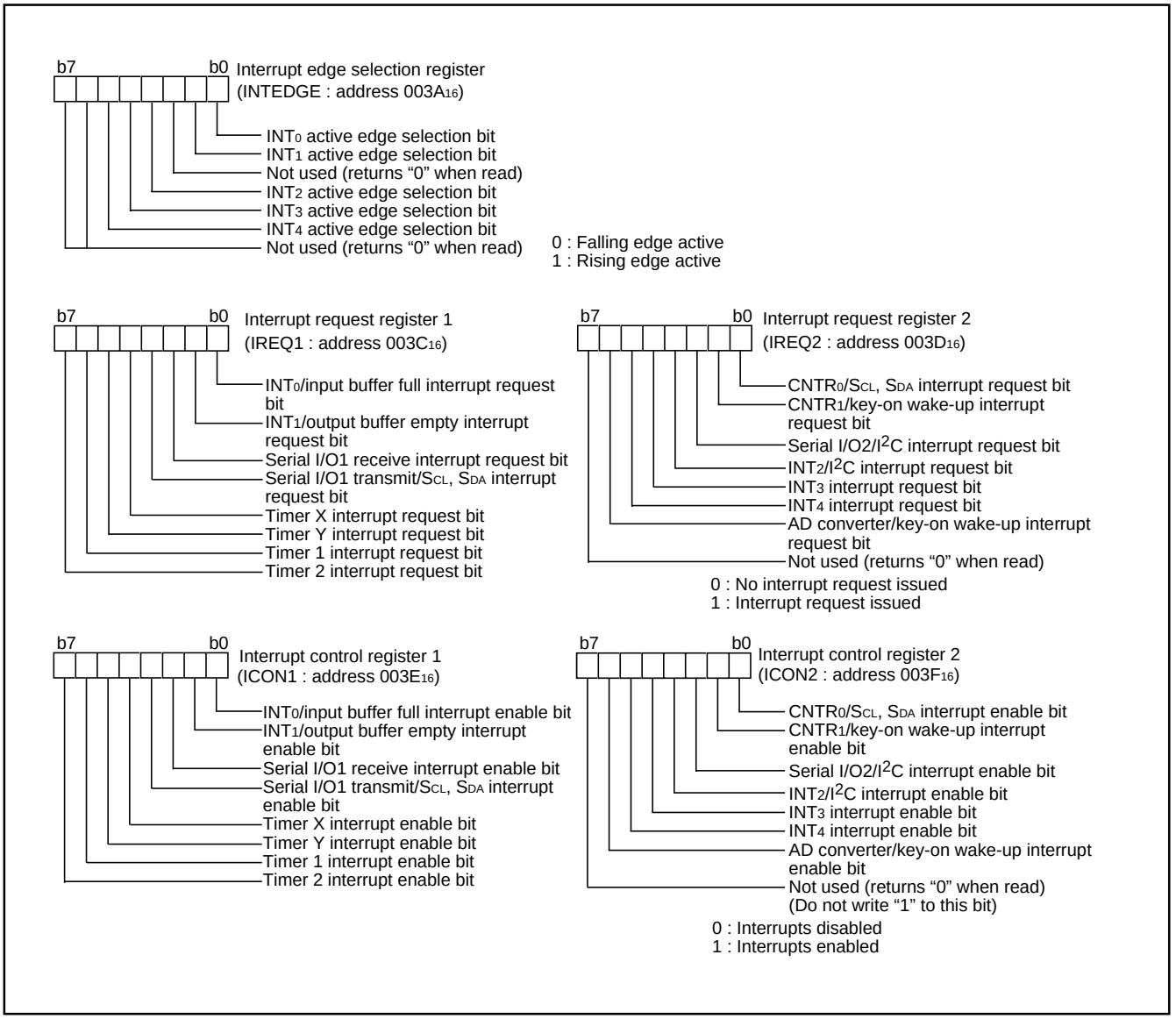


Fig. 16 Structure of interrupt-related registers (1)

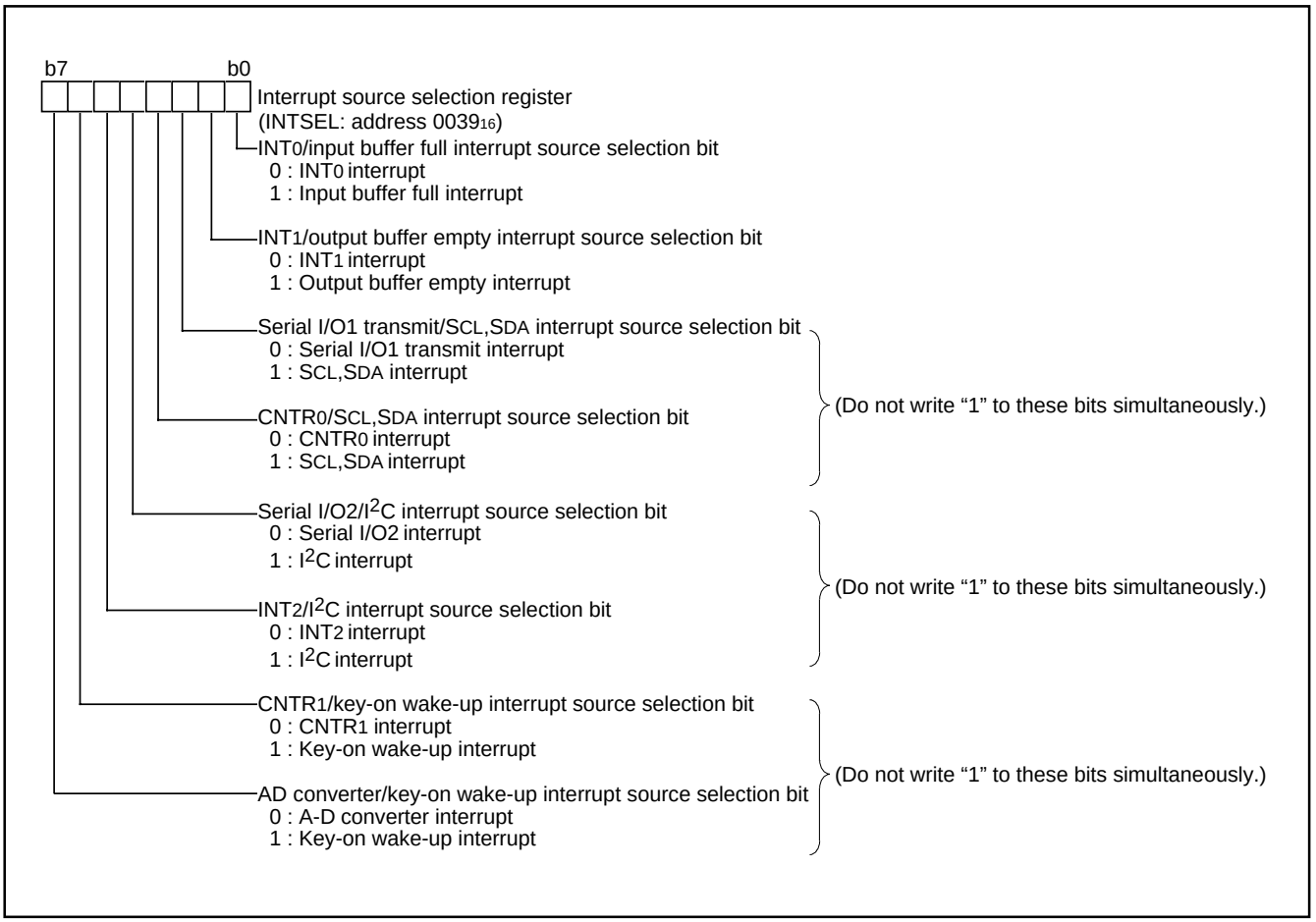


Fig. 17 Structure of interrupt-related registers (2)

Key Input Interrupt (Key-on Wake Up)

A Key input interrupt request is generated by applying "L" level to any pin of port P3 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P30–P33.

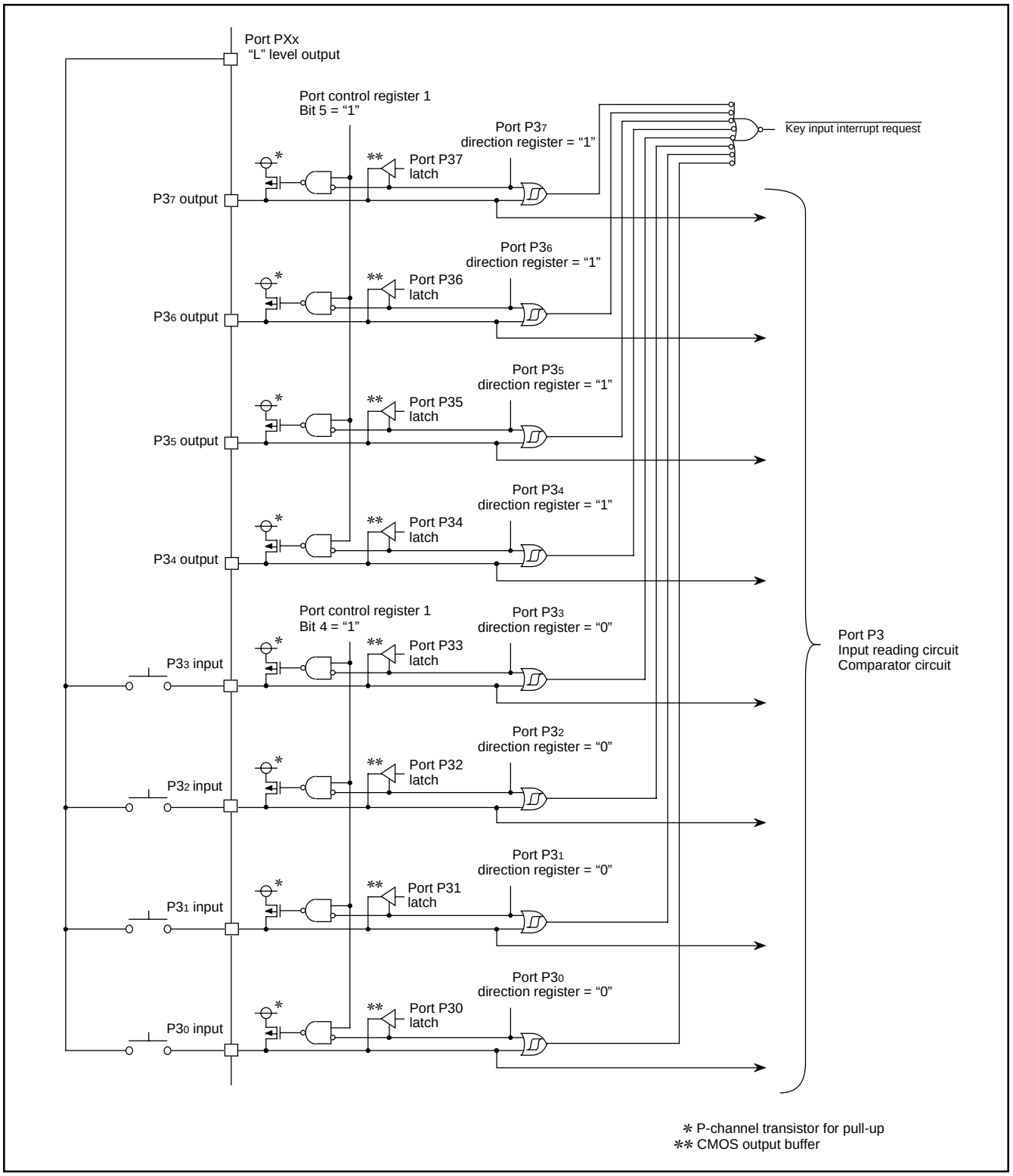


Fig. 18 Connection example when using key input interrupt and port P3 block diagram

TIMERS

The 3886 group has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch. All timers are count down. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

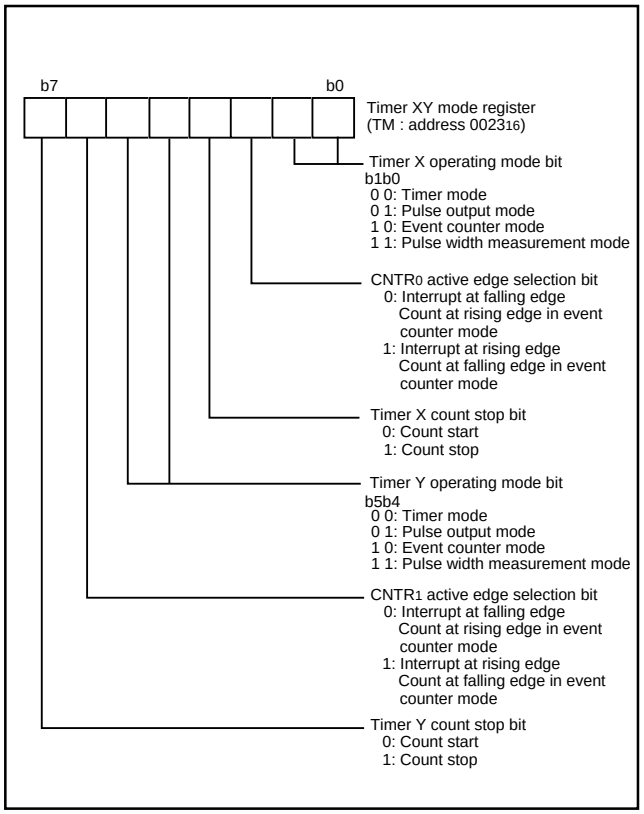


Fig. 19 Structure of timer XY mode register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts f(X_{IN})/16.

(2) Pulse Output Mode

Timer X (or timer Y) counts f(X_{IN})/16. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts f(X_{IN})/16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer overflows.

The count source for timer Y in the timer mode or the pulse output mode can be selected from either f(X_{IN})/16 or f(X_{CIN}) by the timer Y count source selection bit of the port control register 2 (bit 5 of address $002F_{16}$).

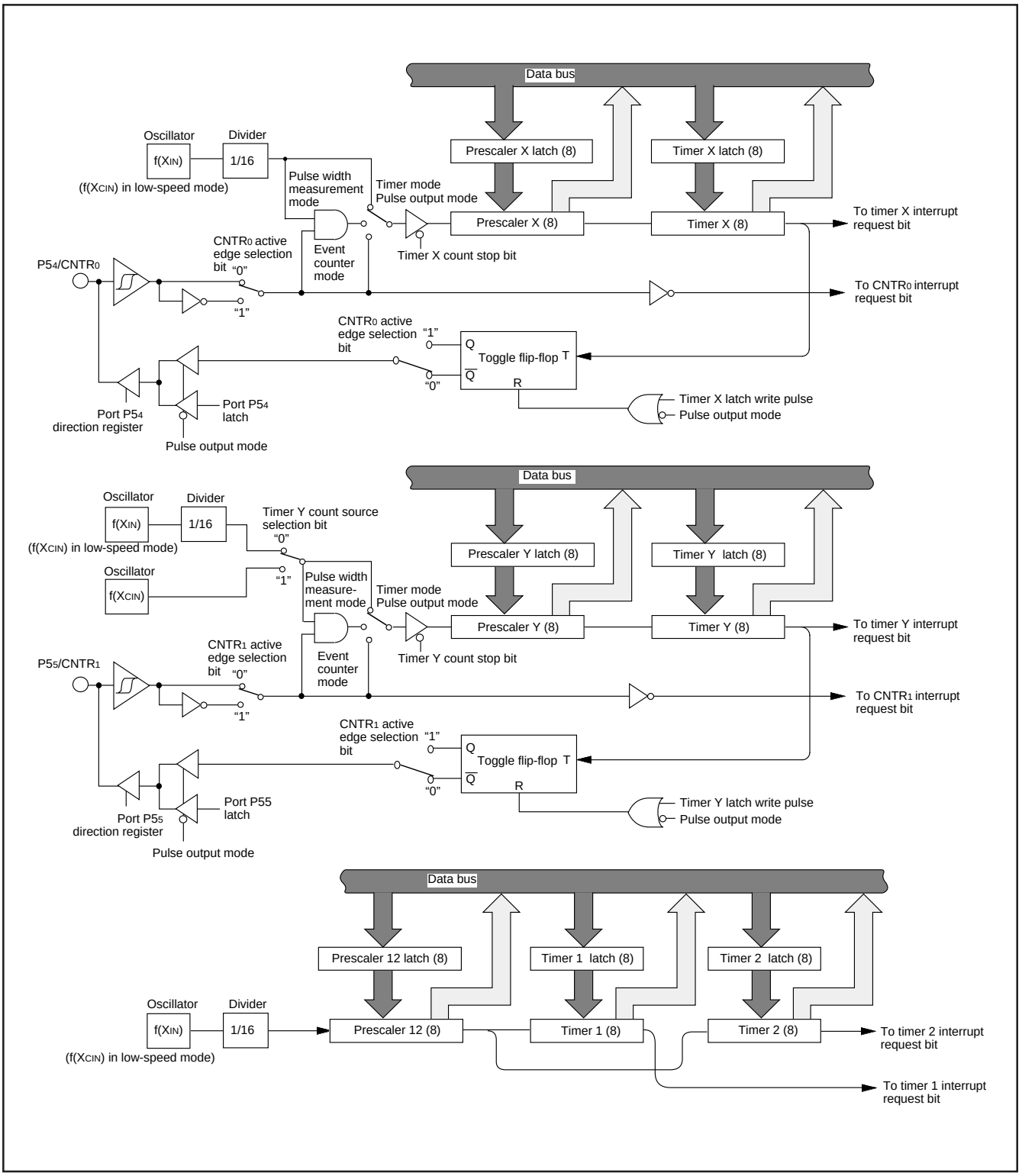


Fig. 20 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O
Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

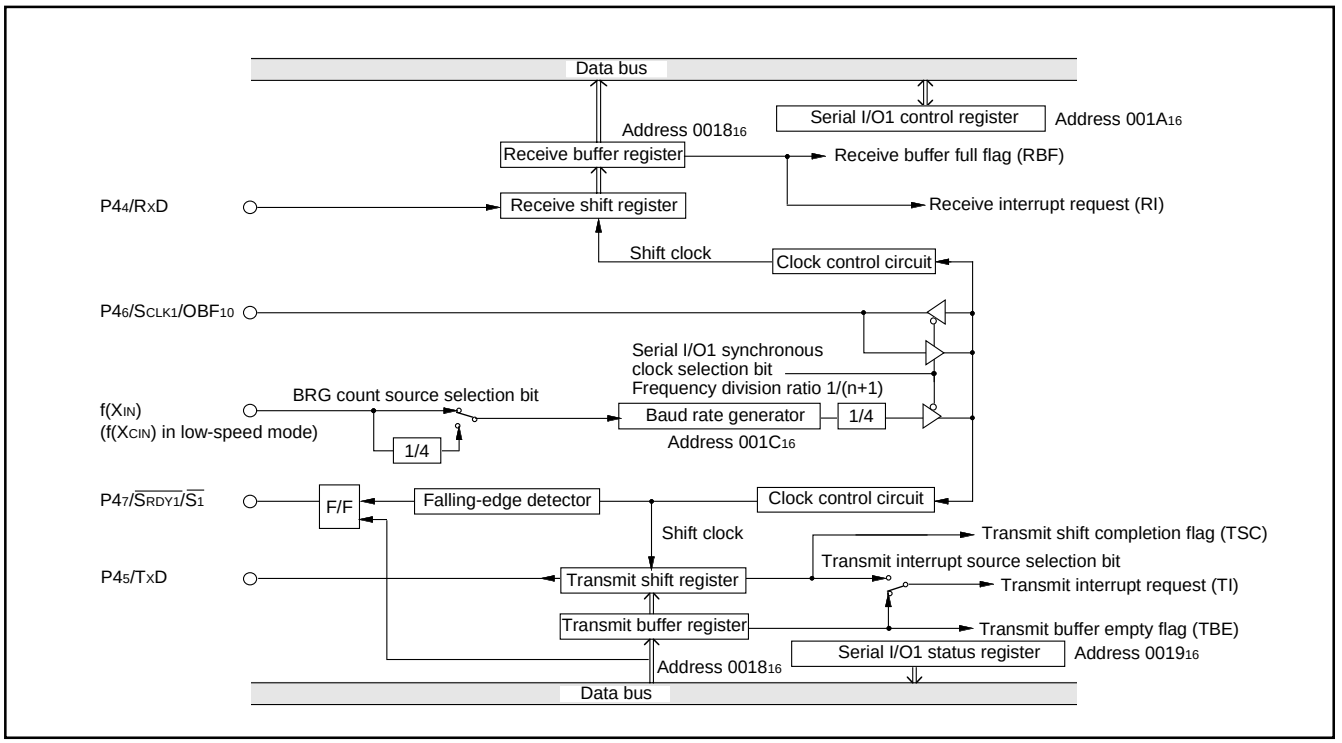
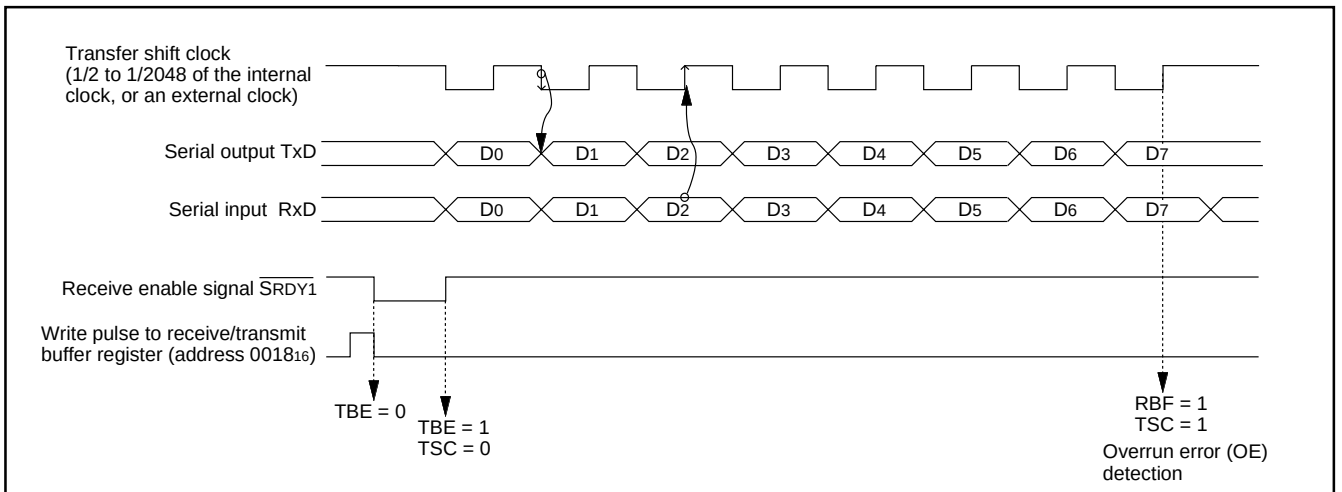


Fig. 21 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 22 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

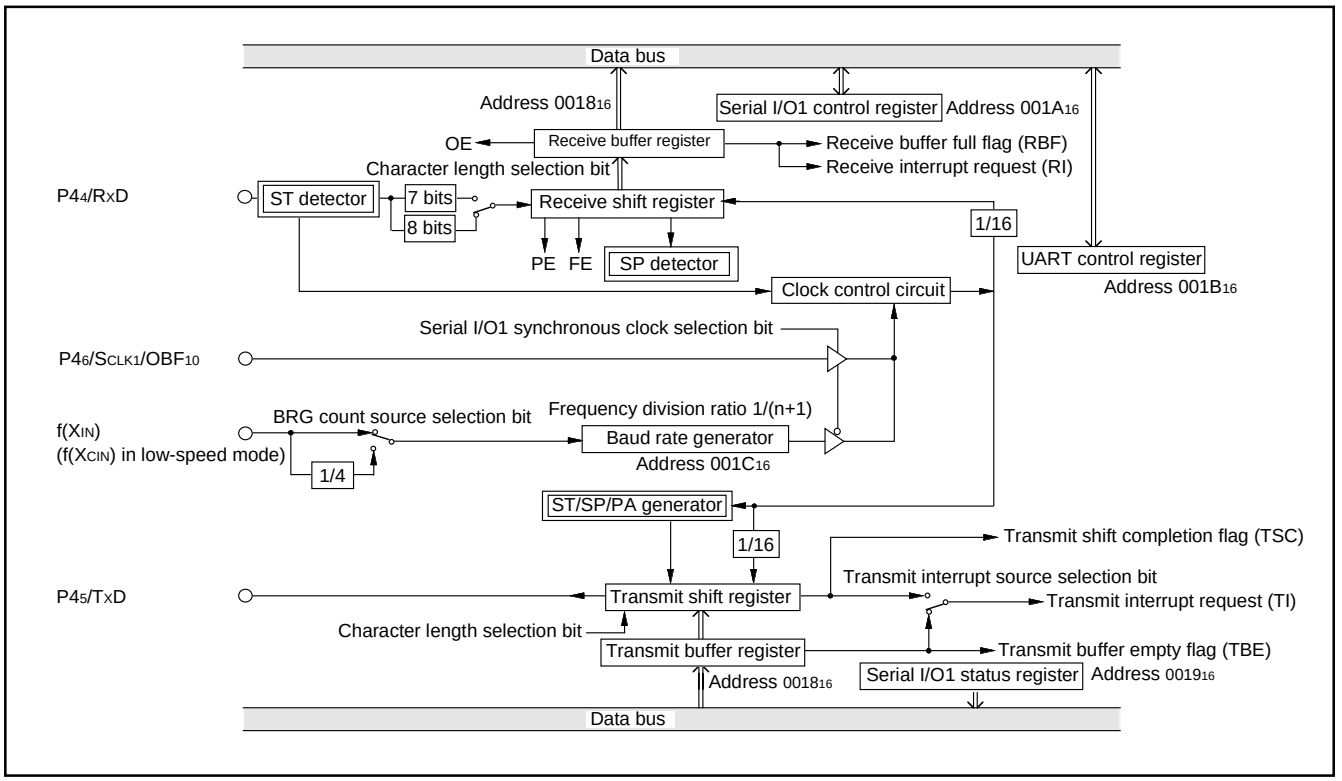
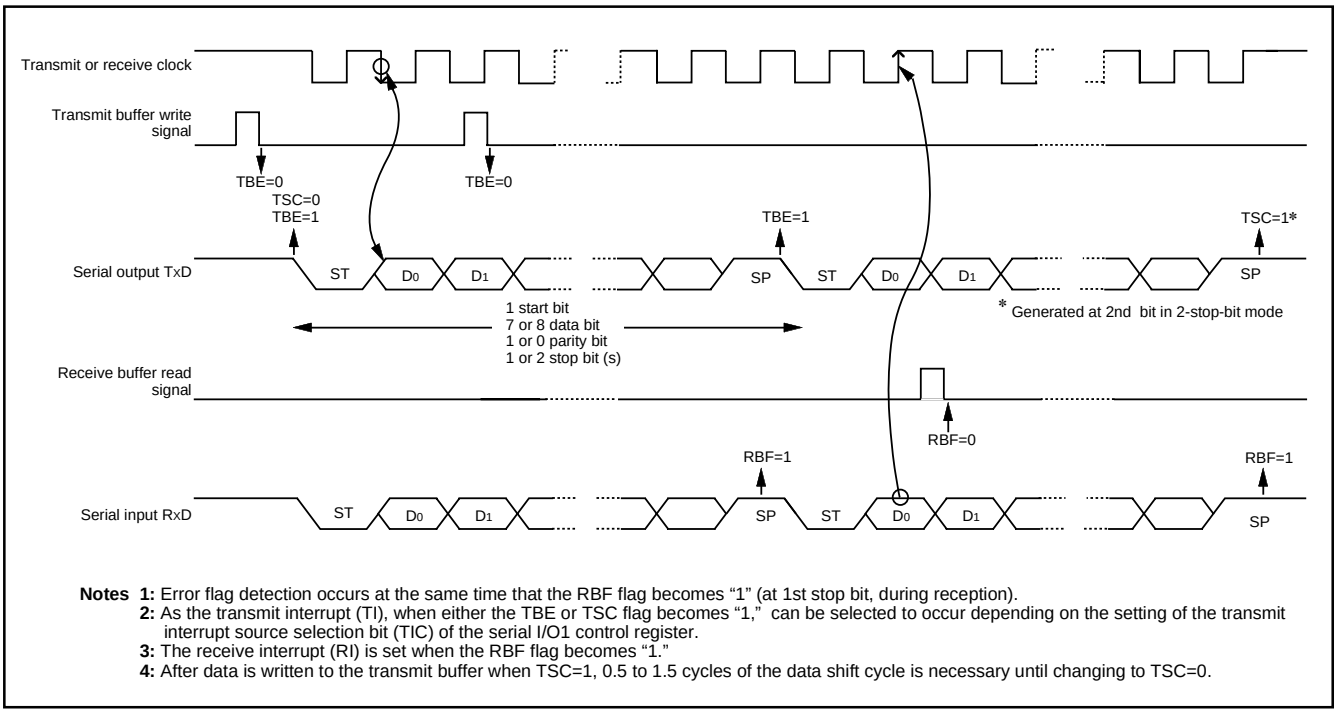


Fig. 23 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1."
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 24 Operation of UART serial I/O1 function

[Serial I/O1 Control Register (SIO1CON)] 001A16

The serial I/O1 control register consists of eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 001B16

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P45/TxD pin.

[Serial I/O1 Status Register (SIO1STS)] 001916

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 001816

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator (BRG)] 001C16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

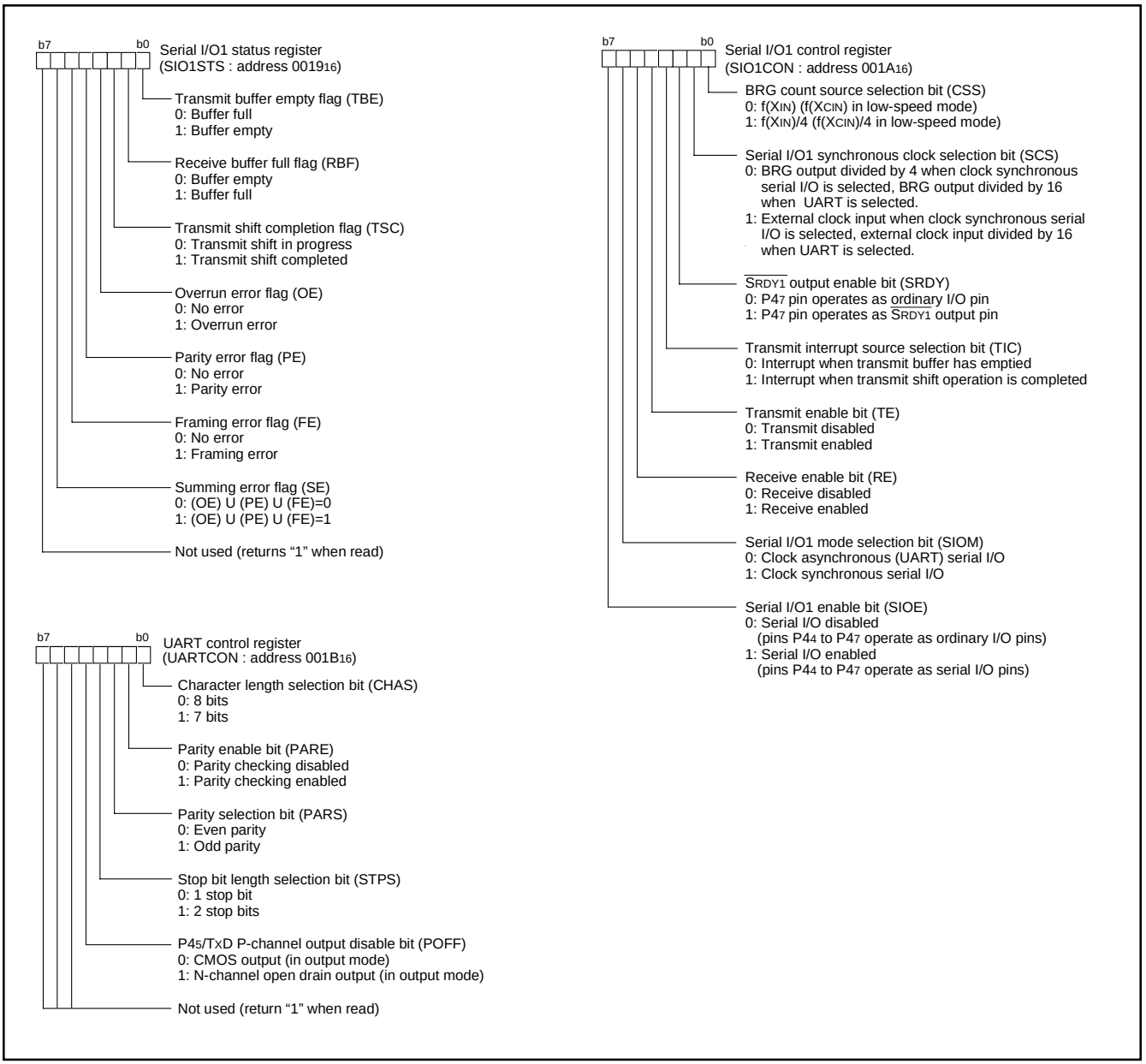


Fig. 25 Structure of serial I/O1 control registers

Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains seven bits which control various serial I/O functions.

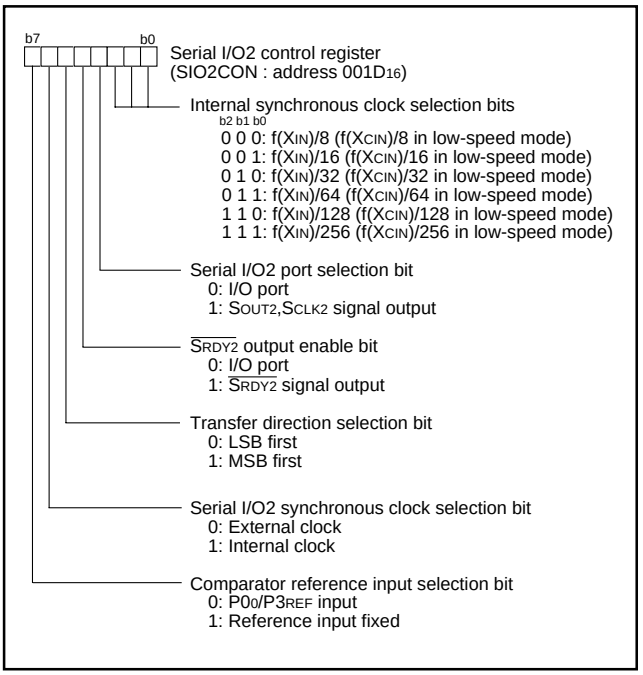


Fig. 26 Structure of serial I/O2 control register

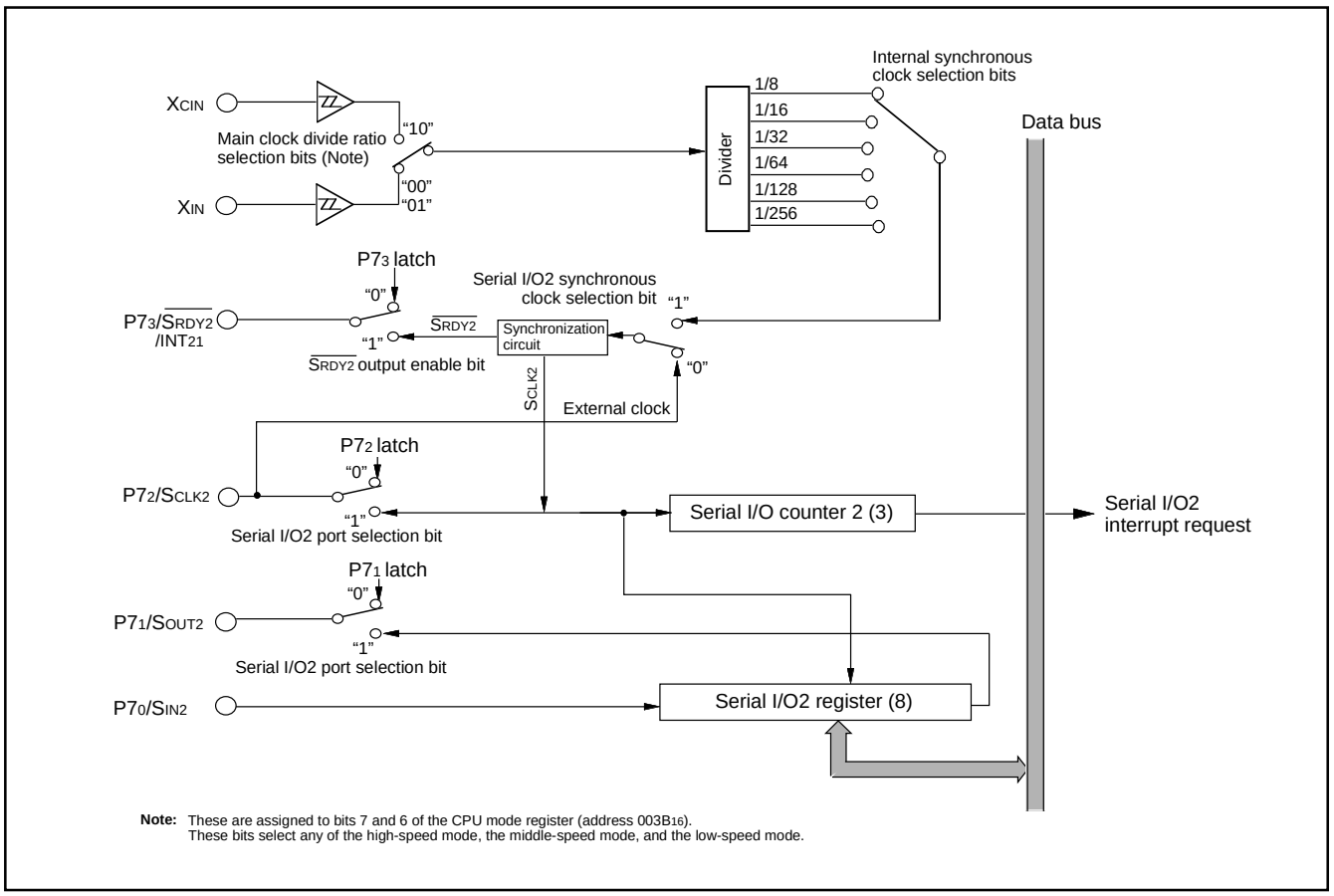
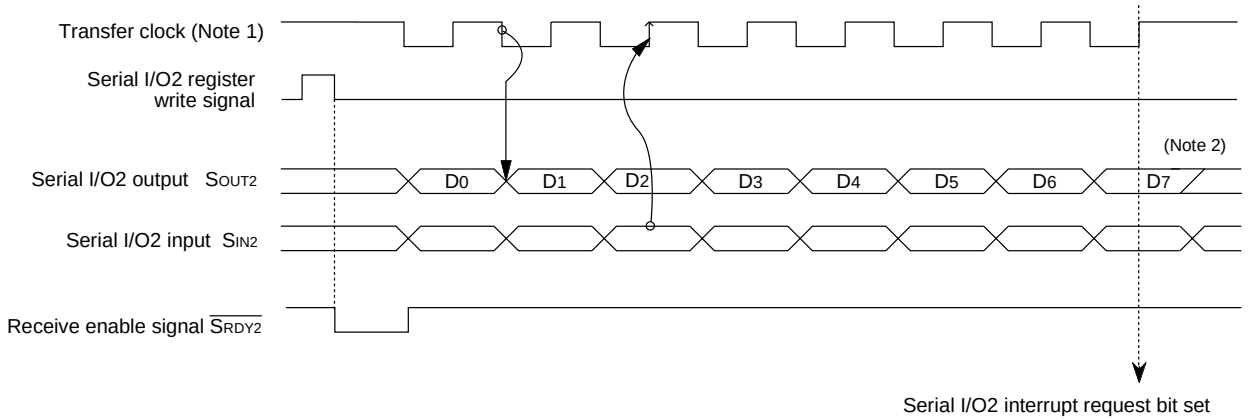


Fig. 27 Block diagram of serial I/O2 function



Notes 1: When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes to high impedance after transfer completion.

Fig. 28 Timing of serial I/O2 function

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

The 3886 group has two PWM output circuits, PWM0 and PWM1, with 14-bit resolution respectively. These can operate independently. When the oscillation frequency XIN is 10 MHz, the minimum resolution bit width is 200 ns and the cycle period is 3276.8 μs. The PWM timing generator supplies a PWM control signal based on a signal that is the frequency of the XIN clock.

The following explanation assumes f(XIN) = 8 MHz.

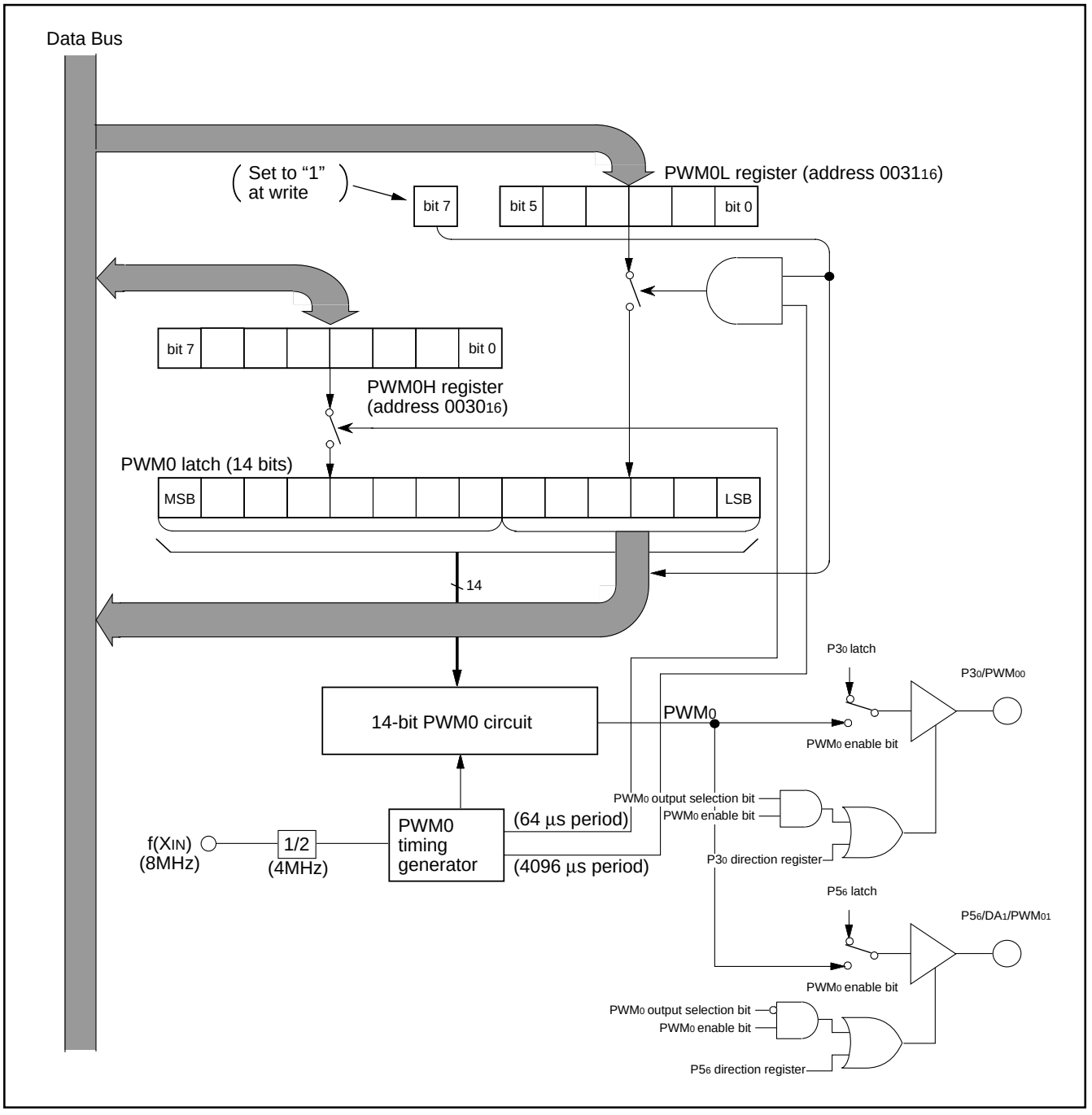


Fig. 29 PWM block diagram (PWM0)

Data Setup (PWM0)

The PWM0 output pin also functions as port $P3_0$ or $P5_6$. The PWM0 output pin is selected from either $P3_0/PWM_{00}$ or $P5_6/PWM_{01}$ by bit 4 of the AD/DA control register (address 0034_{16}).

The PWM0 output becomes enabled state by setting bit 6 of the port control register 1 (address $002E_{16}$). The high-order eight bits of output data are set in the PWM0H register (address 0030_{16}) and the low-order six bits are set in the PWM0L register (address 0031_{16}).

PWM1 is set as the same way.

PWM Operation

The 14-bit PWM data is divided into the low-order six bits and the high-order eight bits in the PWM latch.

The high-order eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256 × τ (64 μs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (250 ns).

"H" or "L" of the bit in the ADD part shown in Figure 30 is added to this "H" duration by the contents of the low-order 6-bit data according to the rule in Table 7.

That is, only in the sub-period tm shown by Table 7 in the PWM cycle period T = 64t, its "H" duration is lengthened to the minimum resolution τ added to the length of other periods.

For example, if the high-order eight bits of the 14-bit data are 03_{16} and the low-order six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4 τ, and its length is 3 τ in all other sub-periods.

Time at the "H" level of each sub-period almost becomes equal, because the time becomes length set in the high-order 8 bits or becomes the value plus τ, and this sub-period t (= 64 μs, approximate 15.6 kHz) becomes cycle period approximately.

Table 7 Relationship between low-order 6 bits of data and period set by the ADD bit

Low-order 6 bits of data (PWML) LSB	Sub-periods tm Lengthened (m=0 to 63)
0 0 0 0 0 0	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m=8, 24, 40, 56
0 0 1 0 0 0	m=4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m=1, 3, 5, 7, ... ,57, 59, 61, 63

Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch at each PWM period (every 4096 μs), and data written to the PWMH register is transferred to the PWM latch at each sub-period (every 64 μs). The signal which is output to the PWM output pin is corresponding to the contents of this latch. When the PWML register is read, the latch contents are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0" and it is not done when bit 7 is "1."

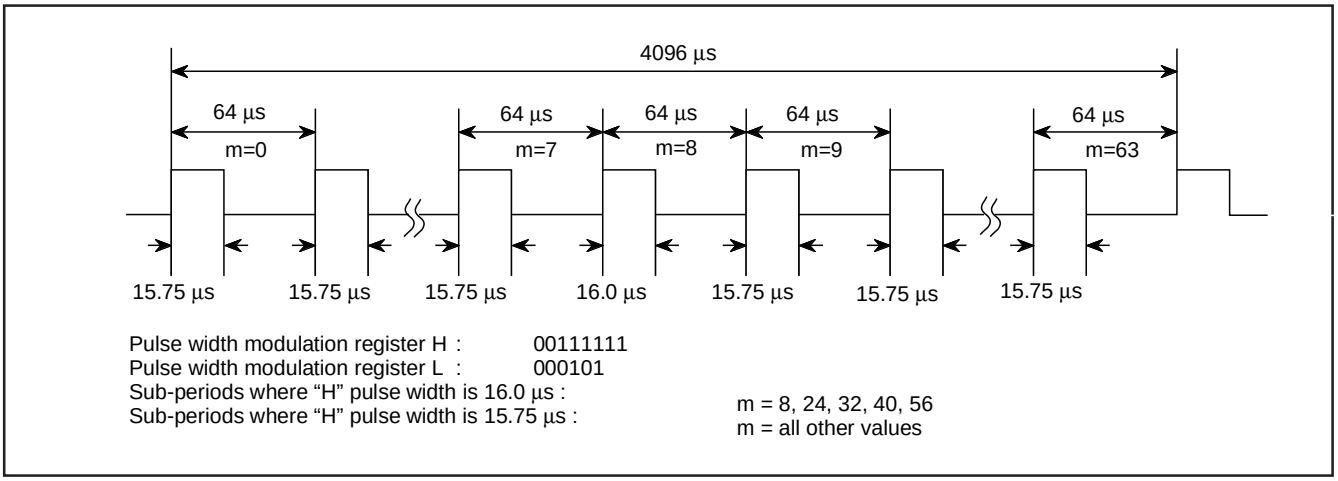


Fig. 30 PWM timing

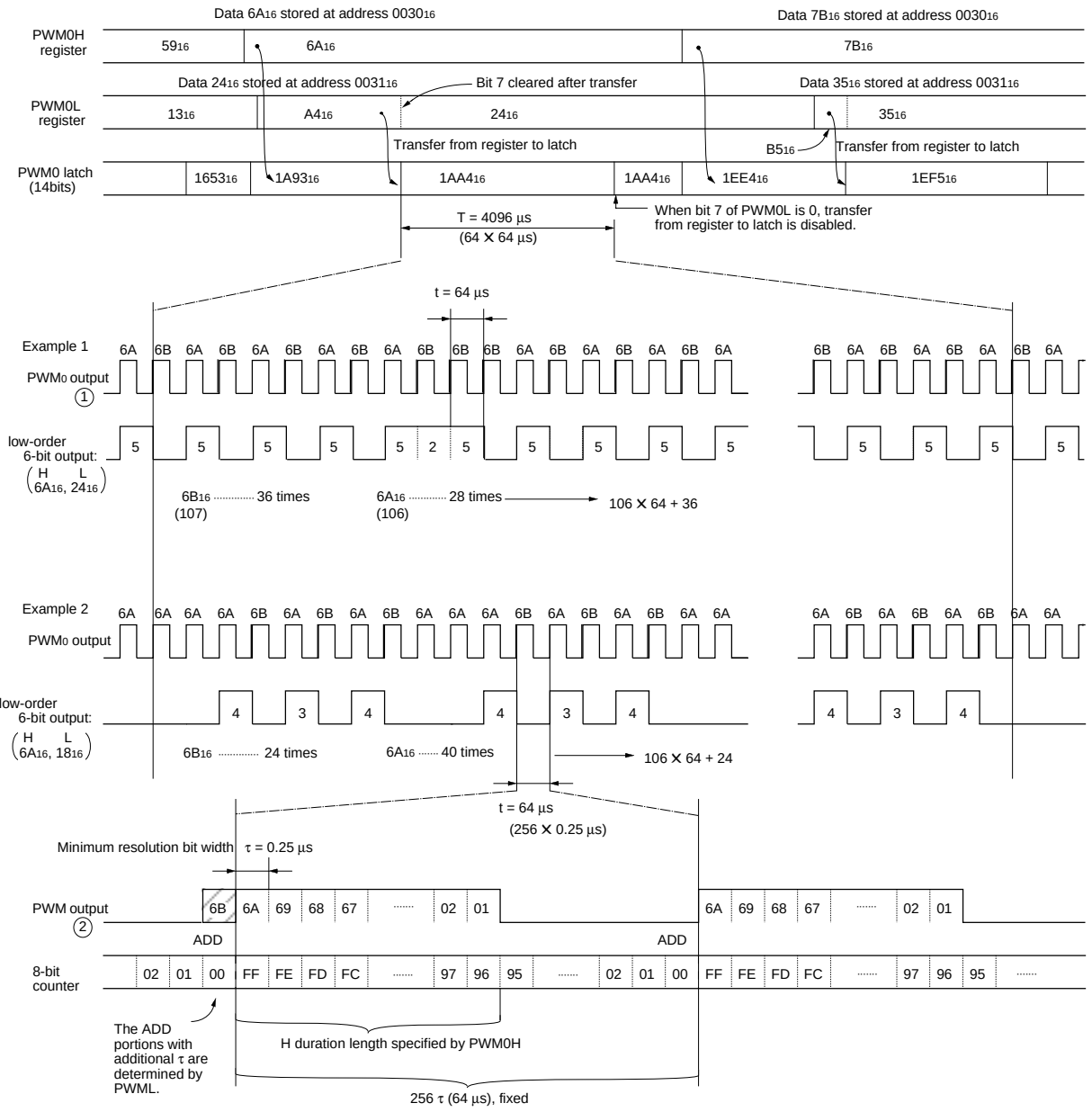


Fig. 31 14-bit PWM timing (PWM0)

BUS INTERFACE

The 3886 group has a 2-byte bus interface function which is almost functionally equal to MELPS8-41 series and the control signal from the host CPU side can operate it (slave mode).

It is possible to connect the 3886 group with the $\overline{RD}$ and $\overline{WR}$ separated CPU bus directly. Figure 34 shows the block diagram of the bus interface function.

The data bus buffer function I/O pins (P4$_2$, P4$_3$, P4$_6$, P4$_7$, P5$_0$–P5$_3$, P8) also function as the normal digital port I/O pins. When bit 0 (data bus buffer enable bit) of the data bus buffer control register (address 002A$_{16}$) is "0," these pins become the normal digital port I/O pins. When it is "1," these bits become the data bus buffer function I/O pins.

The selection of either the single data bus buffer mode, which uses 1 byte: data bus buffer 0 only, or the double data bus buffer mode, which uses 2 bytes: data bus buffer 0 and data bus buffer 1, is performed by bit 1 (data bus buffer function selection bit) of the data bus buffer control register (address 002A$_{16}$). Port P4$_7$ becomes $\overline{S_1}$ input in the double data bus buffer mode. When data is written from the host CPU side, an input buffer full interrupt occurs. When data is read from the host CPU, an output buffer empty interrupt occurs. This microcomputer shares two input buffer full interrupt requests and two output buffer empty interrupt requests as shown in Figure 32, respectively.

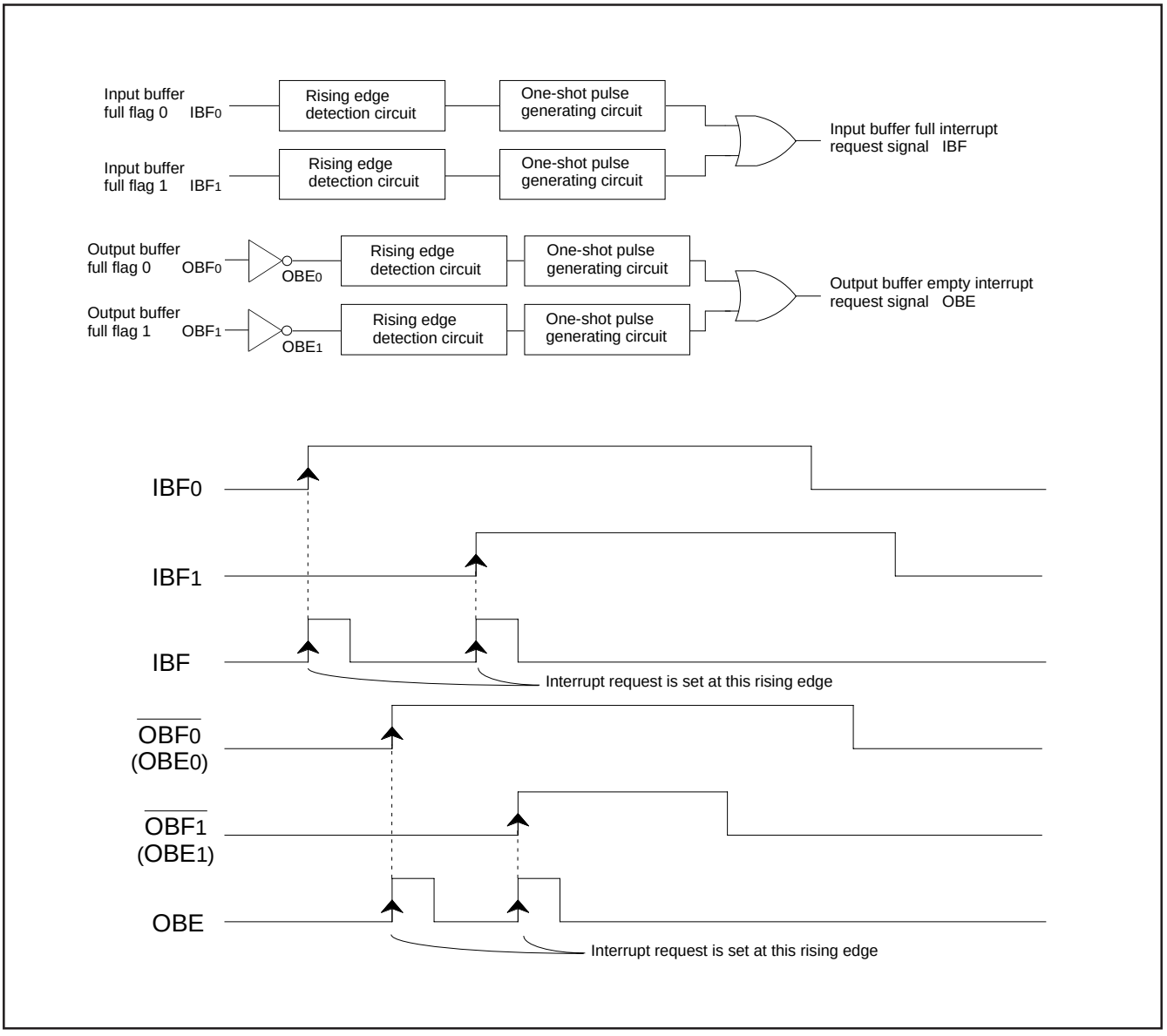


Fig. 32 Interrupt request circuit of data bus buffer

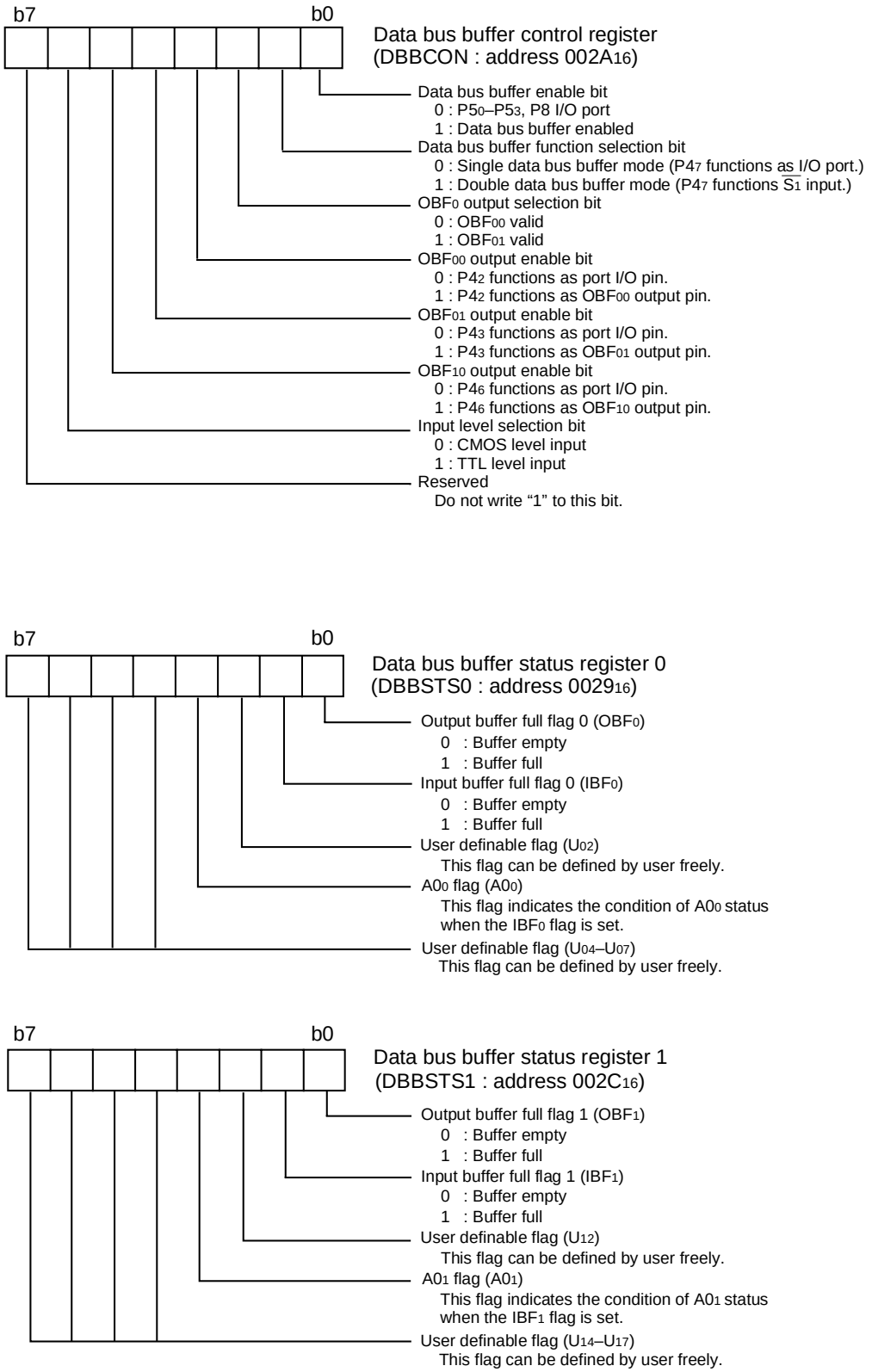


Fig. 33 Structure of bus interface related register

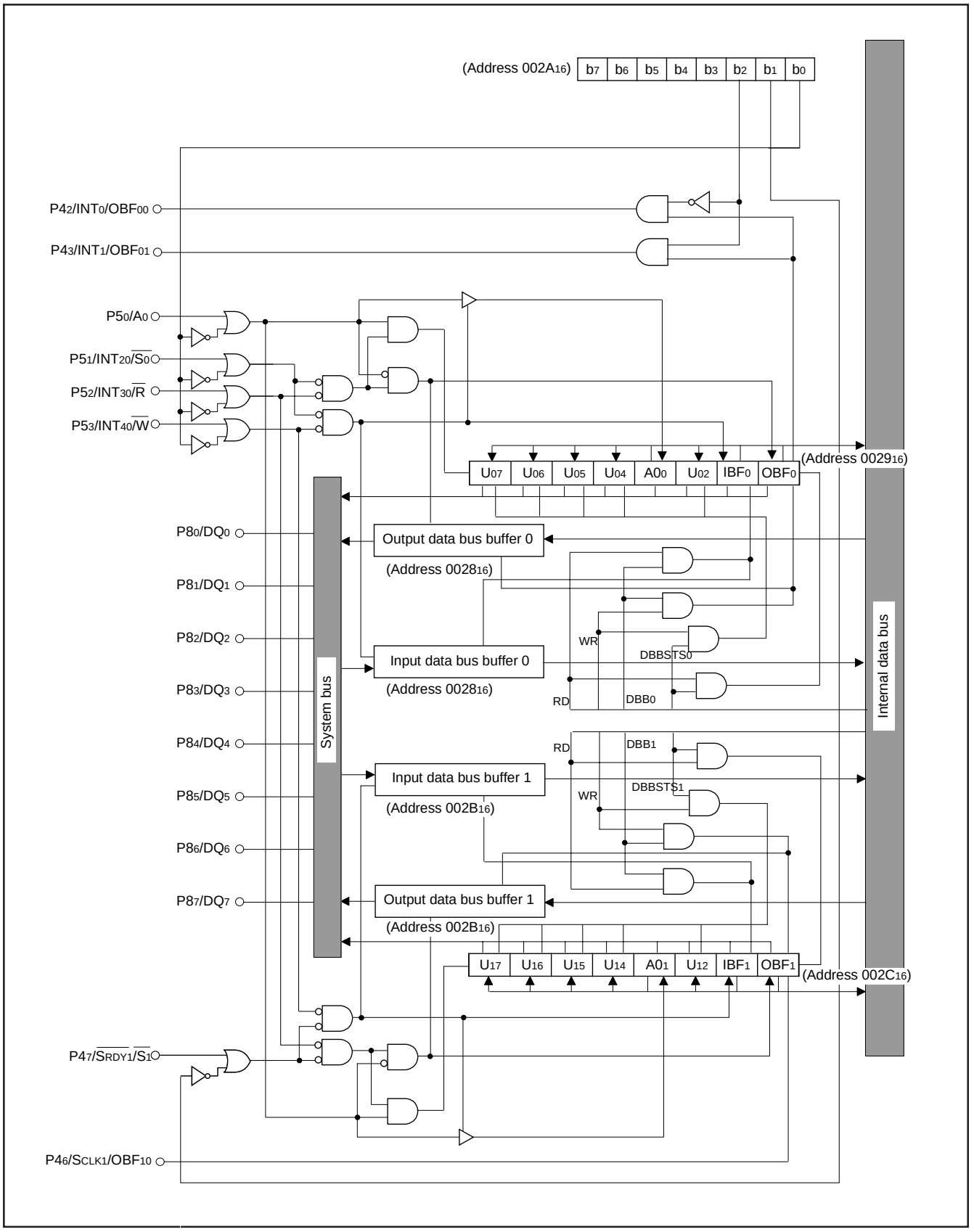


Fig. 34 Bus interface device block diagram

[Data Bus Buffer Status Register 0, 1 (DBBSTS0, DBBSTS1)] 0029$_{16}$, 002C$_{16}$

The data bus buffer status register 0, 1 consist of eight bits.
Bits 0, 1, and 3 are read-only bits and indicate the condition of the data bus buffer. Bits 2, 4, 5, 6, and 7 are user definable flags which can be set by program, and can be read/written. This register can be read from the host CPU when the A_0 pin is set to "H" only.

•Bit 0: Output buffer full flag OBF_0, OBF_1

When writing data to the output data bus buffer, these flags are set to "1". When reading the output data bus buffer from the host CPU, these flags are cleared to "0".

•Bit 1: Input buffer full flag IBF_0, IBF_1

When writing data from the host CPU to the input data bus buffer, these flags are set to "1". When reading the input data bus buffer from the slave CPU side, these flags are cleared to "0".

•Bit 3: A_0 flag $A0_0$, $A0_1$

When writing data from the host CPU to the input data bus buffer, the level of the A_0 pin is latched.

[Input Data Bus Buffer Register 0, 1 (DBBIN0, DBBIN1)] 0028$_{16}$, 002B$_{16}$

Data on the data bus is latched to DBBIN by writing request from the host CPU. Data of DBBIN can be read from the data bus buffer registers (address 0028$_{16}$ or 002B$_{16}$) on SFR.

[Output Data Bus Buffer Register 0, 1 (DBBOUT0, DBBOUT1)] 0028$_{16}$, 002B$_{16}$

When writing data to the data bus buffer registers (address 0028$_{16}$ or 002B$_{16}$) on SFR, data is set to DBBOUT. Data of DBBOUT is output from the host CPU to the data bus by performing the reading request when the A_0 pin is set to "L".

Table 8 Function description of control I/O pins at bus interface function selected

Pin	Name	OBF_{00} output enable bit	OBF_{01} output enable bit	OBF_{10} output enable bit	Input /Output	Functions
$P4_7/\overline{SRDY_1}$ $/\overline{S_1}$	$\overline{S_1}$	–	–	–	Input	Chip select input This is used for selecting the data bus buffer and is selected at “L” level.
$P5_0/A_0$	A_0	–	–	–	Input	Address input This is used for selecting DBBSTS and DBBOUT when the host CPU is read. This is used for distinguishing command from data when writing to the host CPU.
$P5_1/\overline{INT_{20}}$ $/\overline{S_0}$	$\overline{S_0}$	–	–	–	Input	Chip select input This is used for selecting the data bus buffer and is selected at “L” level.
$P5_2/\overline{INT_{30}}$ $/\overline{R}$	$\overline{R}$	–	–	–	Input	This is a timing signal for reading data from the data bus buffer to the host CPU.
$P5_3/\overline{INT_{40}}$ $/\overline{W}$	$\overline{W}$	–	–	–	Output	This is a timing signal for writing data to the data bus buffer by the host CPU.
$P4_2/INT_0$ $/OBF_{00}$	OBF00	1	0	0	Output	Status output signal OBF_{00} signal is output.
$P4_3/INT_1$ $/OBF_{01}$	OBF01	0	1	0	Output	Status output signal OBF_{01} signal is output.
$P4_6/SCLK_1$ $/OBF_{10}$	OBF10	0	0	1	Output	Status output signal OBF_{10} signal is output.

MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 35 shows a block diagram of the multi-master I²C-BUS interface and Table 9 lists the multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register, the I²C start/stop condition control register and other control circuits.

When using the multi-master I²C-BUS interface, set 1 MHz or more to ϕ.

Table 9 Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ= 4 MHz) 20.2 kHz to 312.5 kHz (at ϕ = 5 MHz)

System clock ϕ = f(XIN)/2 (high-speed mode)
ϕ = f(XIN)/8 (middle-speed mode)

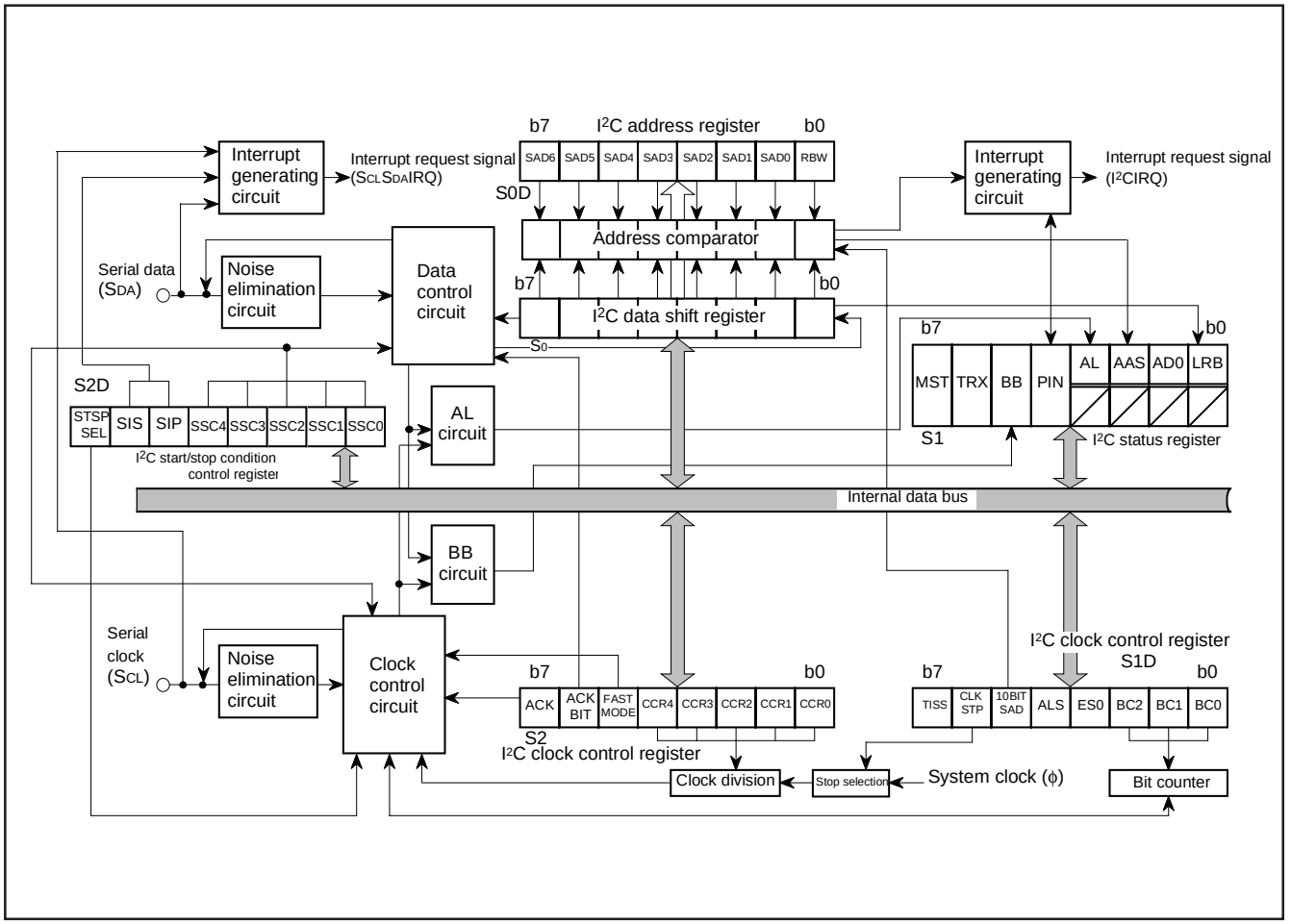


Fig. 35 Block diagram of multi-master I²C-BUS interface

∗ : Purchase of MITSUBISHI ELECTRIC CORPORATIONS I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

[I²C Data Shift Register (S0)] 0012₁₆

The I²C data shift register (S0 : address 0012₁₆) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 cycles of ϕ are required from the rising of the SCL clock until input to this register.

The I²C data shift register is in a write enable status only when the I²C-BUS interface enable bit (ES0 bit : bit 3 of address 15₁₆) of the I²C control register is "1." The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (address 0014₁₆) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

[I²C Address Register (S0D)] 0013₁₆

The I²C address register (address 0013₁₆) consists of a 7-bit slave address and a read/$\overline{\text{write}}$ bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/$\overline{\text{write}}$ bit (RBW)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I²C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

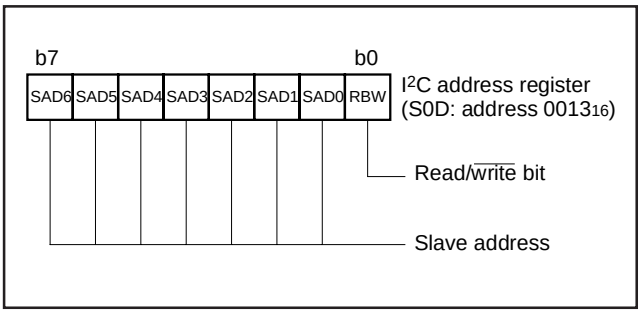


Fig. 36 Structure of I²C address register

[I²C Clock Control Register (S2)] 0016₁₆

The I²C clock control register (address 0016₁₆) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 10.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is selected. When the bit is set to "1," the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C bus standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) and high-speed mode (2 division main clock).

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is selected and SDA goes to "L" at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is selected. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address agree with the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made "L" (ACK is returned). If there is a disagreement between the slave address and the address data, the SDA is automatically made "H" (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to "0," the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

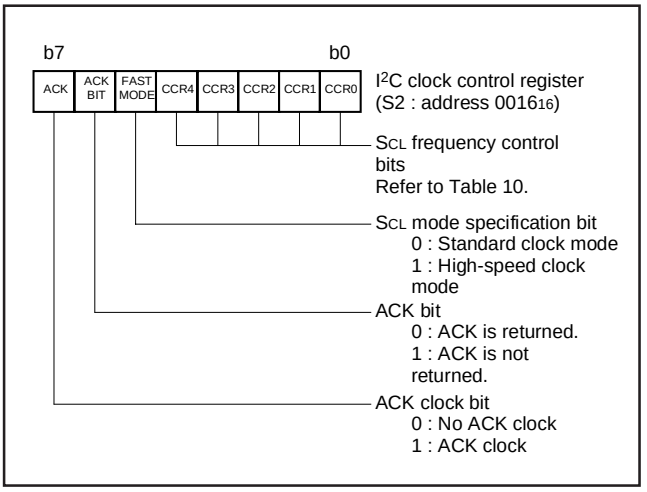


Fig. 37 Structure of I²C clock control register

Table 10 Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at ϕ = 4 MHz, unit : kHz) **(Note 1)**	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	– **(Note 2)**	333
0	0	1	0	0	– **(Note 2)**	250
0	0	1	0	1	100	400 **(Note 3)**
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value **(Note 3)**	1000/CCR value **(Note 3)**
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes 1: Duty of SCL clock output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at ϕ = 4 MHz). "H" duration of the clock fluctuates from –4 to +2 cycles of ϕ in the standard clock mode, and fluctuates from –2 to +2 cycles of ϕ in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because "L" duration is extended instead of "H" duration reduction.
These are value when SCL clock synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at ϕ = 4 MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:
ϕ/(8 × CCR value) Standard clock mode
ϕ/(4 × CCR value) High-speed clock mode (CCR value ≠ 5)
ϕ/(2 × CCR value) High-speed clock mode (CCR value = 5)
Do not set 0 to 2 as CCR value regardless of ϕ frequency.
Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

[I²C Control Register (S1D)] 0015₁₆

The I²C control register (address 0015₁₆) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I²C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK bit (bit 7 of address 0016₁₆)) have been transferred, and BC0 to BC2 are returned to "000₂".

Also when a START condition is received, these bits become "000₂" and the address data is always transmitted and received in 8 bits.

•Bit 3: I²C interface enable bit (ES0)

This bit enables to use the multi-master I²C BUS interface. When this bit is set to "0," the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.

When ES0 = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (which are bits of the I²C status register at address 0014₁₆).
- Writing data to the I²C data shift register (address 0012₁₆) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "(5) I²C Status Register," bit 1) is received, transfer processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 0013₁₆) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, and all the bits of the I²C address register are compared with address data.

•Bit 6: System clock stop selection bit (CLKSTP)

When executing the WIT or STP instruction, this bit selects the condition of system clock provided to the multi-master I²C-BUS interface. When this bit is set to "0," system clock and operation of the multi-master I²C-BUS interface stop by executing the WIT or STP instruction.

When this bit is set to "1," system clock and operation of the multi-master I²C-BUS interface do not stop even when the WIT instruction is executed.

When the system clock stop selection bit is "1," do not execute the STP instruction.

•Bit 7: I²C-BUS interface pin input level selection bit

This bit selects the input level of the SCL and SDA pins of the multi-master I²C-BUS interface.

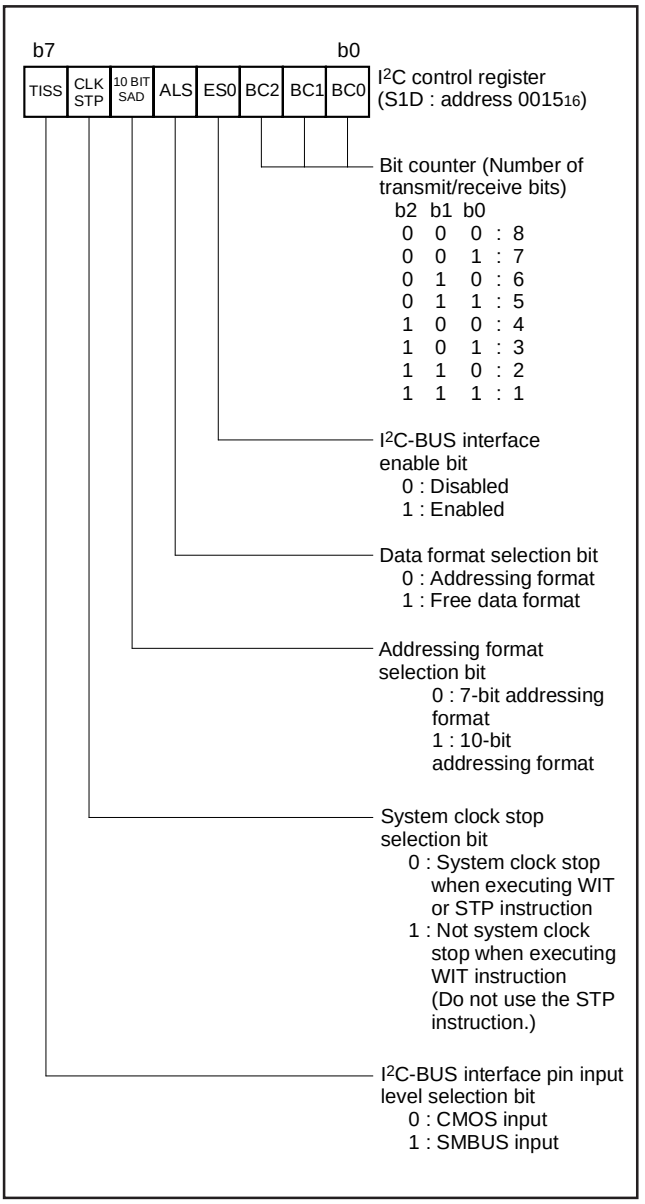


Fig. 38 Structure of I²C control register

[I²C Status Register (S1)] 0014₁₆

The I²C status register (address 0014₁₆) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "0000₂" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 0012₁₆).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0," this bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

*General call: The master transmits the general call address "00₁₆" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is "0".

① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (address 0013₁₆).
- A general call is received.

② In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
- When the address data is compared with the I²C address register (8 bits consisting of slave address and RBW bit), the first bytes agree.

③ This bit is set to "0" by executing a write instruction to the I²C data shift register (address 0012₁₆) when ES0 is set to "1" or reset.

•Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

*Arbitration lost :The status in which communication as a master is disabled.

•Bit 4: I²C-BUS interface interrupt request bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to "0." At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 40 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (address 0012₁₆). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)
- When the ES0 bit is "0"
- At reset
- When writing "1" to the PIN bit by software

The conditions in which the PIN bit is set to "0" are shown below:
- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to "1" by detecting the start condition, and is set to "0" by detecting the stop condition. The condition of these detecting is set by the start/stop condition setting bits (SSC4–SSC0) of the I²C start/stop condition control register (address 0017₁₆). When the ES0 bit (bit 3) of the I²C control register (address 0015₁₆) is "0" or reset, the BB flag is set to "0."

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

•Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to "1" by hardware when all the following conditions are satisfied:

- When ALS is "0"
- In the slave reception mode or the slave transmission mode
- When the R/$\overline{W}$ bit reception is "1"

This bit is set to "0" in one of the following conditions:

- When arbitration lost is detected.
- When a STOP condition is detected.
- When writing "1" to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

•Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transfer when arbitration lost is detected
- When a STOP condition is detected.
- Writing "1" to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- At reset

Note: START condition duplication preventing function
The MST, TRX, and BB bits is set to "1" at the same time after confirming that the BB flag is "0" in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to "1" immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

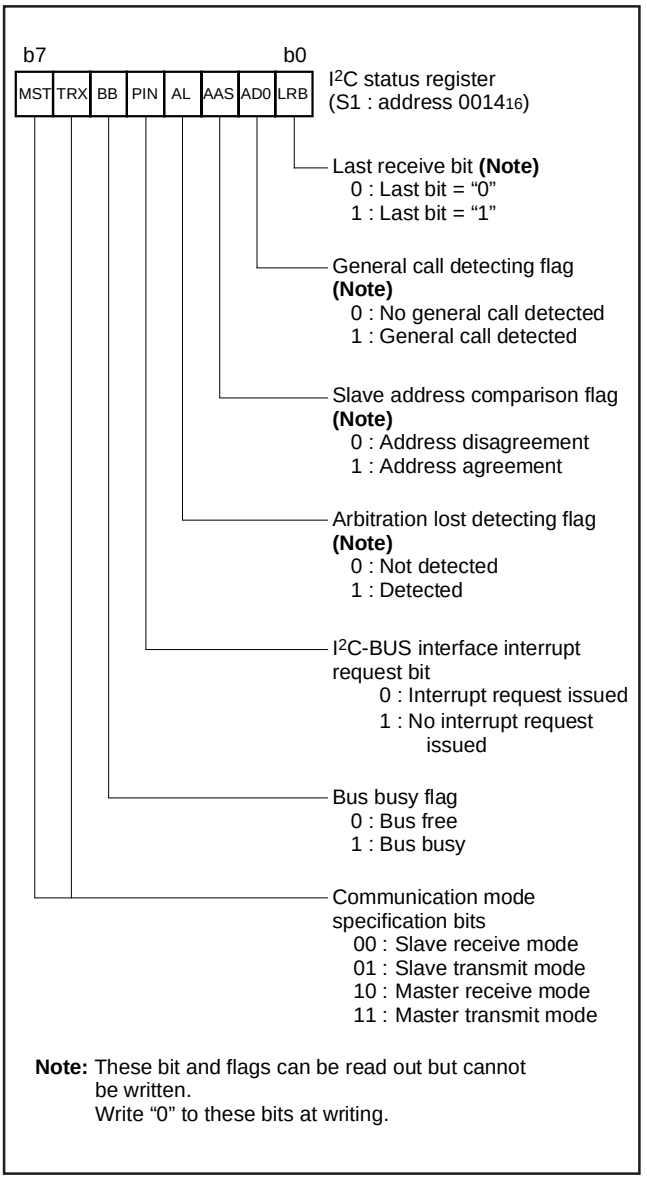


Fig. 39 Structure of I2C status register

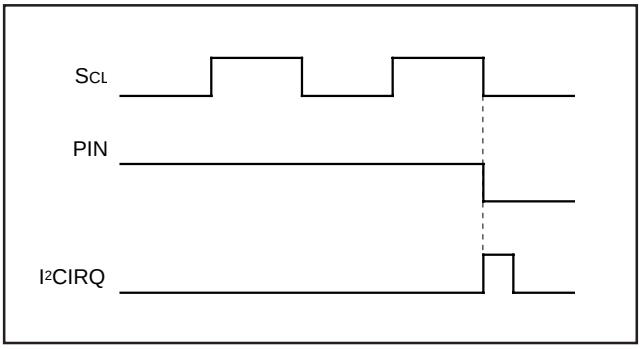


Fig. 40 Interrupt request signal generating timing

START Condition Generating Method

When writing "1" to the MST, TRX, and BB bits of the I²C status register (address 0014₁₆) at the same time after writing the slave address to the I²C data shift register (address 0012₁₆) with the condition in which the ES0 bit of the I²C control register (address 0015₁₆) and the BB flag are "0", a START condition occurs. After that, the bit counter becomes "000₂" and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 41, the START condition generating timing diagram, and Table 11, the START condition generating timing table.

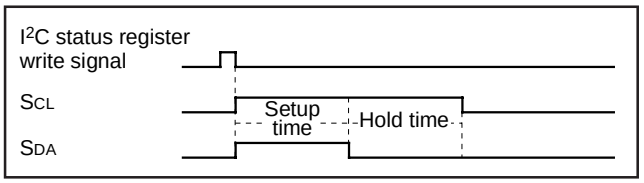


Fig. 41 START condition generating timing diagram

Table 11 START condition generating timing table

Item	START/STOP condition generating selection bit	Standard clock mode	High-speed clock mode
Setup time	"0"	5.0 µs (20 cycles)	2.5 µs (10 cycles)
	"1"	13.0 µs (52 cycles)	6.5 µs (26 cycles)
Hold time	"0"	5.0 µs (20 cycles)	2.5 µs (10 cycles)
	"1"	13.0 µs (52 cycles)	6.5 µs (26 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (address 0015₁₆) is "1," write "1" to the MST and TRX bits, and write "0" to the BB bit of the I²C status register (address 0014₁₆) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 42, the STOP condition generating timing diagram, and Table 12, the STOP condition generating timing table.

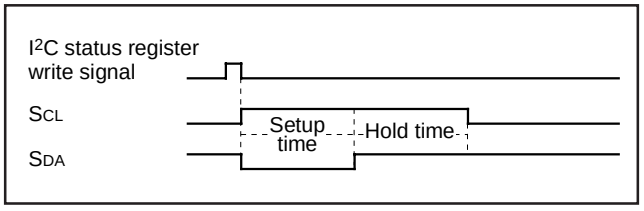


Fig. 42 STOP condition generating timing diagram

Table 12 STOP condition generating timing table

Item	START/STOP condition generating selection bit	Standard clock mode	High-speed clock mode
Setup time	"0"	5.5 µs (22 cycles)	3.0 µs (12 cycles)
	"1"	13.5 µs (54 cycles)	7.0 µs (28 cycles)
Hold time	"0"	5.5 µs (22 cycles)	3.0 µs (12 cycles)
	"1"	13.5 µs (54 cycles)	7.0 µs (28 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 43, 44, and Table 13. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 13).

The BB flag is set to "1" by detecting the START condition and is reset to "0" by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 13, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "I²CIRQ" occurs to the CPU.

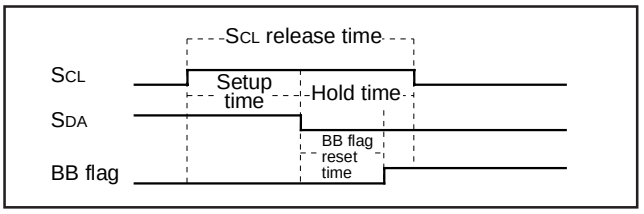


Fig. 43 START condition detecting timing diagram

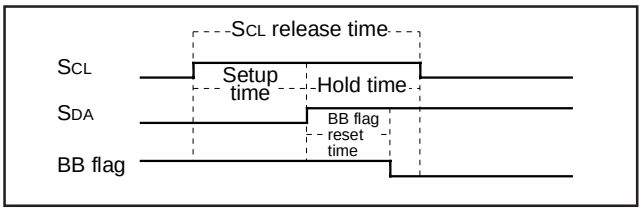


Fig. 44 STOP condition detecting timing diagram

Table 13 START condition/STOP condition detecting conditions

	Standard clock mode	High-speed clock mode
SCL release time	SSC value + 1 cycle (6.25 µs)	4 cycles (1.0 µs)
Setup time	$\frac{\text{SSC value}}{2}$ + 1 cycle < 4.0 µs (3.25 µs)	2 cycles (1.0 µs)
Hold time	$\frac{\text{SSC value}}{2}$ cycle < 4.0 µs (3.0 µs)	2 cycles (0.5 µs)
BB flag set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles (3.375 µs)	3.5 cycles (0.875 µs)

Note: Unit : Cycle number of system clock ϕ
SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set "0" or an odd number to SSC value. The value in parentheses is an example when the I²C START/STOP condition control register is set to "18₁₆" at ϕ = 4 MHz.

[I²C START/STOP Condition Control Register (S2D)] 0017₁₆

The I²C START/STOP condition control register (address 0017₁₆) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bit (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency f(XIN) because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 13.

Do not set "00000₂" or an odd number to the START/STOP condition set bit (SSC4 to SSC0).

Refer to Table 14, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

•Bit 7: START/STOP condition generating selection bit (STSPSEL)

Setup/Hold time when the START/STOP condition is generated can be selected.

Cycle number of system clock becomes standard for setup/hold time. Additionally, setup/hold time is different between the START condition and the STP condition. (Refer to Tables 11 and 12.) Set "1" to this bit when the system clock frequency is 4 MHz or more.

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

① 7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 0015₁₆) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 0013₁₆). At the time of this comparison, address comparison of the RBW bit of the I²C address register (address 0013₁₆) is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 46, (1) and (2).

② 10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 0015₁₆) to "1." An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I²C address register (address 0013₁₆). At the time of this comparison, an address comparison between the RBW bit of the I²C address register (address 0013₁₆) and the R/W bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RBW bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit.

When the first-byte address data agree with the slave address, the AAS bit of the I²C status register (address 0014₁₆) is set to "1." After the second-byte address data is stored into the I²C data shift register (address 0012₁₆), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RBW bit of the I²C address register (address 0013₁₆) to "1" by software. This processing can make the 7-bit slave address and R/$\overline{W}$ data agree, which are received after a RESTART condition is detected, with the value of the I²C address register (address 0013₁₆). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 46, (3) and (4).

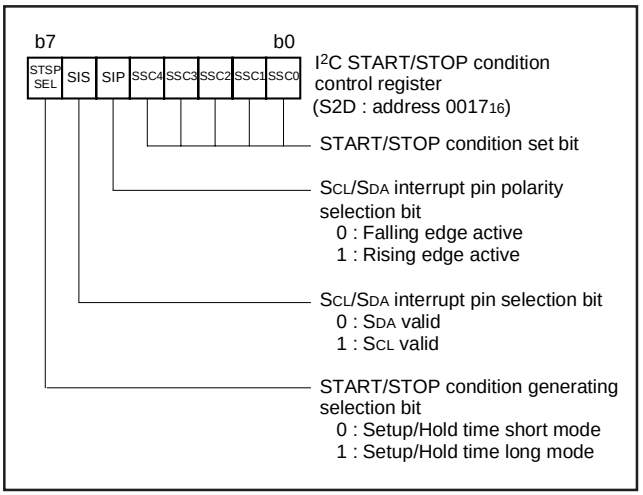


Fig. 45 Structure of I²C START/STOP condition control register

Table 14 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

Oscillation frequency f(XIN) (MHz)	Main clock divide ratio	System clock ϕ (MHz)	START/STOP condition control register	SCL release time (μs)	Setup time (μs)	Hold time (μs)
10	2	5	XXX11110	6.2 μs (31 cycles)	3.2 μs (16 cycles)	3.0 μs (15 cycles)
8	2	4	XXX11010	6.75 μs (27 cycles)	3.5 μs (14 cycles)	3.25 μs (13 cycles)
			XXX11000	6.25 μs (25 cycles)	3.25 μs (13 cycles)	3.0 μs (12 cycles)
8	8	1	XXX00100	5.0 μs (5 cycles)	3.0 μs (3 cycles)	2.0 μs (2 cycles)
4	2	2	XXX01100	6.5 μs (13 cycles)	3.5 μs (7 cycles)	3.0 μs (6 cycles)
			XXX01010	5.5 μs (11 cycles)	3.0 μs (6 cycles)	2.5 μs (5 cycles)
2	2	1	XXX00100	5.0 μs (5 cycles)	3.0 μs (3 cycles)	2.0 μs (2 cycles)

Note: Do not set "00000₂" or an odd number to the START/STOP condition set bit (SSC4 to SSC0).

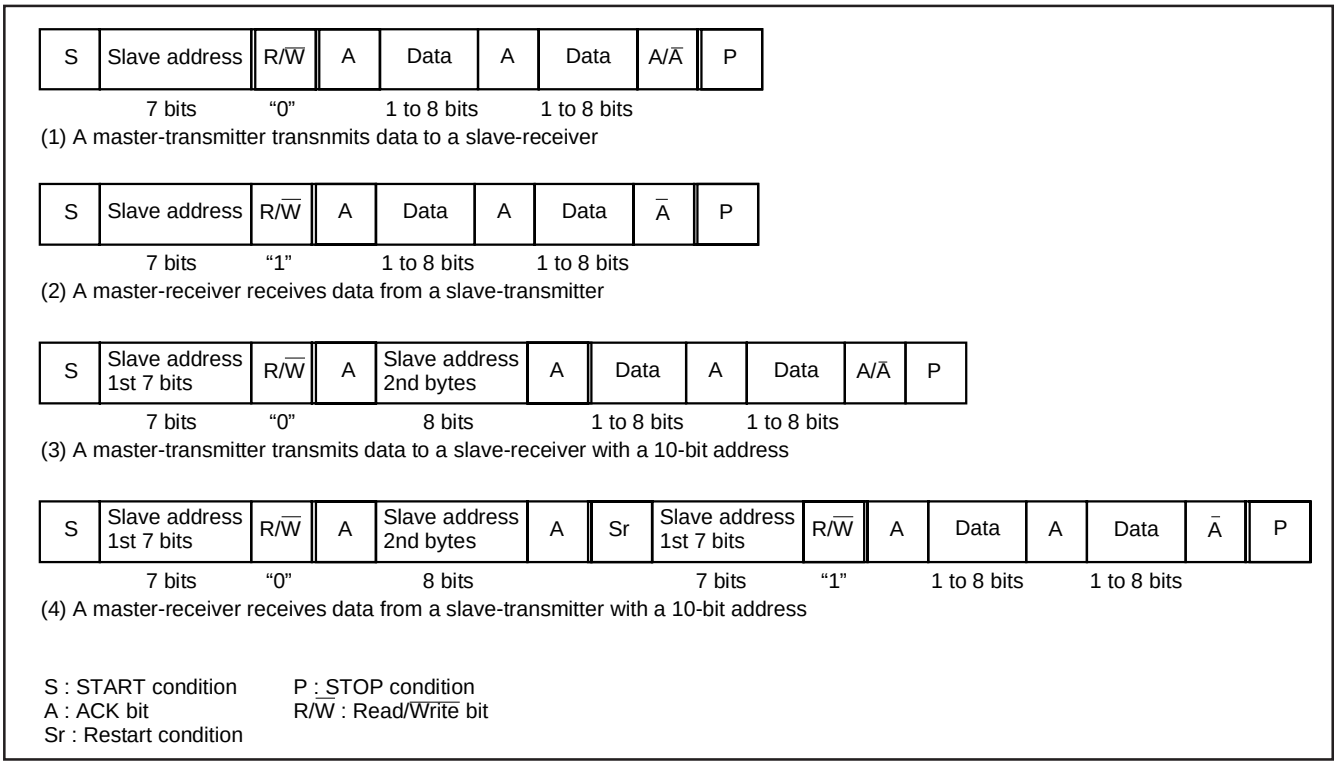


Fig. 46 Address data communication format

Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address 0013_{16}) and "0" into the RBW bit.
② Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (address 0016_{16}).
③ Set "00_{16}" in the I^2C status register (address 0014_{16}) so that transmission/reception mode can become initializing condition.
④ Set a communication enable status by setting "08_{16}" in the I^2C control register (address 0015_{16}).
⑤ Confirm the bus free condition by the BB flag of the I^2C status register (address 0014_{16}).
⑥ Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address 0012_{16}) and set "0" in the least significant bit.
⑦ Set "$F0_{16}$" in the I^2C status register (address 0014_{16}) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occur.
⑧ Set transmit data in the I^2C data shift register (address 0012_{16}). At this time, an SCL and an ACK clock automatically occur.
⑨ When transmitting control data of more than 1 byte, repeat step ⑧.
⑩ Set "$D0_{16}$" in the I^2C status register (address 0014_{16}) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address 0013_{16}) and "0" in the RBW bit.
② Set the no ACK clock mode and SCL = 400 kHz by setting "25_{16}" in the I^2C clock control register (address 0016_{16}).
③ Set "00_{16}" in the I^2C status register (address 0014_{16}) so that transmission/reception mode can become initializing condition.
④ Set a communication enable status by setting "08_{16}" in the I^2C control register (address 0015_{16}).
⑤ When a START condition is received, an address comparison is performed.
⑥ •When all transmitted addresses are "0" (general call):
AD0 of the I^2C status register (address 0014_{16}) is set to "1" and an interrupt request signal occurs.
• When the transmitted addresses agree with the address set in ①:
ASS of the I^2C status register (address 0014_{16}) is set to "1" and an interrupt request signal occurs.
• In the cases other than the above AD0 and AAS of the I^2C status register (address 0014_{16}) are set to "0" and no interrupt request signal occurs.
⑦ Set dummy data in the I^2C data shift register (address 0012_{16}).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

■Precautions when using multi-master I^2C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I^2C-BUS interface are described below.

- I^2C data shift register (S0: address 0012_{16})
  When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I^2C address register (S0D: address 0013_{16})
  When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RBW) at the above timing.
- I^2C status register (S1: address 0014_{16})
  Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I^2C control register (S1D: address 0015_{16})
  When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I^2C clock control register (S2: address 0016_{16})
  The read-modify-write instruction can be executed for this register.
- I^2C START/STOP condition control register (S2D: address 0017_{16})
  The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 5.

```
      ⋮
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  BBS 5, S1, BUSBUSY     (BB flag confirming and branch process)
BUSFREE:
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of START condition generating)
  CLI                    (Interrupt enabled)
      ⋮
BUSBUSY:
  CLI                    (Interrupt enabled)
      ⋮
```

2. Use “Branch on Bit Set” of “BBS 5, $0014, –” for the BB flag confirming and branch process.
3. Use “STA $12, STX $12” or “STY $12” of the zero page addressing instruction for writing the slave address value to the I^2C data shift register.
4. Execute the branch instruction of above 2 and the store instruction of above 3 continuously shown the above procedure example.
5. Disable interrupts during the following three process steps:
   • BB flag confirming
   • Writing of slave address value
   • Trigger of START condition generating

   When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

This cannot be applied when the external memory is used and the bus cycle is extended by $\overline{\text{ONW}}$ function.

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 4.)
   Execute the following procedure when the PIN bit is “0.”

```
      ⋮
  LDM #$00, S1           (Select slave receive mode)
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of RESTART condition generating)
  CLI                    (Interrupt enabled)
      ⋮
```

2. Select the slave receive mode when the PIN bit is “0.” Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.
   The TRX bit becomes “0” and the SDA pin is released.
3. The SCL pin is released by writing the slave address value to the I^2C data shift register.
4. Disable interrupts during the following two process steps:
   • Writing of slave address value
   • Trigger of RESTART condition generating

(4) Writing to I^2C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1.” It is because it may become the same as above.

(5) Process of after STOP condition generating

Do not write data in the I^2C data shift register S0 and the I^2C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

(6) STOP condition input at 7th clock pulse

In the slave mode, the STOP condition is input at the 7th clock pulse while receiving a slave address or data. As the clock pulse is continuously input, the SDA line may be held at LOW even if flag BB is set to “0” (only for M38867M8A and M38867E8).

Countermeasure:

Write dummy data to the I^2C shift register or reset the ES0 bit in the S1D register (ES0 = “L” → ES0 = “H”) during a stop condition interrupt routine with flag PIN = “1”.

Note: Do not use the read-modify-write instruction at this time. Furthermore, when the ES0 bit is set to “0”, it becomes a general-purpose port; so that the port must be set to input mode or “H”.

(7) ES0 bit switch

In standard clock mode when SSC = “00010_2” or in high-speed clock mode, flag BB may switch to “1” if ES0 bit is set to “1” when SDA is “L”.

Countermeasure:

Set ES0 to “1” when SDA is “H”.

A-D CONVERTER
[A-D Conversion Register 1,2 (AD1, AD2)] 003516, 003816

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Bit 7 of the A-D conversion register 2 is the conversion mode selection bit. When this bit is set to "0," the A-D converter becomes the 10-bit A-D mode. When this bit is set to "1," that becomes the 8-bit A-D mode. The conversion result of the 8-bit A-D mode is stored in the A-D conversion register 1. As for 10-bit A-D mode, 10-bit reading or 8-bit reading can be performed by selecting the reading procedure of the A-D conversion register 1, 2 after A-D conversion is completed (in Figure 48).

The A-D conversion register 1 performs the 8-bit reading inclined to MSB after reset, the A-D conversion is started, or reading of the A-D converter register 1 is generated; and the register becomes the 8-bit reading inclined to LSB after the A-D converter register 2 is generated.

[AD/DA Control Register (ADCON)] 003416

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024, and outputs the divided voltages in the 10-bit A-D mode (256 division in 8-bit A-D mode).

The A-D converter successively compares the comparison voltage Vref in each mode, dividing the VREF (see below), with the input voltage.

- 10-bit A-D mode (10-bit reading)

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0–1023)$$

- 10-bit A-D mode (8-bit reading)

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0–255)$$

- 8-bit A-D mode

$$V_{ref} = \frac{V_{REF}}{256} \times (n–0.5) \quad (n = 1–255)$$
$$= 0 \quad (n = 0)$$

Channel Selector

The channel selector selects one of ports P60/AN0 to P67/AN7, and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the A-D conversion registers 1, 2. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion.

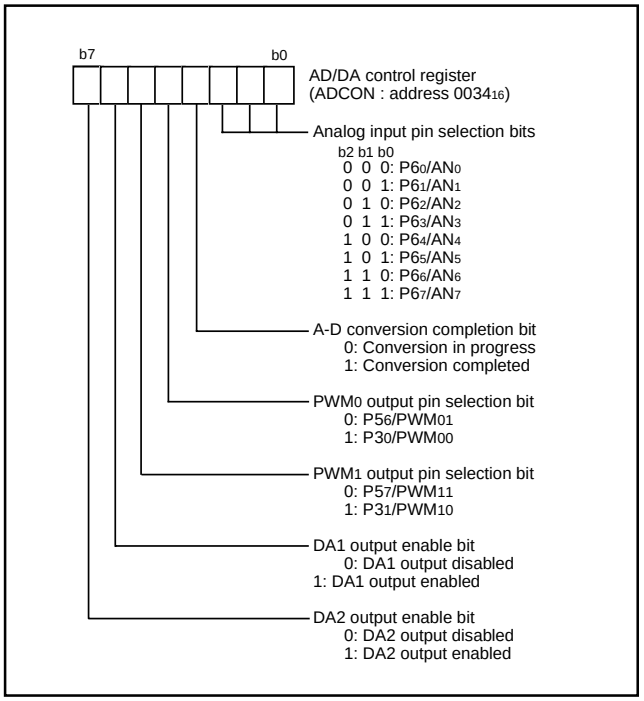


Fig. 47 Structure of AD/DA control register

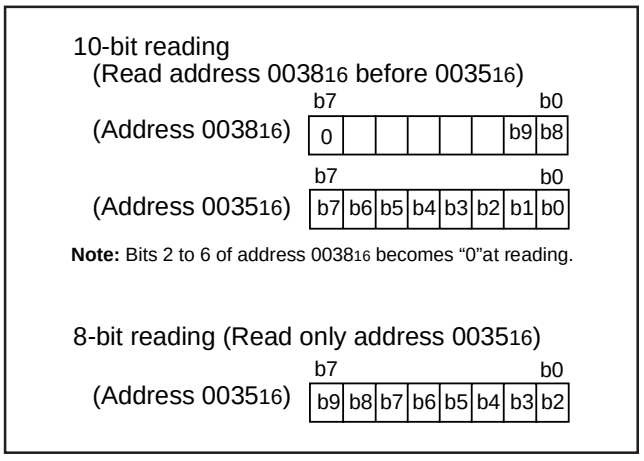


Fig. 48 Structure of 10-bit A-D mode reading

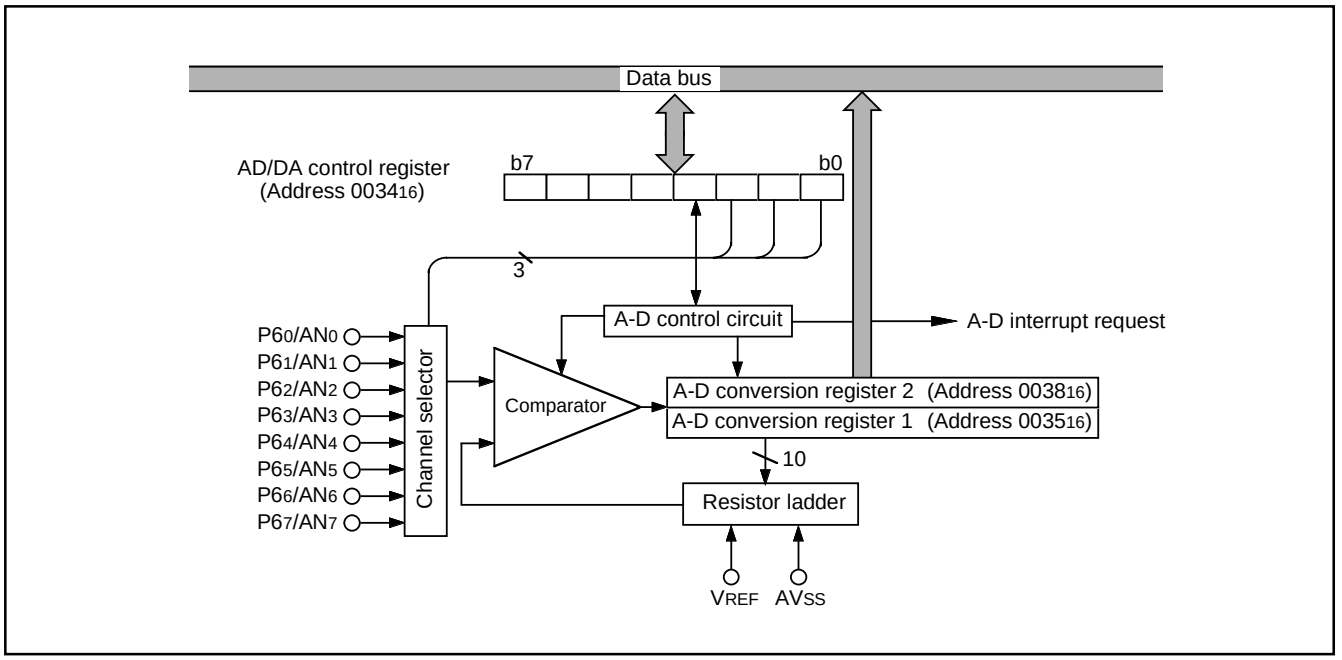


Fig. 49 Block diagram of A-D converter

D-A CONVERTER

The 3886 group has two internal D-A converters (DA_1 and DA_2) with 8-bit resolution.

The D-A converter is performed by setting the value in each D-A conversion register. The result of D-A conversion is output from the DA_1 or DA_2 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit ($P5_6/DA_1/PWM_{01}$ or $P5_7/DA_2/PWM_{11}$) must be set to "0" (input status).

The output analog voltage V is determined by the value n (decimal notation) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n = 0 to 255)

Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to "00_{16}", the DA output enable bits are cleared to "0", and the $P5_6/DA_1/PWM_{01}$ and $P5_7/DA_2/PWM_{11}$ pins become high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

Set V_{CC} to 4.0 V or more when using the D-A converter.

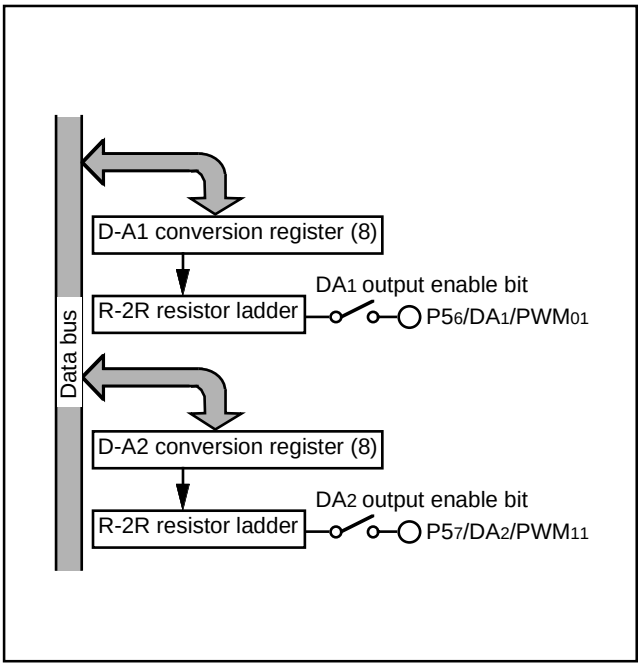


Fig. 50 Block diagram of D-A converter

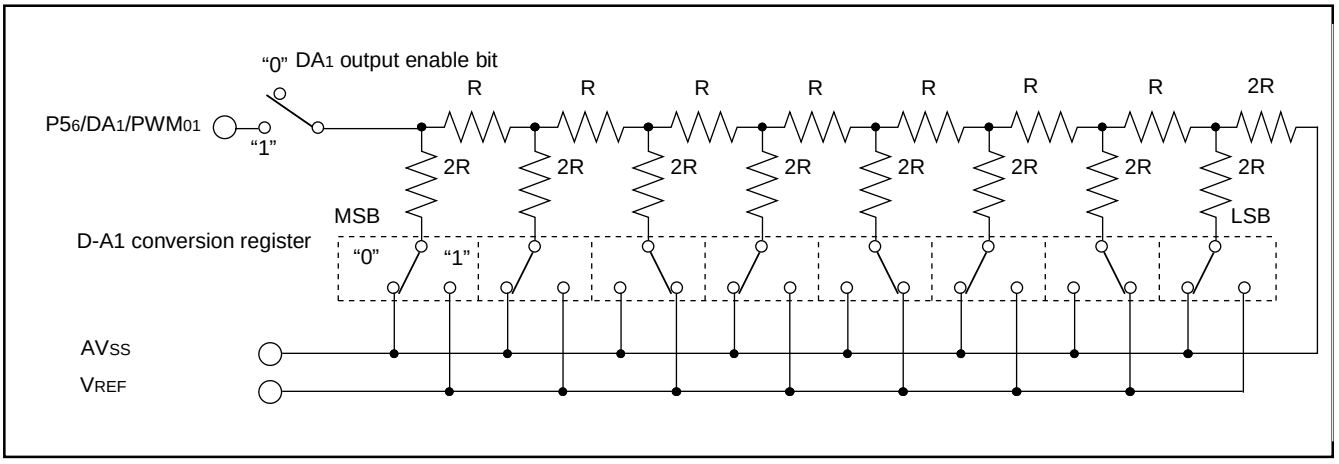


Fig. 51 Equivalent connection circuit of D-A converter (DA1)

COMPARATOR CIRCUIT
Comparator Configuration

The comparator circuit consists of resistors, comparators, a comparator control circuit, the comparator reference input selection bit (bit 7 of address $001D_{16}$), a comparator data register (address $002D_{16}$), the comparator reference power source input pin ($P0_0$/$P3_{REF}$) and analog signal input pins ($P3_0$–$P3_7$). The analog input pin ($P3_0$–$P3_7$) also functions as an ordinary digital port.

Comparator Operation

To activate the comparator, first set port P3 to input mode by setting the corresponding direction register (address 0007_{16}) to "0" to use port P3 as an analog voltage input pin. The internal fixed analog voltage (V_{CC} × 29/32) can be generated by setting "1" to the comparator reference input selection bit (bit 7) of the serial I/O2 control register (address $001D_{16}$). (The internal fixed analog voltage becomes about 4.5 V at V_{CC} = 5.0 V.) When setting "0" to the comparator reference input selection bit, the $P0_0$/$P3_{REF}$ pin becomes the comparator reference power source input pin and it is possible to input the comparator reference power source optionally from the external. The voltage comparison is immediately performed by the writing operation to the comparator data register (address $002D_{16}$). After 14 cycles of the internal system clock ϕ (the time required for the comparison), the comparison result is stored in the comparator register (address $002D_{16}$).

If the analog input voltage is greater than the internal reference voltage, each bit of this register is "1"; if it is less than the internal reference voltage, each bit of this register is "0". To perform another comparison, the voltage comparison must be performed again by writing to the comparator data register (address $002D_{16}$). Read the result when 14 cycles of ϕ or more have passed after the comparator operation starts. The ladder resistor is turned on during 14 cycles of ϕ , which is required for the comparison, and the reference voltage is generated. An unnecessary current is not consumed because the ladder resistor is turned off while the comparator operation is not performed. Since the comparator consists of capacitor coupling, the electric charge is lost if the clock frequency is low.

Keep that the clock frequency is 1 MHz or more during the comparator operation. Do not execute the STP, WIT, or port P3 I/O instruction.

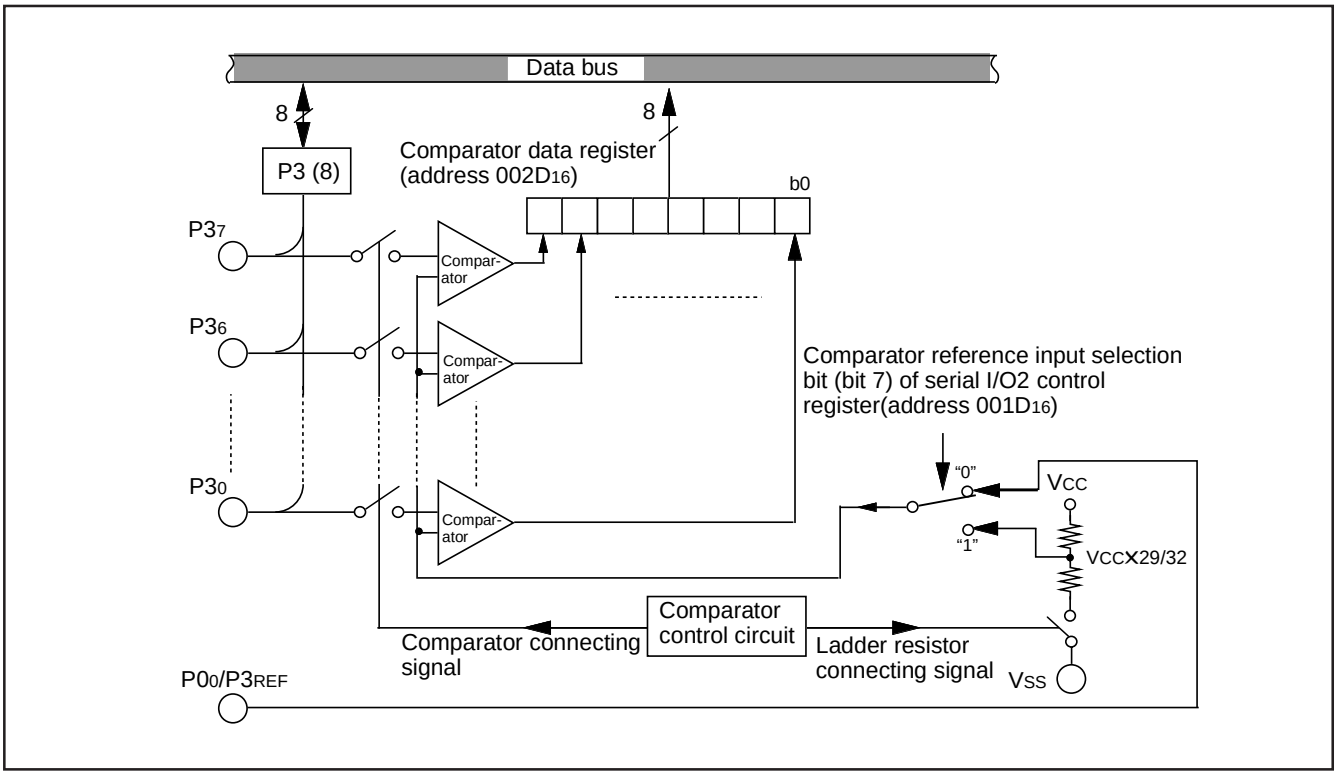


Fig. 52 Comparator circuit

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 001E16) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 001E16) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 001E16) may be started before an underflow. When the watchdog timer control register (address 001E16) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register (address 001E16), each watchdog timer H and L is set to "FF16."

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 001E16) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to f(XIN)=131.072 ms at 8 MHz frequency and f(XCIN)=32.768 s at 32 kHz frequency.

When this bit is set to "1", the count source becomes the signal divided by 16 for f(XIN) (or f(XCIN)). The detection time in this case is set to f(XIN)= 512 μs at 8 MHz frequency and f(XCIN)=128 ms at 32 kHz frequency. This bit is cleared to "0" after resetting.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 001E16) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled.

Once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.

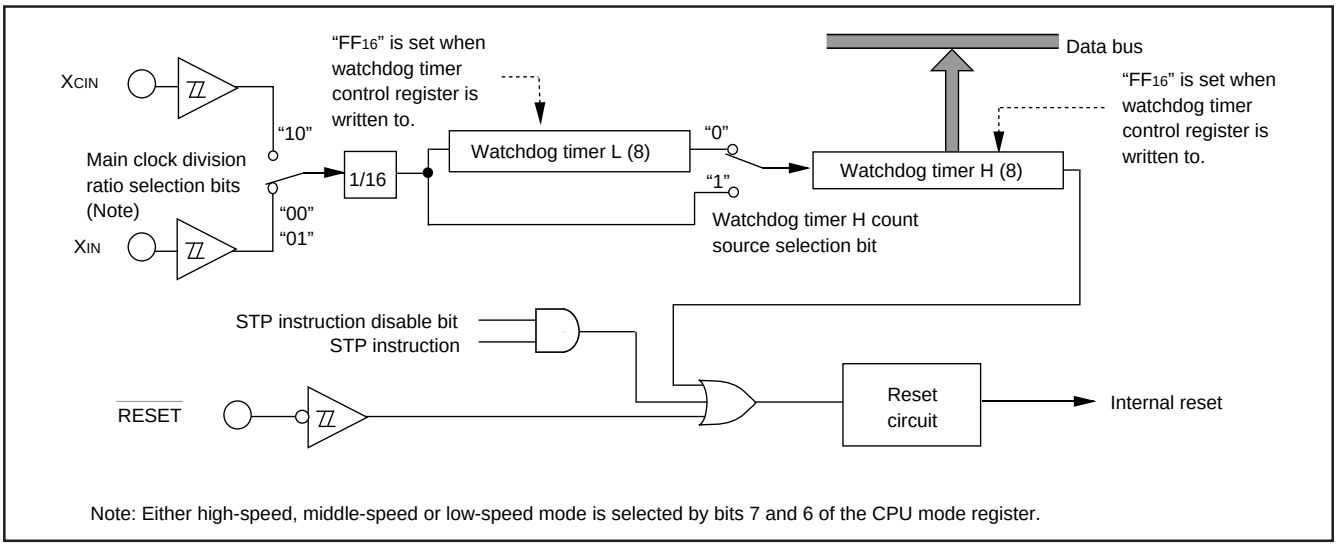


Fig. 53 Block diagram of Watchdog timer

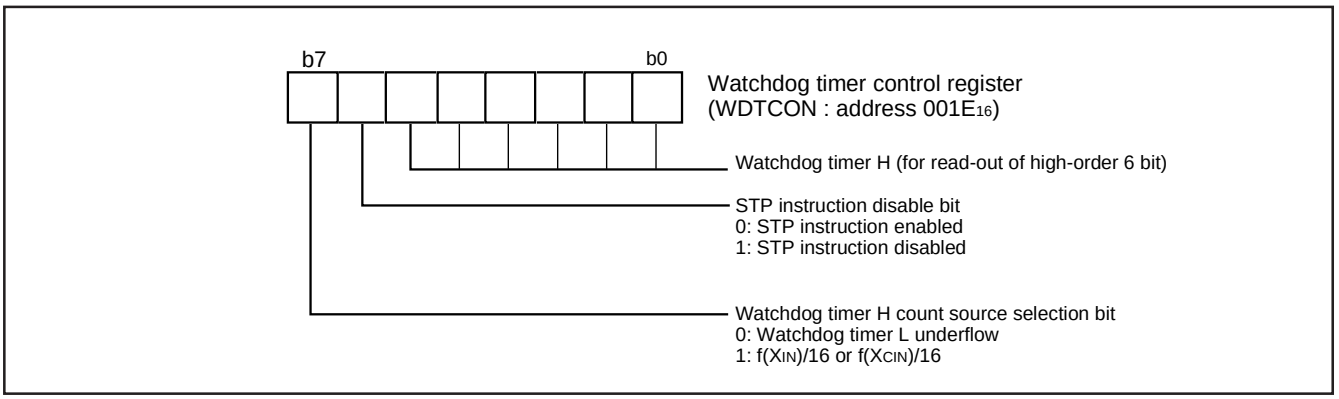


Fig. 54 Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.7 V and 5.5 V (4.0 V to 5.5 V for flash memory version), and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.54 V for Vcc of 2.7 V. For flash memory version, make sure that the reset input voltage is less than 0.8 V for Vcc of 4.0 V.

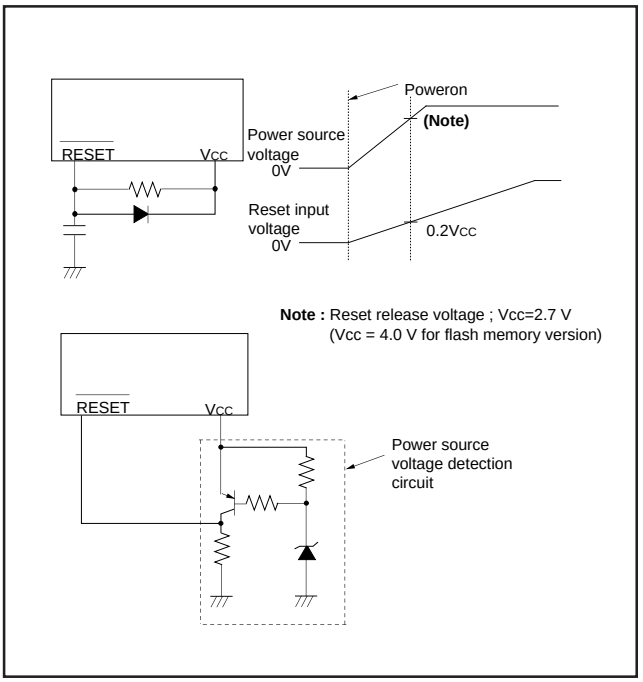


Fig. 55 Reset circuit example

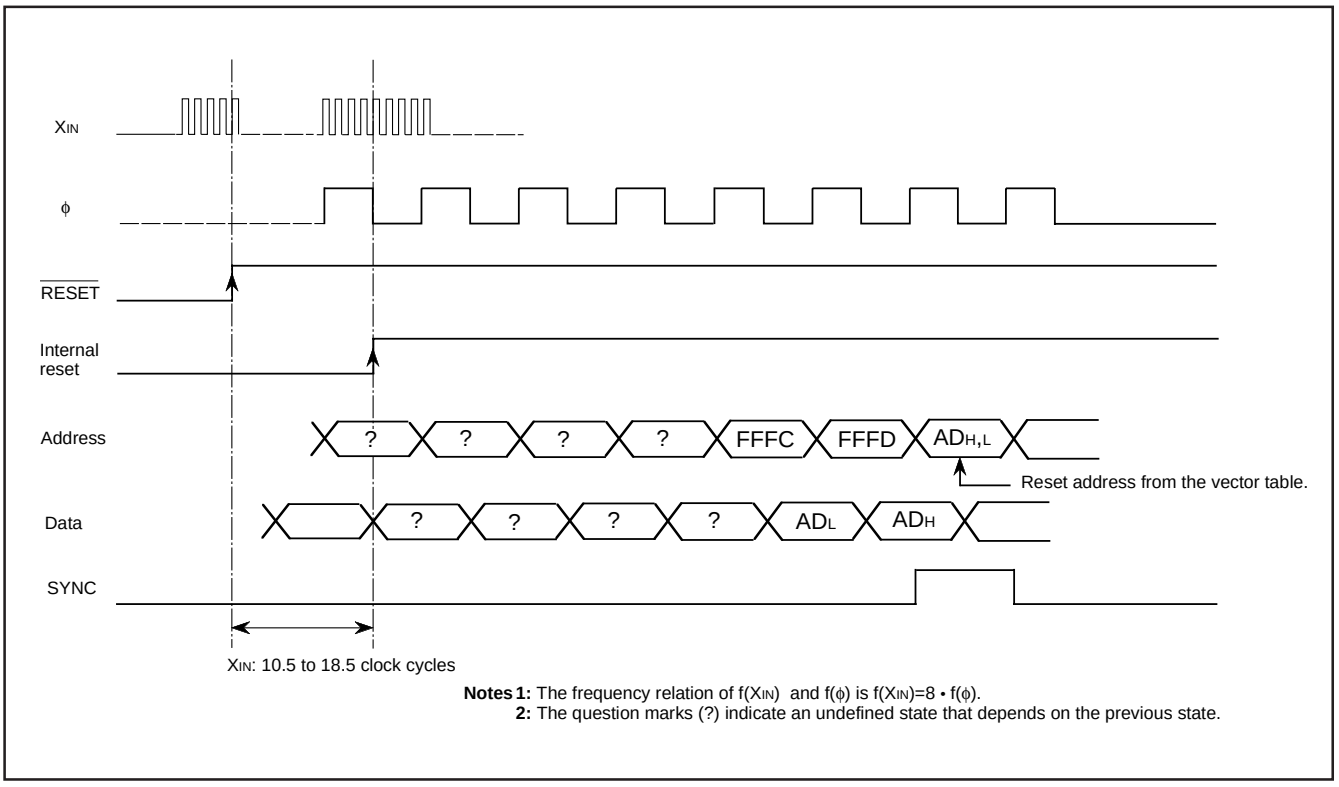


Fig. 56 Reset sequence

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Port P7 (P7)	$000E_{16}$	00_{16}
(16)	Port P7 direction register (P7D)	$000F_{16}$	00_{16}
(17)	Port P8 (P8)	0010_{16}	00_{16}
(18)	Port P8 direction register (P8D)	0011_{16}	00_{16}
(19)	I^2C data shift register (S0)	0012_{16}	X X X X X X X X
(20)	I^2C address register (S0D)	0013_{16}	00_{16}
(21)	I^2C status register (S1)	0014_{16}	0 0 0 1 0 0 0 X
(22)	I^2C control register (S1D)	0015_{16}	00_{16}
(23)	I^2C clock control register (S2)	0016_{16}	00_{16}
(24)	I^2C start/stop condition control register (S2D)	0017_{16}	0 0 0 1 1 0 1 0
(25)	Transmit/Receive buffer register (TB/RB)	0018_{16}	X X X X X X X X
(26)	Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(27)	Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(28)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(29)	Baud rate generator (BRG)	$001C_{16}$	X X X X X X X X
(30)	Serial I/O2 control register (SIO2CON)	$001D_{16}$	00_{16}
(31)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(32)	Serial I/O2 register (SIO2)	$001F_{16}$	X X X X X X X X

		Address	Register contents
(33)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(34)	Timer 1 (T1)	0021_{16}	01_{16}
(35)	Timer 2 (T2)	0022_{16}	FF_{16}
(36)	Timer XY mode register (TM)	0023_{16}	00_{16}
(37)	Prescaler X (PREX)	0024_{16}	FF_{16}
(38)	Timer X (TX)	0025_{16}	FF_{16}
(39)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(40)	Timer Y (TY)	0027_{16}	FF_{16}
(41)	Data bus buffer register 0 (DBB0)	0028_{16}	X X X X X X X X
(42)	Data bus buffer status register 0 (DBBSTS0)	0029_{16}	00_{16}
(43)	Data bus buffer control register (DBBCON)	$002A_{16}$	00_{16}
(44)	Data bus buffer register 1 (DBB1)	$002B_{16}$	X X X X X X X X
(45)	Data bus buffer status register 1 (DBBSTS1)	$002C_{16}$	00_{16}
(46)	Comparator data register (CMPD)	$002D_{16}$	X X X X X X X X
(47)	Port control register 1 (PCTL1)	$002E_{16}$	00_{16}
(48)	Port control register 2 (PCTL2)	$002F_{16}$	00_{16}
(49)	PWM0H register (PWM0H)	0030_{16}	X X X X X X X X
(50)	PWM0L register (PWM0L)	0031_{16}	X 0 X X X X X X
(51)	PWM1H register (PWM1H)	0032_{16}	X X X X X X X X
(52)	PWM1L register (PWM1L)	0033_{16}	X 0 X X X X X X
(53)	AD/DA control register (ADCON)	0034_{16}	0 0 0 0 1 0 0 0
(54)	A-D conversion register 1 (AD1)	0035_{16}	X X X X X X X X
(55)	D-A1 conversion register (DA1)	0036_{16}	00_{16}
(56)	D-A2 conversion register (DA2)	0037_{16}	00_{16}
(57)	A-D conversion register 2 (AD2)	0038_{16}	0 0 0 0 0 0 X X
(58)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(59)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(60)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 * 0
(61)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(62)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(63)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(64)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(65)	Flash memory control register (FCON)	$0FFE_{16}$	00_{16}
(66)	Flash command register (FCMD)	$0FFF_{16}$	00_{16}
(67)	Processor status register	(PS)	X X X X X 1 X X
(68)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : * The initial values depend on level of the CNV_{SS} pin.
X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 57 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3886 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source, and the output of the prescaler 12 is connected to timer 1. Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. Therefore make sure not to set the timer 1 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

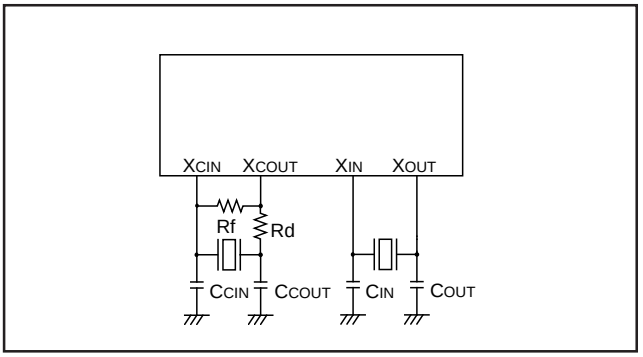


Fig. 58 Ceramic resonator circuit

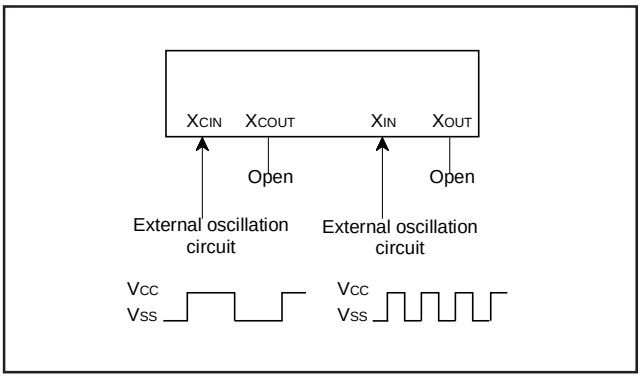
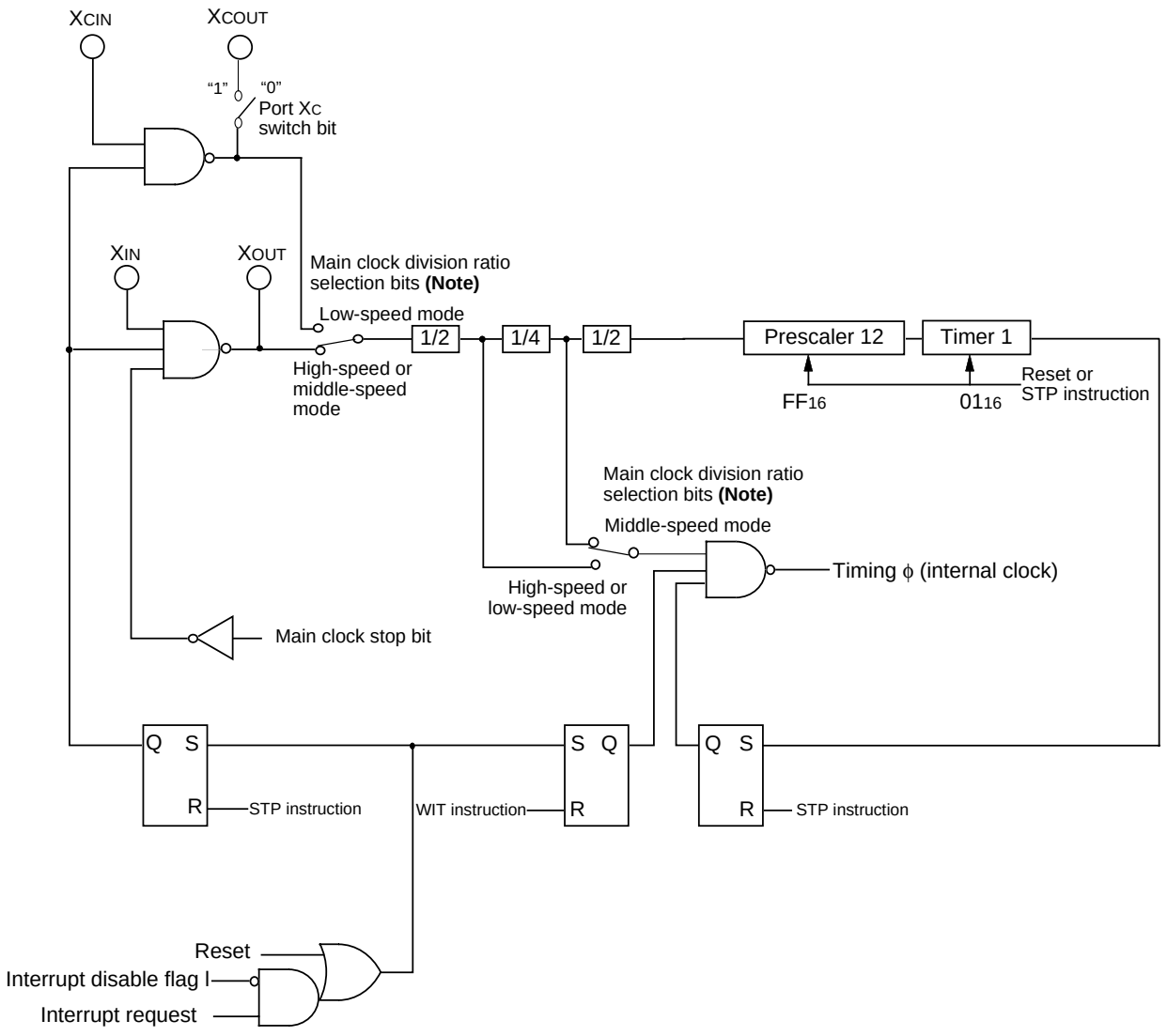
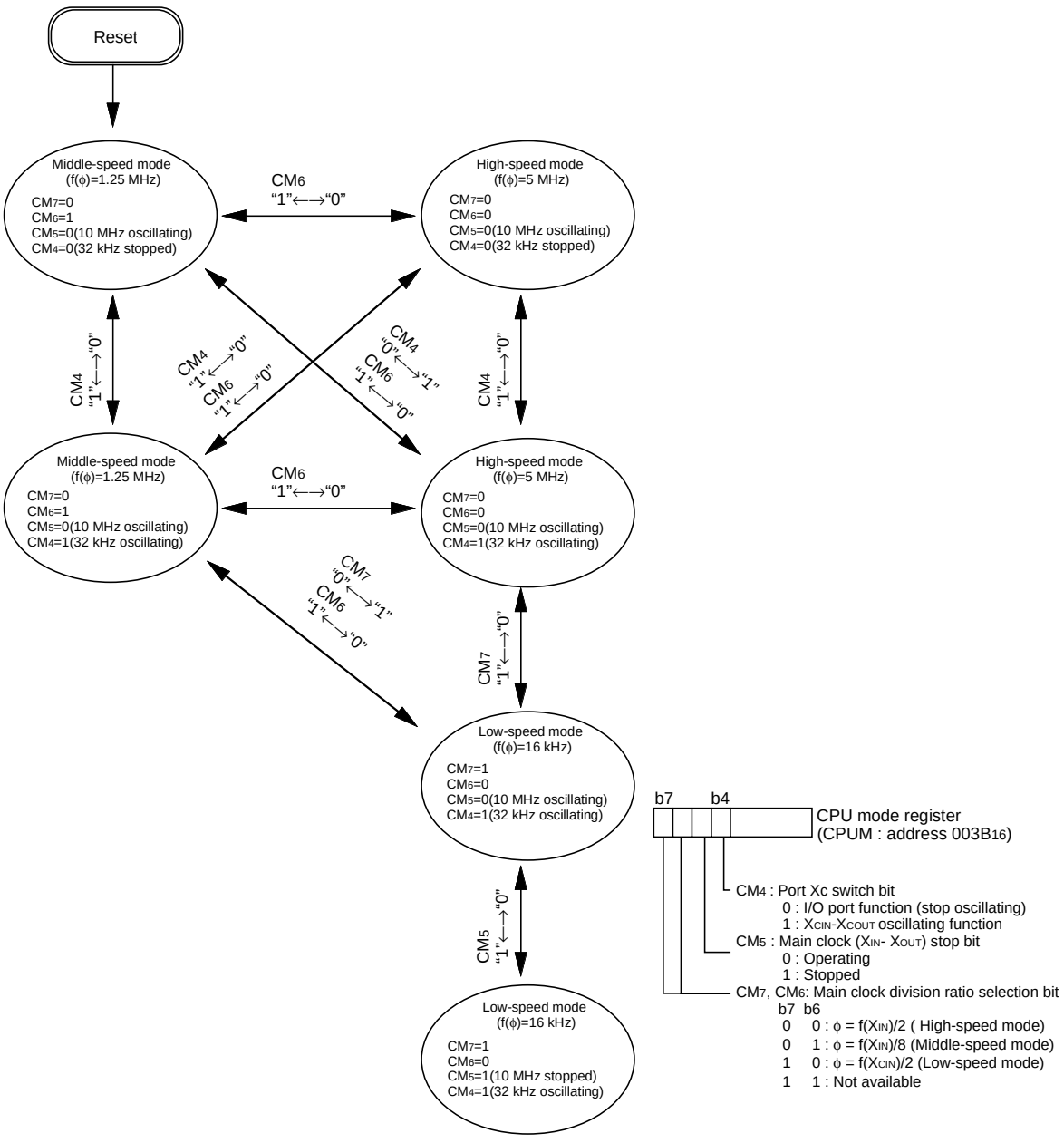


Fig. 59 External clock input circuit



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b4) to "1".

Fig. 60 System clock generating circuit block diagram (Single-chip mode)



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3 : Timer operates in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 and Timer 1 in middle/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 and Timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
7 : The example assumes that 10 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 61 State transitions of system clock

PROCESSOR MODE

Single-chip mode, memory expansion mode, and microprocessor mode in the M38867M8A/E8A can be selected by changing the contents of the processor mode bits (CM_0 and CM_1 : b1 and b0 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table 15 Port functions in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs low-order 8 bits of address.
Port P1	Outputs high-order 8 bits of address.
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction code).
Port P3	$P3_0$ and $P3_1$ function only as output pins (except that the port latch cannot be read). $P3_2$ is the $\overline{ONW}$ input pin. $P3_3$ is the $\overline{RESET}_{OUT}$ output pin. (**Note**) $P3_4$ is the ϕ output pin. $P3_5$ is the SYNC output pin. $P3_6$ is the $\overline{WR}$ output pin, and $P3_7$ is the $\overline{RD}$ output pin.

Note : If CNV_{SS} is connected to V_{SS}, the microcomputer goes to single-chip mode after a reset, so that this pin cannot be used as the $RESET_{OUT}$ output pin.

(1) Single-chip mode

Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{SS}.

(2) Memory expansion mode

Select this mode by setting the processor mode bits (b1, b0) to "01" in software with CNV_{SS} connected to V_{SS}. This mode enables external memory expansion while maintaining the validity of the internal ROM.

However, do not set this mode in the M38869M8A/MCA/MFA and the flash memory version.

(3) Microprocessor mode

Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{CC}, or by setting the processor mode bits to "10" in software with CNV_{SS} connected to V_{SS}. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.

Do not set this mode in the M38869M8A/MCA/MFA and the flash memory version.

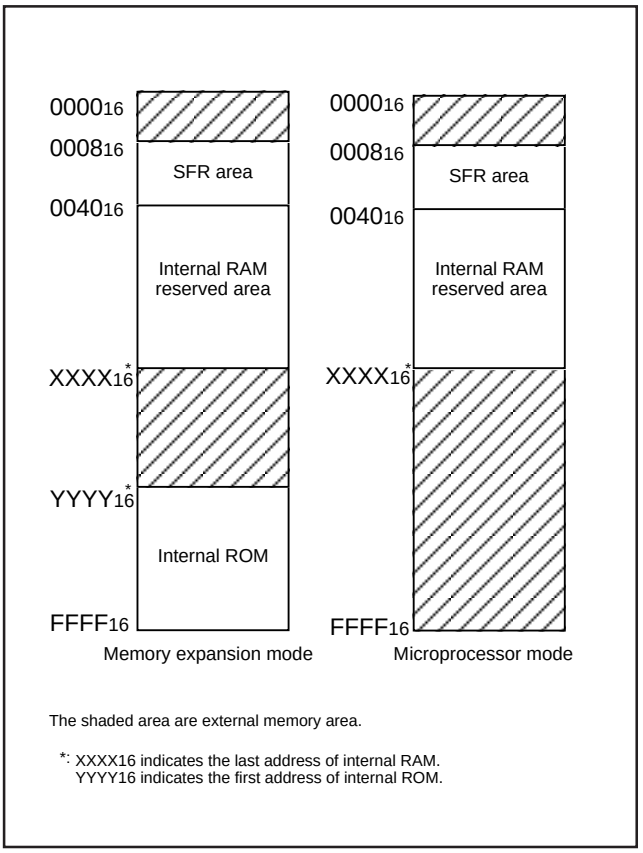


Fig. 62 Memory maps in various processor modes

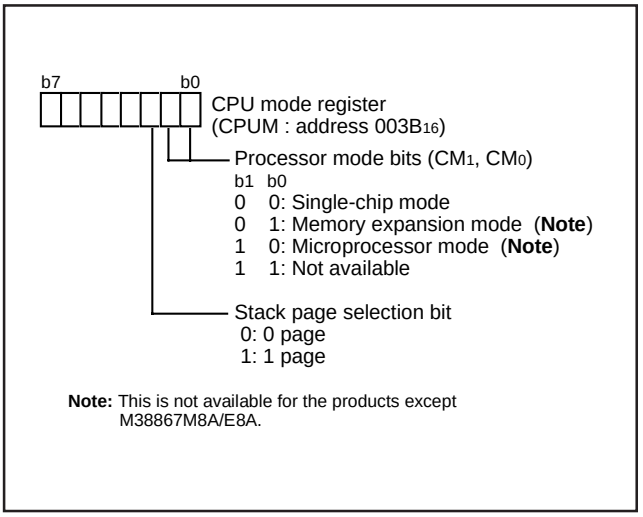
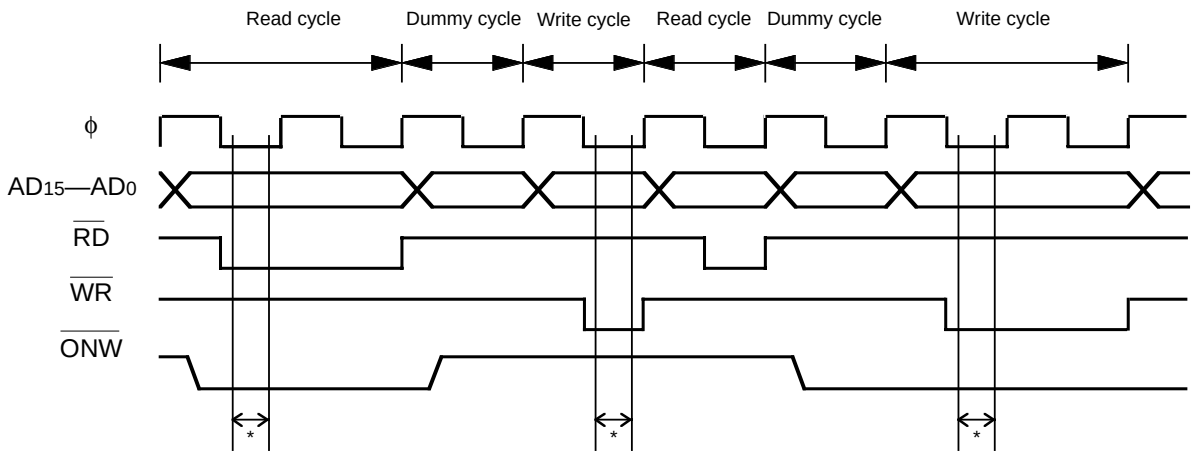


Fig. 63 Structure of CPU mode register

BUS CONTROL AT MEMORY EXPANSION

The M38867M8A/E8A have a built-in $\overline{ONW}$ function to facilitate access to an external (expanded) memory and I/O devices in memory expansion mode or microprocessor mode.

If an "L" level signal is input to the P3$_2$/$\overline{ONW}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended term, the $\overline{RD}$ and $\overline{WR}$ signals remain at "L." This extension function is valid only for writing to and reading from addresses 0000_{16} to 0007_{16} and 0440_{16} to $FFFF_{16}$, and only read and write cycles are extended.



* Term where $\overline{ONW}$ input signal is received.
During this term, the $\overline{ONW}$ signal must be fixed at either "H" or "L". At all other times, the input level of the $\overline{ONW}$ signal has no affect on operations. The bus cycles is not extended for an address in the area 0008_{16} to $043F_{16}$, because the $\overline{ONW}$ signal is not received.

Fig. 64 $\overline{ONW}$ function timing

EPROM MODE

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. The One Time PROM version and the built-in EPROM version have the function of the M5M27C101 corresponding for writing to the built-in PROM. Set the address of PROM programmer in the user ROM area.

Table 16 Programming adapter

Package	Name of Programming Adapter
80P6Q-A	PCA4738H-80A
80D0	PCA4738L-80A

Table 17 PROM programmer setup

Product name	PROM programmer setup		ROM area of microcomputer
	Corresponding device	Writing area	
M38867E8AHP	M5M27C101K byte program	8080_{16} | $0FFFD_{16}$	8080_{16} | $FFFD_{16}$
M38867E8AFS			

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 65 is recommended to verify programming.

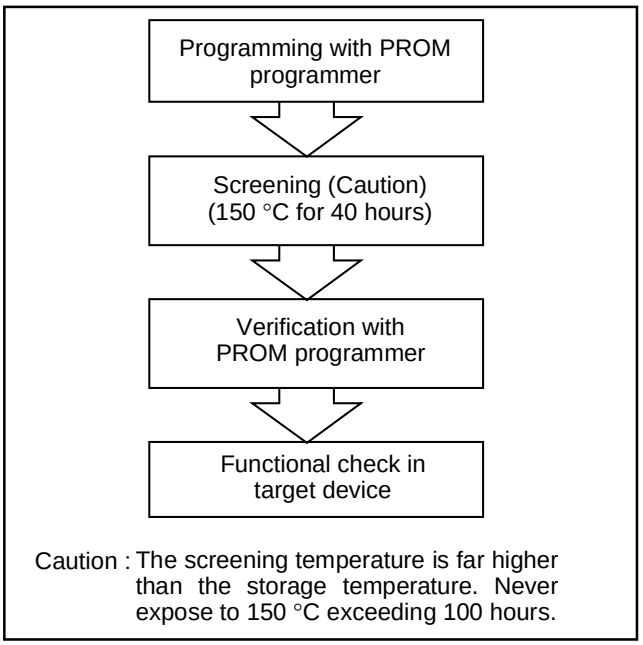


Fig. 65 Programming and testing of One Time PROM version

FLASH MEMORY MODE

The M38869FFAHP/GP has the flash memory mode in addition to the normal operation mode (microcomputer mode). The user can use this mode to perform read, program, and erase operations for the internal flash memory.

The M38869FFAHP/GP has three modes the user can choose: the parallel input/output and serial input/output mode, where the flash memory is handled by using the external programmer, and the CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU). The following explains these modes.

(1) Flash memory mode 1 (parallel I/O mode)

The parallel I/O mode can be selected by connecting wires as shown in Figures 65 and supplying power to the V_{CC} and V_{PP} pins. In this mode, the M38869FFAHP/GP operates as an equivalent of MITSUBISHI's CMOS flash memory M5M28F101. However, because the M38869FFAHP/GP's internal memory has a capacity of 60 Kbytes, programming is available for addresses 01000_{16} to $0FFFF_{16}$, and make sure that the data in addresses 00000_{16} to $00FFF_{16}$ and addresses 10000_{16} to $1FFFF_{16}$ are FF_{16}. Note also that the M38869FFAHP/GP does not contain a facility to read out a device identification code by applying a high voltage to address input (A9). Be careful not to erratically set program conditions when using a general-purpose PROM programmer.

Table 18 shows the pin assignments when operating in the parallel input/output mode.

Table 18 Pin assignments of M38869FFAHP/GP when operating in the parallel input/output mode

	M38869FFAHP/GP	M5M28F101
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV$_{SS}$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1, P3$_1$	A_0–A_{16}
Data I/O	Port P2	D_0–D_7
$\overline{CE}$	P3$_6$	$\overline{CE}$
$\overline{OE}$	P3$_7$	$\overline{OE}$
$\overline{WE}$	P3$_3$	$\overline{WE}$

Functional Outline (parallel input/output mode)

In the parallel input/output mode, the M38869FFAHP/GP allow the user to choose an operation mode between the read-only mode and the read/write mode (software command control mode) depending on the voltage applied to the V_{PP} pin. When $V_{PP} = V_{PP}L$, the read-only mode is selected, and the user can choose one of three states (e.g., read, output disable, or standby) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. When $V_{PP} = V_{PP}H$, the read/write mode is selected, and the user can choose one of four states (e.g., read, output disable, standby, or write) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. Table 19 shows assignment states of control input and each state.

● Read

The microcomputer enters the read state by driving the $\overline{CE}$, and $\overline{OE}$ pins low and the $\overline{WE}$ pin high; and the contents of memory corresponding to the address to be input to address input pins (A_0–A_{16}).

are output to the data input/output pins (D_0–D_7).

● Output disable

The microcomputer enters the output disable state by driving the $\overline{CE}$ pin low and the $\overline{WE}$ and $\overline{OE}$ pins high; and the data input/output pins enter the floating state.

● Standby

The microcomputer enters the standby state by driving the $\overline{CE}$ pin high. the M38869FFAHP/GP is placed in a power-down state consuming only a minimal supply current. At this time, the data input/output pins enter the floating state.

● Write

The microcomputer enters the write state by driving the V_{PP} pin high ($V_{PP} = V_{PP}H$) and then the $\overline{WE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{OE}$ pin is high. In this state, software commands can be input from the data input/output pins, and the user can choose program or erase operation depending on the contents of this software command.

Table 19 Assignment sates of control input and each state

Mode \ Pin / State		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	Data I/O
Read-only	Read	V_{IL}	V_{IL}	V_{IH}	$V_{PP}L$	Output
	Output disable	V_{IL}	V_{IH}	V_{IH}	$V_{PP}L$	Floating
	Standby	V_{IH}	×	×	$V_{PP}L$	Floating
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	$V_{PP}H$	Output
	Output disable	V_{IL}	V_{IH}	V_{IH}	$V_{PP}H$	Floating
	Standby	V_{IH}	×	×	$V_{PP}H$	Floating
	Write	V_{IL}	V_{IH}	V_{IL}	$V_{PP}H$	Input

Note: × can be V_{IL} or V_{IH}.

Table 20 Pin description (flash memory parallel I/O mode)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply	—	Supply 5 V ± 10 % to V_{CC} and 0 V to V_{SS}.
CNV$_{SS}$	V_{PP} input	Input	Connect to 5 V ± 10 % in read-only mode, connect to 11.7 to 12.6 V in read/write mode.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
AV$_{SS}$	Analog supply input	—	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
P0$_0$–P0$_7$	Address input (A$_0$–A$_7$)	Input	Port P0 functions as 8-bit address input (A$_0$–A$_7$).
P1$_0$–P1$_7$	Address input (A$_8$–A$_{15}$)	Input	Port P1 functions as 8-bit address input (A$_8$–A$_{15}$).
P2$_0$–P2$_7$	Data I/O (D$_0$–D$_7$)	I/O	Function as 8-bit data's I/O pins (D$_0$–D$_7$).
P3$_0$–P3$_7$	Control signal input	Input	P3$_7$, P3$_6$ and P3$_3$ function as the $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ input pins respectively. P3$_1$ functions as the A$_{16}$ input pin. Connect P3$_0$ and P3$_2$ to V_{SS}. Input "H" or "L" to P3$_4$, P3$_5$, or keep them open.
P4$_0$–P4$_7$	Input port P4	Input	Connect P4$_4$, P4$_6$ to V_{SS}. Input "H" or "L" to P4$_0$ - P4$_3$, P4$_5$, P4$_7$, or keep them open.
P5$_0$–P5$_7$	Input port P5	Input	Input "H" or "L", or keep them open.
P6$_0$–P6$_7$	Input port P6	Input	Input "H" or "L", or keep them open.
P7$_0$–P7$_7$	Input port P7	Input	Input "H" or "L", or keep them open.
P8$_0$–P8$_7$	Input port P8	Input	Input "H" or "L", or keep them open.

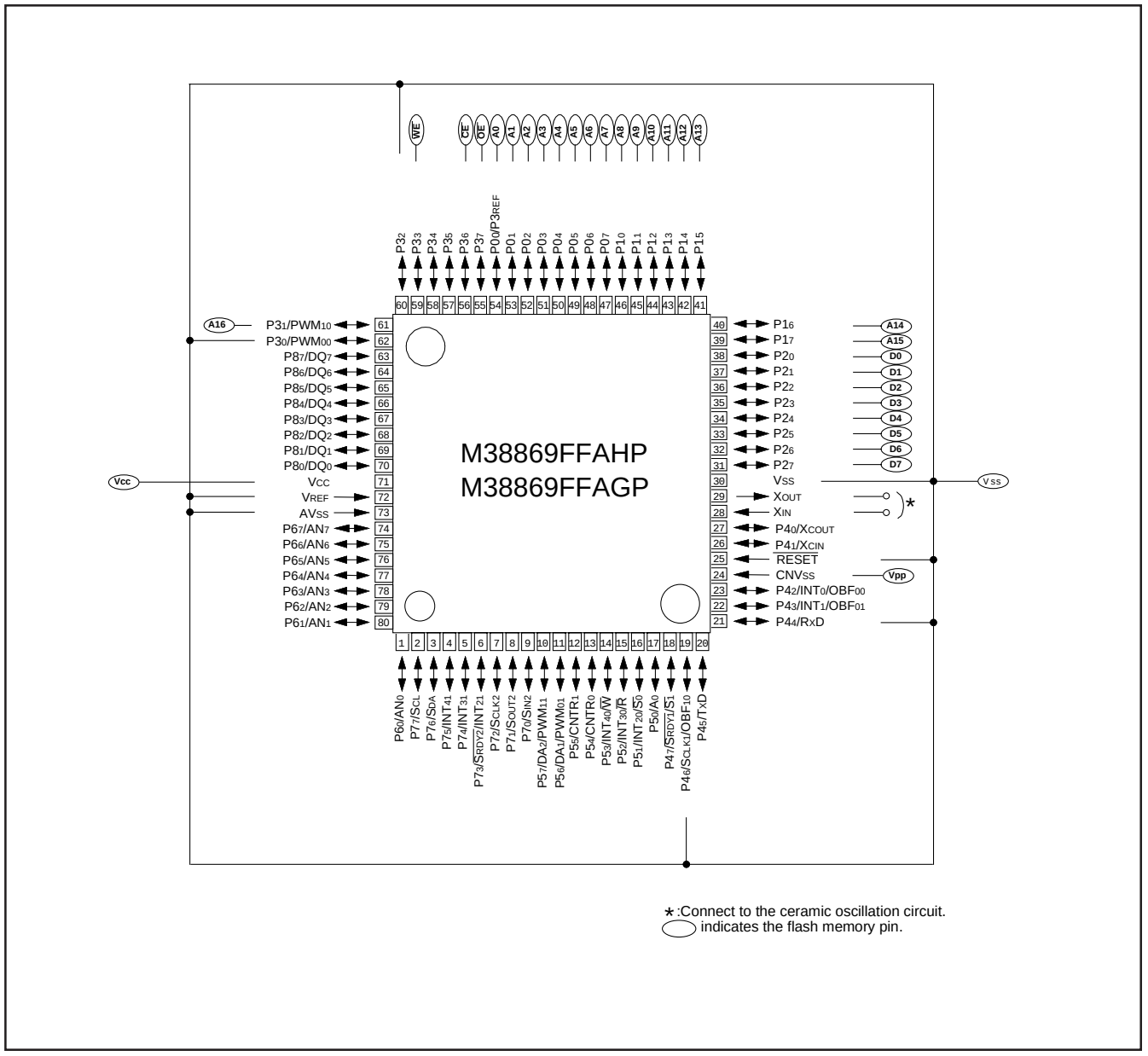


Fig. 66 Pin connection of M38869FFAHP/GP when operating in parallel input/output mode

Read-only Mode

The microcomputer enters the read-only mode by applying VPPL to the VPP pin. In this mode, the user can input the address of a memory location to be read and the control signals at the timing shown in Figure 67, and the M38869FFAHP/GP will output the contents of the user's specified address from data I/O pin to the external. In this mode, the user cannot perform any operation other than read.

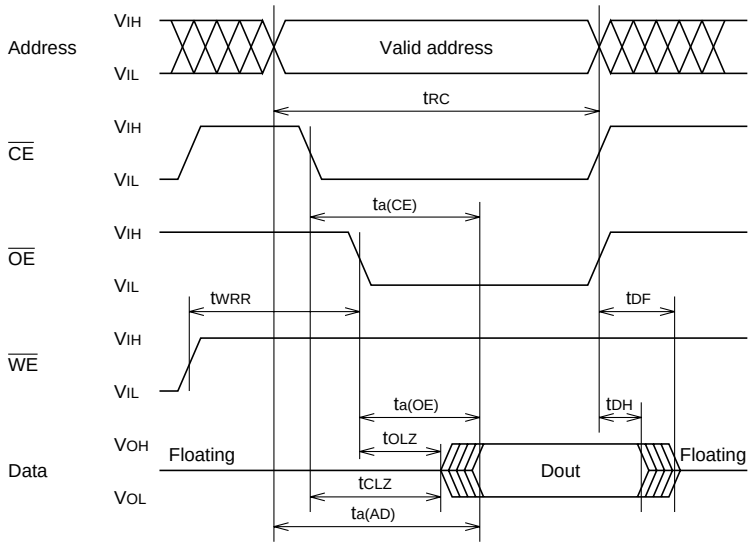


Fig. 67 Read timing

Read/Write Mode

The microcomputer enters the read/write mode by applying VPPH to the VPP pin. In this mode, the user must first input a software command to choose the operation (e. g., read, program, or erase) to be performed on the flash memory (this is called the first cycle), and then input the information necessary for execution of the command (e.g, address and data) and control signals (this is called the second cycle). When this is done, the M38869FFAHP/GP executes the specified operation.

Table 21 shows the software commands and the input/output information in the first and the second cycles. The input address is latched internally at the falling edge of the $\overline{WE}$ input; software commands and other input data are latched internally at the rising edge of the $\overline{WE}$ input.

The following explains each software command. Refer to Figures 68 to 70 for details about the signal input/output timings.

Table 21 Software command (Parallel input/output mode)

Symbol	First cycle		Second cycle	
	Address input	Data input	Address input	Data I/O
Read	×	00_{16}	Read address	Read data (Output)
Program	×	40_{16}	Program address	Program data (Input)
Program verify	×	$C0_{16}$	×	Verify data (Output)
Erase	×	20_{16}	×	20_{16} (Input)
Erase verify	Verify address	$A0_{16}$	×	Verify data (Output)
Reset	×	FF_{16}	×	FF_{16} (Input)
Device identification	×	90_{16}	ADI	DDI (Output)

Note: ADI = Device identification address : manufacturer's code 00000_{16}, device code 0000_{116}
DDI = Device identification data : manufacturer's code $1C_{16}$, device code $D0_{16}$
X can be VIL or VIH.

● **Read command**

The microcomputer enters the read mode by inputting command code "00_{16}" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address of a memory location to be read is input in the second cycle, with control signals input at the timing shown in Figure 68, the M38869FFAHP/GP outputs the contents of the specified address from the data I/O pins to the external.

The read mode is retained until any other command is latched into the command latch. Consequently, once the M38869FFAHP/GP enters the read mode, the user can read out the successive memory contents simply by changing the input address and executing the second cycle only. Any command other than the read command must be input beginning from its command code over again each time the user execute it. The contents of the command latch immediately after power-on is 00_{16}.

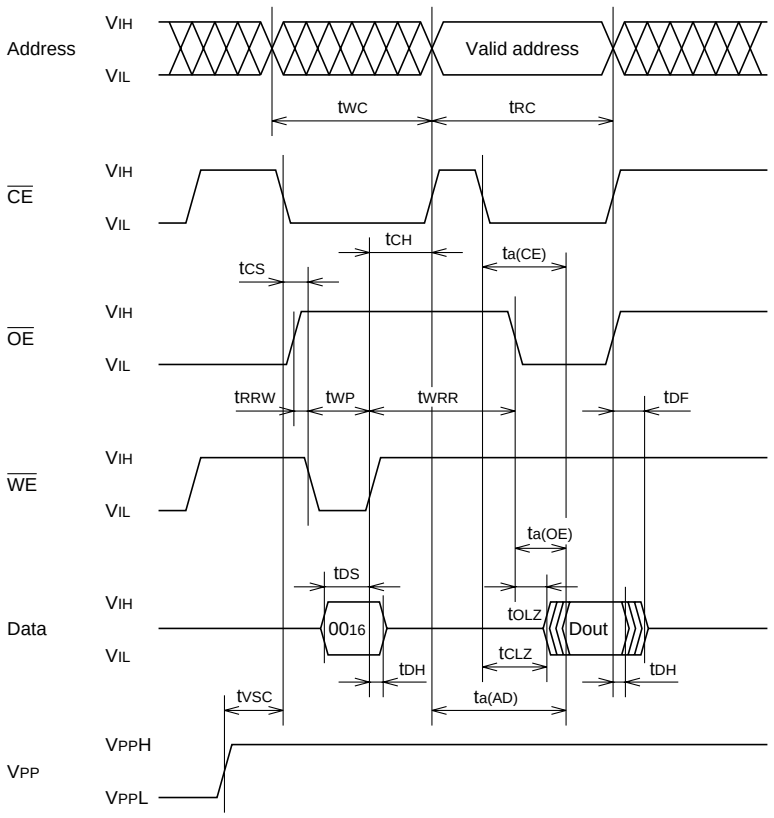


Fig. 68 Timings during reading

● **Program command**

The microcomputer enters the program mode by inputting command code "40$_{16}$" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address which indicates a program location and data is input in the second cycle, the M38869FFAHP/GP internally latches the address at the falling edge of the $\overline{WE}$ input and the data at the rising edge of the $\overline{WE}$ input. The M38869FFAHP/GP starts programming at the rising edge of the $\overline{WE}$ input in the second cycle and finishes programming within 10 μs as measured by its internal timer. Programming is performed in units of bytes.

Note: A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 71 for the programming flowchart.

● **Program verify command**

The microcomputer enters the program verify mode by inputting command code "C0$_{16}$" in the first cycle. This command is used to verify the programmed data after executing the program command. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 69, the M38869FFAHP/GP outputs the programmed address's contents to the external. Since the address is internally latched when the program command is executed, there is no need to input it in the second cycle.

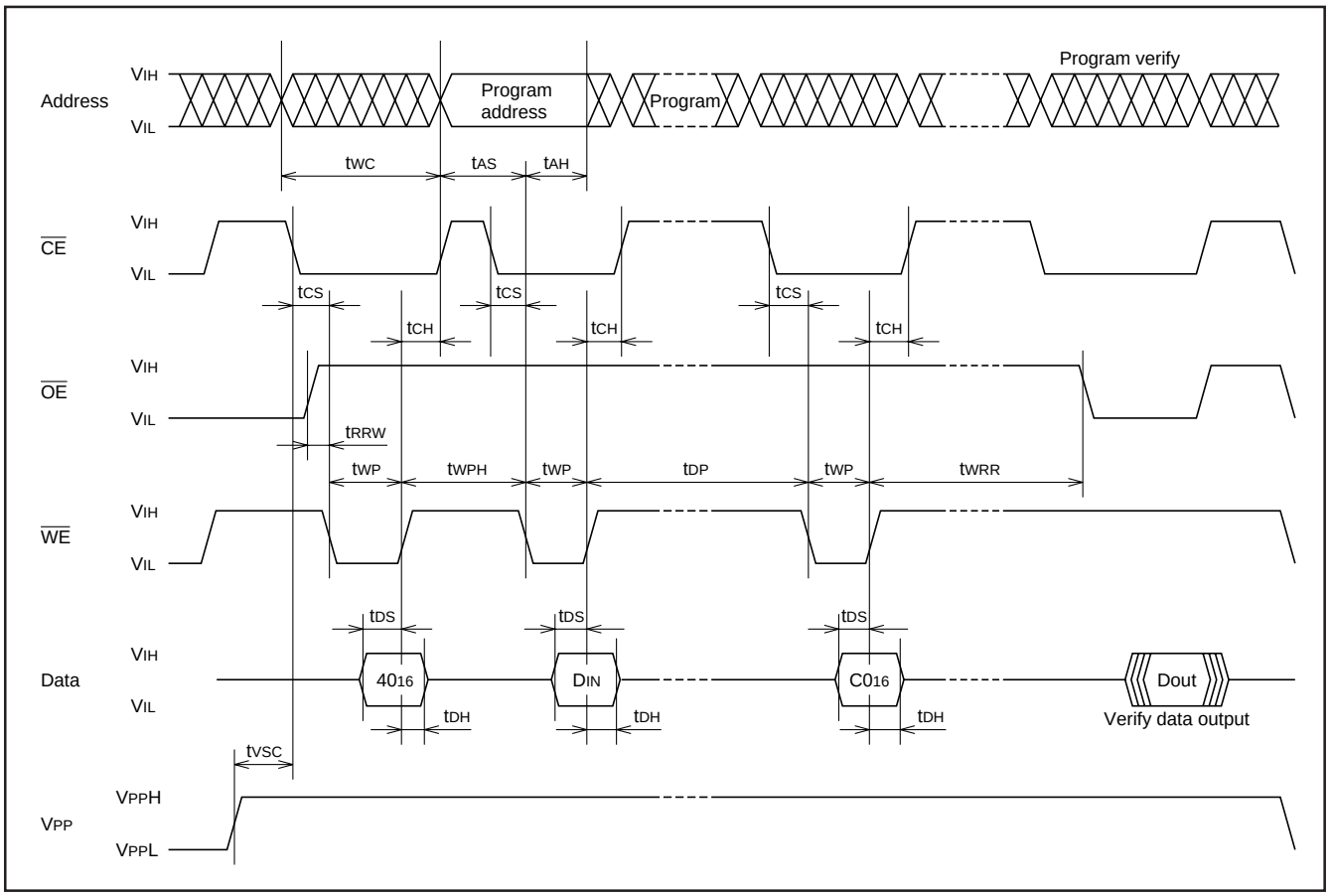


Fig. 69 Input/output timings during programming (Verify data is output at the same timing as for read.)

● **Erase command**

The erase command is executed by inputting command code 20_{16} in the first cycle and command code 20_{16} again in the second cycle. The command code is latched into the internal command latch at the rising edges of the $\overline{WE}$ input in the first cycle and in the second cycle, respectively. The erase operation is initiated at the rising edge of the $\overline{WE}$ input in the second cycle, and the memory contents are collectively erased within 9.5 ms as measured by the internal timer. Note that data 00_{16} must be written to all memory locations before executing the erase command.

Note: An erase operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 71 for the erase flowchart.

● **Erase verify command**

The user must verify the contents of all addresses after completing the erase command. The microcomputer enters the erase verify mode by inputting the verify address and command code $A0_{16}$ in the first cycle. The address is internally latched at the falling edge of the $\overline{WE}$ input, and the command code is internally latched at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 70, the M38869FFAHP/GP outputs the contents of the specified address to the external.

Note: If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data 00_{16} to memory locations before erasing.

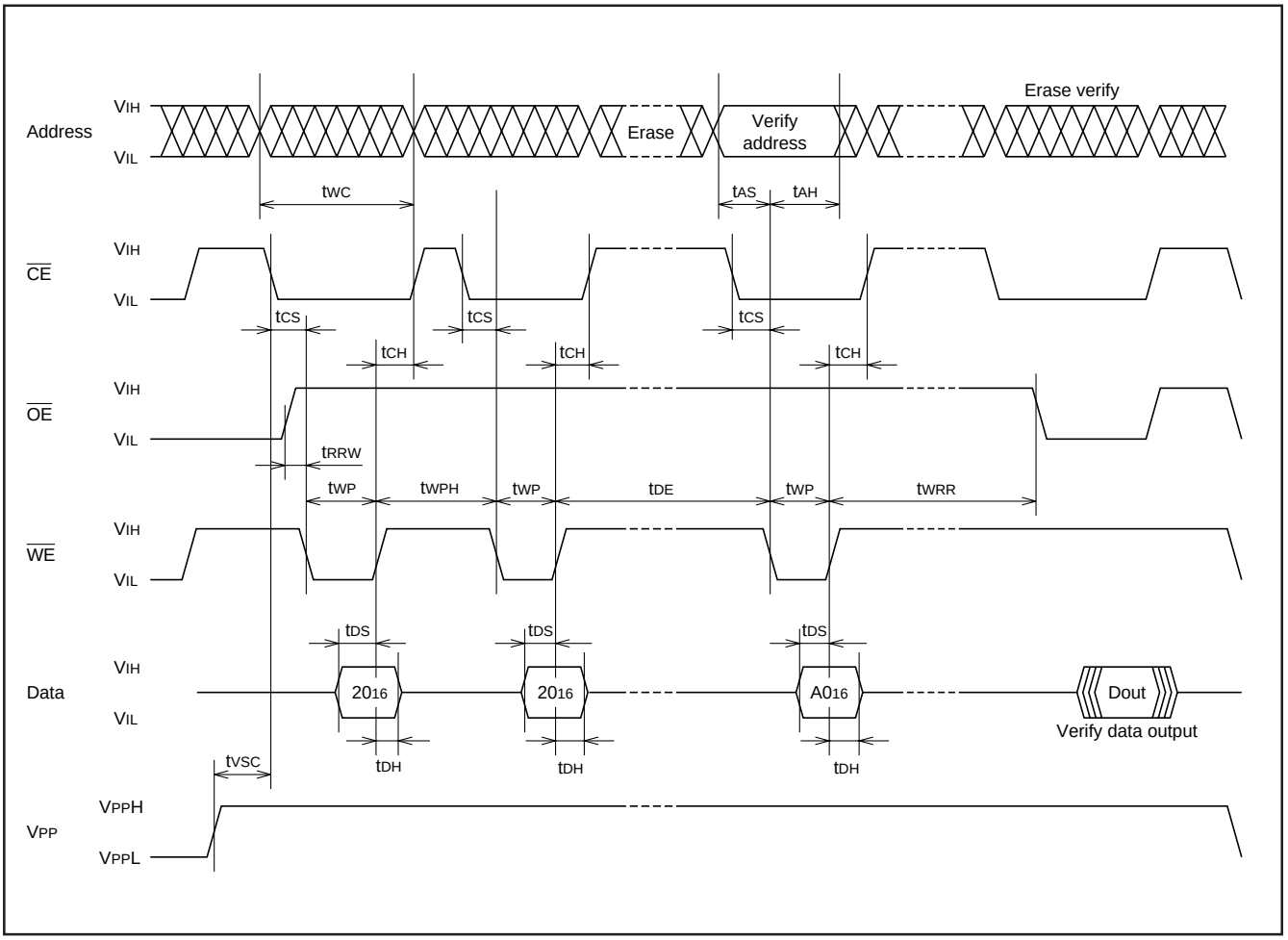


Fig. 70 Input/output timings during erasing (verify data is output at the same timing as for read.)

● **Reset command**

The reset command provides a means of stopping execution of the erase or program command safely. If the user inputs command code FF_{16} in the second cycle after inputting the erase or program command in the first cycle and again input command code FF_{16} in the third cycle, the erase or program command is disabled (i.e., reset), and the M38869FFAHP/GP is placed in the read mode. If the reset command is executed, the contents of the memory does not change.

● **Device identification code command**

By inputting command code 90_{16} in the first cycle, the user can read out the device identification code. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. At this time, the user can read out manufacture's code $1C_{16}$ (i.e., MITSUBISHI) by inputting 0000_{16} to the address input pins in the second cycle; the user can read out device code $D0_{16}$ (i. e., 1M-bit flash memory) by inputting 0001_{16}.

These command and data codes are input/output at the same timing as for read.

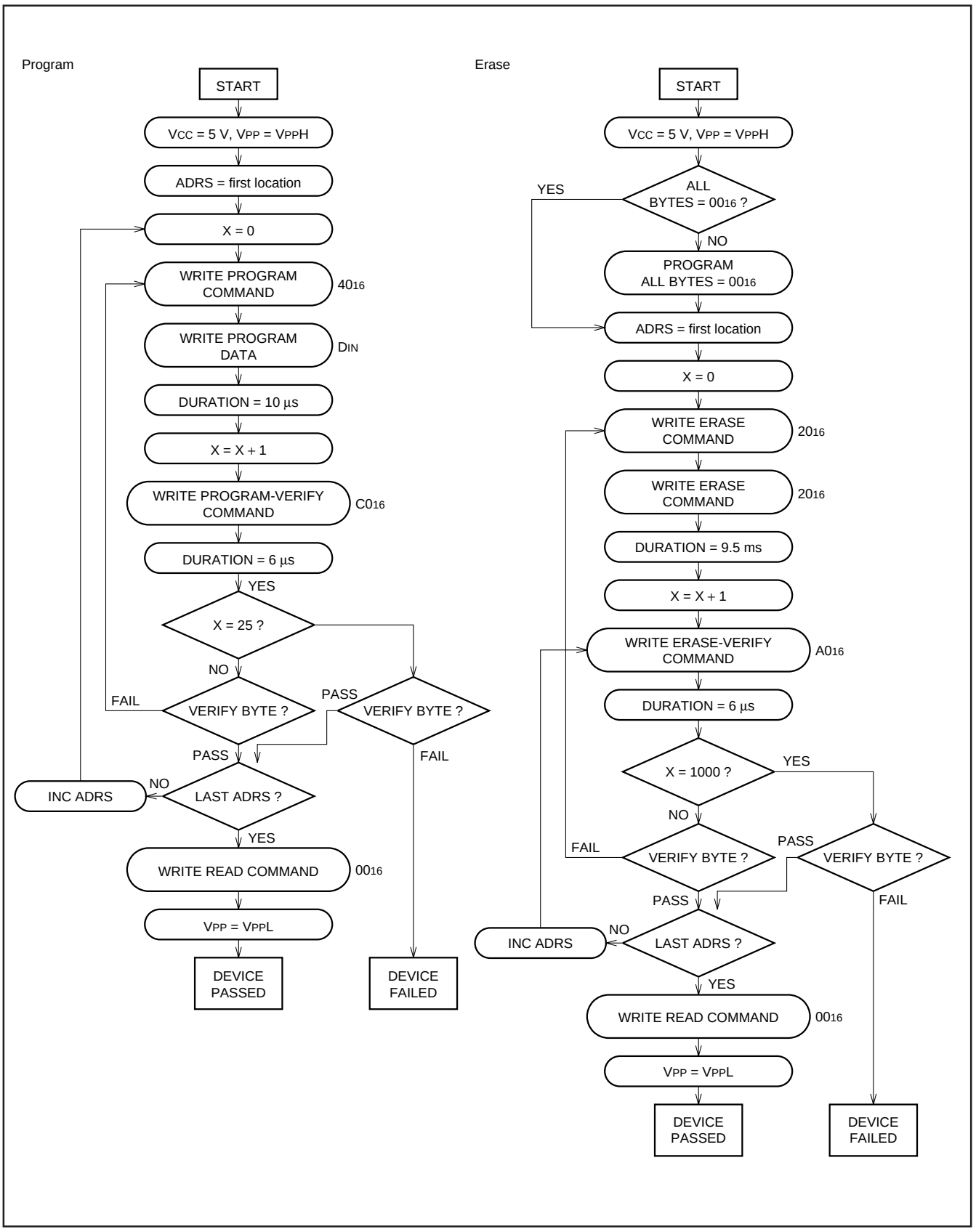


Fig. 71 Programming/Erasing algorithm flow chart

Table 22 DC ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{SB1}	V_{CC} supply current (at standby)	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}			1	mA
I_{SB2}		V_{CC} = 5.5 V, $\overline{CE}$ = V_{CC} ± 0.2 V			100	µA
I_{CC1}	V_{CC} supply current (at read)	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IL}, t_{RC} = 150 ns, I_{OUT} = 0 mA			15	mA
I_{CC2}	V_{CC} supply current (at program)	V_{PP} = V_{PPH}			15	mA
I_{CC3}	V_{CC} supply current (at erase)	V_{PP} = V_{PPH}			15	mA
I_{PP1}	V_{PP} supply current (at read)	0≤V_{PP}≤V_{CC}			10	µA
		V_{CC}<V_{PP}≤V_{CC} + 1.0 V			100	µA
		V_{PP} = V_{PPH}			100	µA
I_{PP2}	V_{PP} supply current (at program)	V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (at erase)	V_{PP} = V_{PPH}			30	mA
V_{IL}	“L” input voltage		0		0.8	V
V_{IH}	“H” input voltage		2.0		V_{CC}	V
V_{OL}	“L” output voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	“H” output voltage	I_{OH} = –400 µA	2.4			V
V_{OH2}		I_{OH} = –100 µA	V_{CC} –0.4			V
V_{PPL}	V_{PP} supply voltage (read only)		V_{CC}		V_{CC} + 1.0	V
V_{PPH}	V_{PP} supply voltage (read/write)		11.7	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Table 23 Read-only mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RC}	Read cycle time	250		ns
$t_{a(AD)}$	Address access time		250	ns
$t_{a(CE)}$	$\overline{CE}$ access time		250	ns
$t_{a(OE)}$	$\overline{OE}$ access time		100	ns
t_{CLZ}	Output enable time (after $\overline{CE}$)	0		ns
t_{OLZ}	Output enable time (after $\overline{OE}$)	0		ns
t_{DF}	Output floating time (after $\overline{OE}$)		35	ns
t_{DH}	Output valid time (after $\overline{CE}$, $\overline{OE}$, address)	0		ns
t_{WRR}	Write recovery time (before read)	6		µs

Table 24 Read/Write mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{WC}	Write cycle time	150		ns
t_{AS}	Address set up time	0		ns
t_{AH}	Address hold time	60		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	10		ns
t_{WRR}	Write recovery time (before read)	6		µs
t_{RRW}	Read recovery time (before write)	0		µs
t_{CS}	$\overline{CE}$ setup time	20		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{WP}	Write pulse width	60		ns
t_{WPH}	Write pulse waiting time	20		ns
t_{DP}	Program time	10		µs
t_{DE}	Erase time	9.5		ms
t_{VSC}	V_{PP} setup time	1		µs

Note: Read timing of Read/Write mode is same as Read-only mode.

(2) Flash memory mode 2 (serial I/O mode)

The M38869FFAHP/GP has a function to serially input/output the software commands, addresses, and data required for operation on the internal flash memory (e. g., read, program, and erase) using only a few pins. This is called the serial I/O (input/output) mode. This mode can be selected by driving the SDA (serial data input/output), SCLK (serial clock input), and $\overline{OE}$ pins high after connecting wires as shown in Figures 72 and powering on the V_{CC} pin and then applying $V_{PP}H$ to the V_{PP} pin.

In the serial I/O mode, the user can use six types of software commands: read, program, program verify, erase, erase verify and error check.

Serial input/output is accomplished synchronously with the clock, beginning from the LSB (LSB first).

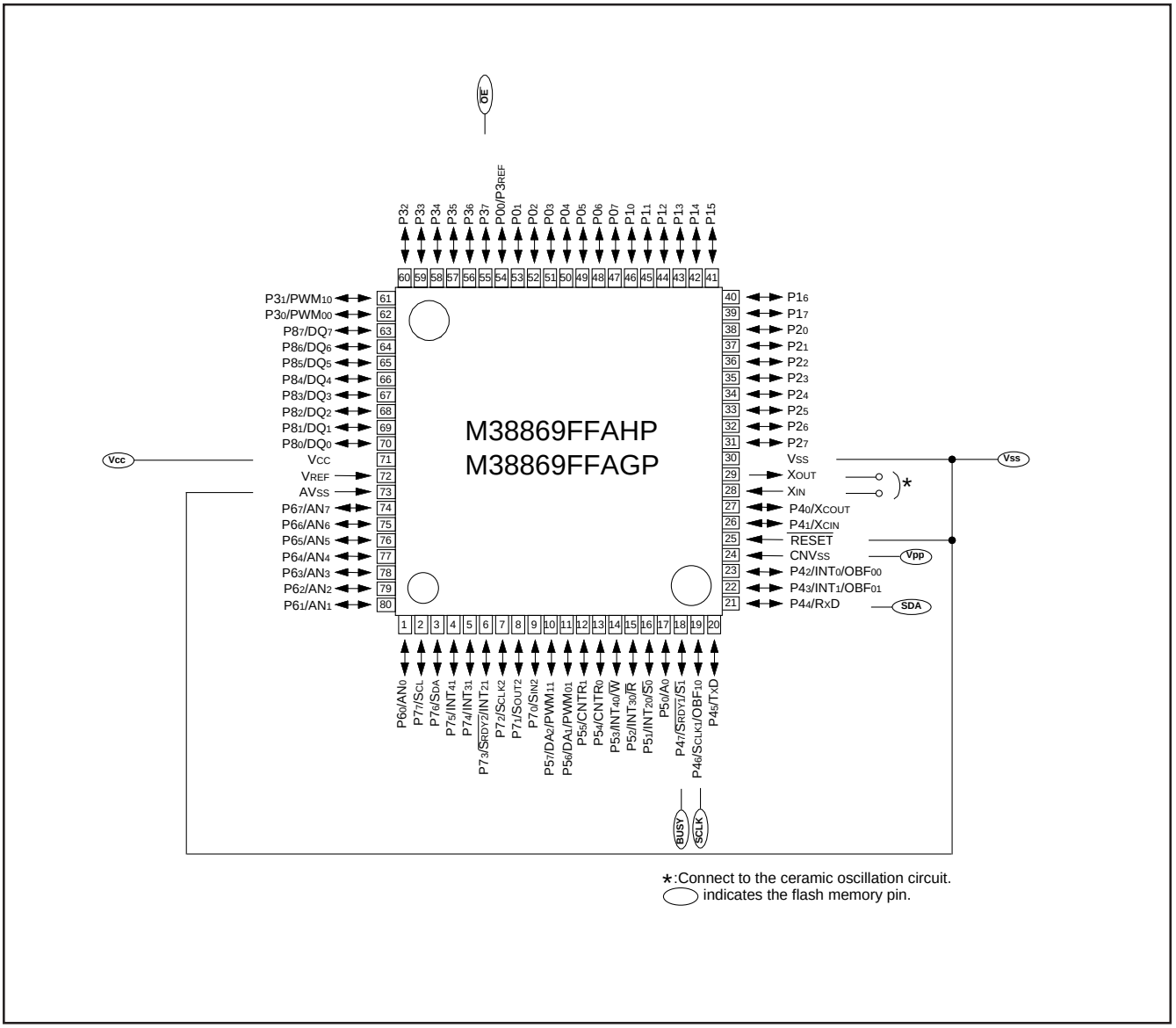


Fig. 72 Pin connection of M38869FFAHP/GP when operating in serial I/O mode

Table 25 Pin description (flash memory serial I/O mode)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply	—	Supply 5 V ± 10 % to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to 11.7 to 12.6 V.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
AV_{SS}	Analog supply input	—	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Input an arbitrary level between the range of V_{SS} and V_{CC}.
$P0_0$–$P0_7$	Input port P0	Input	Input “H” or “L”, or keep them open.
$P1_0$–$P1_7$	Input port P1	Input	Input “H” or “L”, or keep them open.
$P2_0$–$P2_7$	Input port P2	Input	Input “H” or “L”, or keep them open.
$P3_0$–$P3_6$	Input port P3	Input	Input “H” or “L”, or keep them open.
$P3_7$	Control signal input	Input	$\overline{OE}$ input pin
$P4_0$–$P4_3$, $P4_5$	Input port P4	Input	Input “H” or “L” to $P4_0$ - $P4_3$, $P4_5$, or keep them open.
$P4_4$	SDA I/O	I/O	This pin is for serial data I/O.
$P4_6$	SCLK input	Input	This pin is for serial clock input.
$P4_7$	BUSY output	Output	This pin is for BUSY signal output.
$P5_0$–$P5_7$	Input port P5	Input	Input “H” or “L”, or keep them open.
$P6_0$–$P6_7$	Input port P6	Input	Input “H” or “L”, or keep them open.
$P7_0$–$P7_7$	Input port P7	Input	Input “H” or “L”, or keep them open.
$P8_0$–$P8_7$	Input port P8	Input	Input “H” or “L”, or keep them open.

Functional Outline (serial I/O mode)

In the serial I/O mode, data is transferred synchronously with the clock using serial input/output. The input data is read from the SDA pin into the internal circuit synchronously with the rising edge of the serial clock pulse; the output data is output from the SDA pin synchronously with the falling edge of the serial clock pulse.

Data is transferred in units of eight bits.

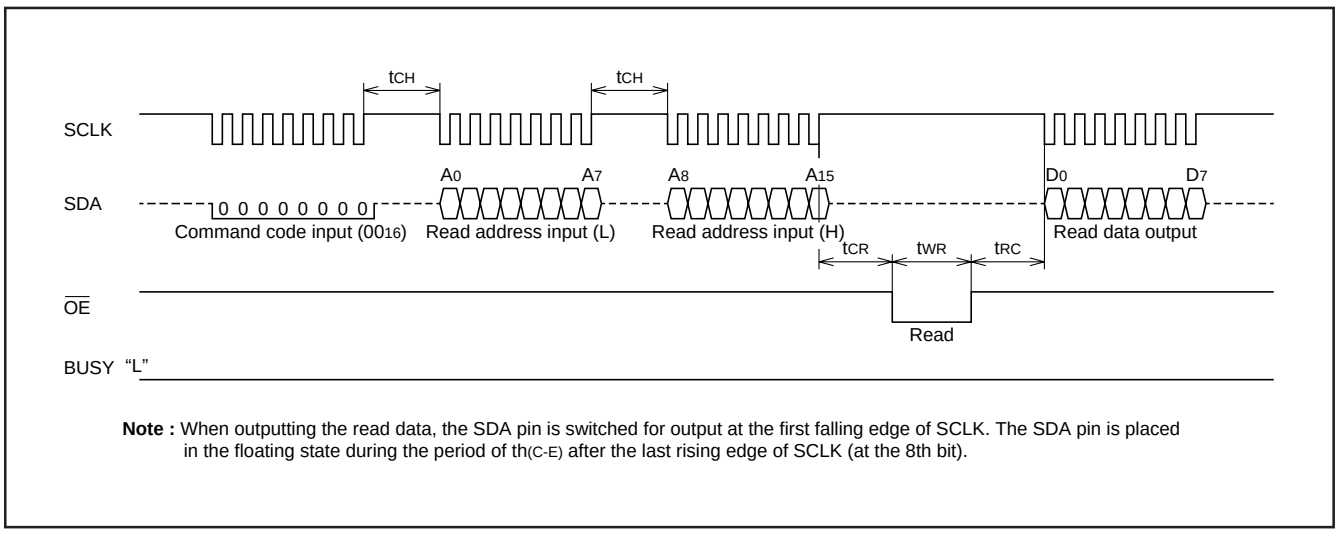
In the first transfer, the user inputs the command code. This is followed by address input and data input/output according to the contents of the command. Table 26 shows the software commands used in the serial I/O mode. The following explains each software command.

Table 26 Software command (serial I/O mode)

Number of transfers / Command	First command code input	Second	Third	Fourth
Read	00_{16}	Read address L (Input)	Read address H (Input)	Read data (Output)
Program	40_{16}	Program address L (Input)	Program address H (Input)	Program data (Input)
Program verify	$C0_{16}$	Verify data (Output)	————	————
Erase	20_{16}	20_{16} (Input)	————	————
Erase verify	$A0_{16}$	Verify address L (Input)	Verify address H (Input)	Verify data (Output)
Error check	80_{16}	Error code (Output)	————	————

● **Read command**

Input command code 00_{16} in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the M38869FFAHP/GP reads out the contents of the specified address, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the read data that has been latched into the data latch is serially output from the SDA pin.



Note : When outputting the read data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 73 Timings during reading

● **Program command**

Input command code 40_{16} in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and then program data. Programming is initiated at the last rising edge of the serial clock during program data transfer. The BUSY pin is driven high during program operation. Programming is completed within 10 μs as measured by the internal timer, and the BUSY pin is pulled low.

Note : A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in the verification, the user must repeatedly execute the program command until the pass in the verification. Refer to Figure 71 for the programming flowchart.

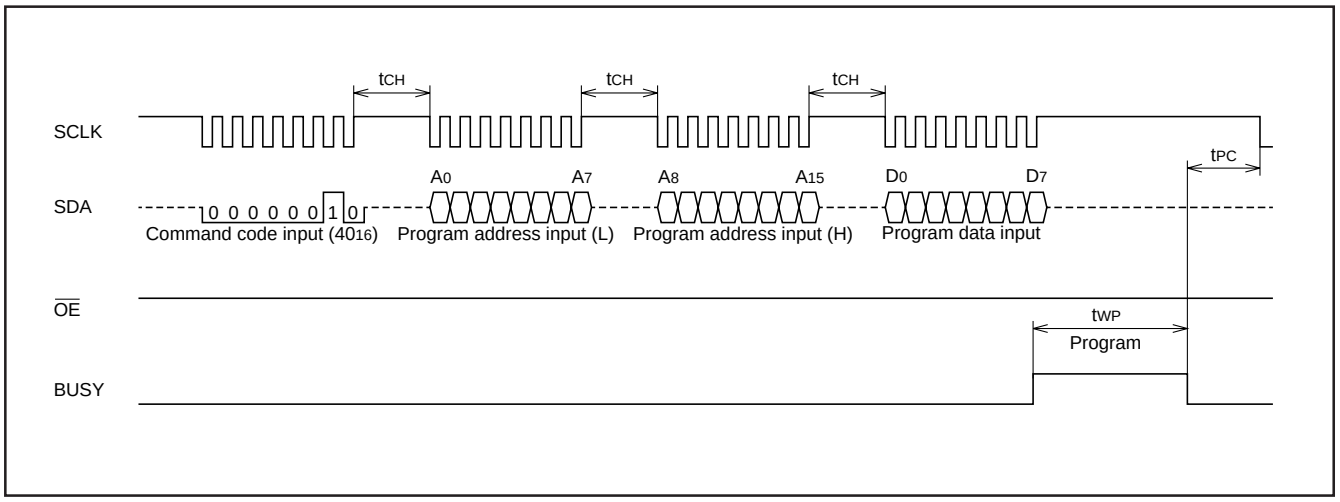
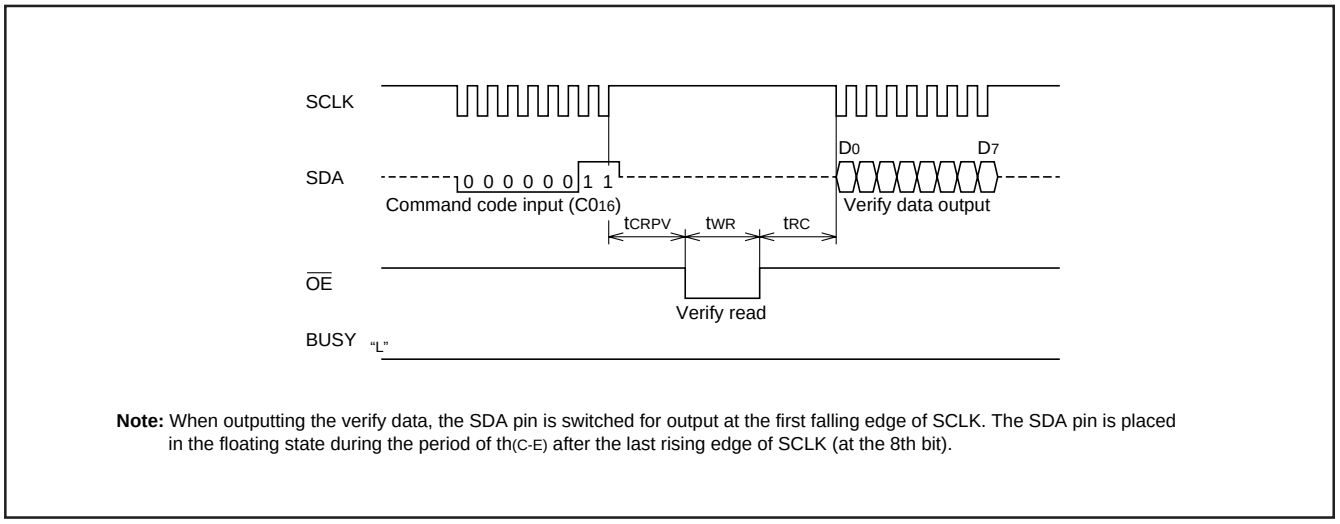


Fig. 74 Timings during programming

● **Program verify command**

Input command code $C0_{16}$ in the first transfer. Proceed and drive the $\overline{OE}$ pin low. When this is done, The M38869FFAHP/GP verify-reads the programmed address's contents, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.



Note: When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 75 Timings during program verify

● **Erase command**

Input command code 20_{16} in the first transfer and command code 20_{16} again in the second transfer. When this is done, the M38869FFAHP/GP executes an erase command. Erase is initiated at the last rising edge of the serial clock. The BUSY pin is driven high during the erase operation. Erase is completed within 9.5 ms as measured by the internal timer, and the BUSY pin is pulled low. Note that data 00_{16} must be written to all memory locations before executing the erase command.

Note: A erase operation is not completed by executing the erase command once. Always be sure to execute a erase verify command after executing the erase command. When the failure is found in the verification, the user must repeatedly execute the erase command until the pass in the verification. Refer to Figure 71 for the erase flowchart.

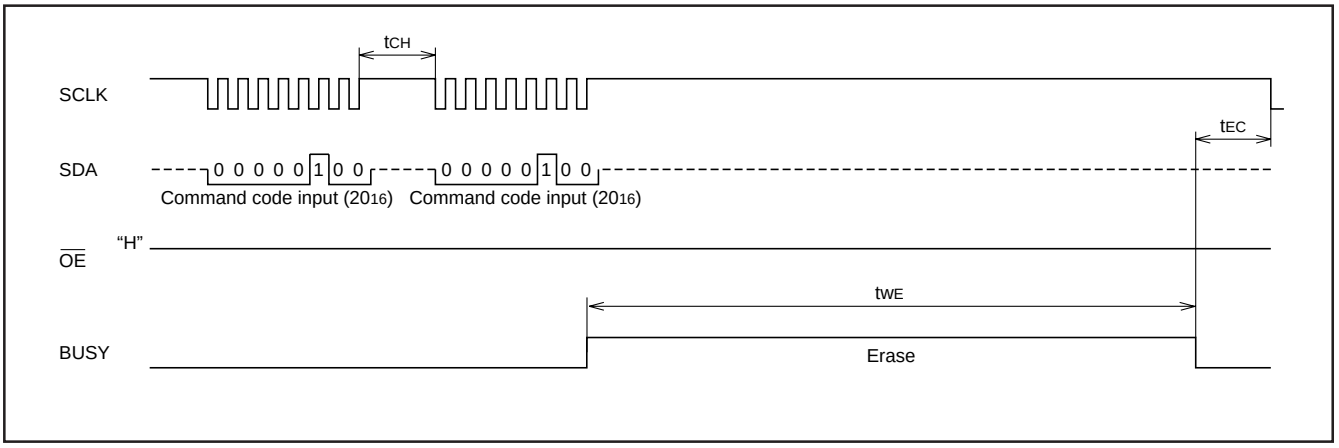
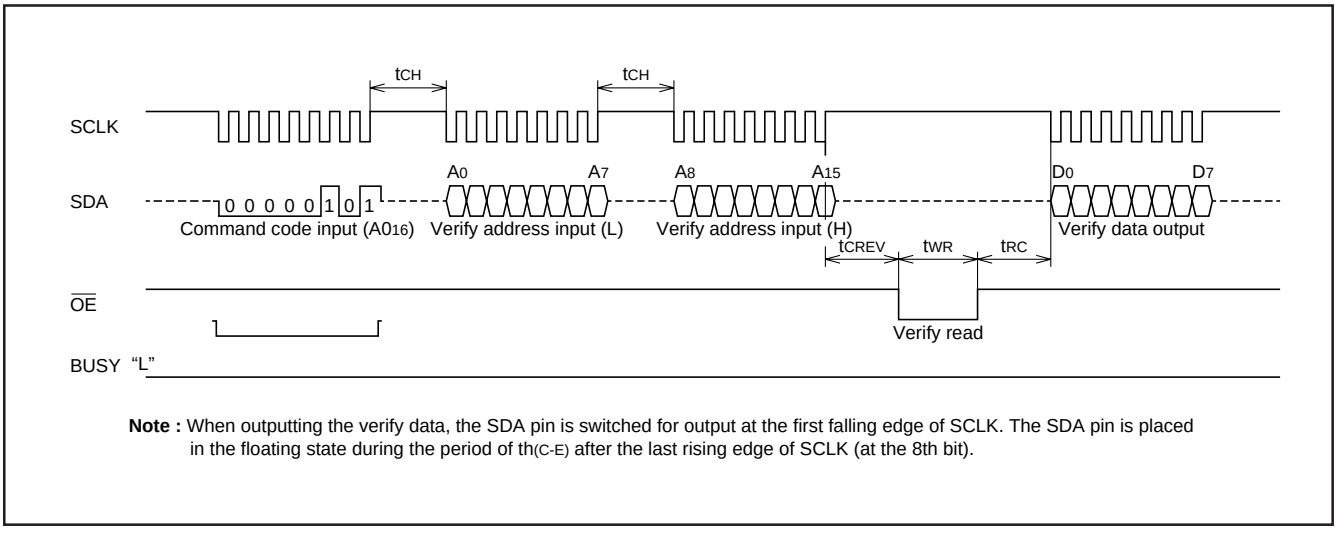


Fig. 76 Timings at erasing

● **Erase verify command**

The user must verify the contents of all addresses after completing the erase command. Input command code $A0_{16}$ in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the M38869FFAHP/GP reads out the contents of the specified address, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.

Note: If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data 00_{16} to memory locations before erasing.



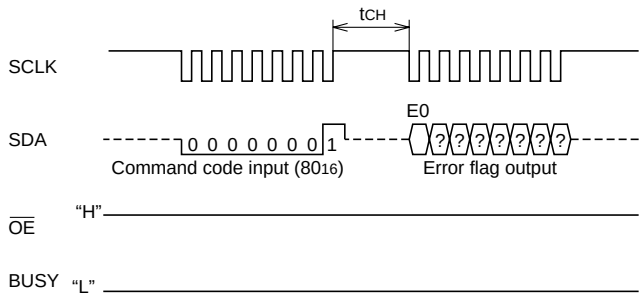
Note : When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 77 Timings during erase verify

● **Error check command**

Input command code 80_{16} in the first transfer, and the M38869FFAHP/GP outputs error information from the SDA pin, beginning at the next falling edge of the serial clock. If the LSB bit of the 8-bit error information is 1, it indicates that a command error has occurred. A command error means that some invalid commands other than commands shown in Table 26 has been input.

When a command error occurs, the serial communication circuit sets the corresponding flag and stops functioning to avoid an erroneous programming or erase. When being placed in this state, the serial communication circuit does not accept the subsequent serial clock and data (even including an error check command). Therefore, if the user wants to execute an error check command, temporarily drop the V_{PP} pin input to the $V_{PP}L$ level to terminate the serial input/output mode. Then, place the M38869FFAHP/GP into the serial I/O mode back again. The serial communication circuit is reset by this operation and is ready to accept commands. The error flag alone is not cleared by this operation, so the user can examine the serial communication circuit's error conditions before reset. This examination is done by the first execution of an error check command after the reset. The error flag is cleared when the user has executed the error check command. Because the error flag is undefined immediately after power-on, always be sure to execute the error check command.



Note: When outputting the error flag, the SDA pin is switched for output at the first falling edge of the serial clock. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of the serial clock (at the 8th bit).

Fig. 78 Timings at error checking

Note: The programming/erasing algorithm flow chart of the serial I/O mode is the same as that of the parallel I/O mode. Refer to Figure 71.

DC ELECTRICAL CHARACTERISTICS (Ta = 25 °C, Vcc = 5 V ± 10 %, Vpp = 11.7 to 12.6 V, unless otherwise noted)

Icc, Ipp-relevant standards during read, program, and erase are the same as in the parallel input/output mode. VIH, VIL, VOH, VOL, IIH, and IIL for the SCLK, SDA, BUSY, $\overline{OE}$ pins conform to the microcomputer modes.

Table 27 AC Electrical characteristics
(Ta = 25 °C, Vcc = 5 V ± 10 %, Vpp = 11.7 to 12.6 V, f(XIN) = 10 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tCH	Serial transmission interval	500(Note 1)		ns
tCR	Read waiting time after transmission	500(Note 1)		ns
tWR	Read pulse width	400(Note 2)		ns
tRC	Transfer waiting time after read	500(Note 1)		ns
tCRPV	Waiting time before program verify	6		µs
tWP	Programming time		10	µs
tPC	Transfer waiting time after programming	500(Note 1)		ns
tCREV	Waiting time before erase verify	6		ns
tWE	Erase time		9.5	ns
tEC	Transfer waiting time after erase	500(Note 1)		ns
tc(CK)	SCLK input cycle time	250		ns
tw(CKH)	SCLK high-level pulse width	100		ns
tw(CKL)	SCLK low-level pulse width	100		ns
tr(CK)	SCLK rise time	20		ns
tf(CK)	SCLK fall time	20		ns
td(C-Q)	SDA output delay time	0	90	ns
th(C-Q)	SDA output hold time	0		ns
th(C-E)	SDA output hold time (only the 8th bit)	150(Note 3)	250(Note 4)	ns
tsu(D-C)	SDA input set up time	30		
th(C-D)	SDA input hold time	90		

Notes 1: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 1.

Formula 1 : $\frac{5000}{f(X_{IN})} \times 10^6$

2: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 2.

Formula 2 : $\frac{4000}{f(X_{IN})} \times 10^6$

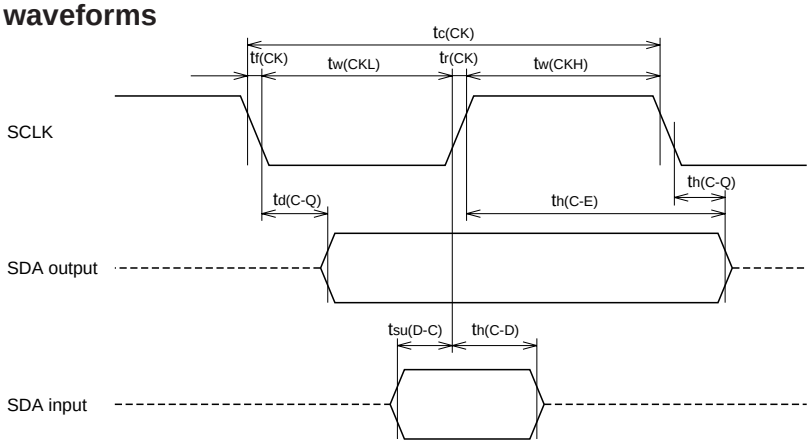
3: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 3.

Formula 3 : $\frac{1500}{f(X_{IN})} \times 10^6$

4: When f(XIN) = 10 MHz or less, calculate the minimum value according to formula 4

Formula 4 : $\frac{2500}{f(X_{IN})} \times 10^6$

AC waveforms



Test conditions for AC characteristics

- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Input timing voltage : VIL = 0.2 Vcc, VIH = 0.8 Vcc

(3) Flash memory mode 3 (CPU reprogramming mode)

The M38869FFAHP/GP has the CPU reprogramming mode where a built-in flash memory is handled by the central processing unit (CPU).

In CPU reprogramming mode, the flash memory is handled by writing and reading to/from the flash memory control register (see Figure 79) and the flash command register (see Figure 80).

The CNVSS pin is used as the VPP power supply pin in CPU reprogramming mode. It is necessary to apply the power-supply voltage of VPPH from the external to this pin.

Functional Outline (CPU reprogramming mode)

Figure 79 shows the flash memory control register bit configuration. Figure 80 shows the flash command register bit configuration.

Bit 0 of the flash memory control register is the CPU reprogramming mode select bit. When this bit is set to “1” and VPPH is applied to the CNVss/VPP pin, the CPU reprogramming mode is selected. Whether the CPU reprogramming mode is realized or not is judged by reading the CPU reprogramming mode monitor flag (bit 2 of the flash memory control register).

Bit 1 is a busy flag which becomes “1” during erase and program execution.

Whether these operations have been completed or not is judged by checking this flag after each command of erase and the program is executed.

Bits 4, 5 of the flash memory control register are the erase/program area select bits. These bits specify an area where erase and program is operated. When the erase command is executed after an area is specified by these bits, only the specified area is erased. Only for the specified area, programming is enabled; for the other areas, programming is disabled.

When CPU reprogramming mode is valid, the area where is not specified by the erase/program area select bits cannot be read out.

Transfer CPU reprogramming mode control program to internal RAM before entering the CPU reprogramming mode, and then execute this program on internal RAM.

If an interrupt occurs while this program is being executed, the flash memory area is accessed, but normally operation cannot be performed because the flash memory area cannot be read out. During CPU reprogramming mode control program execution, execute the processing such as interrupt disabled, etc.

Figure 81 shows the CPU mode register bit configuration in the CPU reprogramming mode. Set bits 1 and 0 to “00” (single-chip mode) in the CPU reprogramming mode.

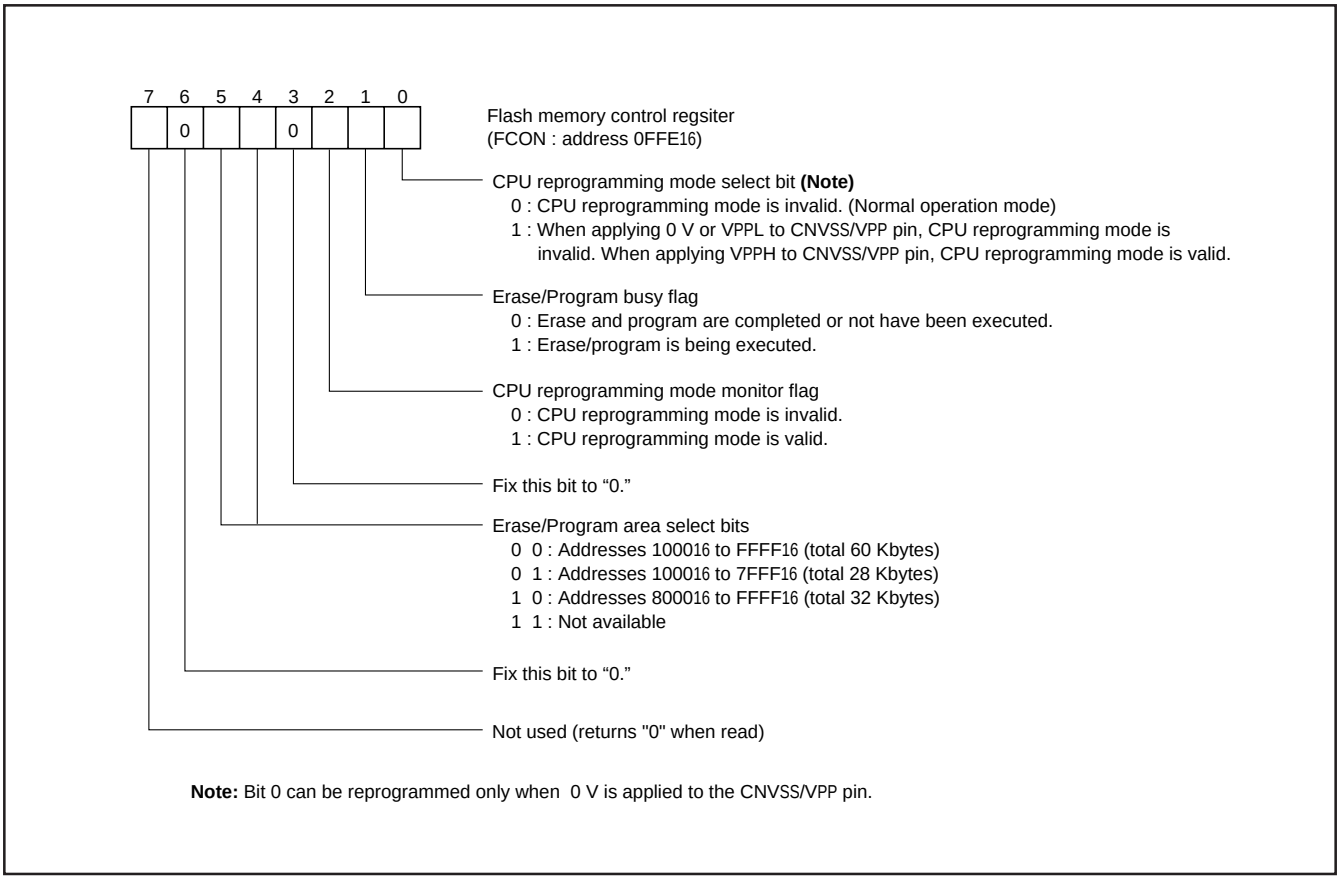


Fig. 79 Flash memory control register bit configuration

● **CPU reprogramming mode operation procedure**

The operation procedure in CPU reprogramming mode is described below.

< Beginning procedure >

① Apply 0 V to the CNVss/VPP pin for reset release.
② After CPU reprogramming mode control program is transferred to internal RAM, jump to this control program on RAM. (The following operations are controlled by this control program).
③ Set "1" to the CPU reprogramming mode select bit.
④ Apply VPPH to the CNVSS/VPP pin.
⑤ Wait till CNVSS/VPP pin becomes 12 V.
⑥ Read the CPU reprogramming mode monitor flag to confirm whether the CPU reprogramming mode is valid.
⑦ The operation of the flash memory is executed by software-command-writing to the flash command register .

Note: The following are necessary other than this:
- •Control for data which is input from the external (serial I/O etc.) and to be programmed to the flash memory
- •Initial setting for ports etc.
- •Writing to the watchdog timer

< Release procedure >

① Apply 0V to the CNVSS/VPP pin.
② Wait till CNVSS/VPP pin becomes 0V.
③ Set the CPU reprogramming mode select bit to "0."

Each software command is explained as follows.

● **Read command**

When "00_{16}" is written to the flash command register, the M38869FFAHP/GP enters the read mode. The contents of the corresponding address can be read by reading the flash memory (For instance, with the LDA instruction etc.) under this condition.
The read mode is maintained until another command code is written to the flash command register. Accordingly, after setting the read mode once, the contents of the flash memory can continuously be read.
After reset and after the reset command is executed, the read mode is set.

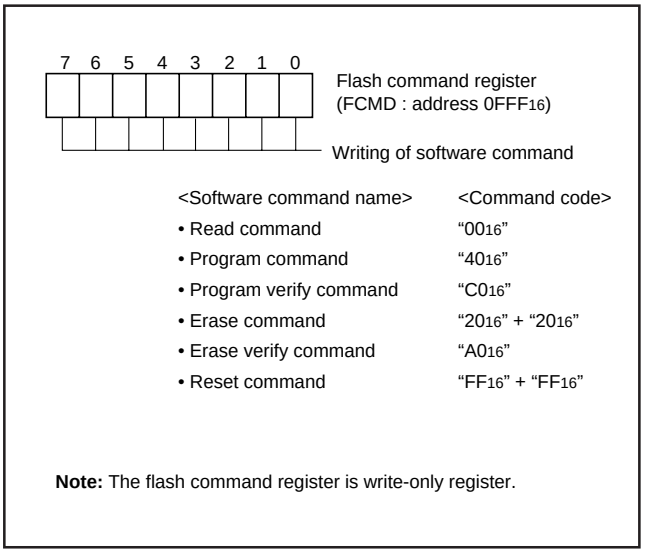


Fig. 80 Flash command register bit configuration

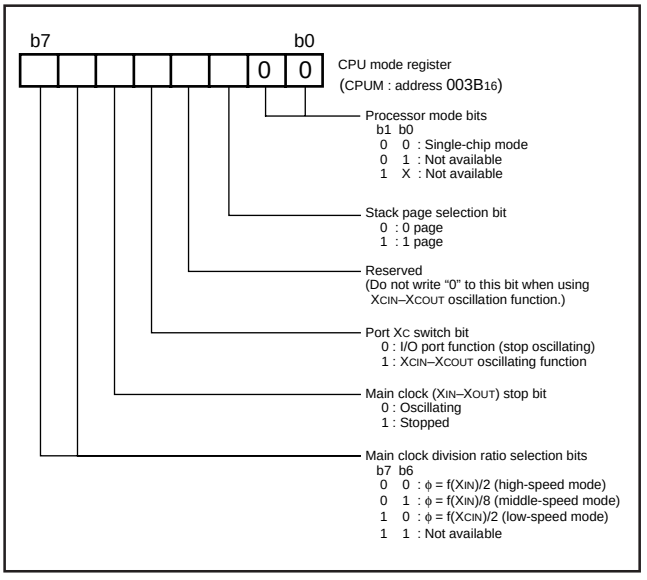


Fig. 81 CPU mode register bit configuration in CPU rewriting mode

● **Program command**

When "40$_{16}$" is written to the flash command register, the M38869FFAHP/GP enters the program mode.

Subsequently to this, if the instruction (for instance, STA instruction) for writing byte data in the address to be programmed is executed, the control circuit of the flash memory executes the program. The erase/program busy flag of the flash memory control register is set to "1" when the program starts, and becomes "0" when the program is completed. Accordingly, after the write instruction is executed, CPU can recognize the completion of the program by polling this bit.

The programmed area must be specified beforehand by the erase/program area select bits.

During programming, watchdog timer stops with "FFFF$_{16}$" set.

Note: A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 82 for the flow chart of the programming.

● **Program verify command**

When "C0$_{16}$" is written to the flash command register, the M38869FFAHP/GP enters the program verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified (i.e., previously programmed address), the contents which has been written to the address actually is read.

CPU compares this read data with data which has been written by the previous program command. In consequence of the comparison, if not agreeing, the operation of "program → program verify" must be executed again.

● **Erase command**

When writing "20$_{16}$" twice continuously to the flash command register, the flash memory control circuit performs erase to the area specified beforehand by the erase/program area select bits.

Erase/program busy flag of the flash memory control register becomes "1" when erase begins, and it becomes "0" when erase completes. Accordingly, CPU can recognize the completion of erase by polling this bit.

Data "00$_{16}$" must be written to all areas to be erased by the program and the program verify commands before the erase command is executed.

During erasing, watchdog timer stops with "FFFF$_{16}$" set.

Note: The erasing operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 82 for the erasing flowchart.

● **Erase verify command**

When "A0$_{16}$" is written to the flash command register, the M38869FFAHP/GP enters the erase verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified, the contents of the address is read.

CPU must erase and verify to all erased areas in a unit of address.

If the address of which data is not "FF$_{16}$" (i.e., data is not erased) is found, it is necessary to discontinue erasure verification there, and execute the operation of "erase → erase verify" again.

Note: By executing the operation of "erase → erase verify" again when the memory not erased is found. It is unnecessary to write data "00$_{16}$" before erasing in this case.

● **Reset command**

The reset command is a command to discontinue the program or erase command on the way. When "FF$_{16}$" is written to the command register two times continuously after "40$_{16}$" or "20$_{16}$" is written to the flash command register, the program, or erase command becomes invalid (reset), and the M38869FFAHP/GP enters the reset mode.

The contents of the memory does not change even if the reset command is executed.

DC Electric Characteristics

Note: The characteristic concerning the flash memory part are the same as the characteristic of the parallel I/O mode.

AC Electric Characteristics

Note: The characteristics are the same as the characteristic of the microcomputer mode.

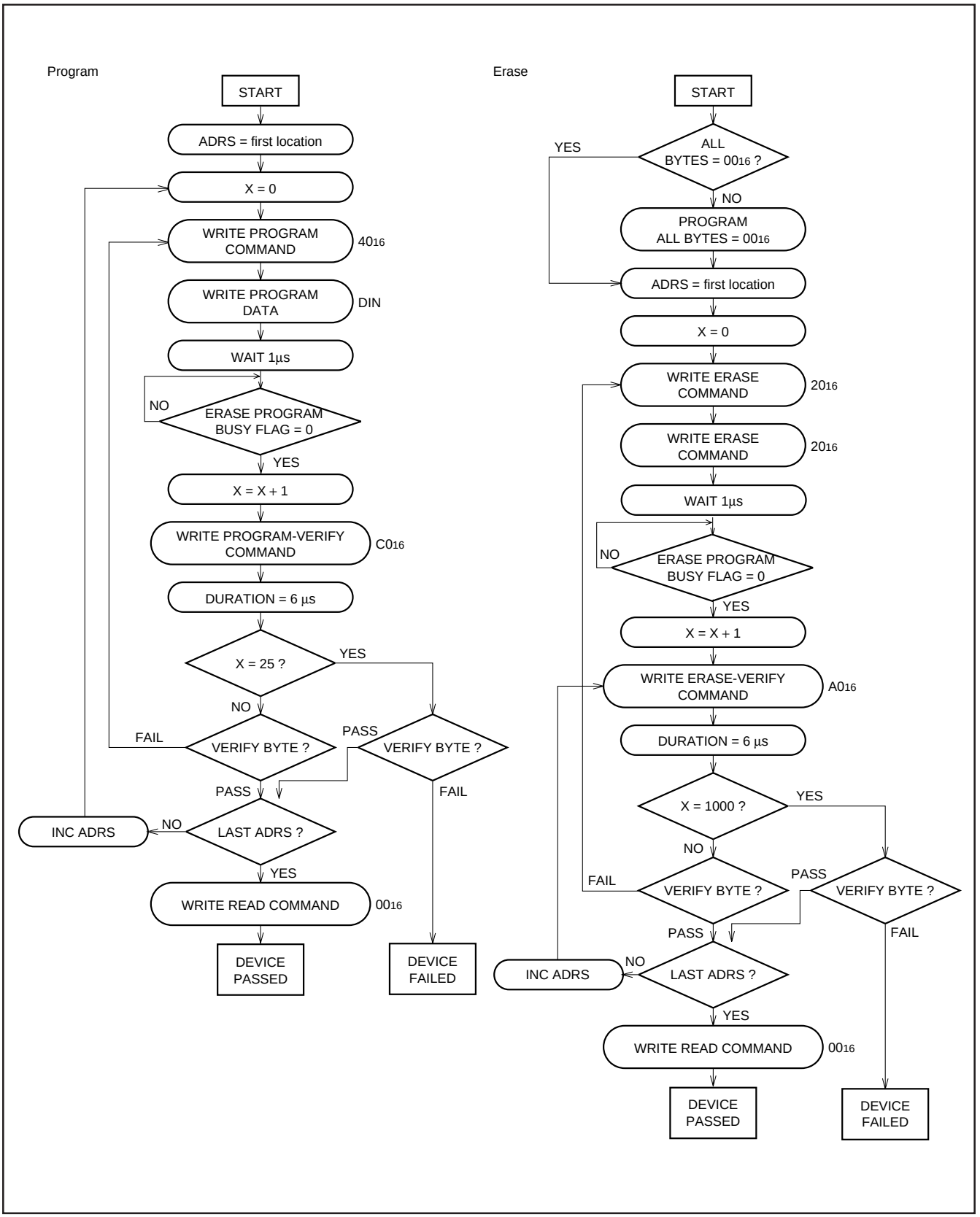


Fig. 82 Flowchart of program/erase operation at CPU reprogramming mode

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY1}}$ output enable bit to "1."

Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.

When in serial I/O1 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is "H."

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes rapidly poor under the V_{CC} = 4.0 V or less condition; a supply voltage of $V_{CC} \geq 4.0$ V is recommended. When a D-A converter is not used, set all values of D-Ai conversion registers (i=1, 2) to "00_{16}."

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is half of the XIN period in high-speed mode.

When the $\overline{\text{ONW}}$ function is used in modes other than single-chip mode, the period of the internal clock ϕ may be four times that of the XIN.

NOTES ON USAGE

Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin), between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin), and between program power source pin (CNV_{SS}/V_{PP}) and GND pin for flash memory version when on-board reprogramming is executed. Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF–0.1 μF is recommended.

EPROM version/One Time PROM version/ Flash memory version

The CNV_{SS} pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNV_{SS} pin and V_{SS} pin or V_{CC} pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNV_{SS} pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

Erasing of Flash memory version

Set addresses 01000_{16} to $0FFFF_{16}$ as memory area for erasing in the parallel serial I/O mode and the serial I/O mode. If the memory area for erasing is set to mistaken area, the product may be permanently damaged.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

DATA REQUIRED FOR One Time PROM PROGRAMMING ORDERS

The following are necessary when ordering a PROM programming service:

1. ROM Programming Confirmation Form
2. Mark Specification Form
3. Data to be programmed to PROM, in EPROM form (three identical copies)

ELECTRICAL CHARACTERISTICS

Table 28 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltages **(Note 1)**	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_{CC}	Power source voltages **(Note 2)**		–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P7_0$–$P7_7$		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS} **(Note 3)**		–0.3 to 7	V
V_I	Input voltage CNV_{SS} **(Note 4)**		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS} **(Note 5)**		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P7_0$–$P7_7$		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	500	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Notes 1: M38867M8A, M38867E8A
2: M38869M8A, M38869MCA, M38869MFA, M38869FFA
3: M38867M8A
4: M38869M8A, M38869MCA, M38869MFA
5: M38867E8A, M38869FFA

Table 29 Recommended operating conditions
(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (except flash memory version)	f(X_{IN}) ≤ 4.1 MHz	2.7	5.0	5.5	V
		f(X_{IN}) = 10 MHz	4.0	5.0	5.5	
V_{CC}	Power source voltage (flash memory version)		4.0	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage	when A-D converter is used	2.0		V_{CC}	V
		when D-A converter is used	2.7		V_{CC}	
AV_{SS}	Analog power source voltage			0		V
V_{IA}	A-D converter input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$, $P4_1$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P7_6$, $P7_7$	0.8V_{CC}		5.5	V
V_{IH}	"H" input voltage (when I^2C-BUS input level is selected)	S_{DA}, S_{CL}	0.7V_{CC}		5.5	V
V_{IH}	"H" input voltage (when SMBUS input level is selected)	S_{DA}, S_{CL}	1.4		5.5	V
V_{IH}	"H" input voltage (when CMOS input level is selected)	$P4_2$–$P4_6$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S0}$, $\overline{S1}$, A_0	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (when CMOS input level is selected)	$P7_0$–$P7_5$	0.8V_{CC}		5.5	V
V_{IH}	"H" input voltage (when TTL input level is selected)	$P4_2$–$P4_6$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S0}$, $\overline{S1}$, A_0 **(Note)**	2.0		V_{CC}	V
V_{IH}	"H" input voltage (when TTL input level is selected)	$P7_0$–$P7_5$ **(Note)**	2.0		5.5	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}, X_{CIN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage (when I^2C-BUS input level is selected)	S_{DA}, S_{CL}	0		0.3V_{CC}	V
V_{IL}	"L" input voltage (when SMBUS input level is selected)	S_{DA}, S_{CL}	0		0.6	V
V_{IL}	"L" input voltage (when CMOS input level is selected)	$P4_2$–$P4_6$, $P7_0$–$P7_5$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S0}$, $\overline{S1}$, A_0	0		0.2V_{CC}	V
V_{IL}	"L" input voltage (when TTL input level is selected)	$P4_2$–$P4_6$, $P7_0$–$P7_5$, DQ_0–DQ_7, $\overline{W}$, $\overline{R}$, $\overline{S0}$, $\overline{S1}$, A_0 **(Note)**	0		0.8	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}, X_{CIN}	0		0.16V_{CC}	V

Note : When V_{CC} is 4.0 to 5.5 V.

Table 30 Recommended operating conditions

(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ **(Note)**			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note)**			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ **(Note)**			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_4$–$P2_7$ **(Note)**	In single-chip mode			80	mA
		In memory expansion mode In microprocessor mode			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ **(Note)**			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ **(Note)**			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note)**			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ **(Note)**			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_4$–$P2_7$ **(Note)**	In single-chip mode			40	mA
		In memory expansion mode In microprocessor mode			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ **(Note)**			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 31 Recommended operating conditions

(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note 1)**			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ **(Note 1)**			10	mA
$I_{OL(peak)}$	"L" peak output current $P2_4$–$P2_7$ **(Note 1)**	In single-chip mode			20	mA
		In memory expansion mode In microprocessor mode			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note 2)**			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ **(Note 2)**			5	mA
$I_{OL(avg)}$	"L" peak output current $P2_4$–$P2_7$ **(Note 2)**	In single-chip mode			15	mA
		In memory expansion mode In microprocessor mode			5	mA
$f(X_{IN})$	Main clock input oscillation frequency **(Note 3)**	High-speed mode 4.0 V≤ V_{CC} ≤ 5.5 V			10	MHz
		High-speed mode 2.7 V≤ V_{CC} ≤ 4.0 V			4.5 V_{CC}–8	MHz
		Middle-speed mode 4.0 V≤ V_{CC} ≤ 5.5 V			10	MHz
		Middle-speed mode 2.7 V≤ V_{CC} ≤ 4.0 V **(Note 5)**			10	MHz
		Middle-speed mode 2.7 V≤ V_{CC} ≤ 4.0 V **(Note 5)**			4.5 V_{CC}–8	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 3, 4)**			32.768	50	kHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.
4: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.
5: When using the timer X/Y, timer 1/2, serial I/O1, serial I/O2, A-D converter, comparator, and PWM, set the main clock input oscillation frequency to the max. 4.5V_{CC}–8 (MHz).

Table 32 Electrical characteristics

(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note)**	I_{OH} = –10 mA V_{CC} = 4.0–5.5 V	V_{CC}–2.0			V
		I_{OH} = –1.0 mA V_{CC} = 2.7–5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 10 mA V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 1.6 mA V_{CC} = 2.7–5.5 V			0.4	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1 INT_{20}–INT_{40}, INT_{21}–INT_{41} $P3_0$–$P3_7$			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{CC} (Pin floating. Pull-up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{SS} (Pin floating. Pull-up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$,CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA
I_{IL}	"L" input current $P3_0$–$P3_7$ (at Pull-up)	V_I = V_{SS} V_{CC} = 4.0–5.5 V	–20	–60	–120	µA
		V_I = V_{SS} V_{CC} = 2.7–5.5 V	–10			µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V

Note: $P0_0$–$P0_3$ are measured when the $P0_0$–$P0_3$ output structure selection bit of the port control register 1 (bit 0 of address $002E_{16}$) is "0".
$P0_4$–$P0_7$ are measured when the $P0_4$–$P0_7$ output structure selection bit of the port control register 1 (bit 1 of address $002E_{16}$) is "0".
$P1_0$–$P1_3$ are measured when the $P1_0$–$P1_3$ output structure selection bit of the port control register 1 (bit 2 of address $002E_{16}$) is "0".
$P1_4$–$P1_7$ are measured when the $P1_4$–$P1_7$ output structure selection bit of the port control register 1 (bit 3 of address $002E_{16}$) is "0".
$P4_2$, $P4_3$, $P4_4$, and $P4_6$ are measured when the P4 output structure selection bit of the port control register 2 (bit 2 of address $002F_{16}$) is "0".
$P4_5$ is measured when the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".

Table 33 Electrical characteristics
(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 10 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			8.0	15	mA
		High-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.8	13	mA
		High-speed mode $f(X_{IN})$ = 10 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			1.6		mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			60	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			20	40	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			20	55	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			8.0	20.0	µA
		Middle-speed mode $f(X_{IN})$ = 10 MHz $f(X_{CIN})$ = stopped Output transistors “off”			4.0	7.0	mA
		Middle-speed mode $f(X_{IN})$ = 10 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			1.5		mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 10 MHz			800		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 34 A-D converter characteristics (1)
(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, V_{REF} = 2.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)
10-bit A-D mode (when conversion mode selection bit (bit 7 of address 003816) is "0")

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	bit
–	Absolute accuracy (excluding quantization error)		V_{CC} = V_{REF} = 5.0 V			±4	LSB
t_{CONV}	Conversion time					61	2tc(X_{IN})
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{VREF}	Reference power source input current	at A-D converter operated	V_{REF} = 5.0 V	50	150	200	µA
		at A-D converter stopped	V_{REF} = 5.0 V			5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

Table 35 A-D converter characteristics (2)
(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, V_{REF} = 2.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)
8-bit A-D mode (when conversion mode selection bit (bit 7 of address 003816) is "1")

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					8	bit
–	Absolute accuracy (excluding quantization error)		V_{CC} = V_{REF} = 5.0 V			±2	LSB
t_{CONV}	Conversion time					50	2tc(X_{IN})
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{VREF}	Reference power source input current	at A-D converter operated	V_{REF} = 5.0 V	50	150	200	µA
		at A-D converter stopped	V_{REF} = 5.0 V			5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

Table 36 D-A converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					8	Bits
–	Absolute accuracy	V_{CC} = 4.0–5.5 V				1.0	%
		V_{CC} = 2.7–4.0 V				2.5	%
tsu	Setting time					3	µs
RO	Output resistor			1	2.5	4	kΩ
I_{VREF}	Reference power source input current (Note 1)					3.2	mA

Note 1: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}".

Table 37 Comparator characteristics
(V_{CC} = 2.7 to 5.5 V, V_{CC} = 4.0 to 5.5 V for flash memory version, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Absolute accuracy	1LSB = V_{CC}/16			1/2	LSB
T_{CONV}	Conversion time	at 10 MHz operating			2.8	µs
		at 8 MHz operating			3.5	µs
		at 4 MHz operating			7	µs
V_{IA}	Analog input voltage		0		V_{CC}	V
I_{IA}	Analog input current				5.0	µA
R_{LADDER}	Ladder resistor		20	40	50	kΩ
CMP_{REF}	Internal reference voltage			29V_{CC} /32		V
	External reference input voltage		V_{CC}/32		V_{CC}	V

TIMING REQUIREMENTS

Table 38 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	Main clock input cycle time	100			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	40			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	40			ns
$t_{C(XCIN)}$	Sub-clock input cycle time	20			µs
$t_{WH(XCIN)}$	Sub-clock input “H” pulse width	5			µs
$t_{WL(XCIN)}$	Sub-clock input “L” pulse width	5			µs
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{WH(INT)}$	INT_0, INT_1, INT_{20}, INT_{30}, INT_{40}, INT_{21}, INT_{31}, INT_{41} input “H” pulse width	80			ns
$t_{WL(INT)}$	INT_0, INT_1, INT_{20}, INT_{30}, INT_{40}, INT_{21}, INT_{31}, INT_{41} input “L” pulse width	80			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time **(Note)**	800			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width **(Note)**	370			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width **(Note)**	370			ns
$t_{su(RxD-SCLK1)}$	Serial I/O1 input setup time	220			ns
$t_{h(SCLK1-RxD)}$	Serial I/O1 input hold time	100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SIN2-SCLK2)}$	Serial I/O2 input setup time	200			ns
$t_{h(SCLK2-SIN2)}$	Serial I/O2 input hold time	200			ns

Note : When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 39 Timing requirements (2)

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(X_{IN})}$	Main clock input cycle time	1000/(4.5V_{CC}–8)			ns
$t_{WH(X_{IN})}$	Main clock input “H” pulse width	400/(4.5V_{CC}–8)			ns
$t_{WL(X_{IN})}$	Main clock input “L” pulse width	400/(4.5V_{CC}–8)			ns
$t_{C(X_{CIN})}$	Sub-clock input cycle time	20			µs
$t_{WH(X_{CIN})}$	Sub-clock input “H” pulse width	5			µs
$t_{WL(X_{CIN})}$	Sub-clock input “L” pulse width	5			µs
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	230			ns
$t_{WH(INT)}$	INT_0, INT_1, INT_{20}, INT_{30}, INT_{40}, INT_{21}, INT_{31}, INT_{41} input “H” pulse width	230			ns
$t_{WL(INT)}$	INT_0, INT_1, INT_{20}, INT_{30}, INT_{40}, INT_{21}, INT_{31}, INT_{41} input “L” pulse width	230			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time **(Note)**	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width **(Note)**	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width **(Note)**	950			ns
$t_{su(R_xD\text{-}SCLK1)}$	Serial I/O1 input setup time	400			ns
$t_{h(SCLK1\text{-}R_xD)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SIN2\text{-}SCLK2)}$	Serial I/O2 input setup time	400			ns
$t_{h(SCLK2\text{-}SIN2)}$	Serial I/O2 input hold time	300			ns

Note : When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 40 Timing requirements for system bus interface
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{su} (S-R)	$\overline{S_0}$, $\overline{S_1}$ setup time	0			ns
t_{su} (S-W)	$\overline{S_0}$, $\overline{S_1}$ setup time	0			ns
t_h (R-S)	$\overline{S_0}$, $\overline{S_1}$ hold time	0			ns
t_h (W-S)	$\overline{S_0}$, $\overline{S_1}$ hold time	0			ns
t_{su} (A-R)	A0 setup time	10			ns
t_{su} (A-W)	A0 setup time	10			ns
t_h (R-A)	A0 hold time	0			ns
t_h (W-A)	A0 hold time	0			ns
t_w (R)	Read pulse width	120			ns
t_w (W)	Write pulse width	120			ns
t_{su} (D-W)	Before write data input setup time	50			ns
t_h (W-D)	After write data input hold time	0			ns

Table 41 Timing requirements for system bus interface
(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{su} (S-R)	$\overline{S_0}$, $\overline{S_1}$ setup time	0			ns
t_{su} (S-W)	$\overline{S_0}$, $\overline{S_1}$ setup time	0			ns
t_h (R-S)	$\overline{S_0}$, $\overline{S_1}$ hold time	0			ns
t_h (W-S)	$\overline{S_0}$, $\overline{S_1}$ hold time	0			ns
t_{su} (A-R)	A0 setup time	30			ns
t_{su} (A-W)	A0 setup time	30			ns
t_h (R-A)	A0 hold time	0			ns
t_h (W-A)	A0 hold time	0			ns
t_w (R)	Read pulse width	250			ns
t_w (W)	Write pulse width	250			ns
t_{su} (D-W)	Before write data input setup time	130			ns
t_h (W-D)	After write data input hold time	0			ns

Table 42 Switching characteristics 1
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (S_{CLK1})	Serial I/O1 clock output “H” pulse width	Fig. 83	$t_{C(SCLK1)}$/2–30			ns
t_{WL} (S_{CLK1})	Serial I/O1 clock output “L” pulse width		$t_{C(SCLK1)}$/2–30			ns
td (S_{CLK1}-TxD)	Serial I/O1 output delay time **(Note 1)**				140	ns
tv (S_{CLK1}-TxD)	Serial I/O1 output valid time **(Note 1)**		–30			ns
tr (S_{CLK1})	Serial I/O1 clock output rising time				30	ns
tf (S_{CLK1})	Serial I/O1 clock output falling time				30	ns
t_{WH} (S_{CLK2})	Serial I/O2 clock output “H” pulse width	Fig. 84	$t_{C(SCLK2)}$/2–160			ns
t_{WL} (S_{CLK2})	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–160			ns
td (S_{CLK2}-S_{OUT2})	Serial I/O2 output delay time				200	ns
tv (S_{CLK2}-S_{OUT2})	Serial I/O2 output valid time		0			ns
tf (S_{CLK2})	Serial I/O2 clock output falling time				30	ns
tr (CMOS)	CMOS output rising time **(Note 2)**	Fig. 83		10	30	ns
tf (CMOS)	CMOS output falling time **(Note 2)**			10	30	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: The X_{OUT} pin is excluded.

Table 43 Switching characteristics 2
(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (S_{CLK1})	Serial I/O1 clock output “H” pulse width	Fig. 83	$t_{C(SCLK1)}$/2–50			ns
t_{WL} (S_{CLK1})	Serial I/O1 clock output “L” pulse width		$t_{C(SCLK1)}$/2–50			ns
td (S_{CLK1}-TxD)	Serial I/O1 output delay time **(Note 1)**				350	ns
tv (S_{CLK1}-TxD)	Serial I/O1 output valid time **(Note 1)**		–30			ns
tr (S_{CLK1})	Serial I/O1 clock output rising time				50	ns
tf (S_{CLK1})	Serial I/O1 clock output falling time				50	ns
t_{WH} (S_{CLK2})	Serial I/O2 clock output “H” pulse width	Fig. 84	$t_{C(SCLK2)}$/2–240			ns
t_{WL} (S_{CLK2})	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–240			ns
td (S_{CLK2}-S_{OUT2})	Serial I/O2 output delay time				400	ns
tv (S_{CLK2}-S_{OUT2})	Serial I/O2 output valid time		0			ns
tf (S_{CLK2})	Serial I/O2 clock output falling time				50	ns
tr (CMOS)	CMOS output rising time **(Note 2)**	Fig. 83		20	50	ns
tf (CMOS)	CMOS output falling time **(Note 2)**			20	50	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: The X_{OUT} pin is excluded.

Table 44 Switching characteristics for system bus interface
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_a(R-D)	After read data output enable time			80	ns
t_v(R-D)	After read data output disable time	0		30	ns
t_{PLH}(R-OBF)	After read OBF_{00}, OBF_{01}, OBF_{10} output propagation time			150	ns

Table 45 Switching characteristics for system bus interface
(V_{CC} =2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_a(R-D)	After read data output enable time			130	ns
t_v(R-D)	After read data output disable time	0		85	ns
t_{PLH}(R-OBF)	After read OBF_{00}, OBF_{01}, OBF_{10} output propagation time			300	ns

Table 46 Timing requirements in memory expansion mode and microprocessor mode
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, in high-speed mode, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{su} ($\overline{ONW}$-ϕ)	$\overline{ONW}$ input setup time	–20			ns
t_h (ϕ-$\overline{ONW}$)	$\overline{ONW}$ input hold time	–20			ns
t_{su} (DB-ϕ)	Data bus setup time	50			ns
t_h (ϕ-DB)	Data bus hold time	0			ns
t_{su} ($\overline{ONW}$-$\overline{RD}$), t_{su} ($\overline{ONW}$-$\overline{WR}$)	$\overline{ONW}$ input setup time	–20			ns
t_h ($\overline{RD}$-$\overline{ONW}$), t_h ($\overline{WR}$-$\overline{ONW}$)	$\overline{ONW}$ input hold time	–20			ns
t_{su} (DB-$\overline{RD}$)	Data bus setup time	50			ns
t_h ($\overline{RD}$-DB)	Data bus hold time	0			ns

Table 47 Switching characteristics in memory expansion mode and microprocessor mode
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, in high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_C(\phi)$	ϕ clock cycle time	Fig. 83		2$t_C(X_{IN})$		ns
$t_{WH}(\phi)$	ϕ clock “H” pulse width		$t_C(X_{IN})$–10			ns
$t_{WL}(\phi)$	ϕ clock “L” pulse width		$t_C(X_{IN})$–10			ns
$t_d(\phi$-AH)	AD_{15}–AD_8 delay time			16	35	ns
$t_d(\phi$-AL)	AD_7–AD_0 delay time			20	40	ns
$t_v(\phi$-AH)	AD_{15}–AD_8 valid time		2	5		ns
$t_v(\phi$-AL)	AD_7–AD_0 valid time		2	5		ns
$t_d(\phi$-SYNC)	SYNC delay time			16		ns
$t_v(\phi$-SYNC)	SYNC valid time			5		ns
$t_d(\phi$-DB)	Data bus delay time			15	30	ns
$t_v(\phi$-DB)	Data bus valid time		10			ns
$t_{WL}(\overline{RD})$, $t_{WL}(\overline{WR})$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_C(X_{IN})$–10			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (When one-wait is valid)		3$t_C(X_{IN})$–10			ns
t_d(AH-$\overline{RD}$), t_d(AH-$\overline{WR}$)	AD_{15}–AD_8 delay time		$t_C(X_{IN})$–35	$t_C(X_{IN})$–16		ns
t_d(AL-$\overline{RD}$), t_d(AL-$\overline{WR}$)	AD_7–AD_0 delay time		$t_C(X_{IN})$–40	$t_C(X_{IN})$–20		ns
t_v($\overline{RD}$-AH), t_v($\overline{WR}$-AH)	AD_{15}–AD_8 valid time		2	5		ns
t_v($\overline{RD}$-AL), t_v($\overline{WR}$-AL)	AD_7–AD_0 valid time		2	5		ns
t_d($\overline{WR}$-DB)	Data bus delay time			15	30	ns
t_v($\overline{WR}$-DB)	Data bus valid time		10			ns
t_d($\overline{RESET}$-$\overline{RESET_{OUT}}$)	$\overline{RESET_{OUT}}$ output delay time				200	ns
t_v(ϕ-$\overline{RESET_{OUT}}$)	$\overline{RESET_{OUT}}$ output valid time **(Note)**		0		100	ns

Note: The $\overline{RESET_{OUT}}$ output goes “H” in synchronized with the rise of the ϕ clock that is anywhere between a few cycles and 10-several cycles after $\overline{RESET}$ input goes “H”.

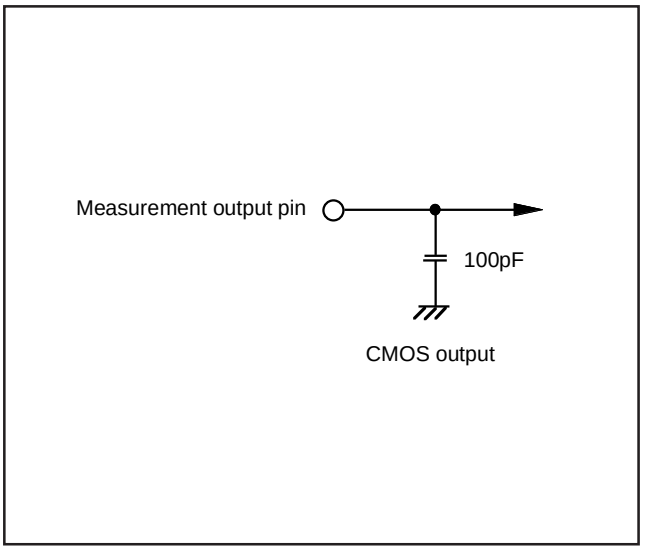


Fig. 83 Circuit for measuring output switching characteristics (1)

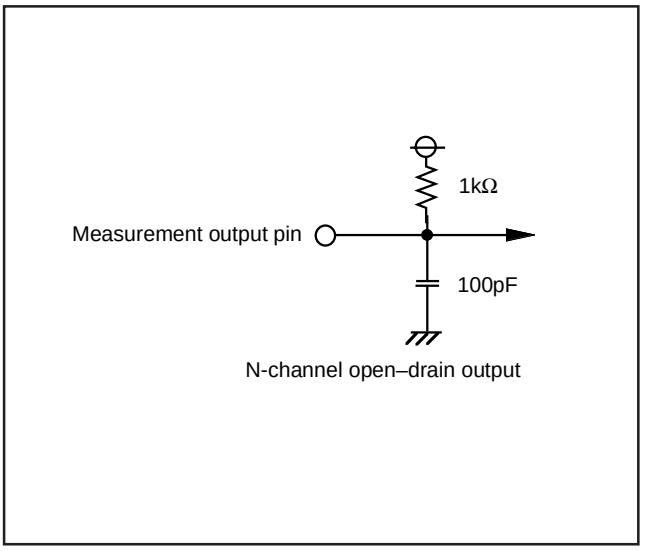


Fig. 84 Circuit for measuring output switching characteristics (2)

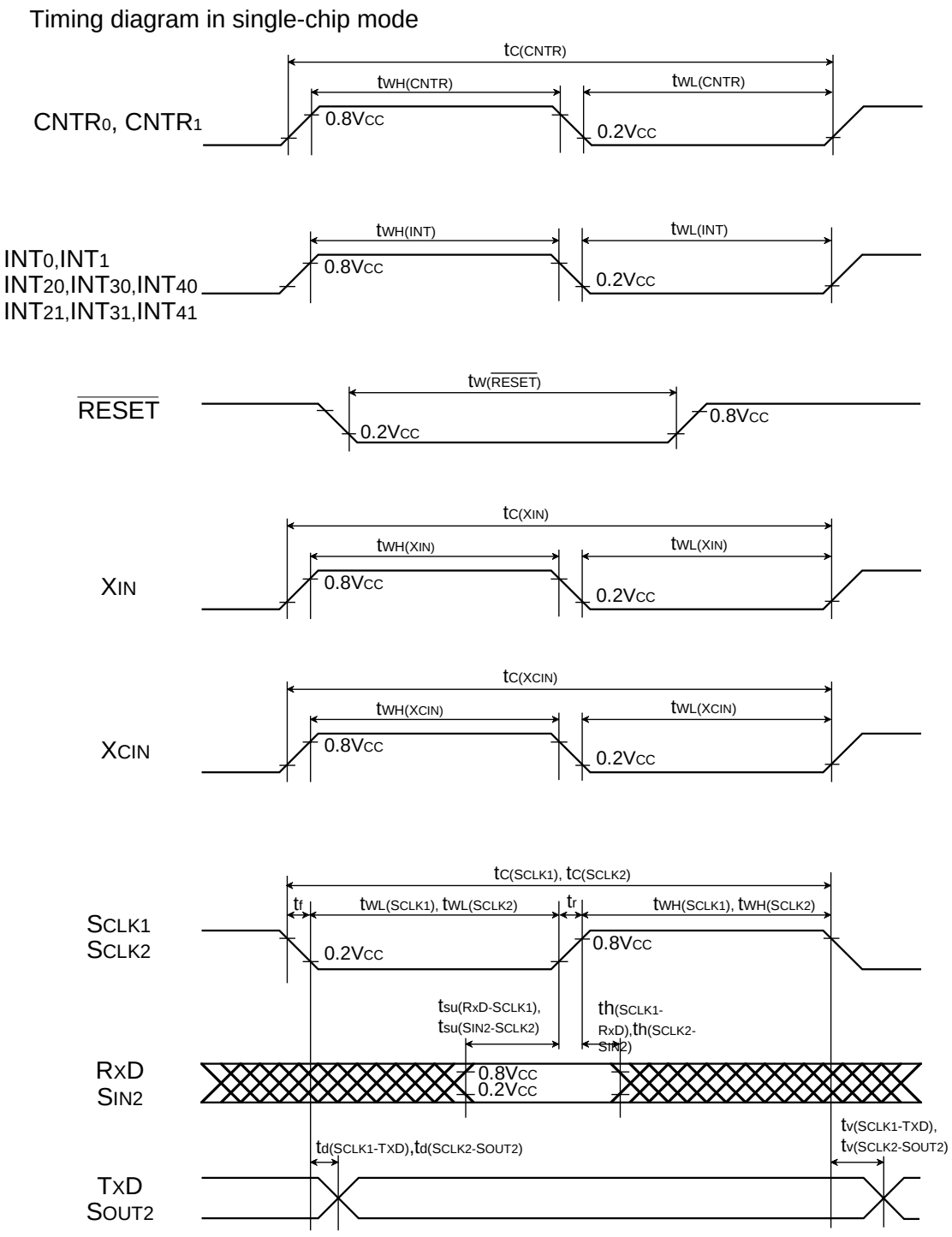
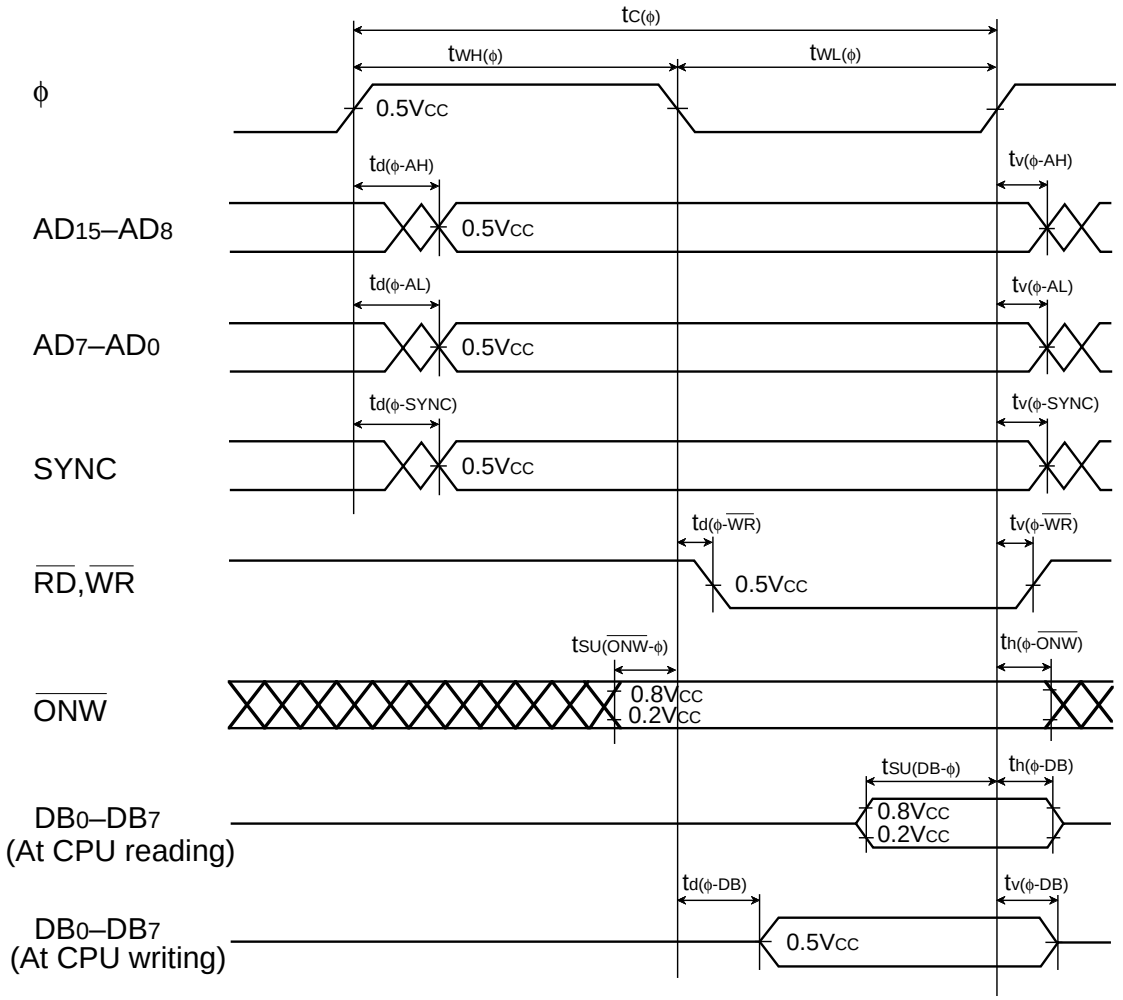


Fig. 85 Timing diagram (1) (in single-chip mode)

Timing diagram in memory expansion mode and microprocessor mode (1)



Timing diagram in microprocessor mode

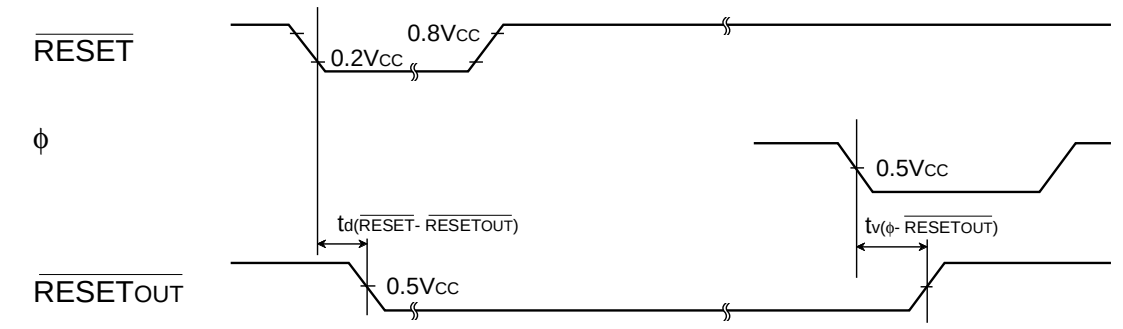


Fig. 86 Timing diagram (2) (in memory expansion mode and microprocessor mode)

Timing diagram in memory expansion mode and microprocessor mode (2)

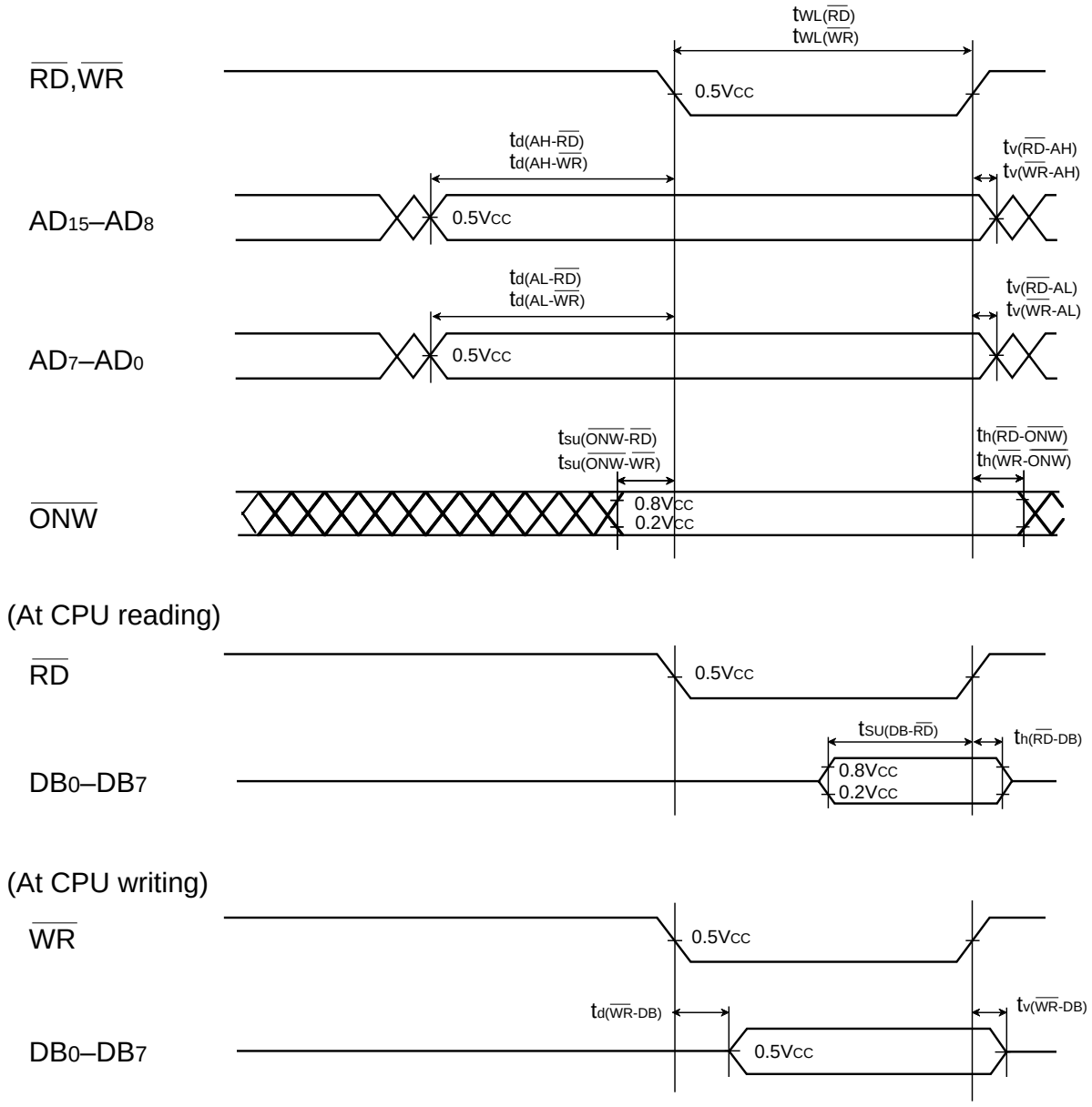
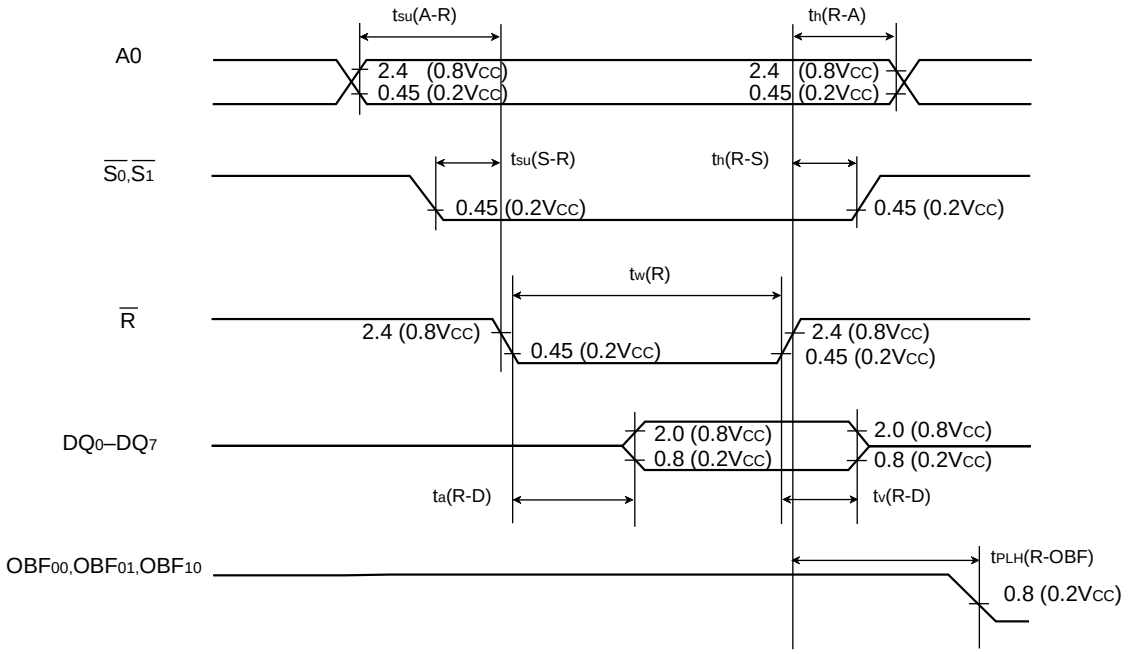


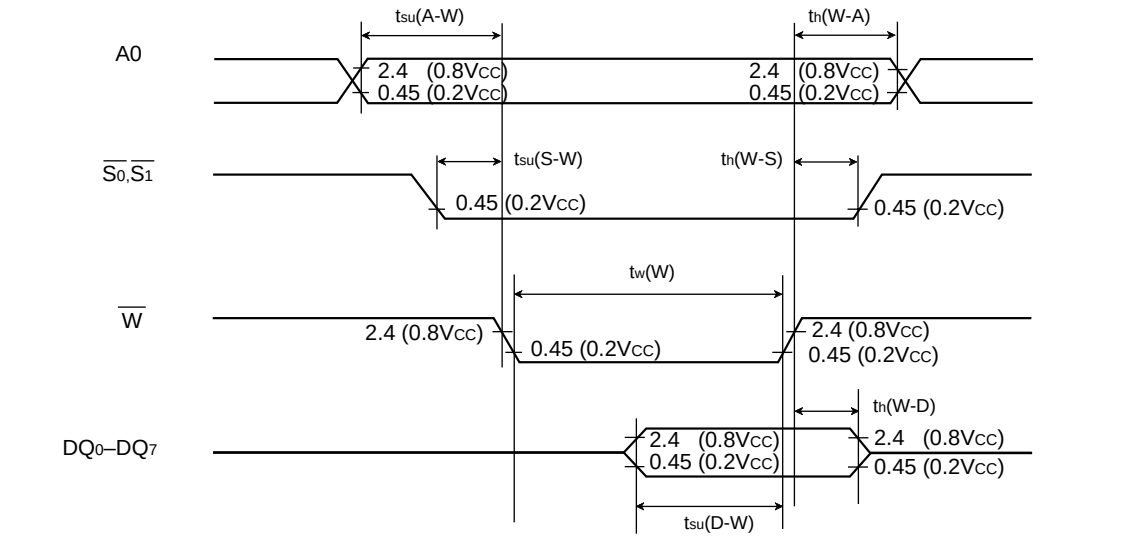
Fig. 87 Timing diagram (3) (in memory expansion mode and microprocessor mode)

System bus interface timing diagram

Read operation



Write operation



Outside of parenthesis : TTL I/O
Inside of parenthesis : CMOS I/O

Fig. 88 Timing diagram (4) (system bus interface)

Table 48 Multi-master I²C-BUS bus line characteristics

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	Hold time for SCL clock = "0"	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time for SCL clock = "1"	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
$t_{SU;DAT}$	Data setup time	250		100		ns
$t_{SU;STA}$	Setup time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Setup time for STOP condition	4.0		0.6		µs

Note: Cb = total capacitance of 1 bus line

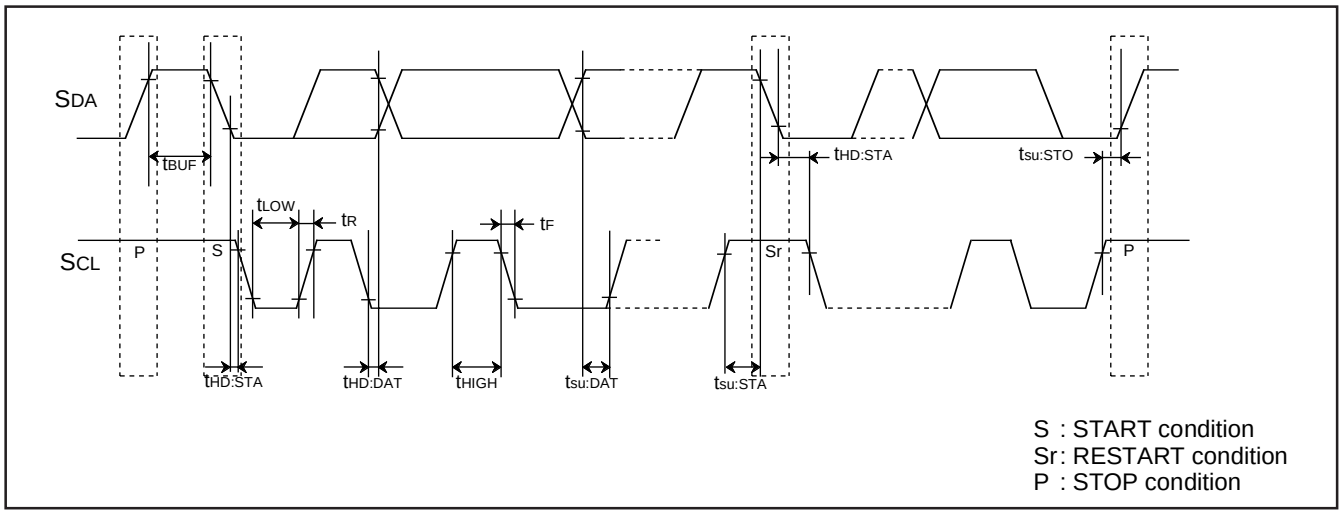


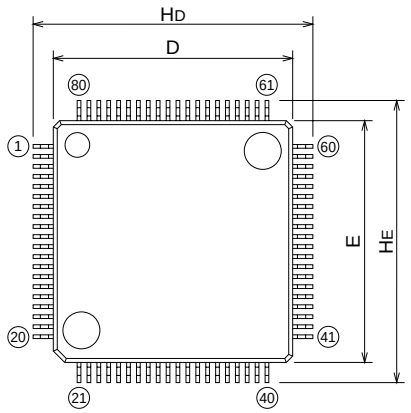
Fig. 89 Timing diagram of multi-master I²C-BUS

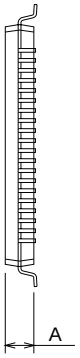
PACKAGE OUTLINE

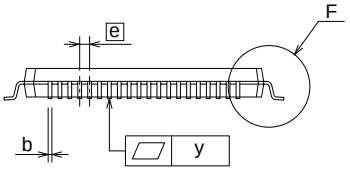
80P6Q-A

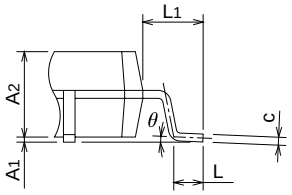
Plastic 80pin 12×12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–		Cu Alloy

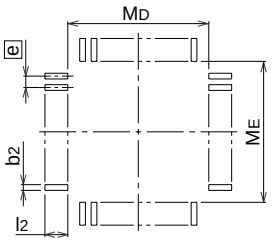








Detail F



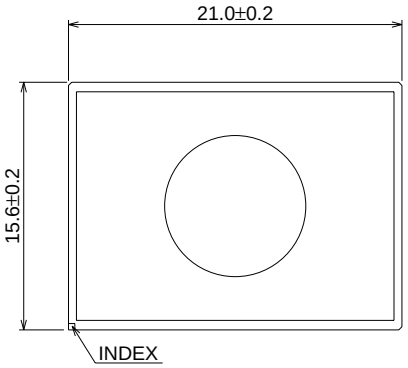
Recommended Mount Pad

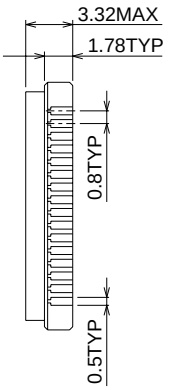
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	1.0	–	–
MD	–	12.4	–
ME	–	12.4	–

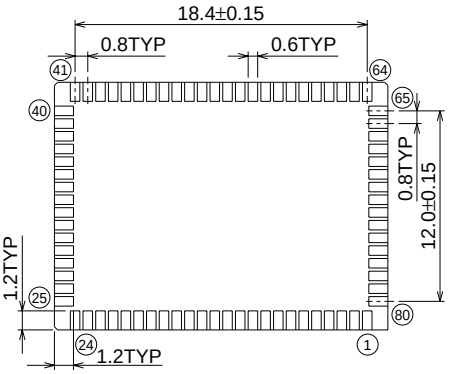
80D0

Glass seal 80pin QFN

EIAJ Package Code	JEDEC Code	Weight(g)
–	–	





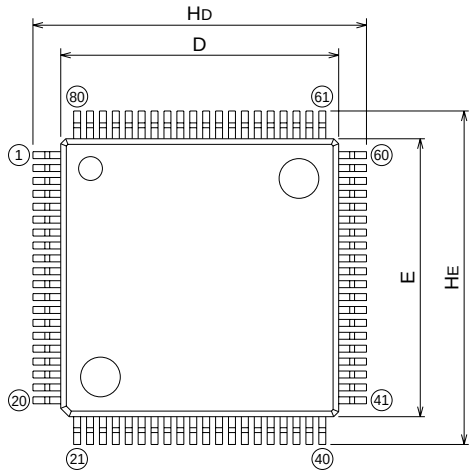


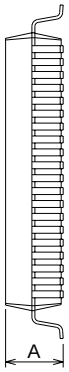
MITSUBISHI ELECTRIC

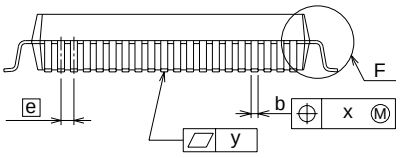
80P6S-A

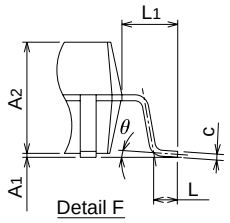
Plastic 80pin 14×14mm body QFP

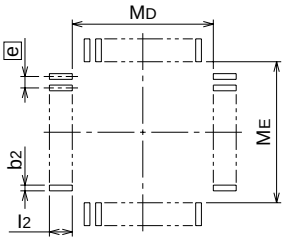
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1414-0.65		1.11	Alloy 42











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	–	0.65	–
H_D	16.5	16.8	17.1
H_E	16.5	16.8	17.1
L	0.4	0.6	0.8
L_1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
l_2	1.3	–	–
M_D	–	14.6	–
M_E	–	14.6	–

REVISION DESCRIPTION LIST	3886 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980216
2.0	The contents of flash memory version were added.	980716
2.1	All pages; “PRELIMINARY Notice: This is...” eliminated. Page 1; The second “In high-speed mode” of “Power dissipation” eliminated. Page 1; “Memory expansion” is revised. Page 1; Explanation of “<Flash memory mode>” is revised. Page 1; Notes 2 is changed. Page 1; Some words of “APPLICATION” are added. Page 2; Figure 1 and Figure 2 are partly revised. Page 3; Figure 3 is added. Page 7; Figure 5 is partly revised. Page 8; Figure 6 is partly revised. Page 8; Some products are added into Table 3. Page 9; Note into Figure 7 is revised. Page 10; Note into Figure 8 is revised. Page 11; Note into Figure 9 is added. Page 41; Explanation of “I^2C Data Shift Register” is partly revised. Page 42; Explanation of “I^2C Clock Control Regsiter” is partly revised. Page 42; Note 1 into Table 10 is partly revised. Page 50; (6) and (7) of “Precaution when using multi-master I^2C BUS interface” are added. Page 51; Figure 48 is partly revised. Page 56; Explanation of “RESET CIRCUIT” is partly revised. Page 56; Note into Figure 55 is revised. Page 60; Figure 61 is partly revised. Page 61; Explanation of “PROCESSOR MODE” is partly revised. Page 61; Explanation into Figure 62 is eliminated partly. Page 61; Note into Figure 63 is revised. Page 66; Figure 66 is partly revised.	000114

REVISION DESCRIPTION LIST	3886 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
2.1	Page 73; Minimum limits of $V_{PP}H$ into Table 22 is revised. Page 74; Figure 72 is partly revised. Page 81; Explanation of “Flash memory mode 3 (CPU reprogramming mode)” is added. Page 81; Note into Figure 79 is eliminated partly. Page 82; “CPU reprogramming mode operation procedure” is eliminated partly. Page 82; Figure 81 is partly revised. Page 86; Explanation of “Handling of Power Source Pins” is added. Page 86; Explanation of “Erasing of Flash memory version” is added. Page 87; Parameter into Table 28 is partly revised. Page 88; Parameter into Table 29 is partly revised. •Mask ROM confirmation forms are eliminated. ✻ Refer to the “Mitsubishi MCU Technical Information” Homepage (http://www.infomicom.mesc.co.jp/indexe/htm). [38000 Series → Mask ROM Confirmation Forms] •ROM programming confirmation form is eliminated. ✻ Refer to the “Mitsubishi MCU Technical Information” Homepage (http://www.infomicom.mesc.co.jp/indexe/htm). [38000 Series → Mask ROM Confirmation Forms] •Mark specification form is eliminated. ✻ Refer to the “Mitsubishi MCU Technical Information” Homepage (http://www.infomicom.mesc.co.jp/indexe/htm). [38000 Series → Mask ROM Confirmation Forms → ROM Ordering Method → Mark Specification Forms] Page 107; Package outline for 80P6S-A is added.	000114

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