

M5M5V408BFP,TP,RT,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V408B is a family of low voltage 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25μm CMOS technology.

The M5M5V408B is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5V408B is packaged in 32-pin plastic SOP, 32-pin plastic TSOP and 32-pin 8mm x 13.4mm STSOP packages. Two types of TSOPs and two types of STSOPs are available, M5M5V408BTP (normal-lead-bend TSOP), M5M5V408BRT (reverse-lead-bend TSOP), M5M5V408BKV (normal-lead-bend STSOP) and M5M5V408BKR (reverse-lead-bend STSOP). These two types TSOPs and two types STSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

FEATURES

- Single +2.7~+3.6V power supply
- Small stand-by current: 0.3μA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Process technology: 0.25μm CMOS
- Package:
 - M5M5V408BFP: 32 pin 525 mil SOP
 - M5M5V408BTP/RT: 32 PIN 400mil TSOP(II)
 - M5M5V408BKV/KR: 32 pin 8mm x13.4mm STSOP

PART NAME TABLE

Version, Operating temperature	Part name (## stands for "FP", "TP", "RT", "KV" or "KR")	Power Supply	Access time max.	Stand-by current I _{cc} (PD), V _{cc} =3.0V						Active current I _{cc1} (3.0V, typ.)
				typical *		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5V408B## -70L	2.7 ~ 3.6V	70ns	---	---	---	---	30μA	---	30mA (10MHz) 5mA (1MHz)
	M5M5V408B## -85L		85ns							
	M5M5V408B## -70H	2.7 ~ 3.6V	70ns	0.3μA	1μA	1μA	3μA	15μA	---	
	M5M5V408B## -85H		85ns							
W-version -20 ~ +85°C	M5M5V408B## -70LW	2.7 ~ 3.6V	70ns	---	---	---	---	30μA	60μA	
	M5M5V408B## -85LW		85ns							
	M5M5V408B## -70HW	2.7 ~ 3.6V	70ns	0.3μA	1μA	1μA	3μA	15μA	30μA	
	M5M5V408B## -85HW		85ns							
I-version -40 ~ +85°C	M5M5V408B## -70LI	2.7 ~ 3.6V	70ns	---	---	---	---	30μA	60μA	
	M5M5V408B## -85LI		85ns							
	M5M5V408B## -70HI	2.7 ~ 3.6V	70ns	0.3μA	1μA	1μA	3μA	15μA	30μA	
	M5M5V408B## -85HI		85ns							

* "typical" parameter is sampled, not 100% tested.

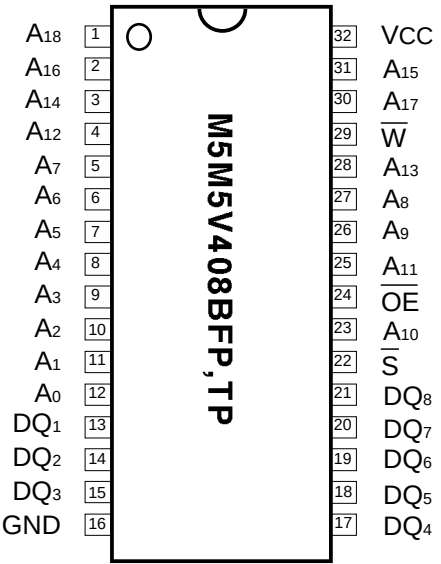


M5M5V408BFP,TP,RT,KV

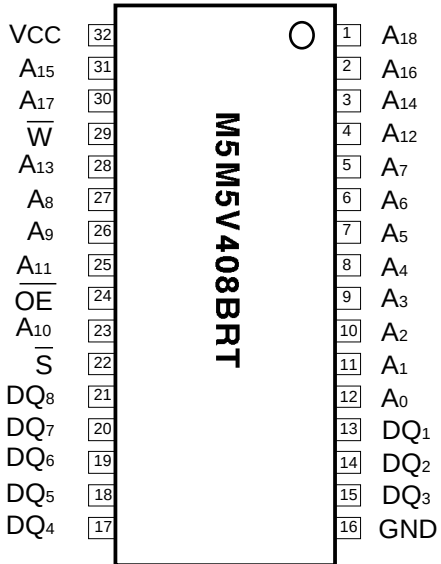
4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

PIN CONFIGURATION (TOP VIEW)

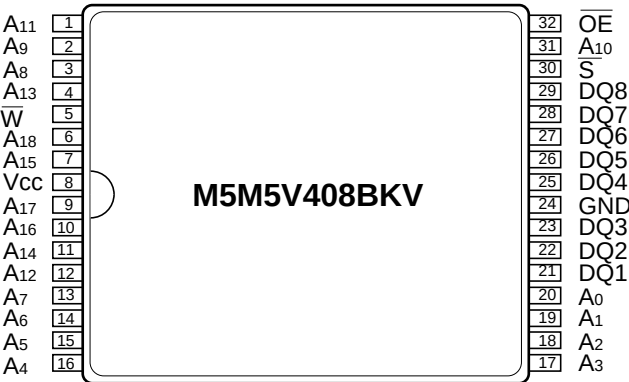
Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
$\overline{S}$	Chip select input
$\overline{W}$	Write control input
$\overline{OE}$	Output inable input
Vcc	Power supply
GND	Ground supply



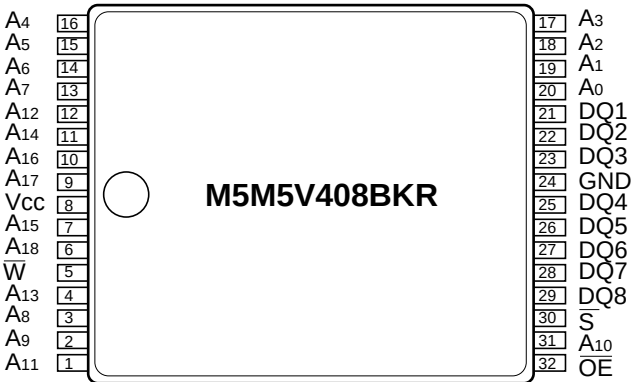
Outline 32P2M-A (FP)
32P3Y-H (TP)



Outline 32P3Y-J (RT)



Outline 32P3K-B



Outline 32P3K-C

M5M5V408BFP,TP,RT,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The M5M5408BFP,TP,RT,KV,KR is organized as 524,288-words by 8-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. The address(A0~A18) must be set up before the write cycle

A read operation is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while S are in an active state($\overline{S}=L$).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

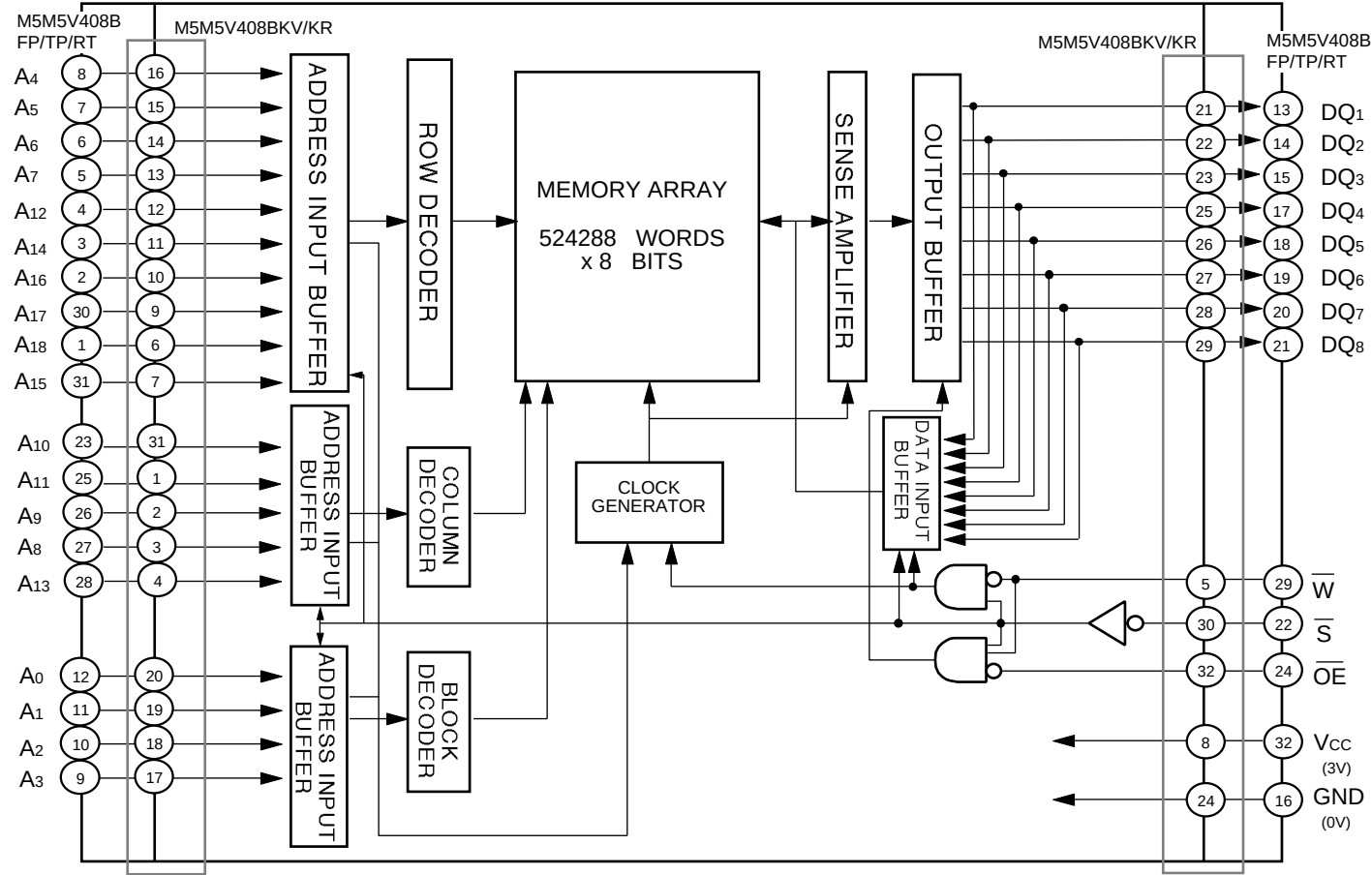
The power supply current is reduced as low as 0.3μA(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	Data input (D)	Active
L	H	L	Read	Data output (Q)	Active
L	H	H	Read	High-impedance	Active

Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
$\overline{S}$	Chip select input
$\overline{W}$	Write control input
$\overline{OE}$	Output inable input
Vcc	Power supply
GND	Ground supply

BLOCK DIAGRAM



M5M5V408BFP,TP,RT,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V _{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V _I	Input voltage	With respect to GND	-0.5* ~ V _{CC} + 0.5	
V _O	Output voltage	With respect to GND	0 ~ V _{CC}	
P _d	Power dissipation	T _a =25°C	700	mW
T _a	Operating temperature	Standard (-L, -H)	0 ~ +70	°C
		W-version (-LW, -HW)	-20 ~ +85	
		I-version (-LI, -HI)	-40 ~ +85	
T _{stg}	Storage temperature		-65 ~ 150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Units	
				Min	Typ	Max		
V _{IH}	High-level input voltage			2.2		V _{CC} +0.3V	V	
V _{IL}	Low-level input voltage			-0.3 *		0.6		
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA		2.4				
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA		V _{CC} -0.5V				
V _{OL}	Low-level output voltage	I _{OL} =2mA				0.4		
I _I	Input leakage current	V _I =0 ~ V _{CC}				±1	μA	
I _O	Output leakage current	$\overline{S}$ =V _{IH} or $\overline{OE}$ =V _{IH} , V _{I/O} =0 ~ V _{CC}				±1		
I _{CC1}	Active supply current (AC, CMOS-level)	$\overline{S}$ ≤0.2V Output-open	f= 10MHz	-	30	40	mA	
		Other inputs ≤0.2V or ≥V _{CC} -0.2V	f= 1MHz	-	5	7		
I _{CC2}	Active supply current (AC,TTL-level)	$\overline{S}$ =V _{IL} Output-open	f= 10MHz	-	30	40		
		Other inputs=V _{IH} or V _{IL}	f= 1MHz	-	5	7		
I _{CC3}	Stand by supply current (CMOS-level input)	V _{CC} =3.6V, max. $\overline{S}$ ≥V _{CC} -0.2V Other inputs=0~V _{CC}	-LW, -LI	+85°C	-	-	80	μA
			-L, -LW, -LI	+70°C	-	-	40	
			-HW, -HI	+85°C	-	-	40	
			-H, -HW, -HI	+70°C	-	-	20	
				+40°C	-	1	5	
			-H	0 ~ +25°C	-	0.3	2	
			-HW	-20 ~ +25°C	-	0.3	2	
I _{CC4}	Stand by supply current (TTL-level input)	$\overline{S}$ =V _{IH} ,Other inputs= 0 ~ V _{CC}			-	-	0.5	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

* -3.0V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical value is for V_{CC}=3.0V

CAPACITANCE

(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	



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AC ELECTRICAL CHARACTERISTICS (V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	2.7V~3.6V
Input pulse	V _{IH} =2.4V, V _{IL} =0.4V
Input rise time and fall time	5ns
Reference level	V _{OH} =V _{OL} =1.5V Transition is measured ±500mV from steady state voltage.(for t _{en} , t _{dis})
Output loads	Fig.1, CL=30pF CL=5pF (for t _{en} , t _{dis})

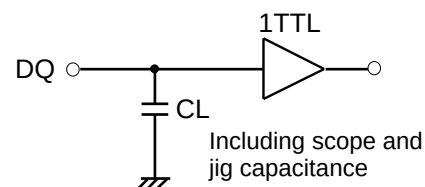


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Units
		M5M5V408B FP,TP,RT,KV,KR-70		M5M5V408B FP,TP,RT,KV,KR-85		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	70		85		ns
t _a (A)	Address access time		70		85	ns
t _a (S)	Chip select access time		70		85	ns
t _a (OE)	Output enable access time		35		45	ns
t _{dis} (S)	Output disable time after $\overline{S}$ high		25		30	ns
t _{dis} (OE)	Output disable time after $\overline{OE}$ high		25		30	ns
t _{en} (S)	Output enable time after $\overline{S}$ low	10		10		ns
t _{en} (OE)	Output enable time after $\overline{OE}$ low	5		5		ns
t _v (A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

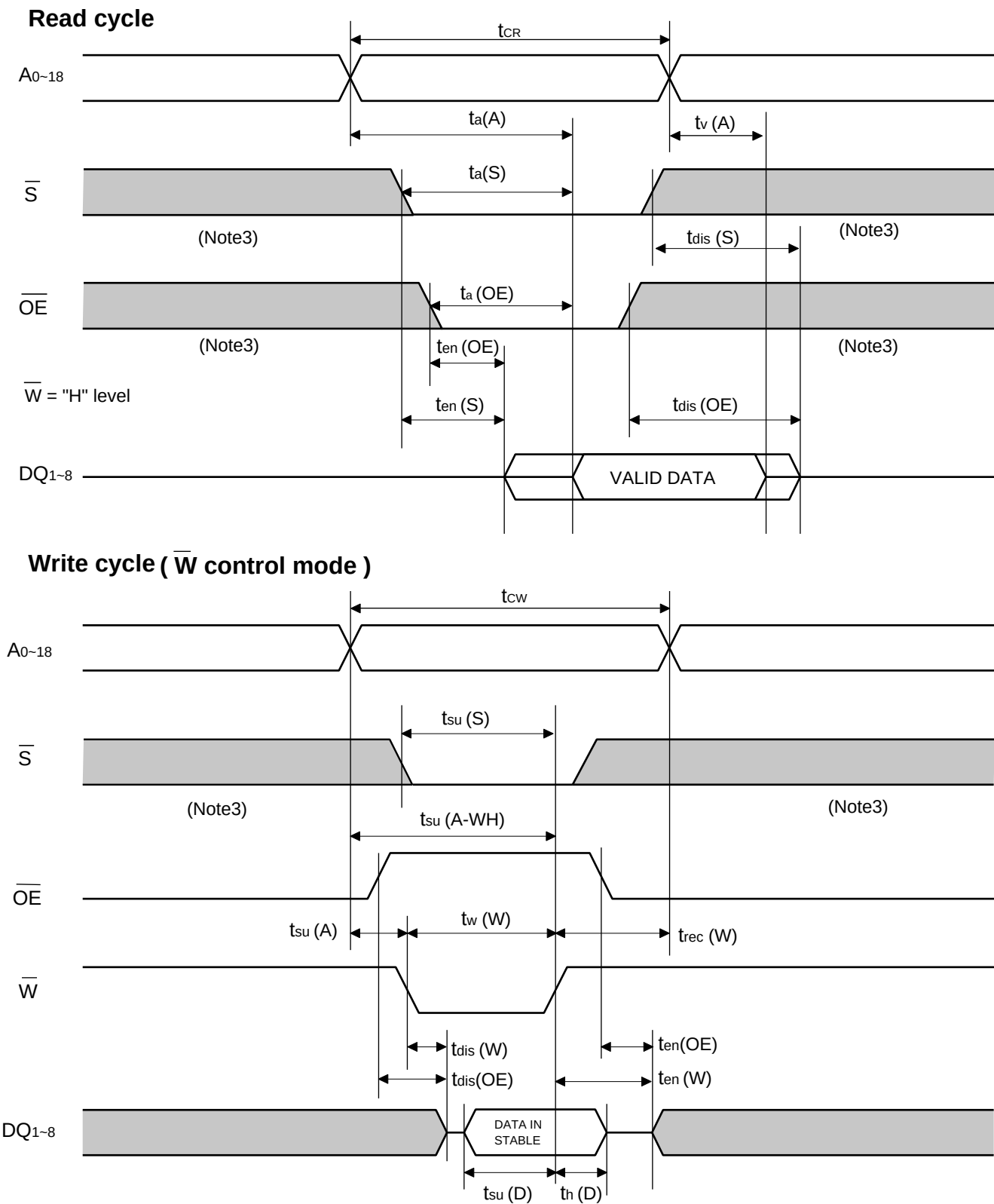
Symbol	Parameter	Limits				Units
		M5M5V408B FP,TP,RT,KV,KR-70		M5M5V408B FP,TP,RT,KV,KR-85		
		Min	Max	Min	Max	
t _{cw}	Write cycle time	70		85		ns
t _{w(W)}	Write pulse width	55		60		ns
t _{su(A)}	Address set up time	0		0		ns
t _{su(A-WH)}	Address set up time with respect to $\overline{W}$ high	65		70		ns
t _{su(S)}	Chip select set up time	65		70		ns
t _{su(D)}	Data set up time	35		35		ns
t _{h(D)}	Data hold time	0		0		ns
t _{rec(W)}	Write recovery time	0		0		ns
t _{dis(W)}	Output disable time after $\overline{W}$ low		25		30	ns
t _{dis(OE)}	Output disable time after $\overline{OE}$ high		25		30	ns
t _{en(W)}	Output enable time after $\overline{W}$ high	5		5		ns
t _{en(OE)}	Output enable time after $\overline{OE}$ low	5		5		ns



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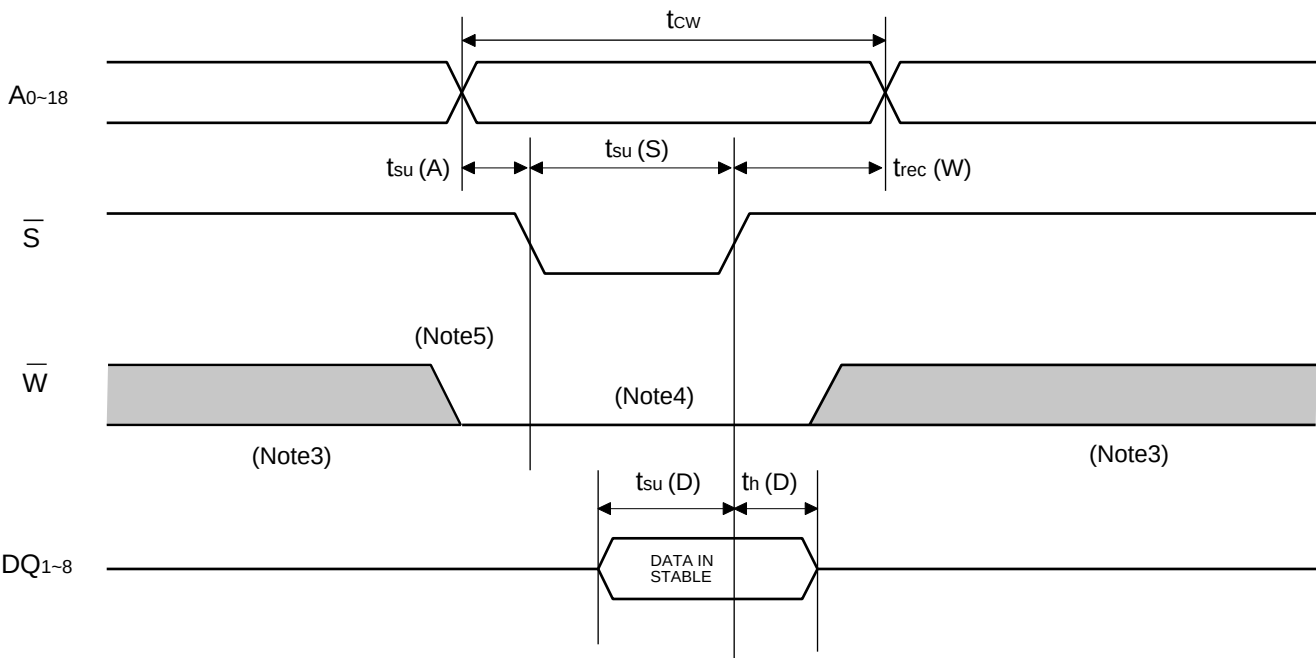
(4)TIMING DIAGRAMS



M5M5V408BFP,TP,RT,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle ($\overline{S}$ control mode)



- Note 3: Hatching indicates the state is "don't care".
- Note 4: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
- Note 5: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high impedance state.
- Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

M5M5V408BFP,TP,RT,KV

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits			Units
					Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage				2.0			V
V _I ($\overline{S}$)	Chip select input $\overline{S}$				2.0			V
I _{CC} (PD)	Power down supply current	V _{CC} =3.0V, S≥V _{CC} -0.2V, Other inputs = 0 ~ V _{CC}	-LW, -LI	+85°C	-	-	60	μA
			-L, -LW, -LI	+70°C	-	-	30	μA
			-HW, -HI	+85°C	-	-	30	μA
			-H, -HW, -HI	+70°C	-	-	15	μA
				+40°C	-	1	3	μA
			-H	0 ~ +25°C	-	0.3	1	μA
			-HW	-20 ~ +25°C	-	0.3	1	μA
-HI	-40 ~ +25°C	-	0.3	1	μA			

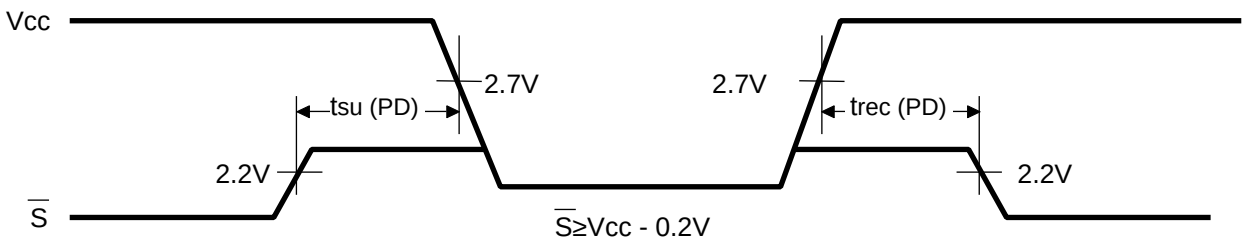
Typical value is based on sampling.

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

$\overline{S}$ control mode



M5M5V408BFP,TP,RT,KV**4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM**

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Date</u>	<u>Remarks</u>
K0.1e	The first edition	'98.3.05	Preliminary
K0.2e	Added M5M5V408BFP/TP/RT	'98.7.30	Preliminary
K1.0e	The first product version	'98.9.7	---
K2.0e	1) Speed items revised: 70ns added and 100ns deleted		
	2) Icc3 and Icc(PD) limits revised	'99.3.10	---



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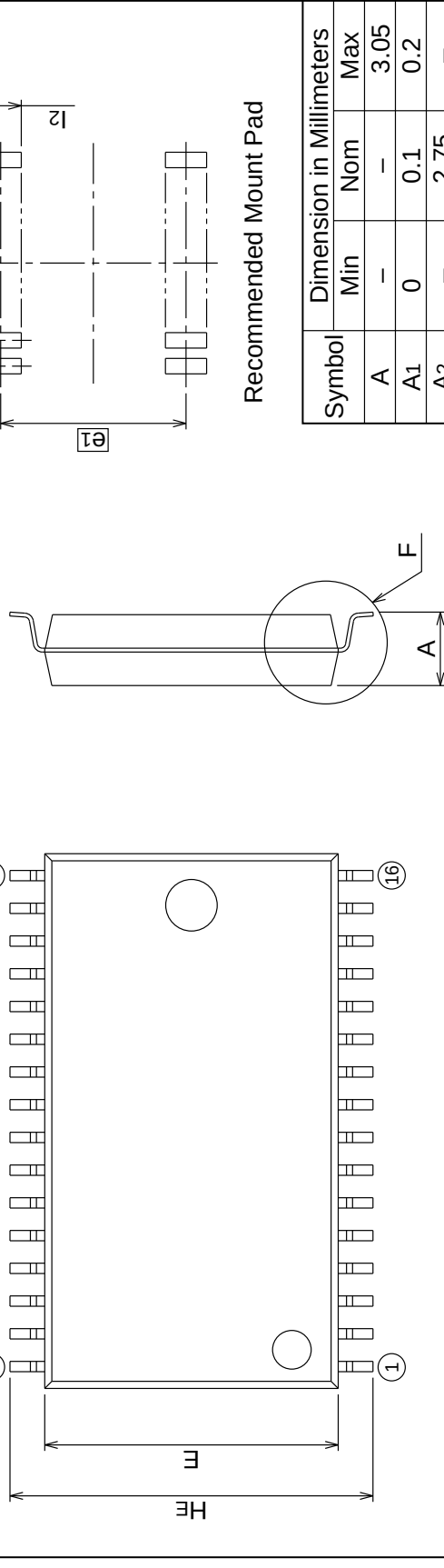
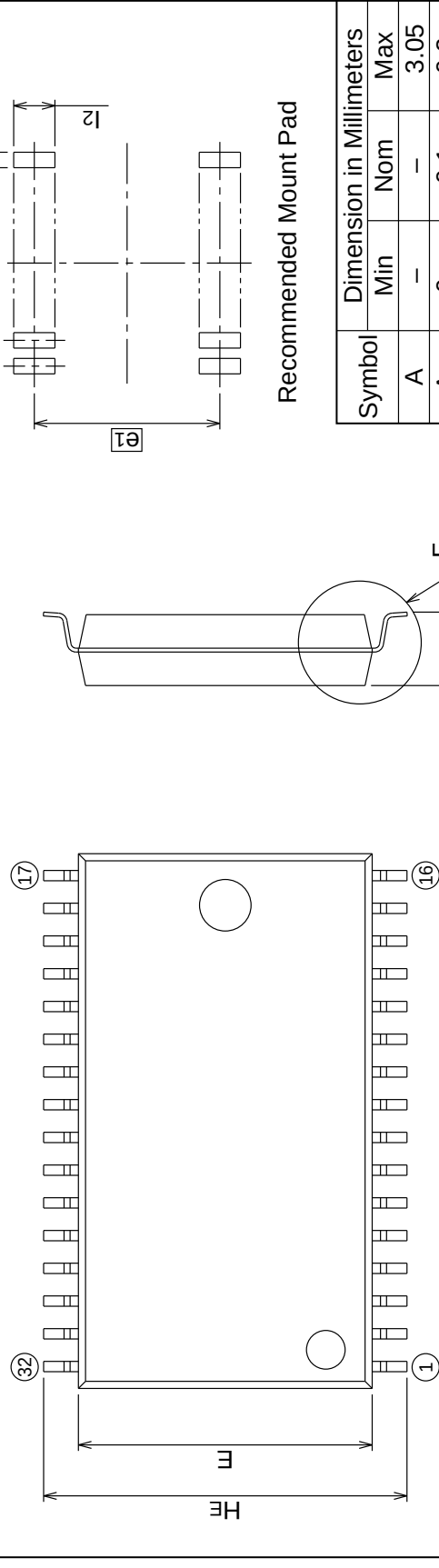
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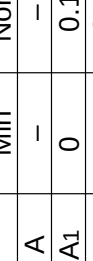
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Plastic 32pin 525mil SOP

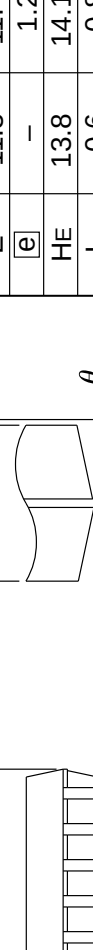
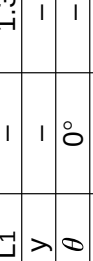
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP32-P-525-1.27	-	1.29	Alloy 42

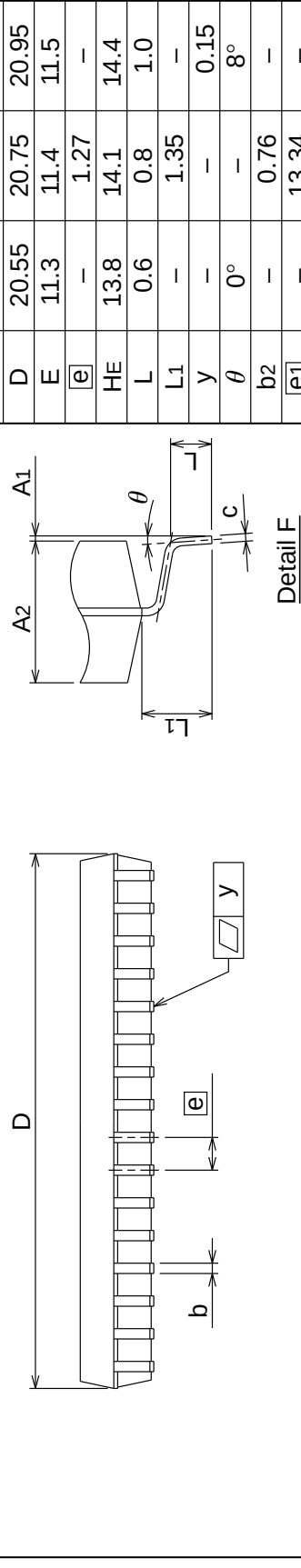
[illegible]

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.75	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	20.55	20.75	20.95
E	11.3	11.4	11.5
<u>e</u>	—	1.27	—
HE	13.8	14.1	14.4
L	0.6	0.8	1.0
L1	—	1.35	—
y	—	—	0.15
θ	0°	—	8°
b2	—	0.76	—
<u>e1</u>	—	13.34	—
l2	1.27	—	—




Detail F

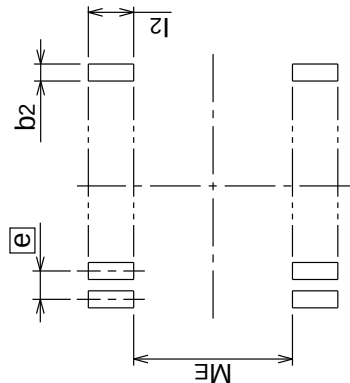
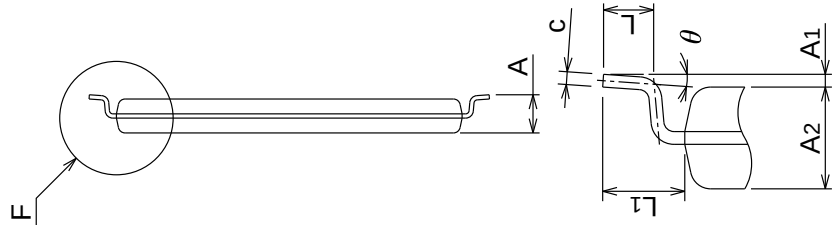
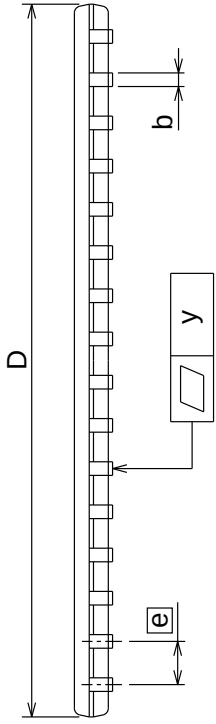
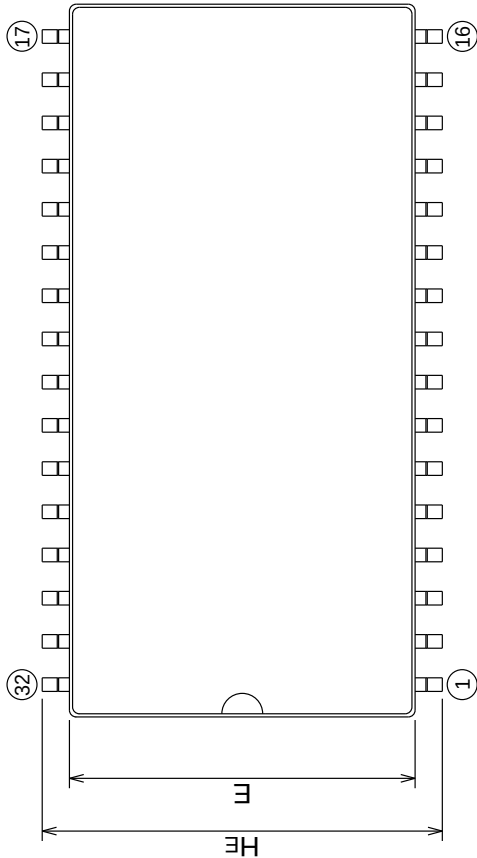





32P3Y-H

Plastic 32pin 400mil TSOP (II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP1132-P-400-1.27	—	0.53	Alloy 42



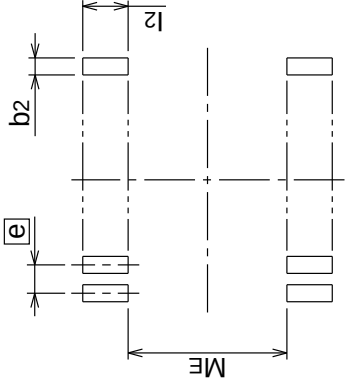
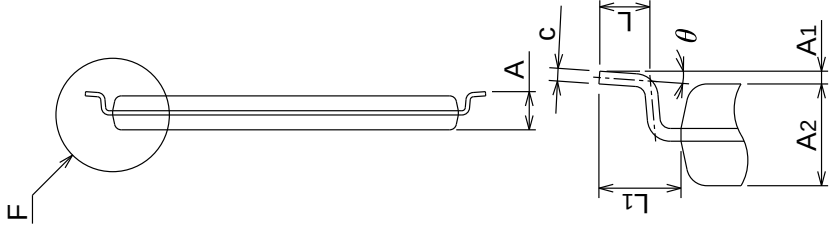
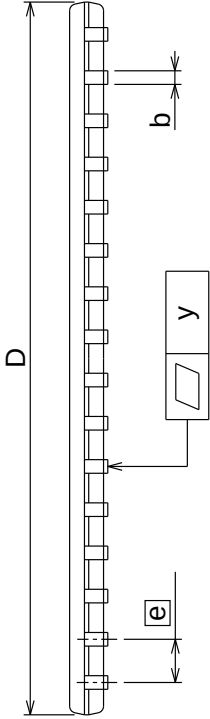
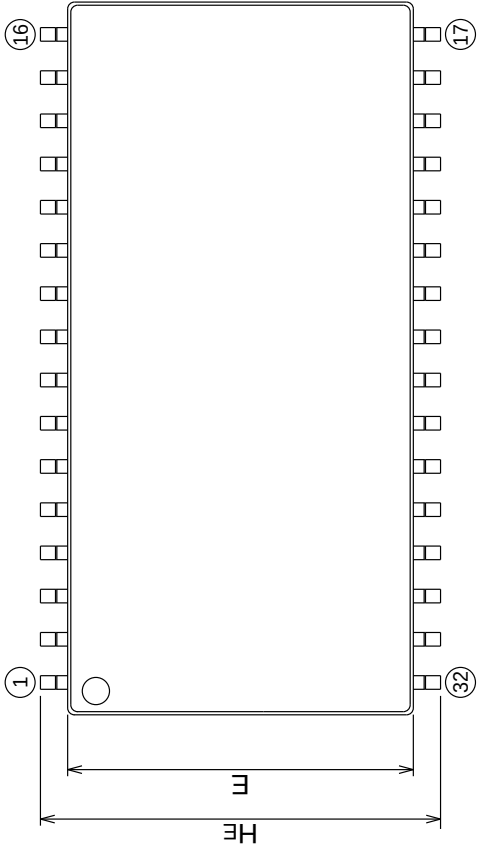
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A1	0.05	0.125	0.2
A2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	—	1.27	—
HE	11.56	11.76	11.96
L	0.4	0.5	0.6
L1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
ME	—	10.36	—
l2	0.9	—	—
b2	—	0.76	—

32P3Y-J

Plastic 32pin 400mil TSOP (II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII32-P-400-1.27	—	0.53	Alloy 42



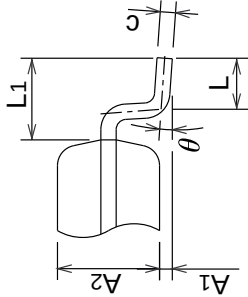
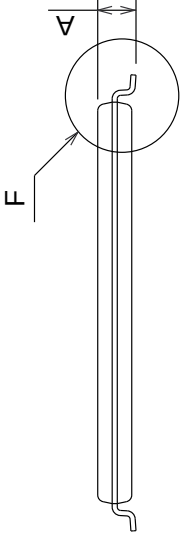
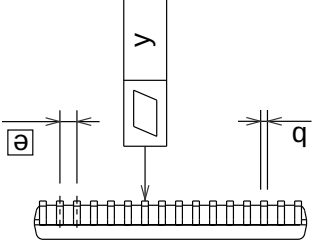
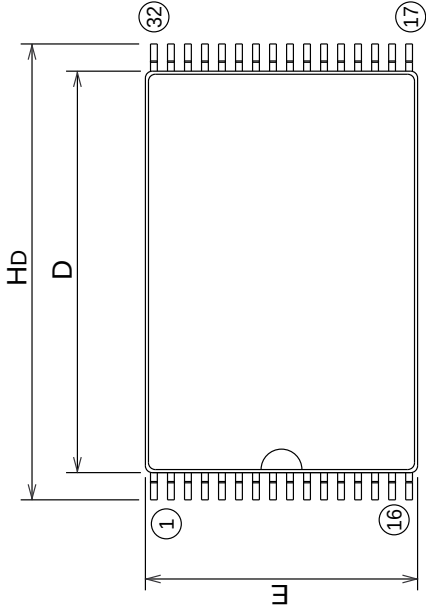
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A1	0.05	0.125	0.2
A2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	—	1.27	—
HE	11.56	11.76	11.96
L	0.4	0.5	0.6
L1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
ME	—	10.36	—
l2	0.9	—	—
b2	—	0.76	—

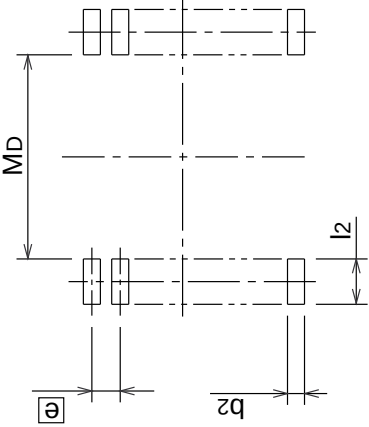
32P3K-B

Plastic 32pin 8X13.4mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
-	-		Alloy 42



Detail F



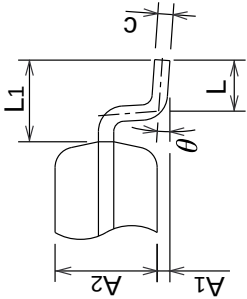
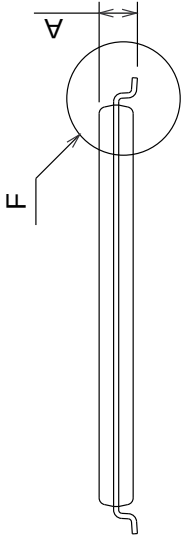
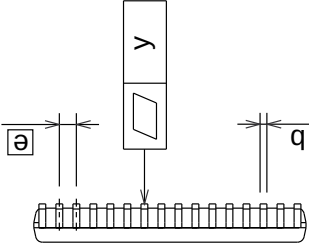
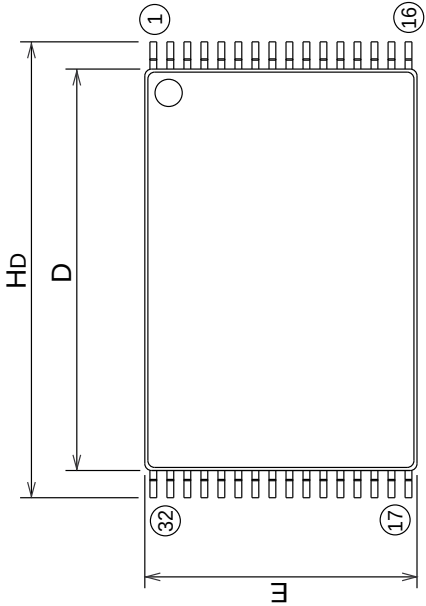
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.2
A1	0.05	0.125	0.2
A2	-	1.0	-
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	11.7	11.8	11.9
E	7.9	8.0	8.1
e	-	0.5	-
HD	13.2	13.4	13.6
L	0.4	0.5	0.6
L1	-	0.8	-
y	-	-	0.1
theta	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	12.0	-

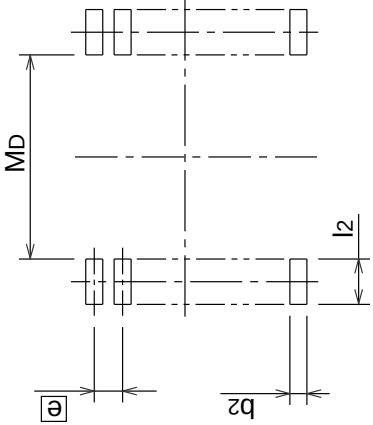
32P3K-C

Plastic 32pin 8X13.4mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
-	-		Alloy 42



Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.2
A1	0.05	0.125	0.2
A2	-	1.0	-
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	11.7	11.8	11.9
E	7.9	8.0	8.1
e	-	0.5	-
HD	13.2	13.4	13.6
L	0.4	0.5	0.6
L1	-	0.8	-
y	-	-	0.1
θ	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	12.0	-

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