FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13727-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90435 Series

MB90437L (S) /438L (S) /F438L (S)
MB90439 (S) /F439 (S) /V540G

■ DESCRIPTION

The MB90435 series with FLASH ROM is specially designed for industrial applications.

The instruction set by F²MC-16LX CPU core inherits an AT architecture of the F²MC* family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions.The micro controller has a 32-bit accumulator for processing long word data.

The MB90435 series has peripheral resources of 8/10-bit A/D converters, UART (SCI) , extended I/O serial interfaces, 8/16-bit timer, I/O timer (input capture (ICU) , output compare (OCU)) .

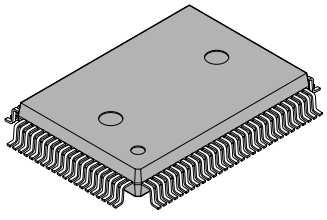
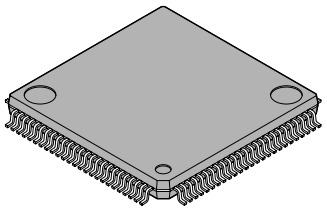
* : F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Embedded PLL clock multiplication circuit
  Operating clock (PLL clock) can be selected from : divided-by-2 of oscillation or one to four times the oscillation
  Minimum instruction execution time : 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V_{CC} of 5.0 V)
  Subsystem Clock : 32 kHz

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■ PACKAGES

100-pin Plastic QFP	100-pin Plastic LQFP
	
(FPT-100P-M06)	(FPT-100P-M05)

FUJITSU

- Instruction set to optimize controller applications
  Rich data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed : 4-byte Instruction queue
- Enhanced interrupt function : 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI^{2}OS)
- Embedded ROM size and types
  Mask ROM : 64 Kbytes / 128 Kbytes / 256 Kbytes
  Flash ROM : 128 Kbytes/256 Kbytes
  Embedded RAM size : 2 Kbytes/4 Kbytes/6 Kbytes/8 Kbytes (evaluation chip)
- Flash ROM
  Supports automatic programming, Embedded Algorithm TM*
  Write/Erase/Erase-Suspend/Resume commands
  A flag indicating completion of the algorithm
  Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
  Erase can be performed on each block
  Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Clock mode
  Hardware stand-by mode
- Process
  0.5 μm CMOS technology
- I/O port
  General-purpose I/O ports : 81 ports
- Timer
  Watchdog timer : 1 channel
  8/16-bit PPG timer : 8/16-bit × 4 channels
  16-bit re-load timer : 2 channels
- 16-bit I/O timer
  16-bit free-run timer : 1 channel
  Input capture : 8 channels
  Output compare : 4 channels
- Extended I/O serial interface : 1 channel
- UART 0
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized (with start/stop bit) transmission can be selectively used.

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- UART 1
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized serial (extended I/O serial) can be used.
- External interrupt circuit (8 channels)
  A module for starting an extended intelligent I/O service (EI^{2}OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module
  Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  8/10-bit resolution can be selectively used.
  Starting by an external trigger input.
  Conversion time : 26.3 µs
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

* : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP

Features	MB90F438L (S) /F439 (S)	MB90437L (S) *1 /438L (S) /439 (S)	MB90V540G
CPU	F²MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop) Minimum instruction exection time : 62.5 ns (4 MHz osc. PLL × 4)		
ROM	Flash memory MB90F438L(S) : 128 Kbytes MB90F439(S) : 256 Kbytes	Mask ROM : MB90437L(S): 64 Kbytes MB90438L(S): 128 Kbytes MB90439(S): 256 Kbytes	External
RAM	MB90F438L(S) : 4 Kbytes MB90F439(S) : 6 Kbytes	MB90437L(S): 2 Kbytes MB90438L(S): 4 Kbytes MB90439(S): 6 Kbytes	8 Kbytes
Clocks	MB90F438L/F439 : Two clocks system MB90F438LS/F439S : One clock system	MB90437L/438L/439 : Two clocks system MB90437LS/438LS/439S : One clock system	Two clocks system*2
Operating voltage range	*5		
Temperature range	–40 °C to 105 °C		
Package	QFP100, LQFP100		PGA-256
Emulator-specify power supply*3	—		None
UART0	Full duplex double buffer Support asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronous (start-stop synchronized) and CLK-synchronous communication Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous) 62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz		
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and nagative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz		
A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 26.3 µs (per one channel)		

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Features	MB90F438L (S) /F439 (S)	MB90437L (S) *1 /438L (S) /439 (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit I/O Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys/2^2, fsys/2^4, fsys/2^6, fsys/2^8 (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit I/O Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal		
Flash Memory	Supports automatic programming, Embeded Algorithm TM*4 Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : Under development

*2 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

*3 : It is setting of DIP switch S2 when Emulator pod (MB2145-507) is used.Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

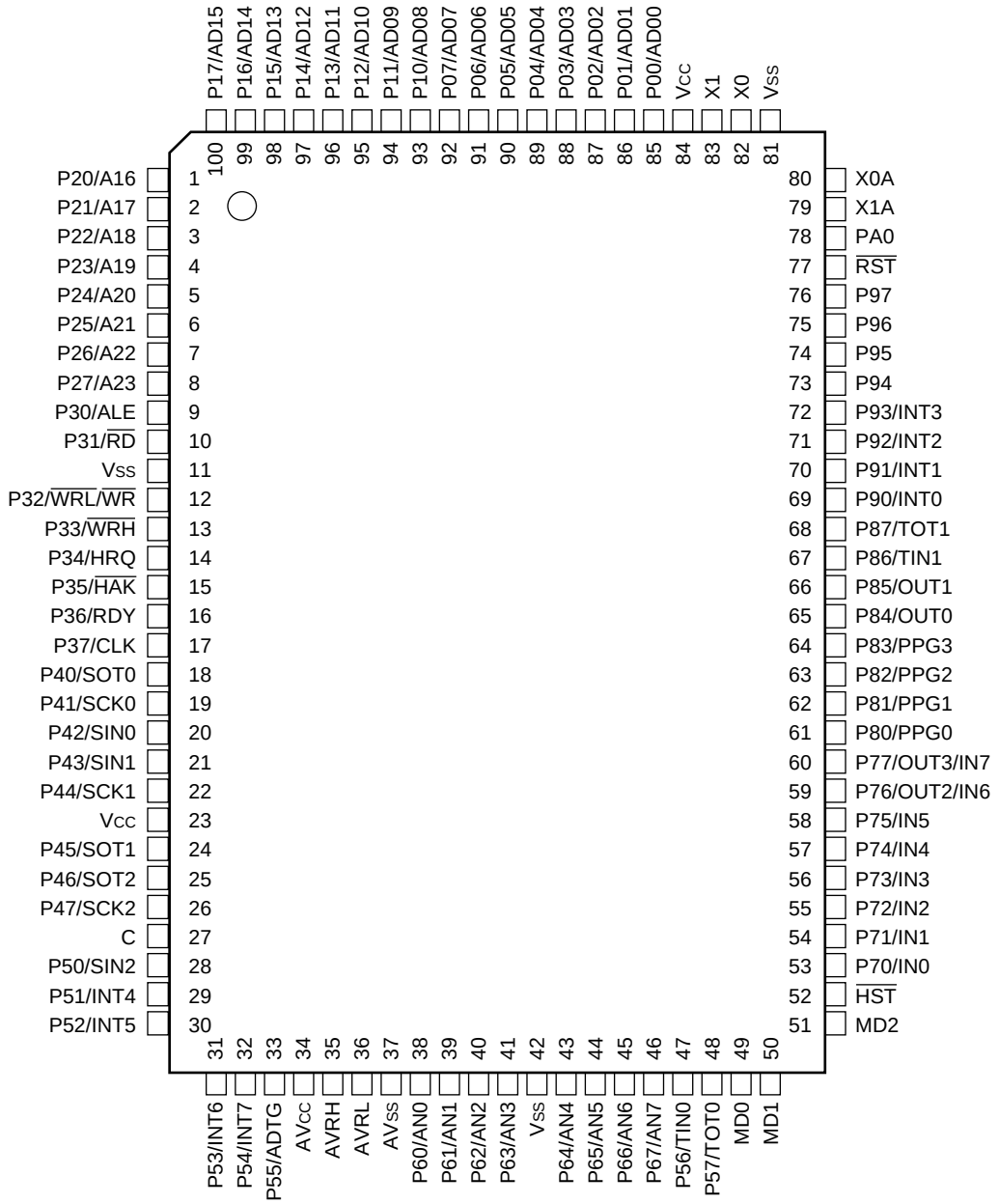
*4 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

*5 : OPERATING VOLTAGE RANGE

Products	Operation guarantee range
MB90F439 (S) /439 (S) /V540G	4.5 V to 5.5 V
MB90F438L (S) /437L (S) /438L (S)	3.5 V to 5.5 V

■ PIN ASSIGNMENT

(TOP VIEW)

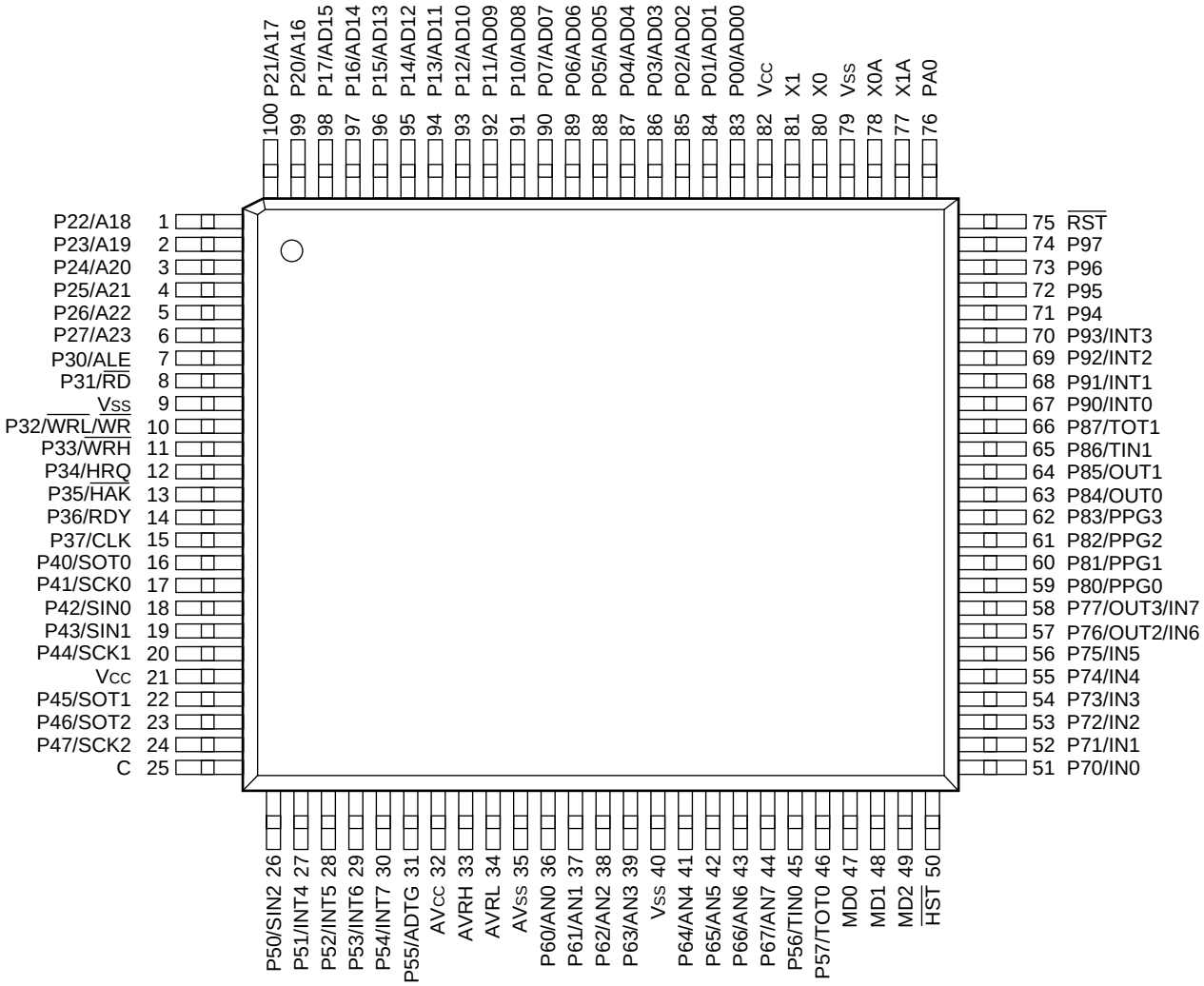


(FPT-100P-M06)

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(TOP VIEW)



(FPT-100P-M05)

■ PIN DESCRIPTION

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pull-up. In external bus mode, this function is valid when the corresponding bits in the external address output control register (HACR) are set to “1”.
		A16 to A23		8-bit output pins for A16 to A23 at the external address bus. In external bus mode, this function is valid when the corresponding bits in the external address output control register (HACR) are set to “0”.
7	9	P30	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
		$\overline{\text{WR}}$		

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode, external bus 8-bit mode or when $\overline{WRH}$ pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pull-up. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pull-up. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface . This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface . Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
46	48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
		TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.
51 to 56	53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
		IN0 to IN5		Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used.
57 , 58	59 , 60	P76 , P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT2 , OUT3		Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
		IN6 , IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used.
59 , 62	61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
		PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
63 , 64	65 , 66	P84 , P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT0 , OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
65	67	P86	D	General I/O port. This function is always enabled.
		TIN1		Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used.
66	68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
		TOT1		Output pin for the 16-bit reload timers 1.This function is enabled when the 16-bit reload timers 1 enables the output.
67 to 70	69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
		INT0 to INT3		External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used.
71	73	P94	D	General I/O port.

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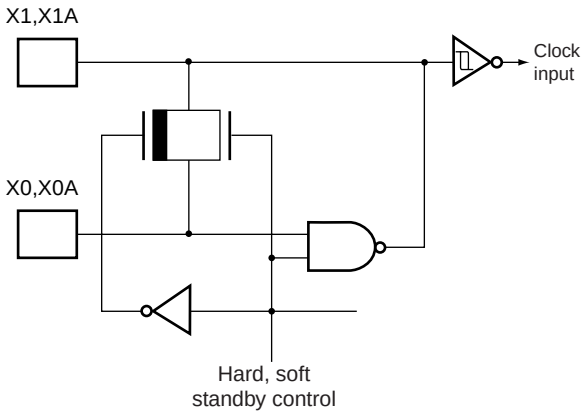
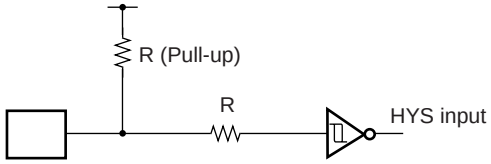
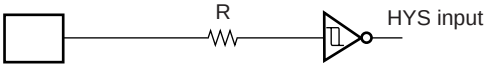
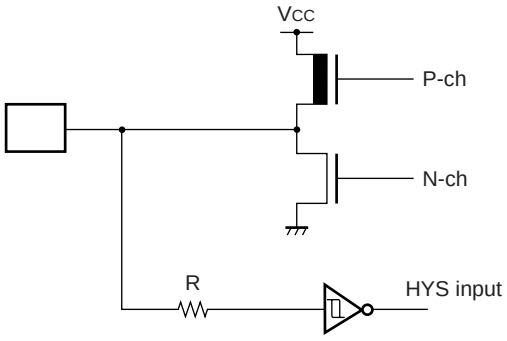
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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port.
73	75	P96	D	General I/O port.
74	76	P97	D	General I/O port.
76	78	PA0	D	General I/O port.
32	34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
35	37	AV_{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47 48	49 50	MD0 MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or V_{SS}.
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or V_{SS}.
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
21, 82	23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

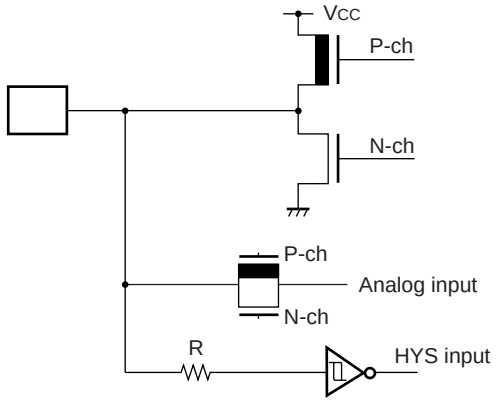
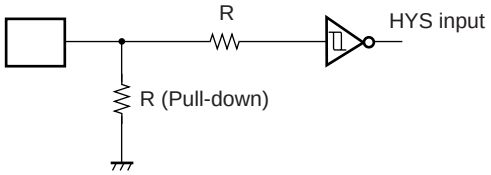
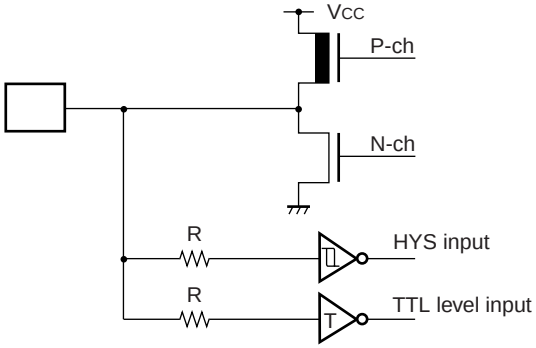
*1 : FPT-100P-M06

*2 : FPT-100P-M05

■ I/O CIRCUIT TYPE

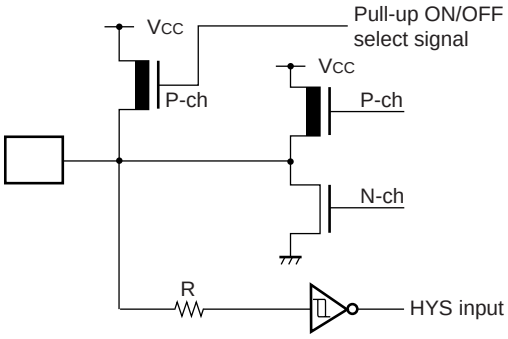
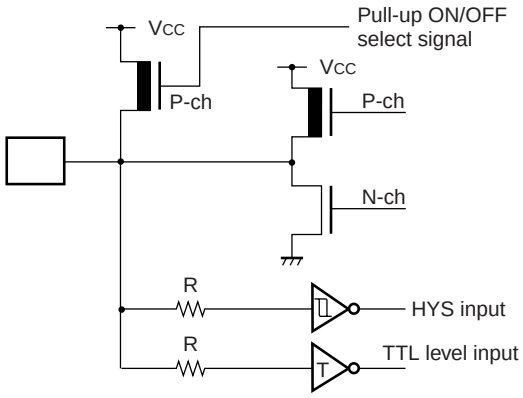
Circuit type	Diagram	Remarks
A		• High-speed oscillation feedback resistor : 1 MΩ approx. • Low-speed oscillation feedback resistor : 10 MΩ approx.
B		• Hysteresis input • Pull-up resistor : 50 kΩ approx.
C		• Hysteresis input
D		• CMOS level output • CMOS Hysteresis input

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Circuit type	Diagram	Remarks
E		• CMOS level output • CMOS Hysteresis input • Analog input
F		• Hysteresis input • Pull-down Resistor : 50 kΩ approx. (except FLASH devices)
G		• CMOS level output • CMOS Hysteresis input • TTL level input (FLASH devices in FLASH writer mode only)

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Circuit type	Diagram	Remarks
H		• CMOS level output • CMOS Hysteresis input • Programmable pull-up resistor : 50 kΩ approx.
I		• CMOS level output • CMOS Hysteresis input • TTL level input (FLASH devices in FLASH writer mode only) • Programmable pull-up resistor : 50 kΩ approx.

■ HANDLING DEVICES

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- The AVcc power supply is applied before the V_{CC} voltage.

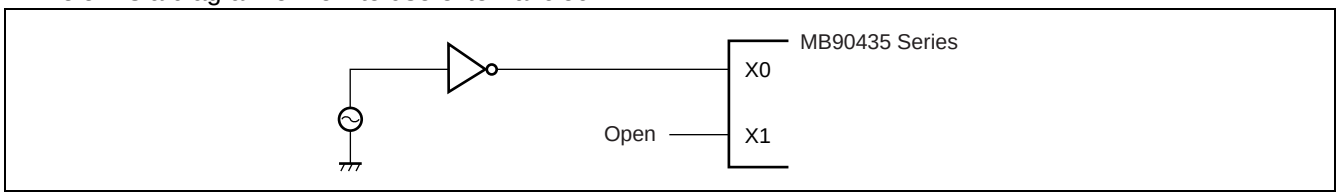
Latch-up may increase the power supply current drastically, causing thermal damage to the device.
For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC}, AVRH) to exceed the digital power-supply voltage.

(2) Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.
Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.
Below is a diagram of how to use external clock.

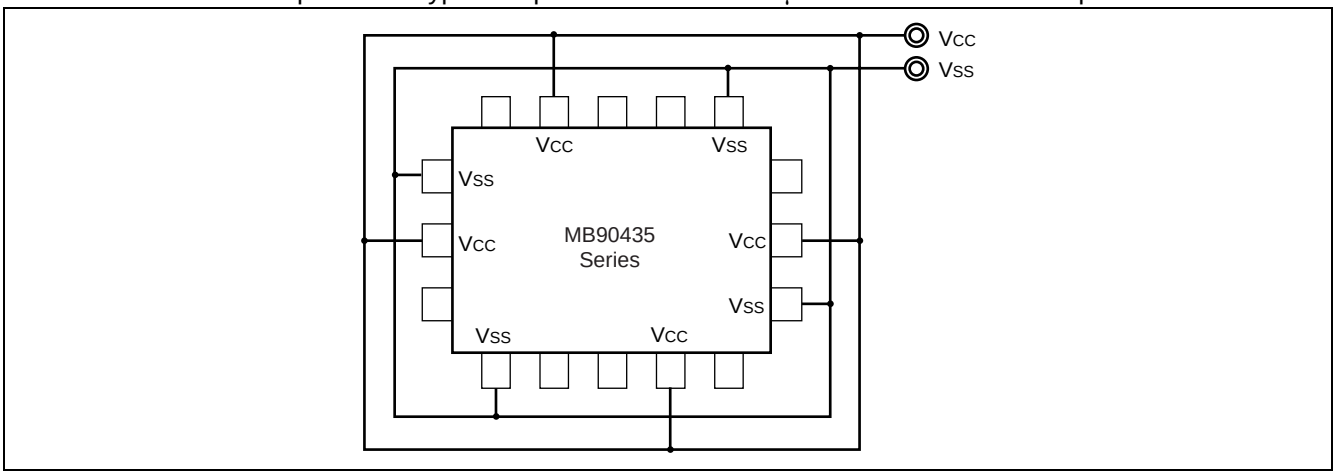


(4) Use of the sub-clock

Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 µF between V_{CC} and V_{SS} pins near the device.



(6) Pull-up/down resistors

The MB90435 Series does not support internal pull-up/down resistors (except Port0 – Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

(12) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

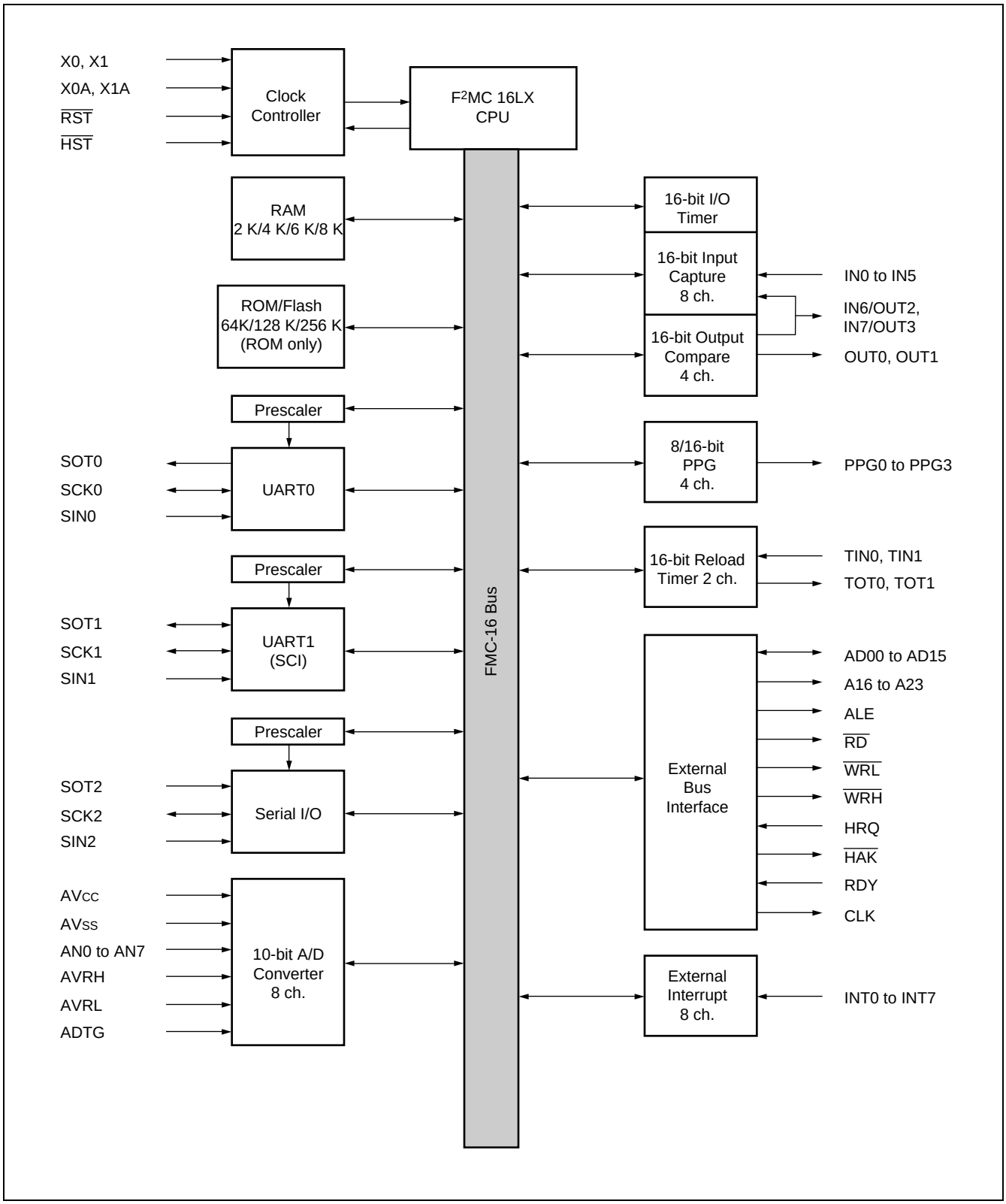
(14) Using REALOS

The use of EI^2OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

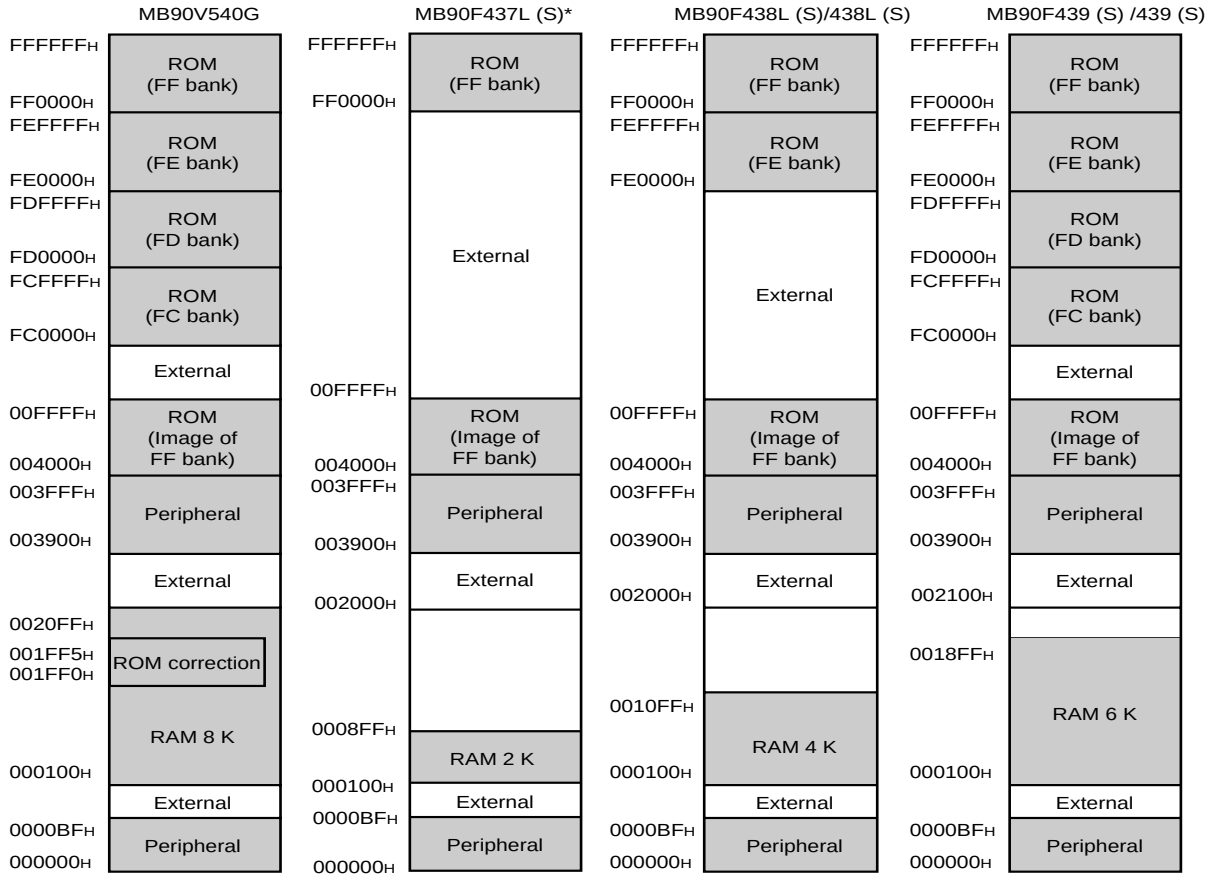
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ BLOCK DIAGRAM



■ MEMORY MAP

The memory space of the MB90435 Series is shown below.



* : Under development

Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00.The image between FF4000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF3FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 data register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 data register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 data register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 data register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 data register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 data register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 data register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H	Port 7 data register	PDR7	R/W	Port 7	$XXXXXXXX_B$
08_H	Port 8 data register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 data register	PDR9	R/W	Port 9	$XXXXXXXX_B$
$0A_H$	Port A data register	PDRA	R/W	Port A	_ _ _ _ _ _ _ X_B
$0B_H$ to $0F_H$	Reserved				
10_H	Port 0 direction register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 direction register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 direction register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 direction register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 direction register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 direction register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 direction register	DDR6	R/W	Port 6	00000000_B
17_H	Port 7 direction register	DDR7	R/W	Port 7	00000000_B
18_H	Port 8 direction register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 direction register	DDR9	R/W	Port 9	00000000_B
$1A_H$	Port A direction register	DDRA	R/W	Port A	_ _ _ _ _ _ _ 0_B
$1B_H$	Analog Input Enable register	ADER	R/W	Port 6, A/D	11111111_B
$1C_H$	Port 0 pull-up control register	PUCR0	R/W	Port 0	00000000_B
$1D_H$	Port 1 pull-up control register	PUCR1	R/W	Port 1	00000000_B
$1E_H$	Port 2 pull-up control register	PUCR2	R/W	Port 2	00000000_B
$1F_H$	Port 3 pull-up control register	PUCR3	R/W	Port 3	00000000_B
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	00000100_B
21_H	Serial Status Register 0	USR0	R/W		00010000_B
22_H	Serial input data register 0/ Serial output data register 0	UIDR0/ UODR0	R/W		$XXXXXXXX_B$
23_H	Rate and data register 0	URD0	R/W		$0000000X_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
24H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0B
25H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0B
26H	Serial input data register 1/ Serial output data register 1	SIDR1/ SODR1	R/W		XXXXXXXXB
27H	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0B
28H	UART1 prescaler control register	U1CDCR	R/W		0_ _ _1 1 1 1B
29H	Serial Edge select register	SES1	R/W		_ _ _ _ _ _ _ 0B
2AH	Prohibited				
2BH	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0_ _ _1 1 1 1B
2CH	Serial mode control register	SMCS	R/W		_ _ _ _0 0 0 0B
2DH	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial data register	SDR	R/W		XXXXXXXXB
2FH	Serial Edge select register	SES2	R/W		_ _ _ _ _ _ _ 0B
30H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External interrupt request register	EIRR	R/W		XXXXXXXXB
32H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D data register 0	ADCR0	R		XXXXXXXXB
37H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Prohibited				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _1B
3DH	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Prohibited				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Prohibited				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 0 _ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
47H to 4BH	Prohibited				
4CH	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0B
4DH	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0B
4EH	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0B
4FH	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0B
50H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0B
51H	Timer control status register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0B
52H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
53H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
54H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0B
55H	Timer control status register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0B
56H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
57H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
58H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0B
59H	Output compare control status register 1	OCS1	R/W		_ _ _0 0 0 0 0B
5AH	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0B
5BH	Output compare control status register 3	OCS3	R/W		_ _ _ 0 0 0 0 0B
5CH to 6BH	Prohibited				
6CH	Timer Counter Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0B
6DH	Timer Counter Data register	TCDT	R/W		0 0 0 0 0 0 0 0B
6EH	Timer Counter Control status register	TCCS	R/W		0 0 0 0 0 0 0 0B
6FH	ROM mirror function selection register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1B
70H to 7FH	Reserved				
80H to 8FH	Reserved				
90H to 9DH	Prohibited				
9EH	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0B
9FH	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0B
A0H	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0B
A1H	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0B

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
A2H to A4H	Prohibited				
A5H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0B
A6H	External address output control register	HACR	W		0 0 0 0 0 0 0 0B
A7H	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 _B
A8H	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1B
A9H	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0B
AAH	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0B
ABH to ADH	Prohibited				
AEH	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0B
AFH	Prohibited				
B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
B1H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1B
B2H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1B
B3H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1B
B4H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1B
B5H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1B
B6H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1B
B7H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1B
B8H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1B
B9H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1B
BAH	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1B
BBH	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1B
BCH	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1B
BDH	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1B
BEH	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1B
BFH	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1B
C0H to FFH	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
1FF0H	Program address detection register 0	PADR0	R/W	Address Match Detection Function	XXXXXXXXB
1FF1H	Program address detection register 0	PADR0	R/W		XXXXXXXXB
1FF2H	Program address detection register 0	PADR0	R/W		XXXXXXXXB
1FF3H	Program address detection register 1	PADR1	R/W		XXXXXXXXB
1FF4H	Program address detection register 1	PADR1	R/W		XXXXXXXXB
1FF5H	Program address detection register 1	PADR1	R/W		XXXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3900H	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXXB
3901H	Reload H	PRLH0	R/W		XXXXXXXXB
3902H	Reload L	PRLL1	R/W		XXXXXXXXB
3903H	Reload H	PRLH1	R/W		XXXXXXXXB
3904H	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXXB
3905H	Reload H	PRLH2	R/W		XXXXXXXXB
3906H	Reload L	PRLL3	R/W		XXXXXXXXB
3907H	Reload H	PRLH3	R/W		XXXXXXXXB
3908H	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
3909H	Reload H	PRLH4	R/W		XXXXXXXXB
390AH	Reload L	PRLL5	R/W		XXXXXXXXB
390BH	Reload H	PRLH5	R/W		XXXXXXXXB
390CH	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
390DH	Reload H	PRLH6	R/W		XXXXXXXXB
390EH	Reload L	PRLL7	R/W		XXXXXXXXB
390FH	Reload H	PRLH7	R/W		XXXXXXXXB
3910H to 3917H	Reserved				
3918H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
3919H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
391AH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391BH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391CH	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
391DH	Input Capture Register 2	IPCP2	R		XXXXXXXXB
391EH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
391FH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
3920H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
3921H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
3922H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3923H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3924H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXXB
3925H	Input Capture Register 6	IPCP6	R		XXXXXXXXB
3926H	Input Capture Register 7	IPCP7	R		XXXXXXXXB
3927H	Input Capture Register 7	IPCP7	R		XXXXXXXXB

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3928H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare Register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved				
3B00H to 3BFFH	Reserved				
3C00H to 3CFFH	Reserved				
3D00H to 3DFFH	Reserved				
3E00H to 3FFFH	Reserved				

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.

Note : Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

■ INTERRUPT MAP

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
Reserved	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
Reserved	N/A	#12	FFFFCC$_H$		
Reserved	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
Reserved	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
I/O Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

*1 : The interrupt request flag is cleared by the EI^{2}OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI^{2}OS interrupt clear signal. A stop request is available.

Notes :
- N/A : The interrupt request flag is not cleared by the EI^{2}OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI^{2}OS interrupt clear signal.
- At the end of EI^{2}OS, the EI^{2}OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI^{2}OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI^{2}OS clear signal caused by the first event. So it is recommended not to use the EI^{2}OS for this interrupt number.
- If EI^{2}OS is enabled, EI^{2}OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI^{2}OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI^{2}OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/AVRL, AVRH ≥ AVRL *1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*6
Total maximum clamp current	$\sum\|I_{CLAMP}\|$	—	20	mA	*6
“L” level max output current	I_{OL}	—	15	mA	*3
“L” level avg. output current	I_{OLAV}	—	4	mA	*4
“L” level max overall output current	$\sum I_{OL}$	—	100	mA	
“L” level avg. overall output current	$\sum I_{OLAV}$	—	50	mA	*5
“H” level max output current	I_{OH}	—	–15	mA	*3
“H” level avg. output current	I_{OHAV}	—	–4	mA	*4
“H” level max overall output current	$\sum I_{OH}$	—	–100	mA	
“H” level avg. overall output current	$\sum I_{OHAV}$	—	–50	mA	*5
Power consumption	P_D	—	500	mW	Flash device
		—	400	mW	Mask ROM
Operating temperature	T_A	–40	+105	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : AV_{CC}, AVRH, AVRL should not exceed V_{CC}. Also, AVRH, AVRL should not exceed AV_{CC}, and AVRL does not exceed AVRH.

*2 : V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

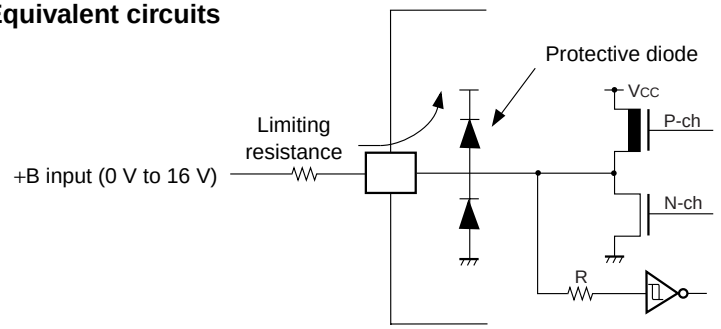
*6 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.

(Continued)

(Continued)

- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

- **Input/Output Equivalent circuits**



Note : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : MB90F439 (S) /439 (S) /V540G
		3.5	5.0	5.5	V	Under normal operation : MB90F438L (S) /437L (S) /438L (S)
		3.0	—	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	–40	—	+105	°C	

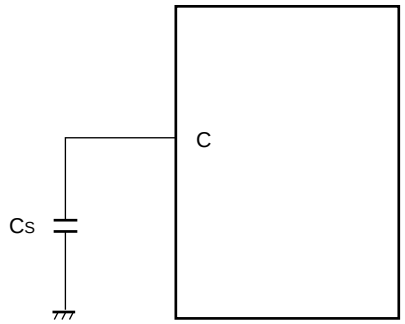
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The V_{CC} Capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

- **C Pin Connection Diagram**



3. DC Characteristics

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IH}	TTL input pin	—	2.0	—	—	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{CC} – 0.3	—	0.2 V_{CC}	V	
	V_{IL}	TTL input pin	—	—	—	0.8	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
Output H voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	5	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

(Continued)

(Continued)

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I_{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I_{CTS}		V_{CC} = 5.0 V ± 1%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	µA	
				—	600	1100	µA	MB90F348L (S)
				—	200	400	µA	MB90437L (S) / 438L (S)
	I_{CCL}		Internal frequency : 8 kHz, At sub operation, T_A = 25 °C	—	400	750	µA	MB90F438L (S)
				—	50	100	µA	Mask ROM
				—	150	300	µA	Flash device
	I_{CCLS}		Internal frequency : 8 kHz, At sub sleep, T_A = 25 °C	—	15	40	µA	
	I_{CCT}		Internal frequency : 8 kHz, At timer mode, T_A = 25 °C	—	7	25	µA	
	I_{CCH1}		At stop, T_A = 25 °C	—	5	20	µA	
	I_{CCH2}		At hardware standby mode, T_A = 25 °C	—	50	100	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

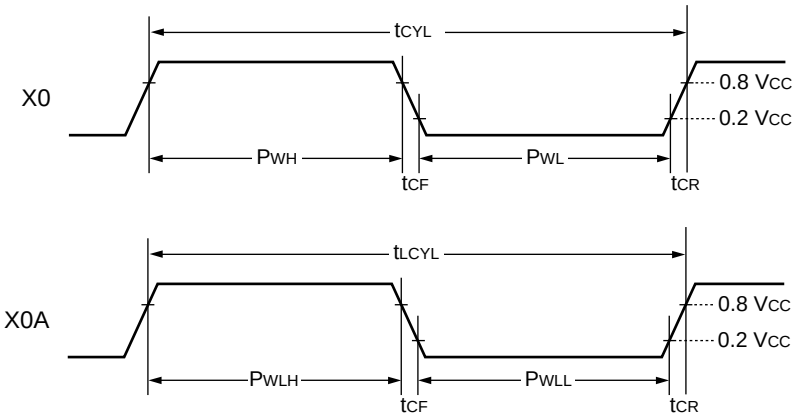
4. AC Characteristics

(1) Clock Timing

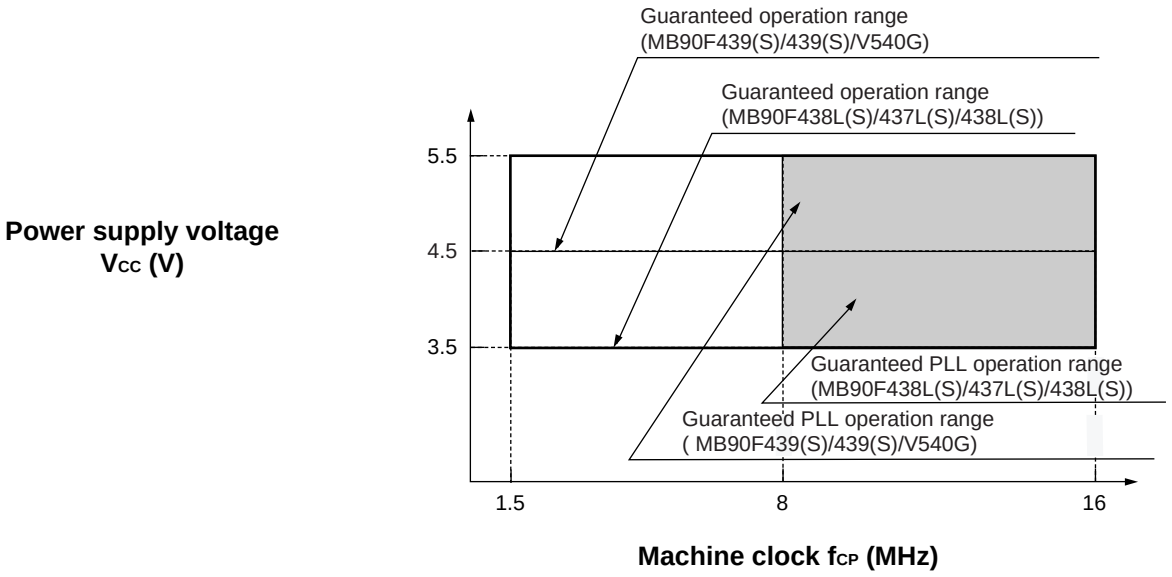
(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	V_{CC} = 5.0 V±10%
			3	—	5	MHz	V_{CC}<4.5 (MB90F438L (S) / 437L (S) /438L (S))
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Oscillation cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	V_{CC} = 5.0 V±10%
			200	—	333	ns	V_{CC}<4.5 (MB90F438L (S) / 437L (S) /438L (S))
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

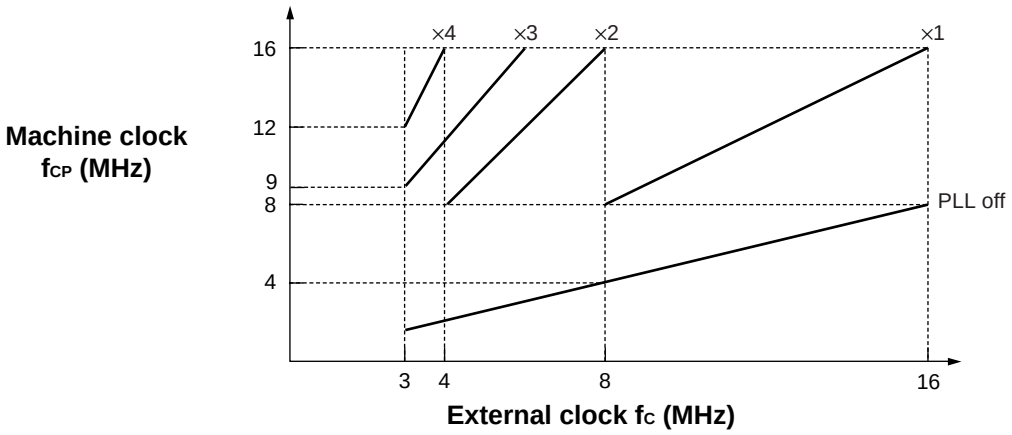
- **Clock Timing**



- **Guaranteed PLL operation range**



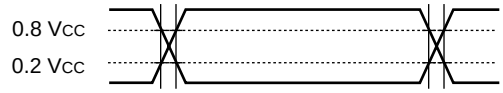
- **External clock frequency and Machine clock frequency**



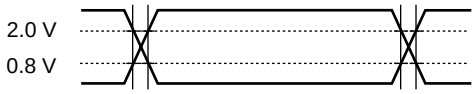
AC characteristics are set to the measured reference voltage values below.

- **Input signal waveform**

Hysteresis Input Pin

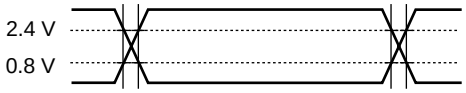


TTL Input Pin



- **Output signal waveform**

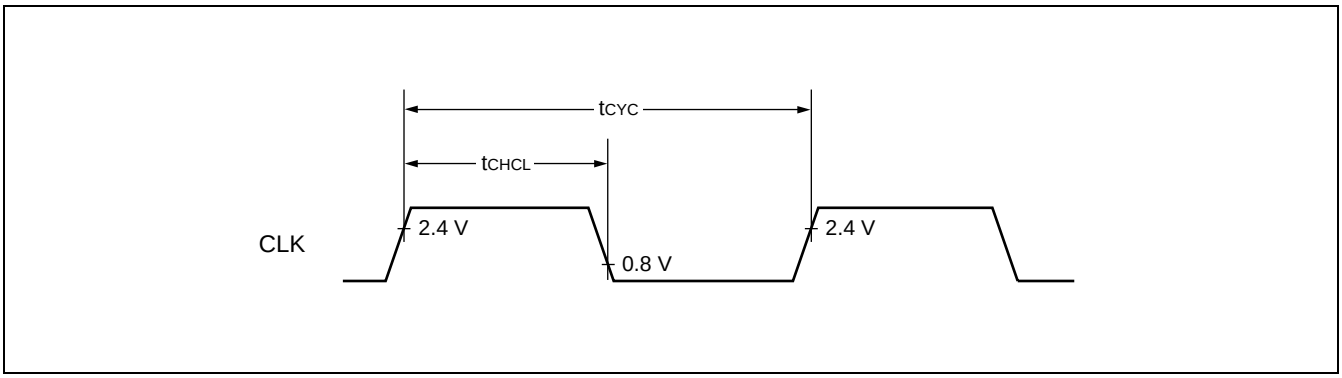
Output Pin



(2) Clock Output Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	V_{CC} = 5 V ± 10%	62.5	—	ns	
CLK↑ →CLK↓	t_{CHCL}			20	—	ns	



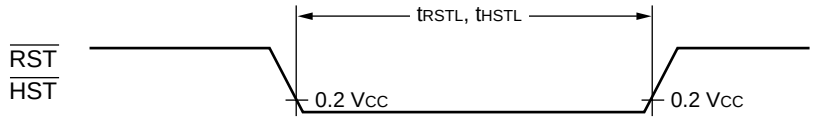
(3) Reset and Hardware Standby Input Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

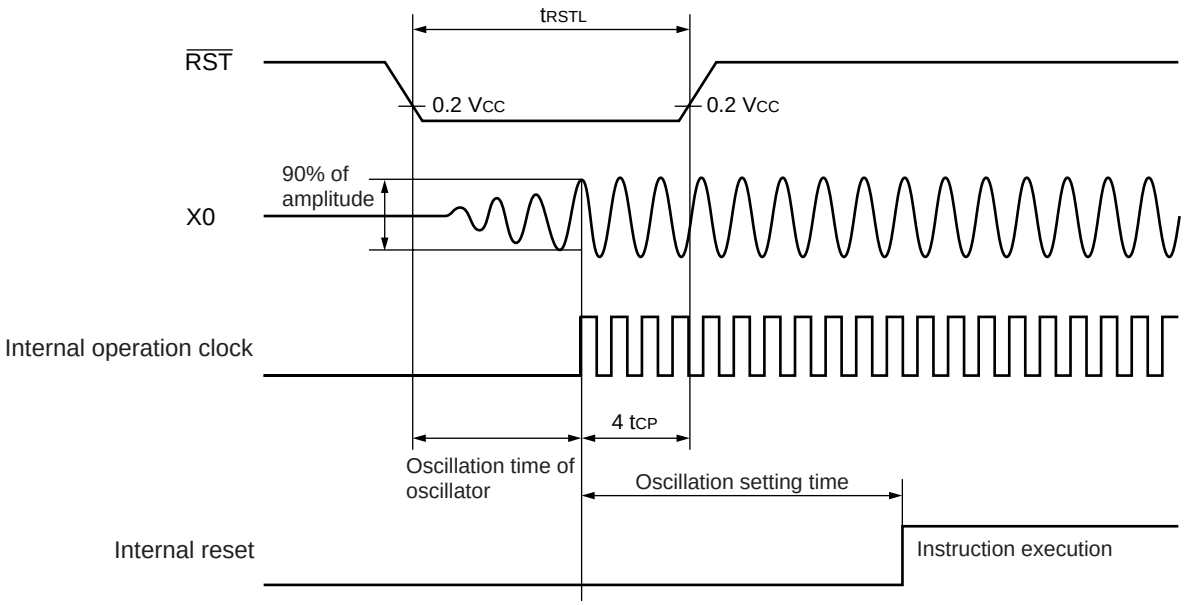
Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	4 t_{CP}	—	ns	Under normal operation
			Oscillation time of oscillator + 4 t_{CP}	—	ms	In stop mode
			100	—	µs	Pseudo timer mode (MB90437L (S) /438L (S))
			4 t_{CP}	—	ns	Pseudo timer mode (Other than MB90437L (S) /438L (S))
			2 t_{CP}	—	µs	In sub clock mode, sub sleep mode and watch mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	4 t_{CP}	—	ns	Under normal operation

"t_{cp}" represents one cycle time of the machine clock.
Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR/ceramic oscillator, the oscillation time is between handreds of µs to several ms. In the external clock, the oscillation time is 0 ns.
Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

- **Under normal operation, Pseudo timer mode, Sub clock mode, Sub sleep mode, Watch mode**



- **In stop mode**



(4) Power On Reset

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

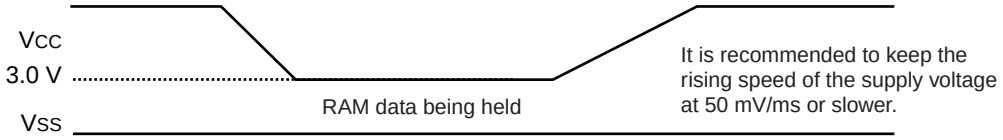
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : • The above values are used for creating a power-on reset.
• Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



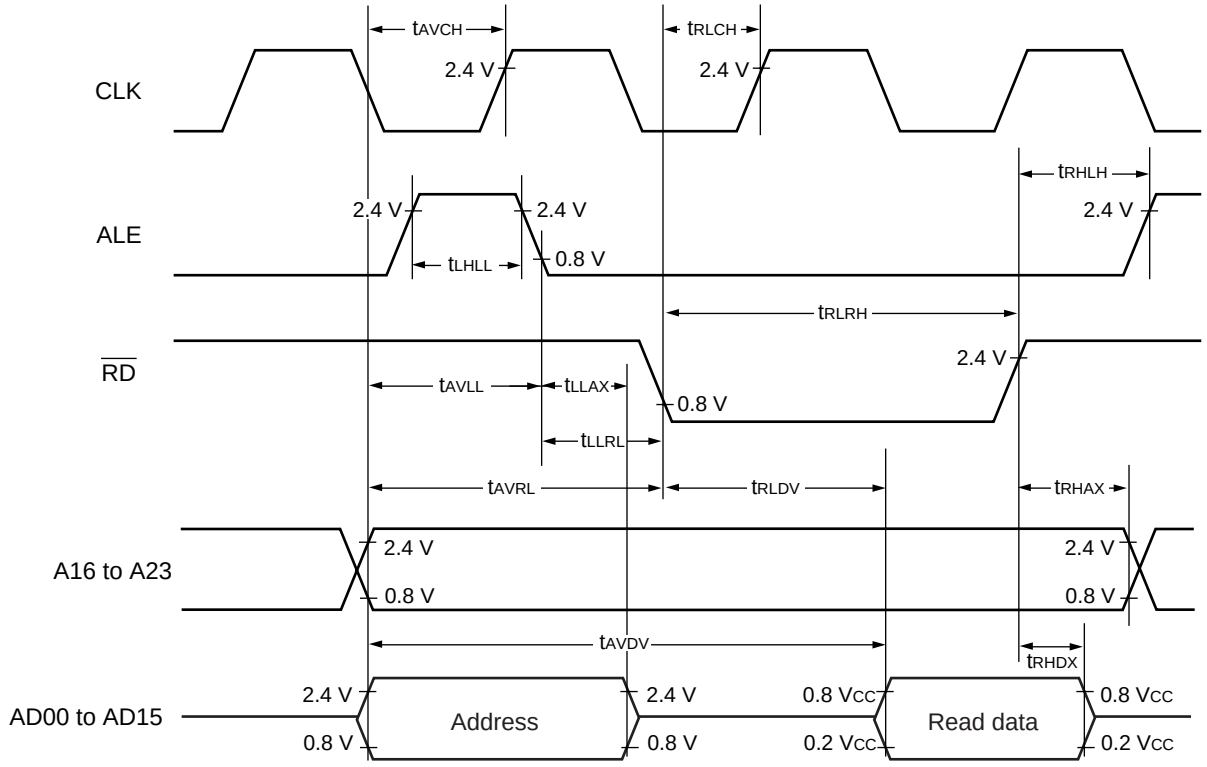
(5) Bus Timing (Read)

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Valid address→ALE↓time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	—	ns	
ALE↓→Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	—	ns	
Valid address→$\overline{RD}$↓time	t_{AVRL}	A16 toA23, AD00 to AD15, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address→Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$3\ t_{CP}/2 - 20$	—	ns	
$\overline{RD}$↓→Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		—	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$↑→Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	—	ns	
$\overline{RD}$↓→ALE↑time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$↑→Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23		$t_{CP}/2 - 10$	—	ns	
Valid address→CLK↑time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$↓→CLK↑time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	
ALE↓→$\overline{RD}$↓time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

- **Bus Timing (Read)**



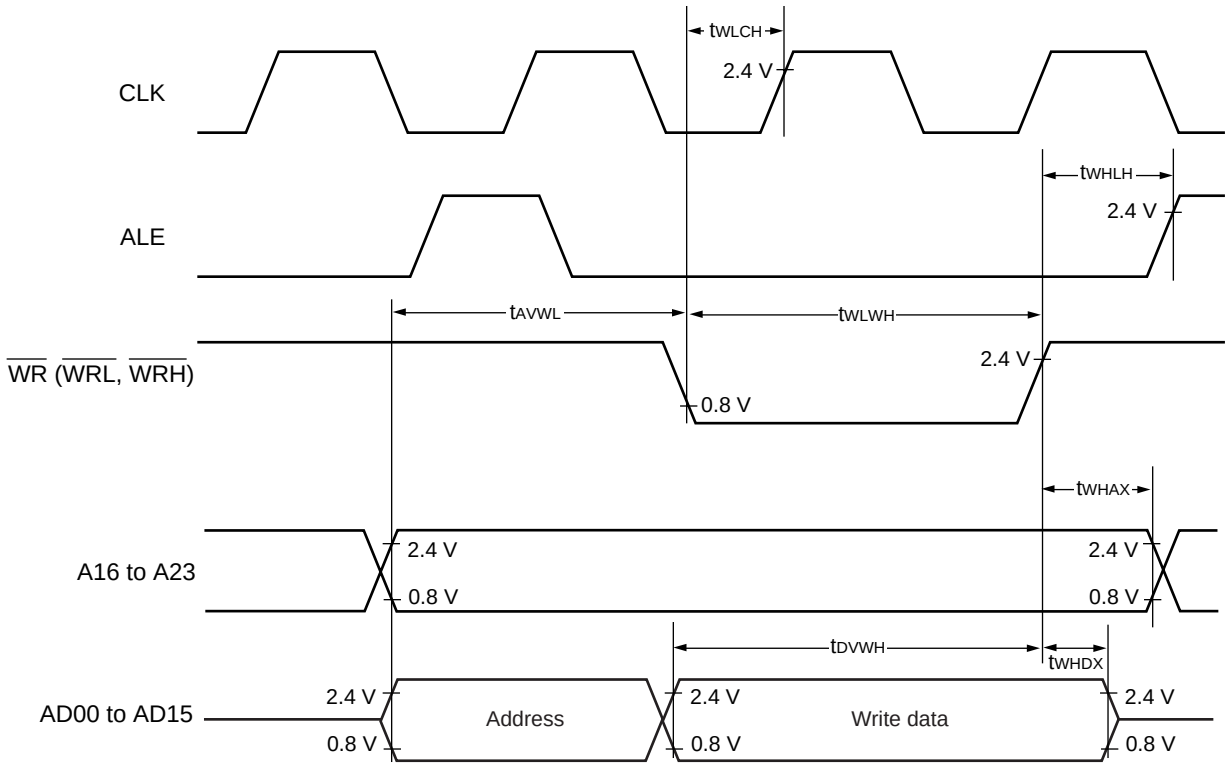
(6) Bus Timing (Write)

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address→$\overline{WR}$↓time	t_{AVWL}	A16 to A23 AD00 to AD15, $\overline{WR}$	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 – 20	—	ns	
Valid data output→$\overline{WR}$↑time	t_{DVWH}	AD00 to AD15, $\overline{WR}$		3 t_{CP}/2 – 20	—	ns	
$\overline{WR}$↑→Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$		20	—	ns	
$\overline{WR}$↑→Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$		t_{CP}/2 – 10	—	ns	
$\overline{WR}$↑→ALE↑time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WR}$↑→CLK↑time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 20	—	ns	

- **Bus Timing (Write)**



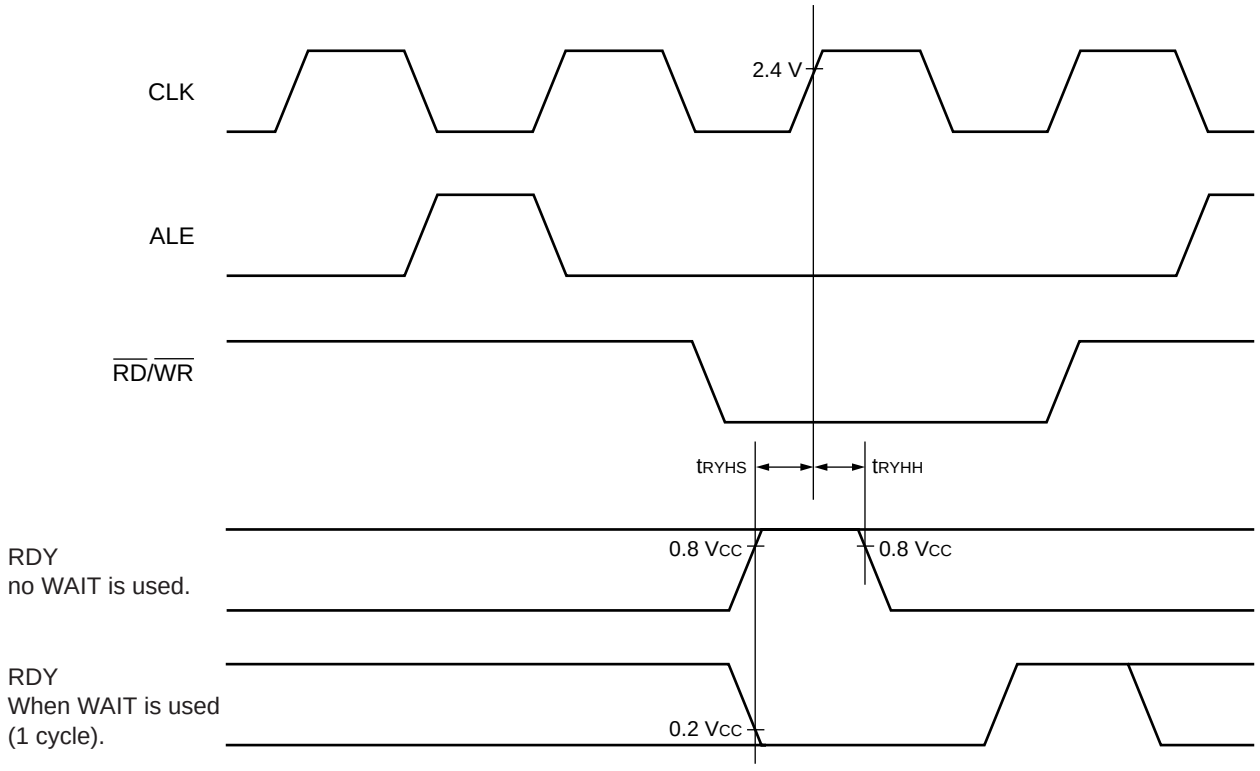
(7) Ready Input Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

- **Ready Input Timing**



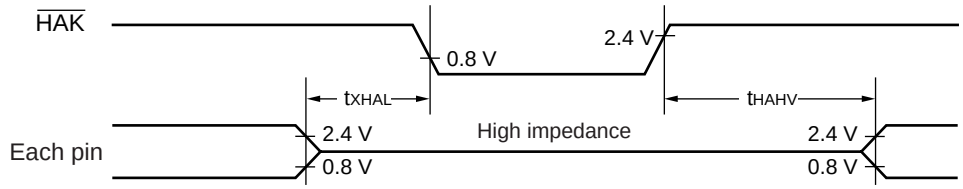
(8) Hold Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating→$\overline{HAK}$↓time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$↑time→Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{HAK}$ is changed.

- **Hold Timing**



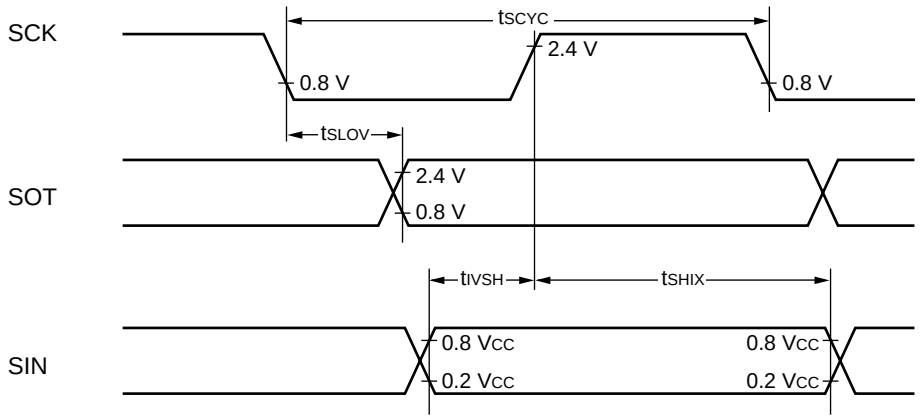
(9) UART0/1, Serial I/O Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

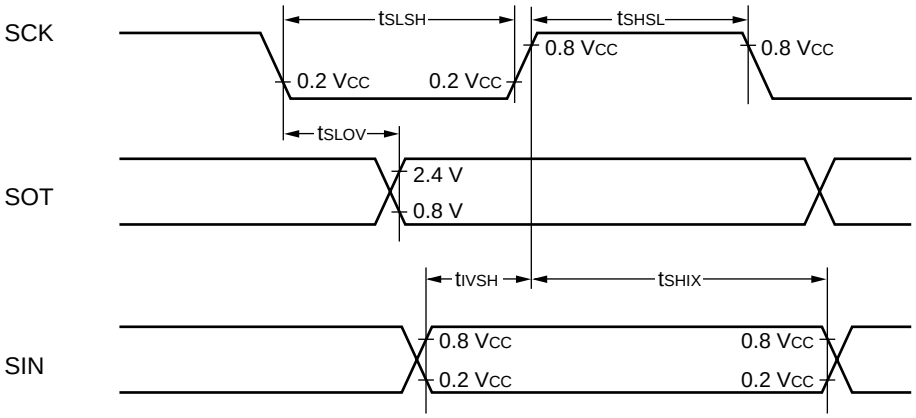
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK↓→SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	80	ns	
Valid SIN→SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK↑→Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK↓→SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN→SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK↑→Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes : • AC characteristic in CLK synchronized mode.
• C_L is load capacity value of pins when testing.
• For t_{CP} (Machine clock cycle time) , refer to “ (1) Clock Timing”.

- Internal Shift Clock Mode



- External Shift Clock Mode

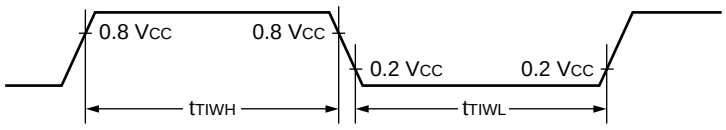


(10) Timer Input Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

- **Timer Input Timing**

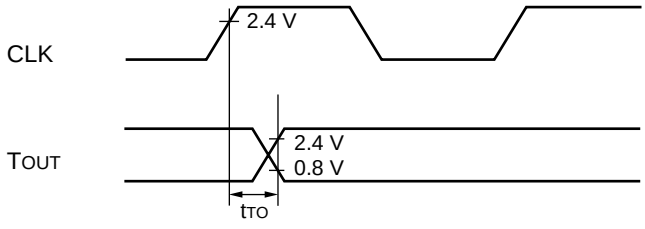


(11) Timer Output Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)
(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK↑→T_{OUT} change time	t_{TO}	TOT0 to TOT1, PPG0 to PPG3	—	30	—	ns	

- **Timer Output Timing**



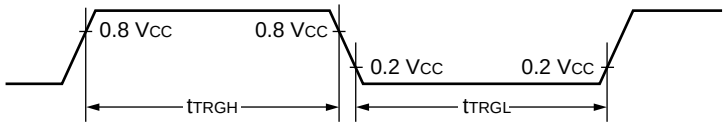
(12) Trigger Input Timing

(MB90F438L (S) /437L (S) /438L (S) : V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

(MB90F439 (S) /439 (S) /V540G : V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under nomal operation
				1	—	µs	In stop mode

- **Trigger Input Timing**



5. A/D Converter

- **Electrical Characteristics**

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, 3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	mV	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	mV	
Compare time	—	—	352 t_{CP}	—	—	ns	Internal frequency : 16 MHz
Sampling time	—	—	64 t_{CP}	—	—	ns	Internal frequency : 16 MHz
Analog port input current	I_{AIN}	AN0 to AN7	−1	—	1	µA	V_{CC} = AV_{CC} = 5.0 V ± 1%
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	400	600	µA	Flash device
			—	140	260	µA	Mask ROM
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not using an A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

Note: The functionality of the A/D converter is only guaranteed for VCC = 5.0 V ± 10 % (also for MB90F438L (S) / 437L (S) /438L (S)) .

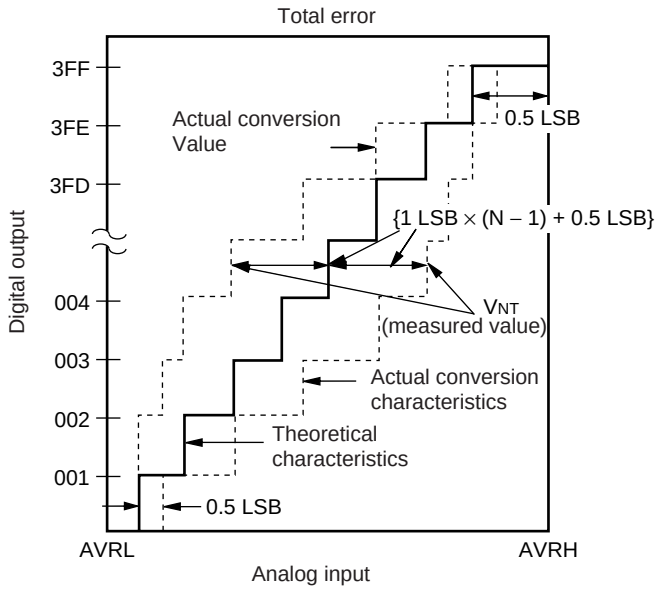
- **A/D Converter Glossary**

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ←→ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ←→ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1\,\text{LSB} = (\text{Theoretical value})\,\frac{\text{AVRH} - \text{AVRL}}{1024}\,[\text{V}]$$

V_{OT} (Theoretical value) = AVRL + 0.5 LSB [V]

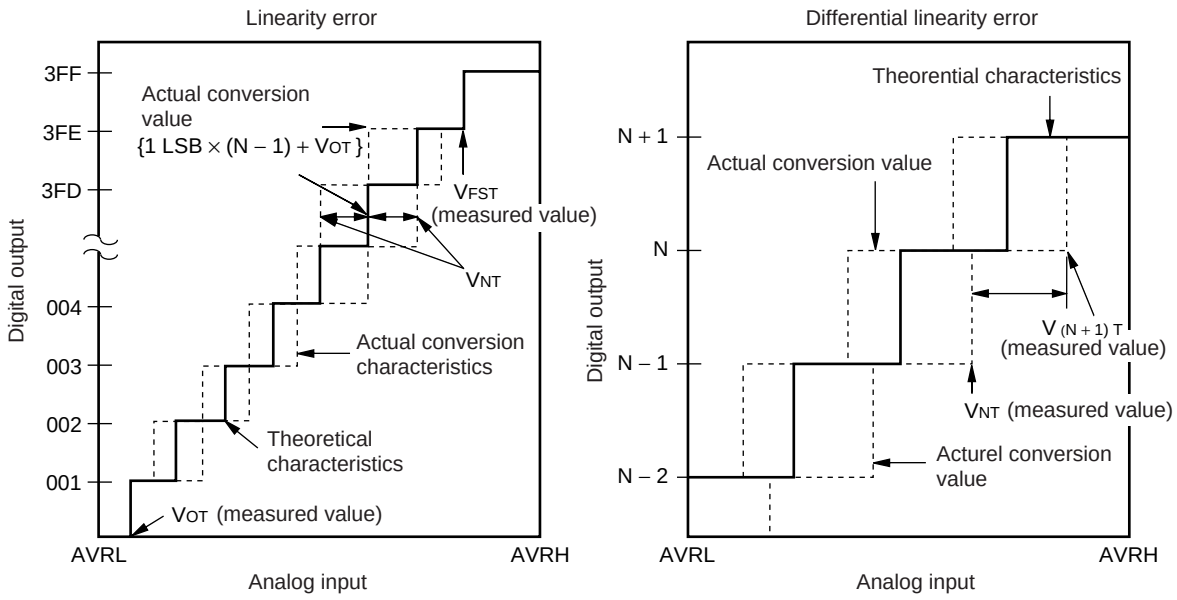
V_{FST} (Theoretical value) = AVRH – 1.5 LSB [V]

$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\,\text{LSB} \times (\text{N} - 1) + 0.5\,\text{LSB}\}}{1\,\text{LSB}}\,[\text{LSB}]$$

V_{NT} : Voltage at a transition of digital output from (N – 1) to N

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

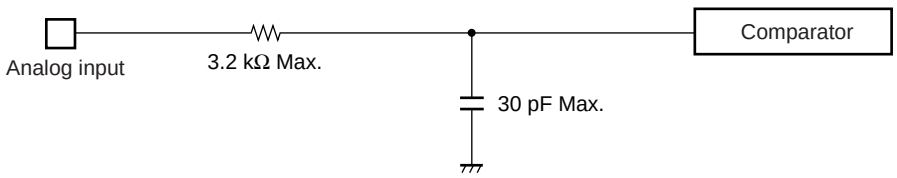
- **Notes on Using A/D Converter**

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @machine clock of 16 MHz) .

- **Equipment of analog input circuit model**



- **Error**

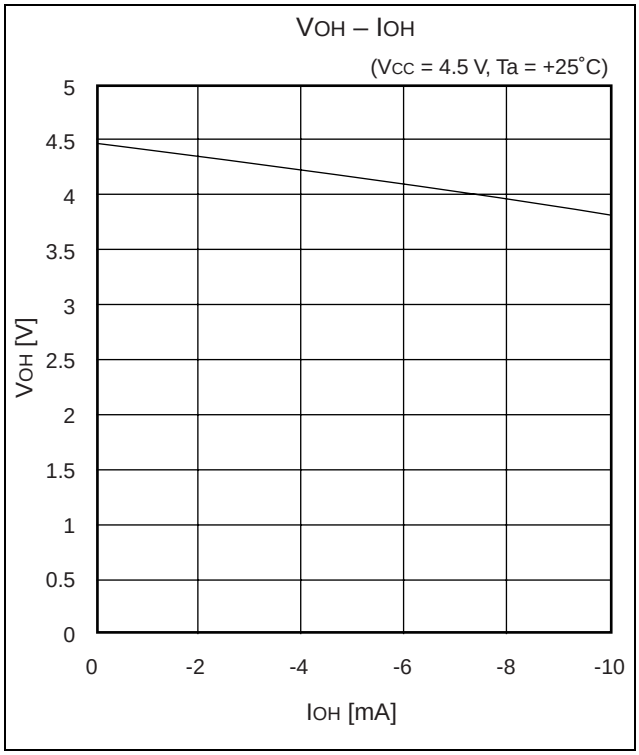
The smaller the | AVRH – AVRL |, the greater the error would become relatively.

6. Flash Memory Program/Erase Characteristics

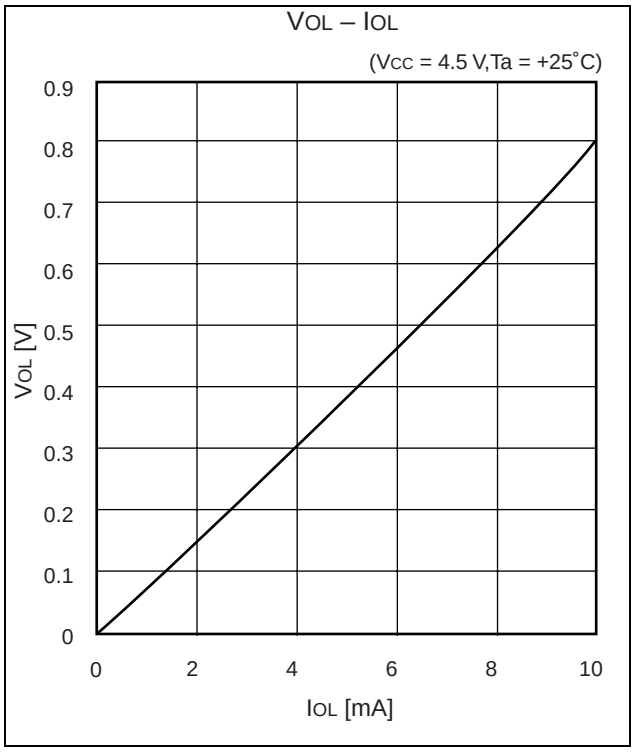
Parameter	Condition	Value			Units	Remarks	
		Min	Typ	Max			
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes 00_H programming prior erasure	
Chip erase time		—	5	—	s	MB90F438L (S)	Excludes 00_H programming prior erasure
			7	—	s	MB90F439 (S)	
Word (16 bit width) programming time		—	16	3,600	µs	Excludes system-level overhead	
Erase/Program cycle	—	10,000	—	—	cycle		

■ EXAMPLE CHARACTERISTICS

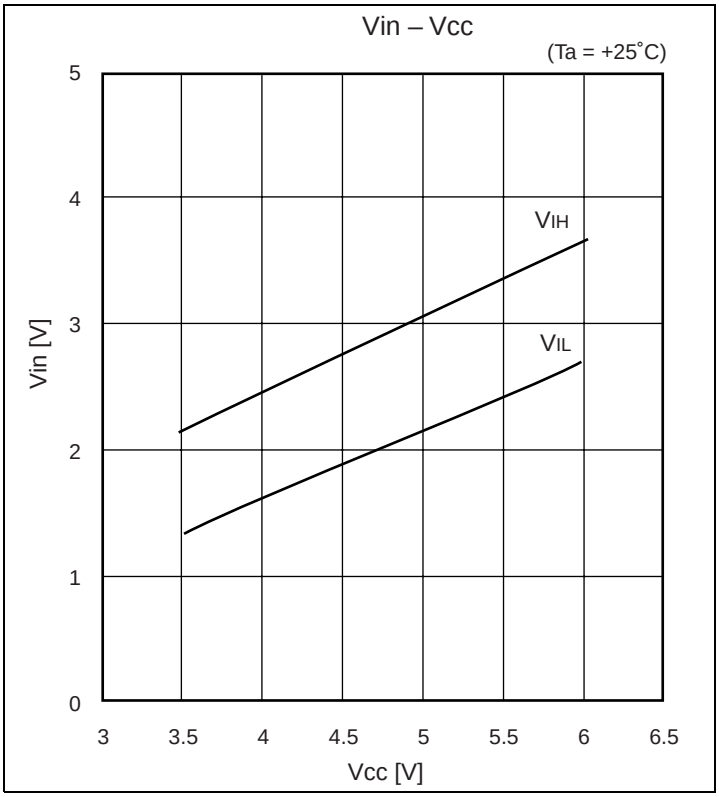
• “H” level output voltage



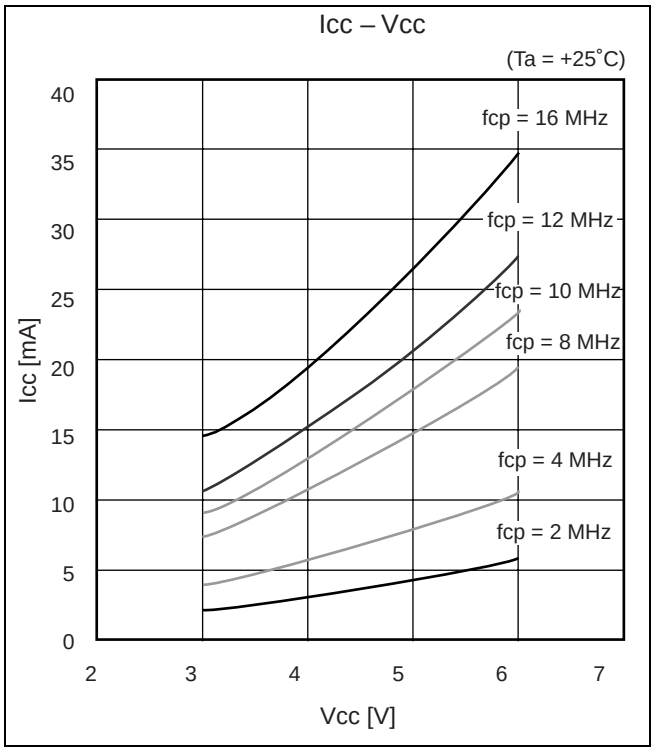
• “L” level output voltage

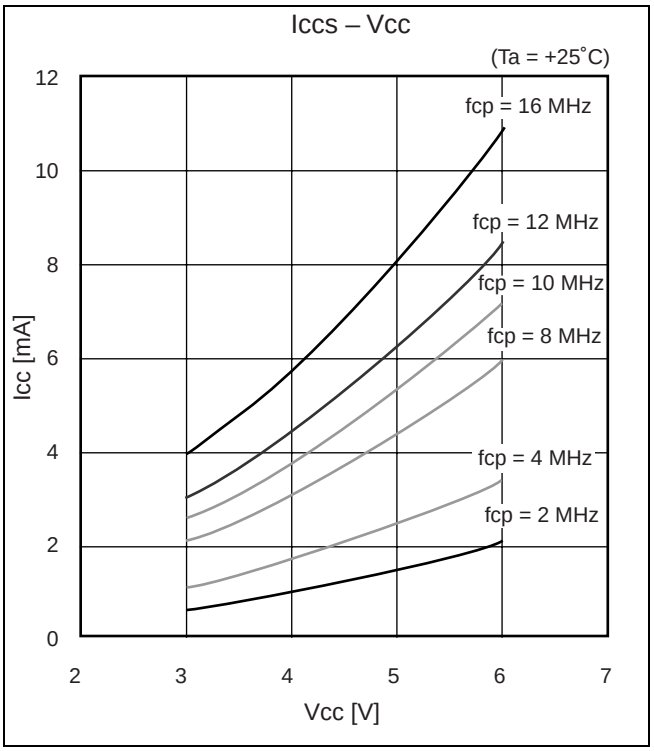


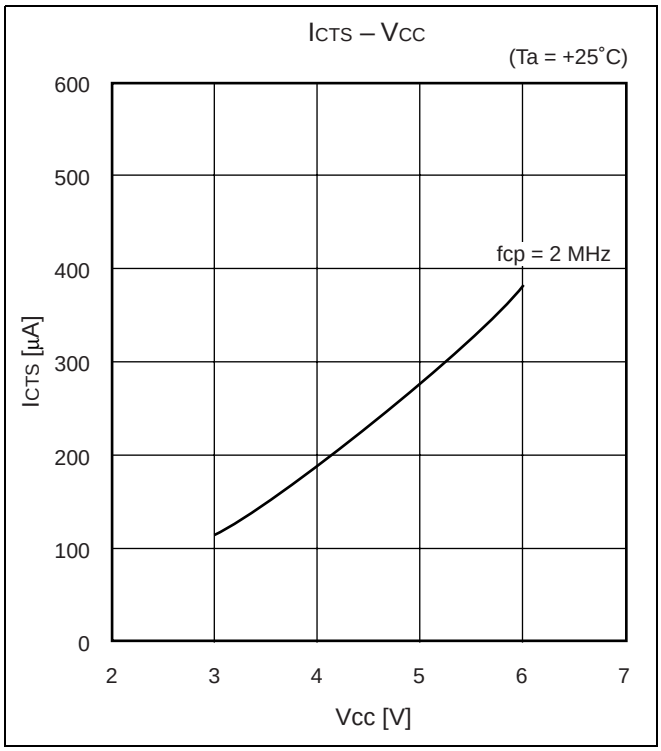
• “H” level input voltage/ “L” level input voltage (Hysterisis inpiut)

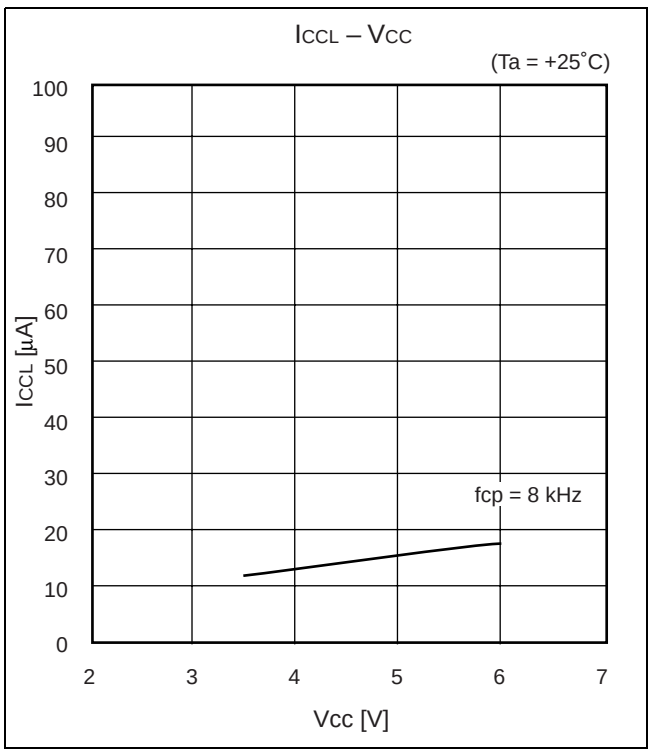


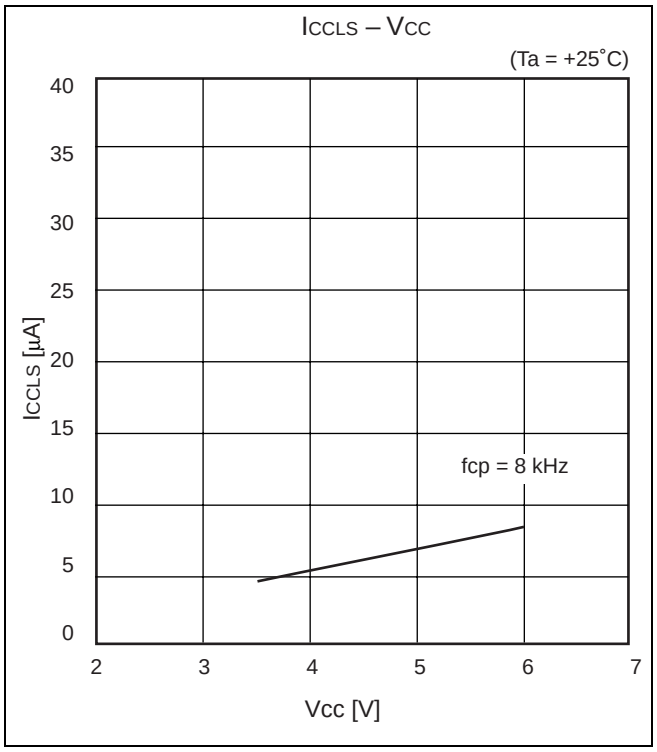
• Power supply current (MB90439)

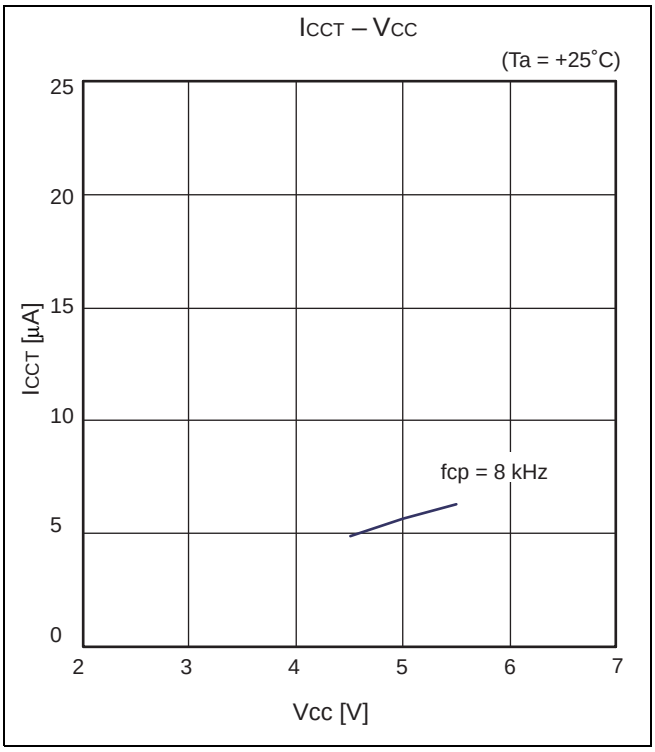


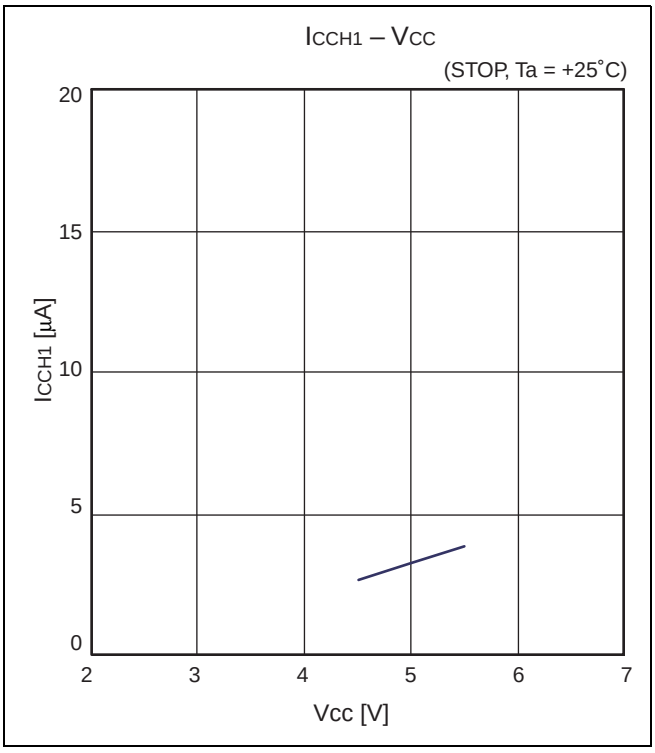




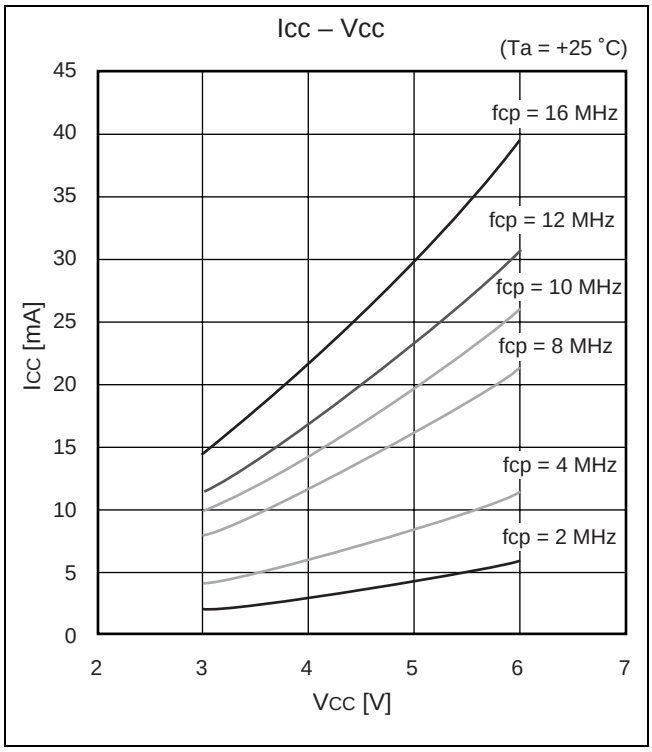


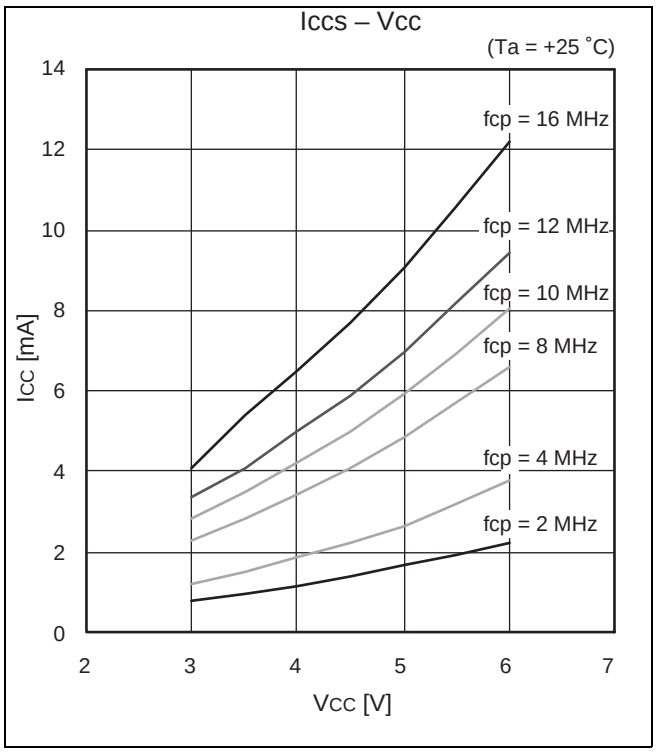

ICCLS – VCC
(Ta = +25˚C)
ICCLS [µA]
40
35
30
25
20
15
10
5
0
2
3
4
5
6
7
Vcc [V]
fcp = 8 kHz

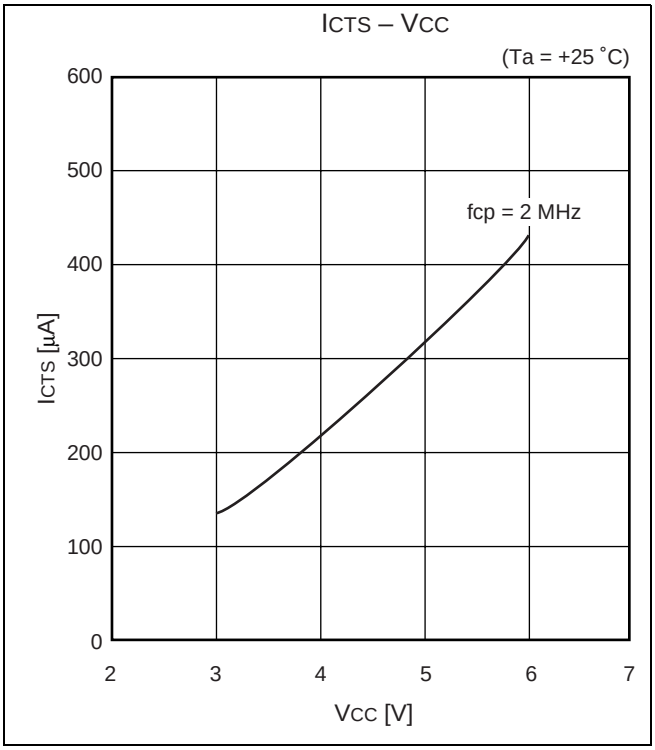

ICCT – VCC
(Ta = +25˚C)
ICCT [µA]
25
20
15
10
5
0
2
3
4
5
6
7
Vcc [V]
fcp = 8 kHz

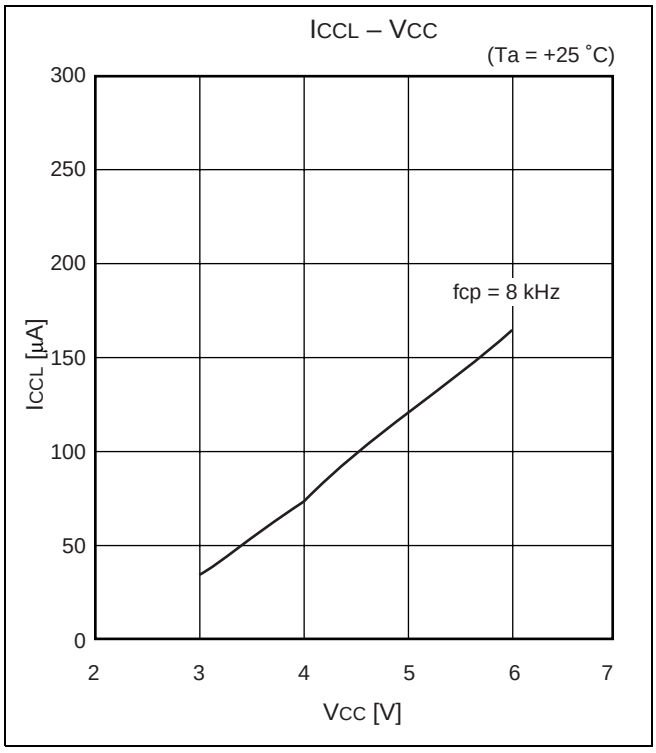

ICCH1 – VCC
(STOP, Ta = +25˚C)
ICCH1 [µA]
20
15
10
5
0
2
3
4
5
6
7
Vcc [V]

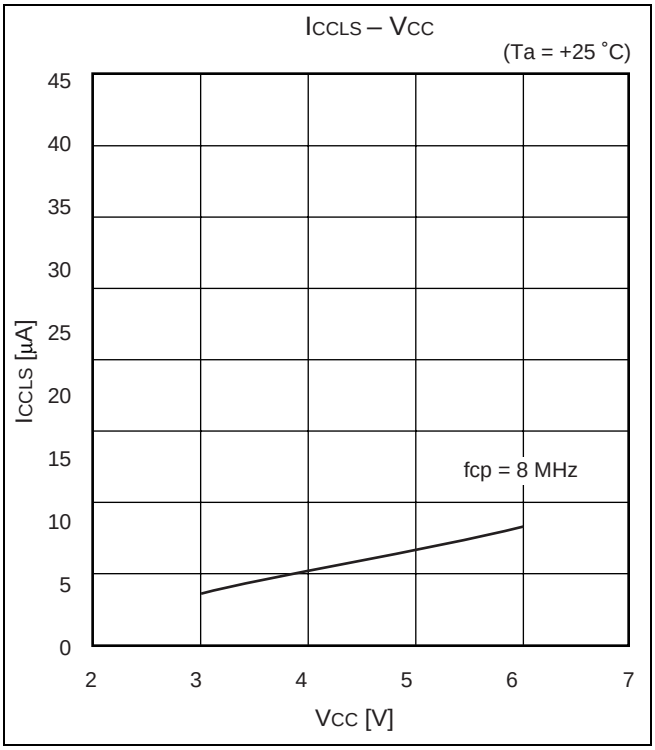
• Power supply current (MB90F439)

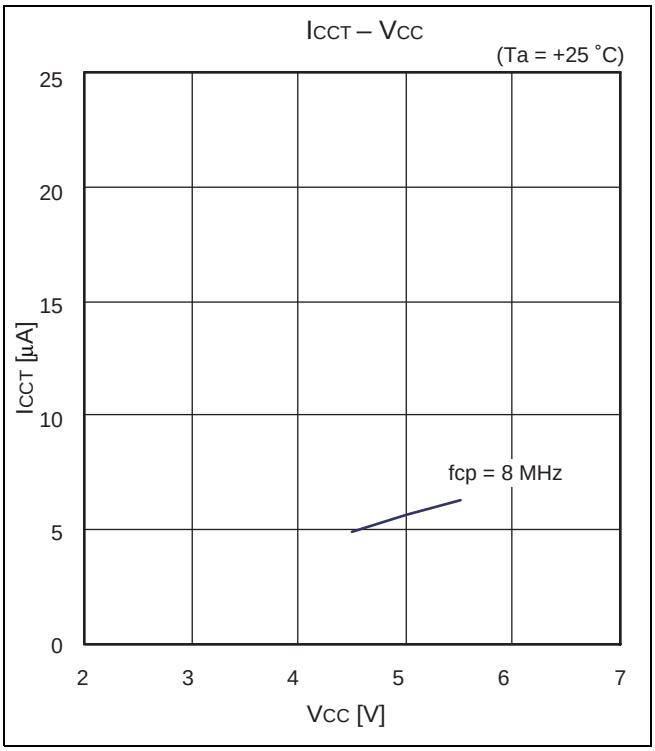


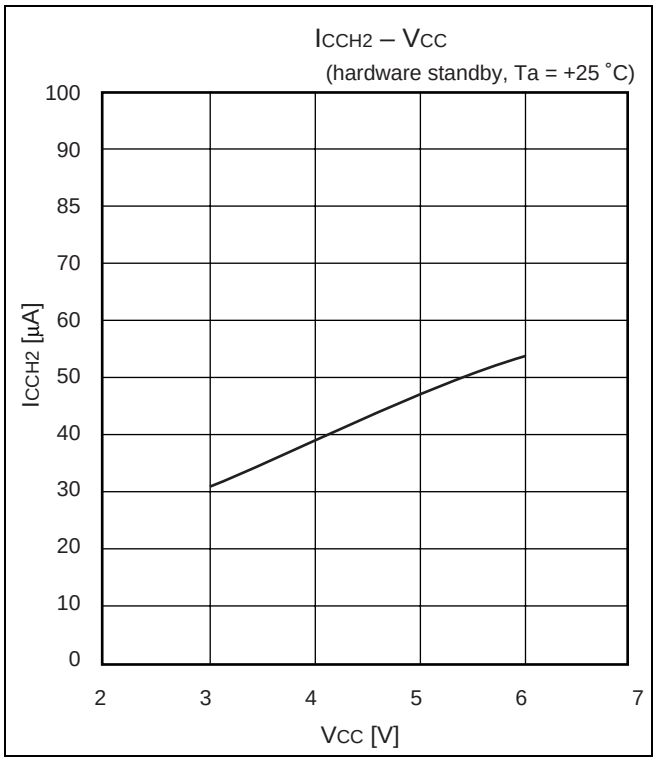


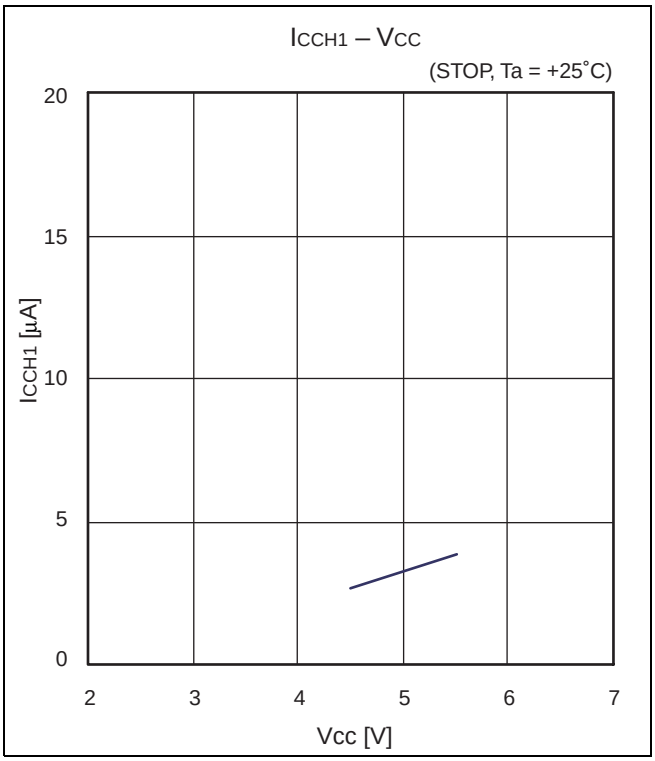





ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25˚C)
ICCH1 [µA]
20
15
10
5
0
2
3
4
5
6
7
Vcc [V]

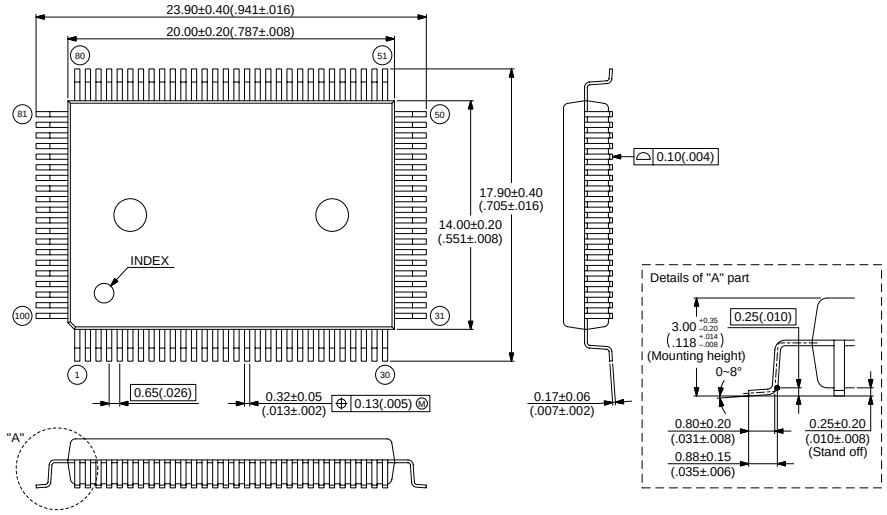
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F438LPF MB90F438LSPF MB90F439PF MB90F439SPF MB90437LPF MB90437LSPF MB90438LPF MB90438LSPF MB90439PF MB90439SPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F438LPFV MB90F438LSPFV MB90F439PFV MB90F439SPFV MB90437LPFV MB90437LSPFV MB90438LPFV MB90438LSPFV MB90439PFV MB90439SPFV	100-pin Plastic LQFP (FPT-100P-M05)	

■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)

Note: Pins width and pins thickness include plating thickness.

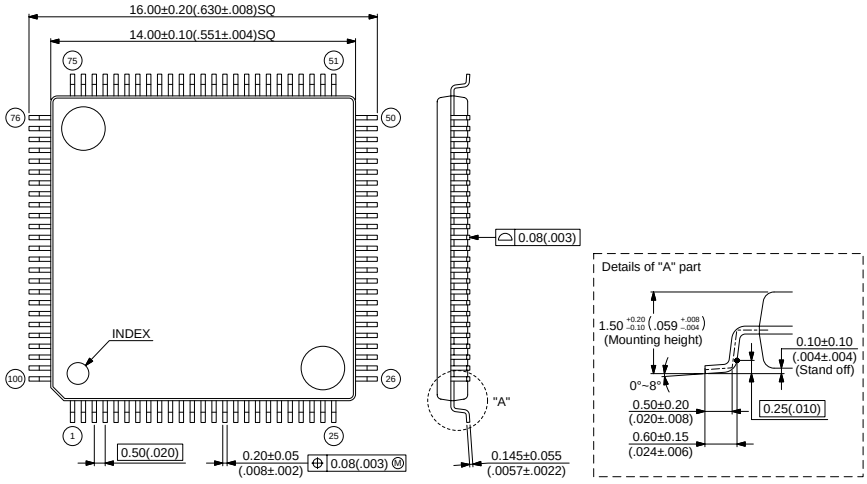


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Dimensions in mm (inches)

100-pin Plastic LQFP
(FPT-100P-M05)

Note : Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)

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