

PUSB3TB6

ESD protection for ultra high-speed interfaces

Rev. 1 — 19 August 2014 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed and Hi - Speed USB combination, Secure Digital (SD) card 3.0 and Thunderbolt interfaces against ElectroStatic Discharge (ESD).

The device includes six high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in a DFN2111-7 (SOT1358-1) leadless ultra small Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode structure offering ultra low line capacitance of only 0.27 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to ±10 kV contact exceeding IEC 61000-4-2, level 4.

1.2 Features and benefits

- System ESD protection for USB 2.0 and USB 3.0 combination, SD card 3.0 and Thunderbolt interfaces
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.27 pF for each channel
- Design-friendly pass-through signal routing

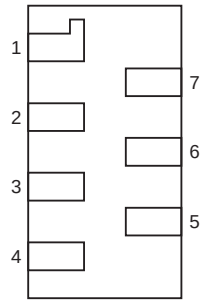
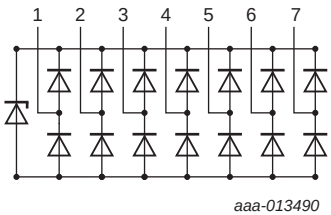
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- Portable and wearable devices
- Smartphones and tablet PCs
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 Transparent top view	 aaa-013490
2	GND	ground[1]		
3	CH2	channel 2 ESD protection		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	CH5	channel 5 ESD protection		
7	CH6	channel 6 ESD protection		

[1] Any pin can be chosen for ground connection; one pin must be connected to ground.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3TB6	DFN2111-7	plastic extremely thin small outline package; no leads; 7 terminals; body 1.1 × 2.1 × 0.5 mm	SOT1358-1

4. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3TB6	3T

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			–5.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4	[1]			
		contact discharge		–10	+10	kV
		air discharge		–15	+15	kV
T_{amb}	ambient temperature			–40	+85	°C
T_{stg}	storage temperature			–55	+125	°C

[1] All pins to ground.

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6. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_I = 1 mA		6	-	-	V
I_{LR}	reverse leakage current	per channel; V_I = 3 V		-	1	100	nA
C_{line}	line capacitance	f = 1 MHz; V_I = 0 V	[1]	-	0.27	0.35	pF
ΔC_{line}	line capacitance difference	f = 1 MHz; V_I = 0 V	[1]	-	0.03	0.05	pF
r_{dyn}	dynamic resistance	surge	[2]				
		positive transient		-	0.5	-	Ω
		negative transient		-	0.5	-	Ω
		TLP	[3]				
		positive transient		-	0.6	-	Ω
		negative transient		-	0.6	-	Ω
V_{CL}	clamping voltage	I_{PP} = 3.5 A	[2]				
		positive transient		-	4.8	-	V
		I_{PP} = −3.5 A	[2]				
		negative transient		-	−4.8	-	V

[1] This parameter is guaranteed by design.

[2] According to IEC 61000-4-5, pulse time t_p = 8/20 μs.

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.

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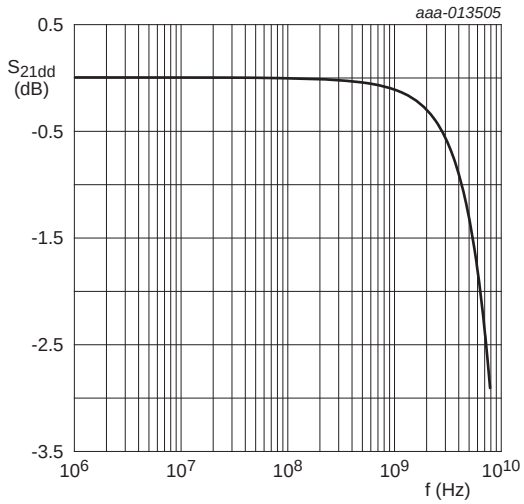
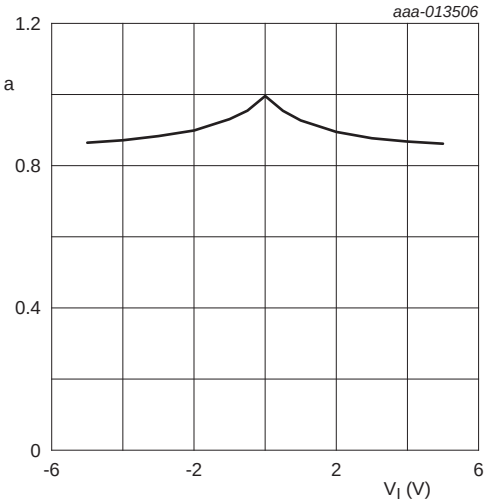


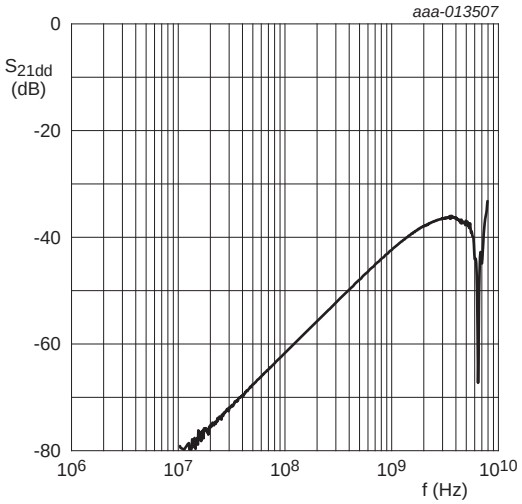
differential mode

Fig 1. Insertion loss; typical values



$$a = \frac{C_{line}}{C_{line(V_I = 0\ V)}}$$

Fig 2. Relative capacitance as a function of input voltage; typical values



normalized to 100 Ω

Fig 3. Crosstalk; typical values

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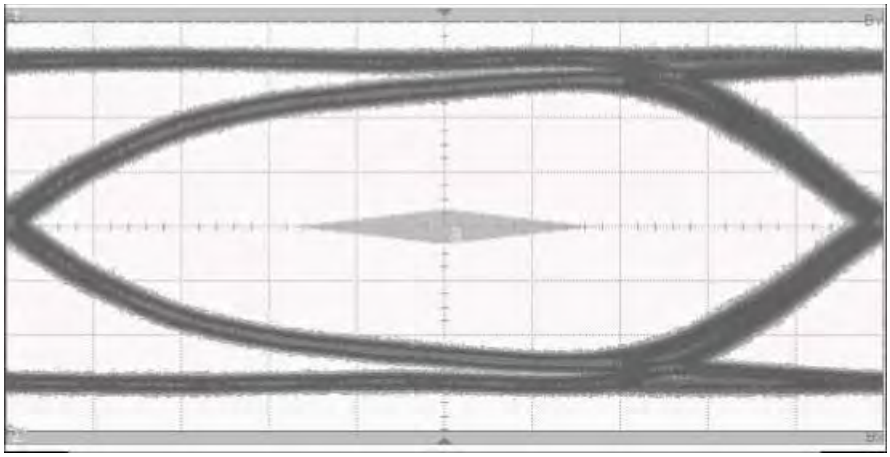
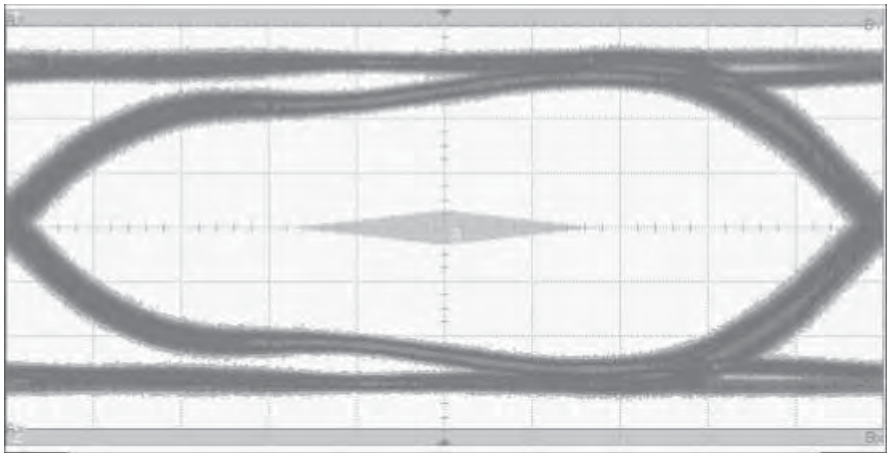


aaa-014154

Data rate: 5 Gbit/s
Vertical scale = 160 mV/div
Horizontal scale = 20 ps/div

Fig 4. USB 3.0 eye diagram Printed-Circuit Board (PCB) with PUSB3TB6



aaa-014155

Data rate: 5 Gbit/s
Vertical scale = 162.5 mV/div
Horizontal scale = 20 ps/div

Fig 5. USB 3.0 eye diagram PCB without PUSB3TB6 (reference)

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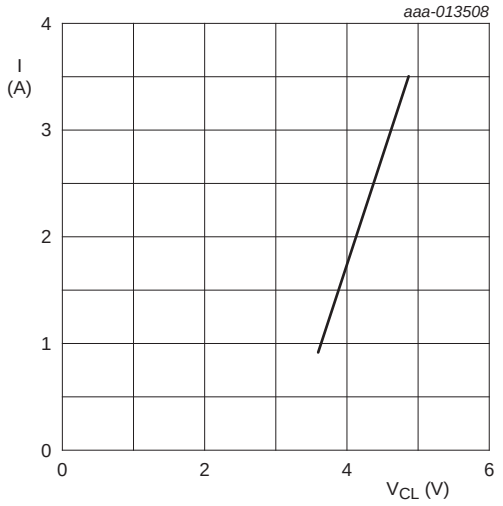
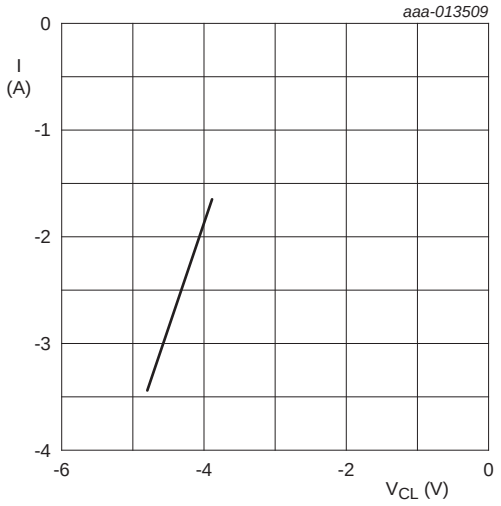


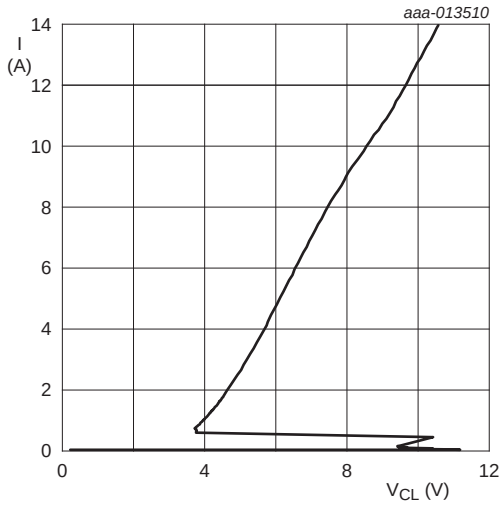
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 6. Dynamic resistance with positive clamping; typical values



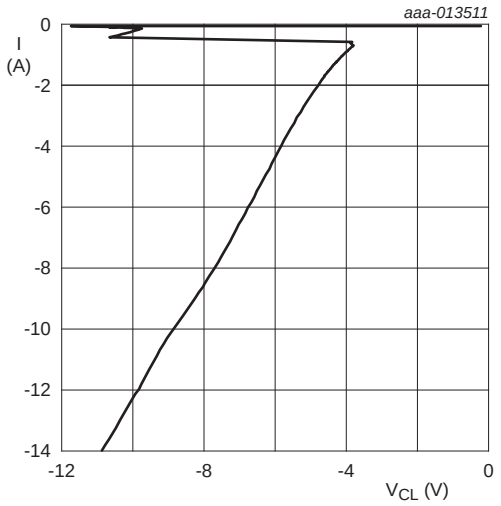
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 7. Dynamic resistance with negative clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 8. Dynamic resistance with positive clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 9. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

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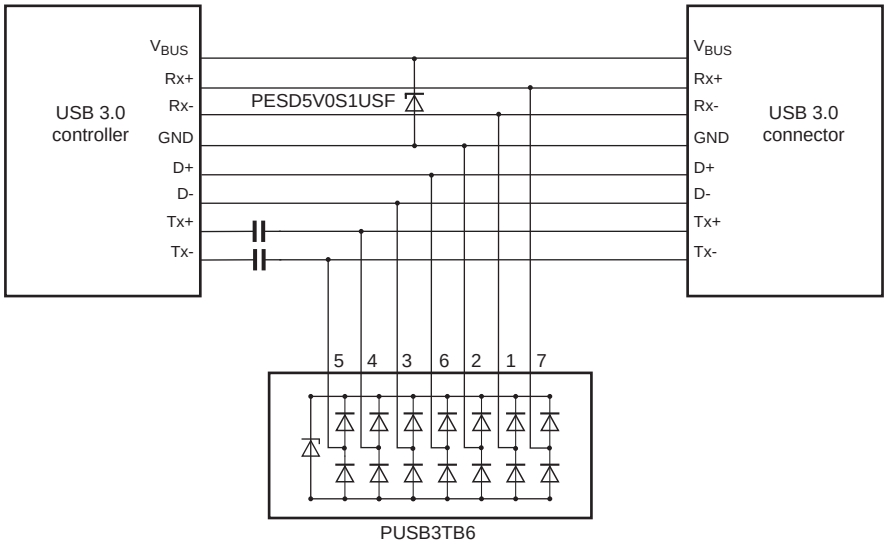
7. Application information

The device is designed to provide high level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources such as battery.

ESD protection schematic diagram for USB 3.0 or USB 2.0 interface is shown on Figure 10.



Any pin can be chosen for ground connection; one pin must be connected to ground.

Fig 10. Demo PCB of ESD protection for USB 3.0 or USB 2.0 interfaces using PUSB3TB6

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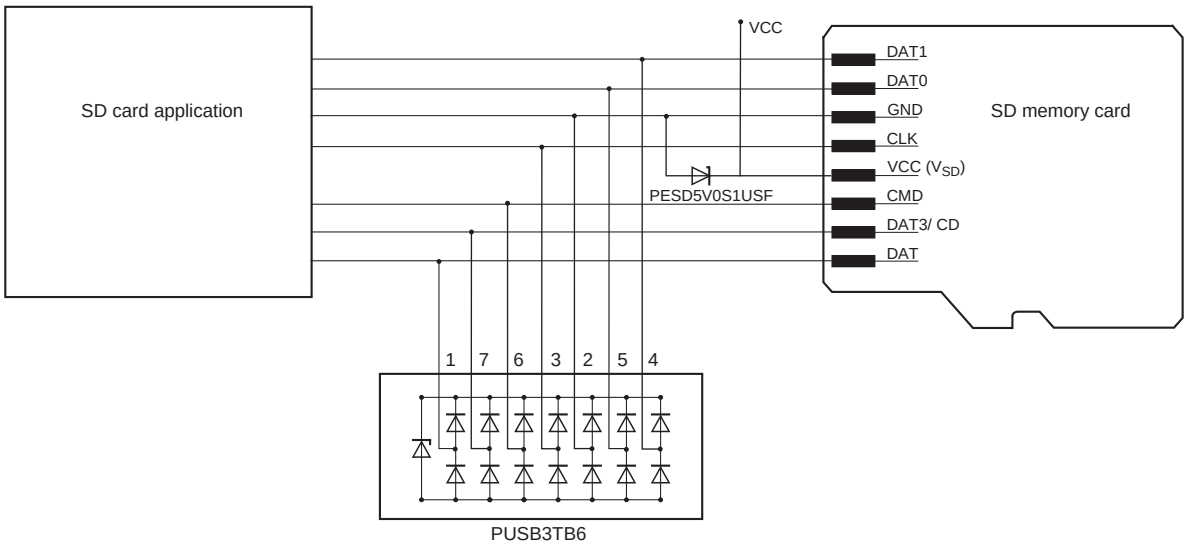
A basic application diagram for ESD protection of SD card interface is shown on Figure 11. GND can be connected to pin 2 for easy routing or to any other rail-to-rail structure.



Any pin can be chosen for ground connection; one pin must be connected to ground.

Fig 11. Application diagram of SD card ESD protection using PUSB3TB6

8. Package outline

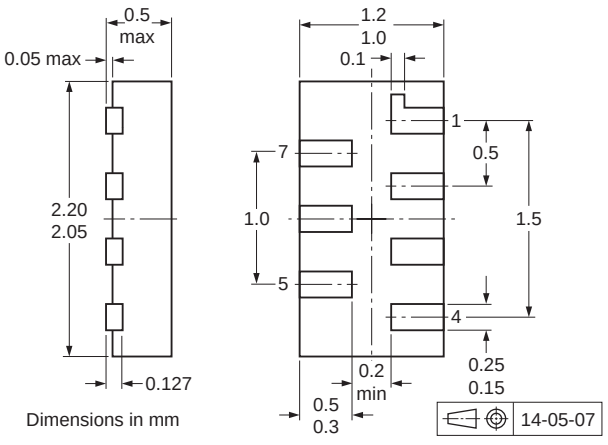


Fig 12. Package outline DFN2111-7 (SOT1358-1)

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9. Soldering

Footprint information for reflow soldering of DFN2111-7 (SOT1358-1) package **SOT1358-1**

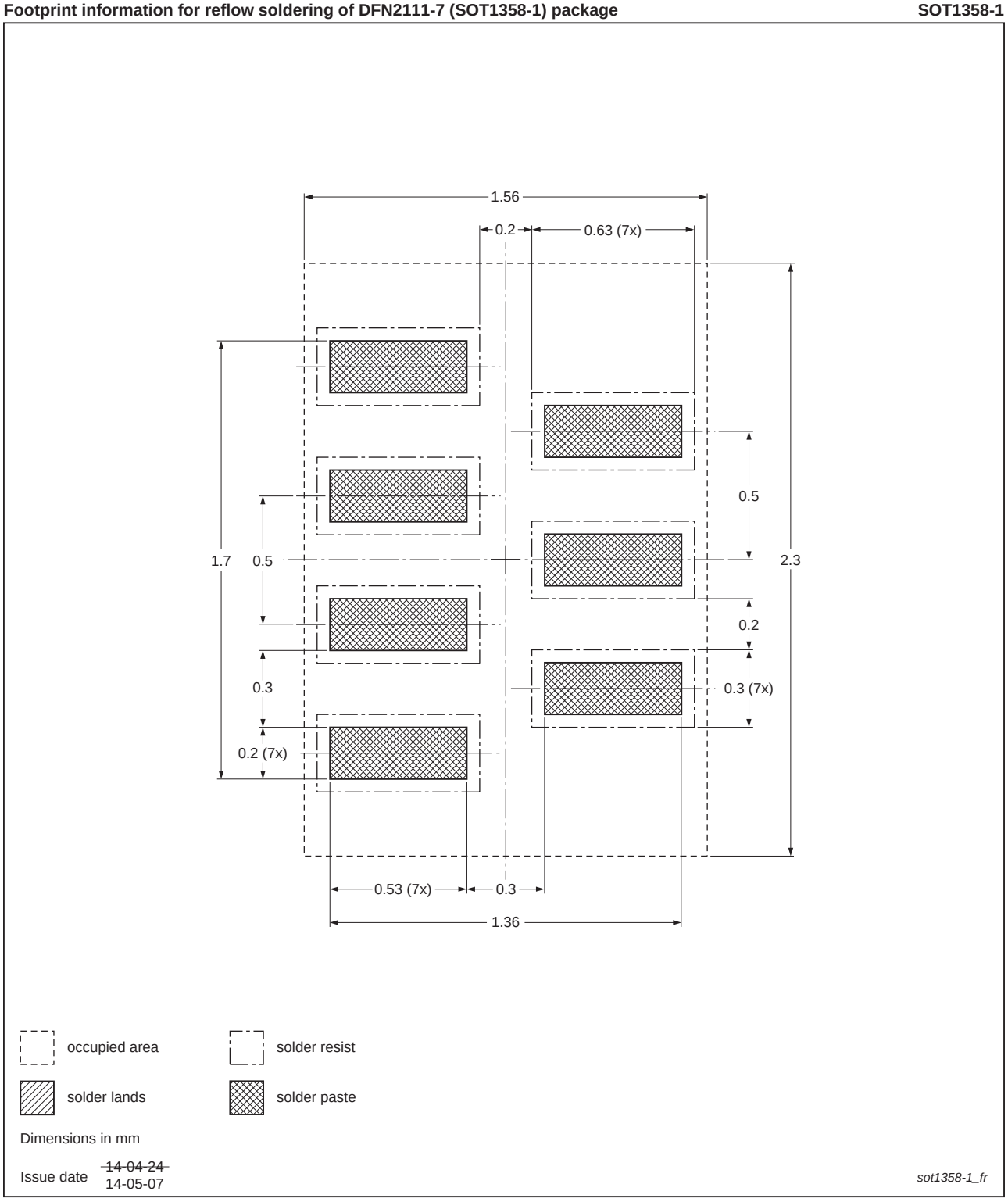

Fig 13. Reflow soldering footprint DFN2111-7 (SOT1358-1)

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10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3TB6 v.1	20140819	Product data sheet	-	-

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