JANUARY 21, 2009 V1.0

SC14480A5M, SC14480A2M6
1.8V Single Chip for DECT

General Description

The SC14480A5M, SC14480A2M6 are family members of digital CMOS ICs with fully integrated radio transceivers and baseband processors for DECT & DECT 6.0 CAT-iQ handsets and basestations.

The SC14480A5M has a FLASH version with CR16 trace unit for development of all family members.

For the family overview refer to SiTel Portal SC1448x_product_overview.xls

The radio transceiver, when combined with a power amplifier and a Tx/Rx switch, implements a complete DECT radio transceiver compiant with the ETSI CTR6 standard.

The audio path comprises a 16 bit CODEC, analog frontend, including a high efficiency 4 Ohm audio amplifier (Class-D) and user programmable Gen2DSP.

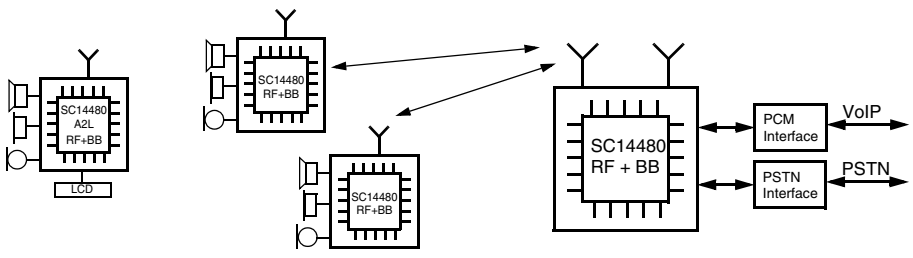
The CompactRISCTM CR16Cplus microprocessor with a one wire debug port running from ROM controls the protocol stack and the I/O peripherals, keyboard, UART, ACCESS bus, SPI, LED drivers, RF switches.

Features

- Complies with DECT ETS 300 175-2,3 & 8 and DECT 6.0.
- 10.368/20.736 MHz xtal digital controlled oscillator.
- Processing power
  - 41.472 MHz 16 bit CompactRISC™ CR16Cplus with a four channel DMA controller.
  - Eight/two debug channels for ROM patching.
  - Programmable Gen2DSP supporting various algorithms for telecom applications in ROM. Development version has 2k Micro Code RAM
  - Dedicated Instruction Processor (DiP) with a new 32 bits CRC and a support for a new 640 bits slot format with a minimum delay.
- Device Memories configuration
  - A2M6: 2.6Mbit ROM + 16k shared RAM,
  - A5M 5.0 Mbit ROM/FLASH +16k shared + 8k non shared RAM.
  - ROM/FLASH access maximum 20.736 MHz
  - Instruction/Data/Event Trace unit in FLASH version for fast program development.
- Power management
  - 1.8 Volt operating voltage with 1.8V I/O pads, P0 and P2 port groups are 3.45V tolerant.
  - Charge control for 2xNiMH batteries and Li-Ion
  - Voltage trippler for white LEDs and supply of external 2.5/3V devices
- Analog and Audio Interfaces
  - 8, 16, 32 kHz 16-bit linear audio CODEC.
  - Analog Front End to differential and single ended. microphones and 28 ohm loudspeaker.
  - High efficiency 0.5 W 2.5 V (4 ohm) switching amplifier.
  - 10bit ADC with 8/16kHz sample rate.
  - Integrated opamp for caller-id
- Digital interfaces
  - Three general purpose I/O ports
  - Keyboard interface with debounce counter
  - Serial Debug interface, Nexus Class-1 compliant.
  - UART Full duplex 9600-230.4 kbaud.
  - SPI™ interface 20.736 MHz (Master/Slave).
  - Dual ACCESS bus 100 kHz, 400 kHz, 1.152 MHz
  - PCM Interface master/slave (I2S compatible)
- Three general purpose timers and watch dog timer.
- Radio transceiver
  - Fully integrated 1.9GHz CMOS transceiver
  - <70 µs RF PLL lock time
  - Six digital output ports (including two for fast antenna diversity switching)
  - 2 dBm PA driver RF output (A +25 dBm PA is under investigation)
  - -96 dBm receiver sensitivity
- e-TQFP-80 package with exposed pad and KGD

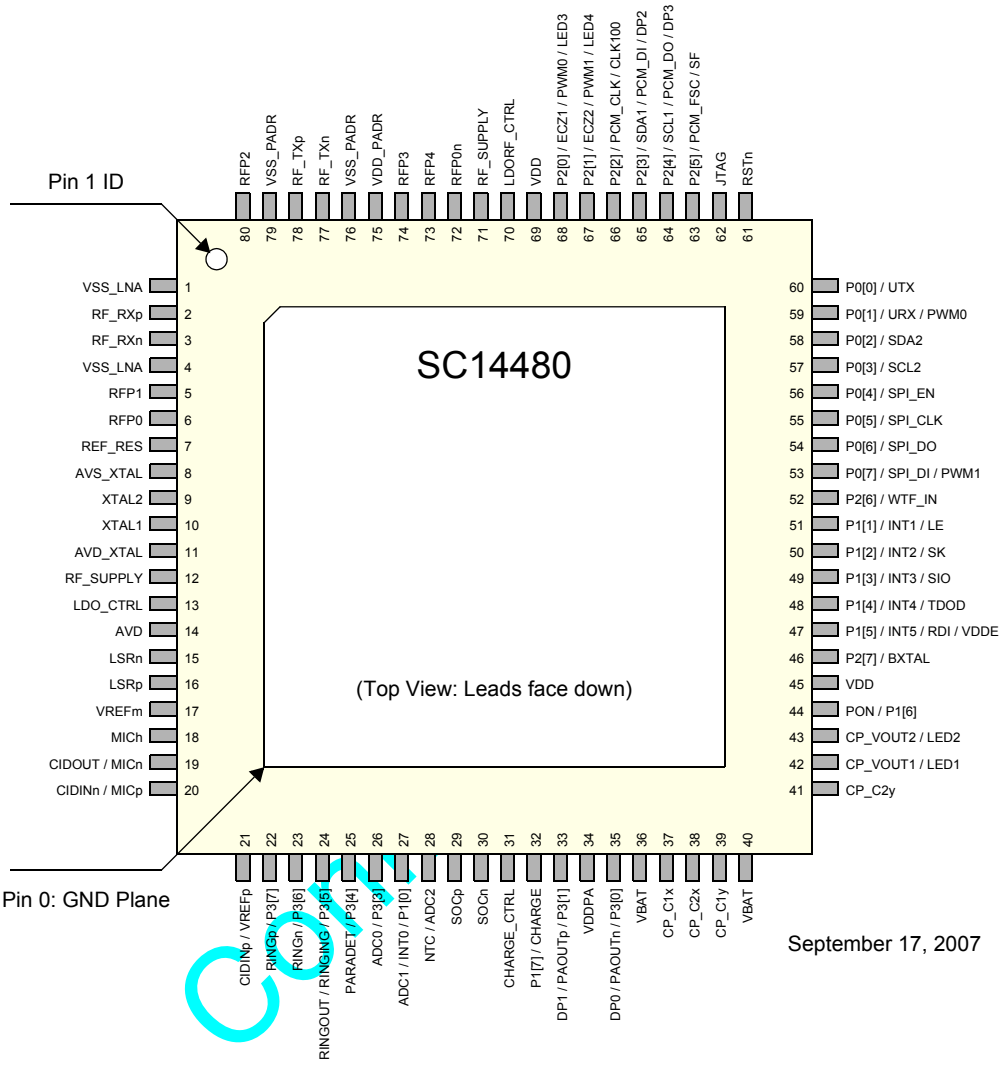
Note 1: CompactRISC™ is a trademark of National Semiconductor
SPI™ is trademark of Motorola.

System Diagram



1.8V Single Chip for DECT

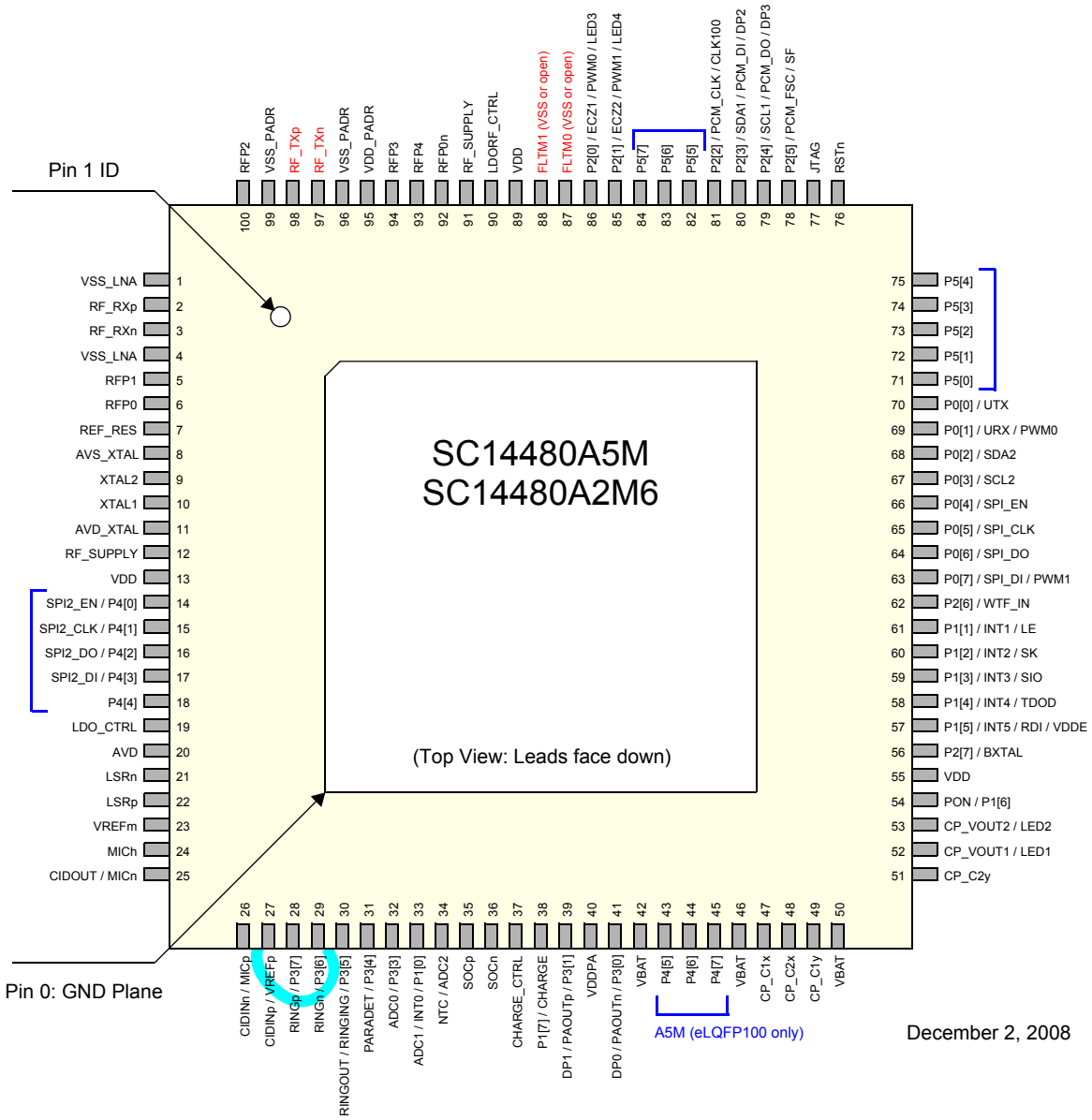
1.0 Connection diagram



Order numbers: (Note 1)
SC14480A5M80VE (5Mbit FLASH, 16kbyte shared RAM, 8kbyte non shared RAM, package eTQFP80)
SC14480A5MxxxxVE (5Mbit ROM, 16kbyte shared RAM, 8kbyte non shared RAM, package eTQFP80)

SC14480A2M6xxxxVE (2.6Mbit ROM, 16k shared RAM, package eTQFP80)

Note 1: Refer to Order_Number_and_Package_Marking.pdf on www.sitelsemi.com for a definition of the order numbers and package marking. Lead free devices have always an 'N' in the last three digits of the order number.



Order numbers:

SC14480A5M80VM (5Mbit FLASH, 16kbyte shared RAM, 8kbyte non shared RAM, package eLQFP100)
SC14480A5MxxxxVM (5Mbit ROM, 16kbyte shared RAM, 8kbyte non shared RAM, package eLQFP100)
SC14480A5MxxxxMDC (5Mbit ROM, 16kbyte shared RAM, 8k Non shared, KGD)
SC14480A2M6xxxxMDC (2.6Mbit ROM, 16kbyte shared RAM, KGD)
Refer to SiTel Portal for KGD datasheets

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 2)	DESCRIPTION
Ports				
P0[7] P0[6] P0[5] P0[4] P0[3] P0[2] P0[1] P0[0]	DIO-BP DIO-BP DIO-BP DIO-BP DIO-BP DIO-BP DIO-BP DIO-BP	8 8 8 8 8 8 8 8	I-PU I-PU I-PU I-PU I-PU I-PU I-PU (10k) I-PU	INPUT/OUTPUT with selectable pull up/down resistor. Pull-up enabled during and after reset. General purpose I/O port bit or alternate function nodes. DIO_BP have backdrive protection **(Note 3)**
P1[5] P1[4] P1[3] P1[2] P1[1] P1[0]	DIO DIO DIO DIO DIO A4S	8 1,2 1,2 2 2 2	O-1 I-PD I-PD I-PU I-PU I-PU	INPUT/OUTPUT with selectable pull up/down resistor. Pull-up enabled during and after reset. General purpose I/O port bit or alternate function nodes. P1[5] Used for supply of external EEPROM (See VDDE) P1[3], P1[4] 1mA mode used to bias external NPN transistor without external resistor.
P2[7] P2[6] P2[5] P2[4] P2[3] P2[2] P2[1] P2[0]	DIO-BP DIO DIO-BP DIO-BP DIO-BP DIO-BP DIO-BP DIO-BP	8 2 8 8 8 8 8 8	I-PU I-PU I-PU I-PU I-PU I-PU I I	INPUT/OUTPUT with selectable pull up/down resistor. Pull-up enabled during and after reset. General purpose I/O port bit or alternate function nodes. DIO_BP have backdrive protection **(Note 3)**
P3[7] P3[6] P3[5] P3[4] P3[3] P3[1] P3[0]	A2S A2S A2S A2S A4S DO DO 	4 4 4 8 8 500 500 	I I I I I O-0 (5k fixed pull down) O-0 (5k fixed pull down)	INPUT/OUTPUT with selectable pull up/down resistor. Pull-up/ down disabled during and after reset. General purpose I/O port bit or alternate function nodes. See also PAOUTp/PAOUTn description
Port 4, 5 (Only on KGD and 100 pins device, not tested unless commercially discussed)				
P5[7-0] P4[7-0]	DIO-BP DIO-BP	8 8	I-PU I-PU	INPUT/OUTPUT port with selectable pull up/down resistor. Pull-up enabled during and after reset. DIO_BP have backdrive protection **(Note 3)**
Power management				
PON / P1[6]	A3	-	I-PD (fixed 270k pulldown)	INPUT. Power on, Switchies on the device if Voltage > Vih_a3pad. May be directly connected to VBAT. If used as port pin, the maximum input switching speed of this pin is 100 kHz.
CHARGE / P1[7]	A3	-	I-PD (fixed 270k pulldown)	INPUT. Charger connected indication and supply voltage for power management. Switches on the device if voltage > Vih_a3pad. Must be connected to charger via resistor R>(Vcharger_max-3V)/10 mA (round to next largest value in range). An internal 10 ms hold circuit keeps device on if the charger voltage ripple momentarily drop below Vil_charge. This eliminates the use of expensive ripple filter. If used as port pin, the maximum input switching speed of this pin is 100 kHz.

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 2)	DESCRIPTION
CHARGE_CTRL	A1	1	O-0	ANALOG output. Charge control pin. Supplied by VBAT
Debug interface				
JTAG	DIOD-BP	8	I-PU	INPUT/OUTPUT. INPUT/OUTPUT. JTAG-SDI+ one wire interface with opendrain. An external 1k pull-up resistor must be present on the board for debugging.(see also Figure 83) Default hot insertion is enabled; if JTAG pin pulled low after reset, the JTAG-SDI is enabled and consumes power. DEBUG_REG[CR16_DBGM] either allows ROM patching or JTAG port. Refer to register description. Disabling the JTAG-SDI port is possible if this pin is high during reset or by writing to TEST__REG[_SDI] = '1'.
Interrupts				
INT8 INT7 INT6	DI DI / DI-BP DI / DI-BP		I-PU	INPUT. 3 general purpose interrupts with rising/falling edge or high/low levels. All inputs generate a KEYB_INT. INT8 is connected to P1[3] INT7 is connected to P1[2] or P2[7] INT6 is connected to P1[1] or P2[6]
INT5-INT0	DI		 O-1 I-PD I-PD I-PU I-PU I-PU	INPUT. 6 Keyboard input interrupts requests with or without debounce timer and programmable rising/falling edges. All inputs generate a KEYB_INT. INT5 is connected to P1[5] INT4 is connected to P1[4] INT3 is connected to P1[3] INT2 is connected to P1[2] INT1 is connected to P1[1] INT0 is connected to P1[0]
SPI Interface				
SPI_CLK	DO-BP	8	I-PU	INPUT/OUTPUT. Clock
SPI_DI	DI-BP		I-PU	INPUT. Data input
SPI_DO	DO-BP	8	I-PU	OUTPUT. Data output
SPI_EN	DI-BP		I-PU	INPUT. Clock enable
SPI2 Interface (Only on KGD and 100 pins device, not tested unless commercially discussed)				
SPI2_DI	DIO-BP	8 8	I-PU I-PU	INPUT/OUTPUT port with selectable pull up/down resistor. INPUT. SPI2 Data input
SPI2_DO	DIO-BP	8 8	I-PU I-PU	INPUT/OUTPUT port with selectable pull up/down resistor. OUTPUT. SPI2 Data output
SPI2_CLK	DIO-BP	8 8	I-PU I-PU	INPUT/OUTPUT port with selectable pull up/down resistor. INPUT/OUTPUT. SPI2 Clock
SPI2_EN	DIO-BP	8 8	I-PU I-PU	INPUT/OUTPUT port with selectable pull up/down resistor. INPUT. SPI2 Clock enable
ACCESS bus 1 Interface				
SDA1	DIO-BP/ DIOD-BP	8	I-PU	INPUT / OUTPUT. ACCESS bus 1 Data with programmable Push-pull or open drain
SCL1	DIO-BP/ DIOD-BP	8	I-PU	INPUT / OUTPUT. ACCESS bus 1 Clock with programmable Push-pull or open drain. In open drain mode, SCL is monitored to support bit stretching by a slave
ACCESS bus 2 Interface				
SDA2	DIO-BP/ DIOD-BP	8	I-PU	INPUT / OUTPUT. ACCESS bus 2 Data with programmable Push-pull or open drain

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 2)	DESCRIPTION
SCL2	DIO-BP/ DIOD-BP	8	I-PU	INPUT / OUTPUT. ACCESS bus 2 Clock with programmable Push-pull or open drain. In open drain mode, SCL is monitored to support bit stretching by a slave
UART Interface				
UTX	DO-BP	8	I-PU	OUTPUT. UART transmit data
URX	DI-BP	8	I-PU	INPUT. UART receive data
Radio transceiver				
RF_RXp	A9	-	I	RF Receiver input. Must be AC coupled
RF_RXn	A9	-	I	
VSS_LNA	A9	-	I	LNA Ground
RF_TXp	A10	-	O	RF PA driver (open drain) outputs. Must be connected to VDD_PADR by external matching circuit.
RX_TXn	A10	-	O	
VDD_PADR	A10	-	O	Internally regulated power supply for the PA driver matching circuit
VSS_PADR	A10	-	I	PA driver matching circuit Ground
REF_RES	A7	-	O	Connection for bias resistor to ground (56kΩ). For stability the maximum paracitic load on this pin may not exceed 10 pF.
RFP0	D2	8	Hi-Z	Digital outputs supplied with internal RF LDOs. (1.7V) If the RF LDOs are not enabled, the output of these port can not be used. Refer to Table 282 on page 225
RFP0n	D2	8	Hi-Z	
RFP1	D2	8	Hi-Z	
RFP2	D2	8	Hi-Z	
RFP3	D2	8	Hi-Z	
RFP4	D2	8	Hi-Z	
Internal Baseband RF interface (for monitoring/debugging purposes only)				**For more information, refer to chapter "Microwire"**
LE	DIO	2	I-PU	INPUT/OUTPUT. Microwire latch enable
SK	DIO	2	I-PU	INPUT/OUTPUT. Microwire clock
SIO	DIO	1/2	I-PD	INPUT/OUTPUT. Microwire data
TDOD	DIO	1/2	I-PD	INPUT/OUTPUT. Baseband Transmit Digital BMC Data.
RDI	DIO	8	O-1	INPUT/OUTPUT. Baseband Receive Data
CLASSD power amplifier				
PAOUTp PAOUTn	DOPD DOPD	500	O-0 (5k fixed pull down) O-0 (5k fixed pull down)	OUTPUT. CLASSD positive and negative output to 4 ohm loudspeaker. These pin can be configured as general purpose outputs, but this will result is an extra static DC current, so this not recommended in portable applications. (see DC characteristics and **(Note 5)**. PAOUTp and PAOUTn are forced to VSSPA if VDDPA > 3.3V ... 3.45V (trimmed BANDGAP_REG: AVD = 1.8V) VDDPA > 3.15V ... 3.6V (BANDGAP_REG = 0x8) **(Note 6)**
VDDPA	A1		-	Supply voltage CLASSD audio amplifier up to 3.45V
VSSPA		-	-	Ground for CLASSD power amplifier, connected to GND plane
Audio Codec				
LSRp or AGND	A1	-	O	OUTPUT. Positive loudspeaker output OUTPUT. Buffered analog ground if LSRP_MODE = 00.

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 2)	DESCRIPTION
LSRn or AGND	A1	-	O	OUTPUT. Negative loudspeaker output. OUTPUT. Buffered analog ground if LSRN_MODE = 00.
MICh	A2	-	I	INPUT. Headset microphone input with fixed input protection
MICp	A2	-	I	INPUT. Positive microphone input
MICn	A2	-	I	INPUT. Negative microphone input.
VREFp	A2	-	I	OUTPUT. Positive microphone reference. This pin is shared in with CIDINp. Make sure that CIDINp input protection is disabled if using VREFp. (CODEC_TONE_REG[CID_PR_DIS] is set to 1)
VREFm	A1	-	-	Negative microphone reference. This pin must also be connected to VSS Ground, but make sure that the microphone ground is directly routed to VREFm (VREFm is the star point).
Caller-id opamps + RINGING				
CIDINp	A2	-	I	INPUT. Caller-id opamp positive input with switchable input protection enabled from start-up. This pin is shared in with VREFp.
CIDINn	A2	-	I	INPUT. Caller-id opamp negative input with switchable input protection enabled from start-up. CODEC_TONE_REG[CID_PR_DIS]). Input is shared with MICp.
CIDOUT	A2	-	I	OUTPUT. Caller-id opamp output to ADC. This pin is shared with MICn
RINGING	A2S		I	INPUT. Ringer signal detection input to capture timers and ADC. Shared with RINGOUT and P3[5]
RINGn	A2S	-	I	ANALOG INPUT. Negative Ringing signal opamp input with switchable input protection (CODEC_TONE_REG[RNG_PR_DIS]).
RINGp	A2S	-	I	ANALOG INPUT. Positive Ringing signal opamp input with switchable input protection (CODEC_TONE_REG[RNG_PR_DIS].
RINGOUT	A2S	-	I	OUTPUT. Ringing opamp output to ADC. Shared with RINGING and P3[5].
PARADET	A2S	-	I	ANALOG INPUT. Parallel set detection input to ADC with switchable input protection (CODEC_TONE_REG[PARA_PR_DIS]).
State of Charge				
SOCp	A1		I	INPUT. Battery State of charge positive input
SOCn	A1		I	INPUT. Battery State of charge negative input
Charge pump/ trippler for White LED				
CP_C1x	A1	-	I	ANALOG INPUT/OUTPUT. Charge pump Capacitor 1 pin 1
CP_C1y	A1	-	I	ANALOG INPUT/OUTPUT. Charge pump Capacitor 1 pin 2
CP_C2x	A1	-	I	ANALOG INPUT/OUTPUT. Charge pump Capacitor 2 pin 1
CP_C2y	A1	-	I	ANALOG INPUT/OUTPUT. Charge pump Capacitor 2 pin 2
CP_VOUT1 / LED1	A1	-	I	ANALOG OUTPUT. Charge pump output 1 for White LED group1. (This pin can also be used as digital port output with open drain. Refer to AN-D-155 for more information).
CP_VOUT2 / LED2	A1	-	I	ANALOG OUTPUT. Charge pump output 2 for White LED group2 or VDDIO for external digital circuit. The booter enables this output as supply for an external FLASH to boot from. (This pin can also be used as digital port output with open drain. Refer to AN-D-155 for more information).

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 2)	DESCRIPTION
LED3	A1	2.5/5	I	ANALOG INPUT. Current sink for LED 3. Anode of the LED is connected to max 3.3V (VBAT). Cathode is connected to this pin.
LED4	A1	2.5/5	I	ANALOG INPUT. Current sink for LED group 2. Anode of the LED is connected to max 3.3V (VBAT). Cathode is connected to this pin.
Miscellaneous				
CLK100	DO-BP	8	I-PU	OUTPUT. DIP 100 Hz output set by <SLOTZERO> instruction
PWM[1-0]	DO-BP	8	I-PU	OUTPUT. Timer 0 PWM 1 or PWM0 outputs
ECZ1	DO	8	I-PU	OUTPUT. Gen2DSP output port set by DSP_ZCROSS1_OUT_REG[15].
ECZ2	DO	8	I-PU	OUTPUT. Gen2DSP output port set by DSP_ZCROSS2_OUT_REG[15]
DP[3-2] DP[1-0]	DO-BP DO	8 500	I-PU O-0	OUTPUT. DPx_OUT outputs (<R_LDx> DCF groups signals "ored" with the MicroWire DCF signal. See RF_MONITOR_REG)
SF	DO-BP	8	I-PU	OUTPUT. S-field Sync Found signal indicating the 00 or 11 preamble to unique word transition with 96 ns resolution. Used for debugging purposes
WTF_IN	DO-BP	8	I-PU	OUTPUT. Gen2DSP enable signal used to monitor DSP load
ADC0	A4S		I	INPUT. ADC0 input to ADC with programmable input protection enabled from reset (ADC0_PR_DIS) **(Note 4)**
ADC1	A4S		I-PU	INPUT. ADC1 input to ADC with programmable input protection enabled from reset (ADC1_PR_DIS) **(Note 4)**
ADC2 NTC	A4		I	INPUT. ADC2 input to ADC with programmable input protection (ADC2_PR_DIS) **(Note 4).** This ADC input is linear from 0-1.35 V INPUT. Li-Ion NTC protection input. Used to automatically switch off the charger circuit if this input goes outside specified voltage ranges. **In this mode ADC2_PR_DIS must be set to have the full input detection range upto 3.45V**. To disable the charge auto switch-off feature, either BAT_CTRL2_REG[NTC_DISABLE] must be set within 200ms after power up, or the ADC2/NTC pin must be tied to ground.
FLTM[1-0]	A4		-	INPUT. Analog FLASH test signals. In ROM and FLASH device connect to VSS or left unconnected.
Power and supply				
LDO_CTRL	A1	-	O-1	OUTPUT. Supply control signal connected to the base of an external PNP transistor used as VDD LDO.
RSTn	A5	8	I-PU (200k pull up)	INPUT/OUTPUT. Active low Reset input with Schmitt trigger input, open drain output and pull up resistor to internal VDD. Input may not exceed 2.0V
VBAT	A1	-	-	INPUT Main Battery supply voltage <5.5V
VDDE	DIO	8	O-1	1.8V Supply for an external EEPROM OUTPUT. Realized with P1[5] is output P1_OUTPUT_REG[5] =1 at start-up.
LDORF_CTRL	A1			INPUT. Supply control signal connected to base of an **optional** NPN transistor in case VBAT > 3.45V. This pin must be left unconnected if not used and BAT_CTRL_REG[LDORF_ON] must be set 0 to switch off the LDO.

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 2)	DESCRIPTION
RF_SUPPLY	A7			INPUT Battery supply 1.9V-3.45V. Connected to VBAT if <3.45V. Connected to collector of optional NPN transistor in case 3.45V<VBAT<5.5V. Pin 12 and Pin 71 must be connected together (preferably directly to the 2-cell battery). Only use LDO-RF for Li-ion headset applications when the load current is small (no RF-PA and no class-D connected to it) Pin 71 supplies LDOs for image reject mixer, RF port 2, 3, 4, 0n, LNA, VCO, Phase frequency detector, PA driver. Pin 12 supplies LDOs for IF filter, RX ADC, RF ports 0 and 1, frequency divider, MMC, LDO Xtal.
AVD	A1			Codec Analog Frontend End and ADC Supply voltage. Internally startpoint connected to VDD
VDD	A1			Digital Core and Digital PAD supply (VDDIO) voltage
VSS	A1	-	-	Digital ground and LDO_XTAL ground, all connected to GND plane
GND Plane	-	-	-	Common ground for all circuits, except VSS_LNA, AVS_XTAL, VREFm, VSS_PADR.
Xtal				
AVD_XTAL	A6		-	OUTPUT Supply voltage (1.7V) LDO for XTAL. Must be decoupled with 1uF ceramic capacitor.
AVS_XTAL	A6	-	-	Analog ground AVD_XTAL
XTAL1 XTAL2	A6	-	I	INPUT 10.368/20.736 MHz crystal connection. See chapter XTAL Oscillator.
BXTAL	DO-BP	8	I-PU	OUTPUT. Digital buffered Xtal oscillator, can be switched on/off using DIP <RF_EN>/<RF_DIS> instructions. This pin is not optimized as reference clock for external RF devices
N.C>				Not connected, VDD or VSS

Note 2: All digital outputs can sink/source 2 mA unless otherwise specified. All digital inputs have Schmitt trigger inputs. After reset all I/Os are set to input and all pull-up or pull-down resistors are enabled unless otherwise specified.
PU = Pull-up resistor enabled, PD = Pull-down resistor enabled, I = input,
O=output, Hi-Z= high impedance, 1= logic HIGH level, 0= logic LOW level
Refer also to Px_DIR_REGs for INPUT/OUTPUT and Pull-up/Pull-down configurations

Note 3: Backdrive protected pins allow always interfacing with devices using VDDIO upto 3.45V.
If PAD_CTRL_REG[xxx_OD] bit is set then 1) the internal Pull-up resistors are always disabled to prevent currents from 1.8V< Vin <3.45 to VDD.
2) If port is set to output, the output is always configured as opendrain to allow the output level to reach VDDIO >1.8V. The external pull-up resistor value determines the rise time of the signal.

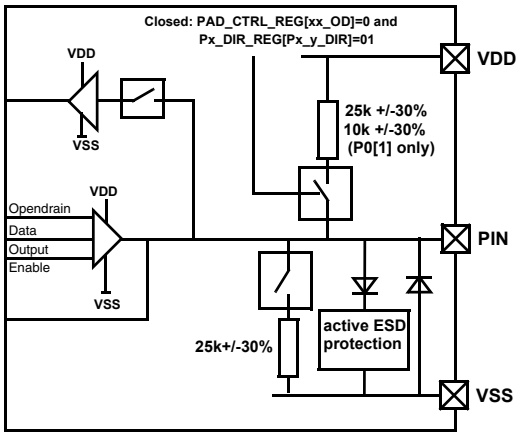
Note 4: For basestation applications with high line input voltages, an input protecton on all ADC inputs can be enabled with AD_CTRL_REG[ADCx_PR_DIS] ='0'. To limit the input current as specified in chapter "specifications", an external resistor must placed in series with the ADC inputs. With the input protection enabled, the ADC is linear from 0 to 0.9V. With ADCx_PR_DIS='1' the ADC0 and ADC1 are linear from 0-1.8V, but ADC2 is linear from 0-1.35V due to a voltage limiter which protects the ADC input for the NTC input above 1.8V.

Note 5: In digital mode extra static VDDPA current will flow (See Supply currents (Indicative value) (table 275, page 221)). So the digital mode is not recommended in portable applications.

Note 6: The reason for this output overvoltage protection is that a speaker is an inductor (which can store energy). In case the battery is removed from the handset while handsfree speaker is active, the battery voltage could become too high when the inductor releases its energy to the battery (which is not present anymore as a buffer). To prevent this electrical overstress situation, the overvoltage protection is added

1.1 PIN TYPE DEFINITIONS

Table 2: PIn type definitions



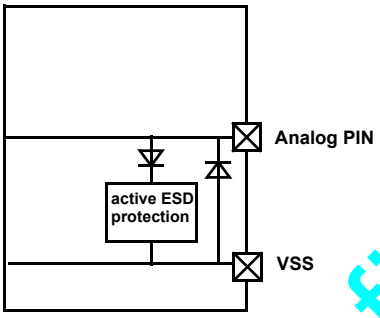
Digital / analog PADs

Digital/analog PAD IO Configurations:

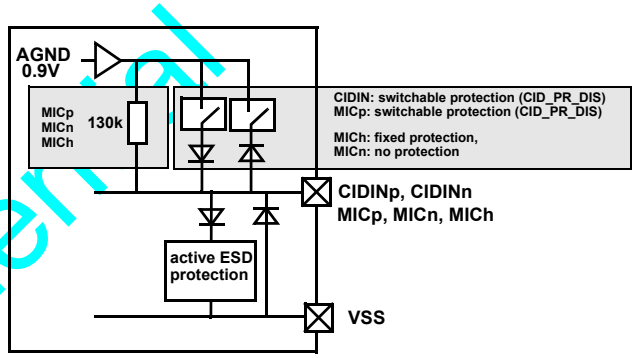
DO:	Digital Output
DI:	Digital Input
DIO:	Digital Input/Output
DIO-BP:	Digital Input/Output with backdrive protection
DIOD:	Digital Input/Output opendrain
AI:	Analog input
AO:	Analog Output
AIO:	Analog Input/Output

Pullup/pulldown extensions:

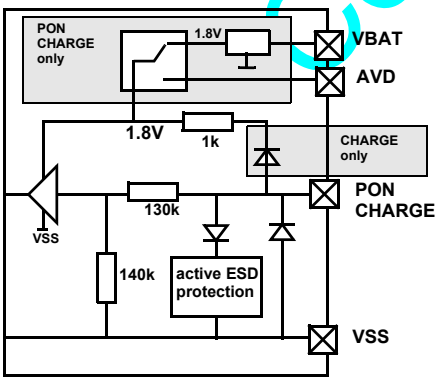
PU:	Fixed pull-up resistor
PD:	Fixed pull-down resistor
SPU:	Switchable pull-up resistor
SPD:	Switchable pull-down resistor



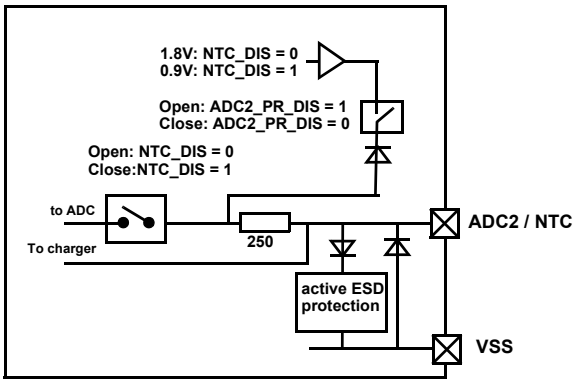
PAD A1



PAD A2

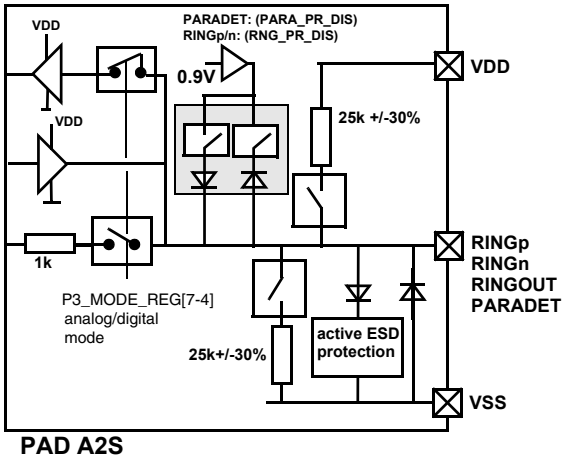


PAD A3

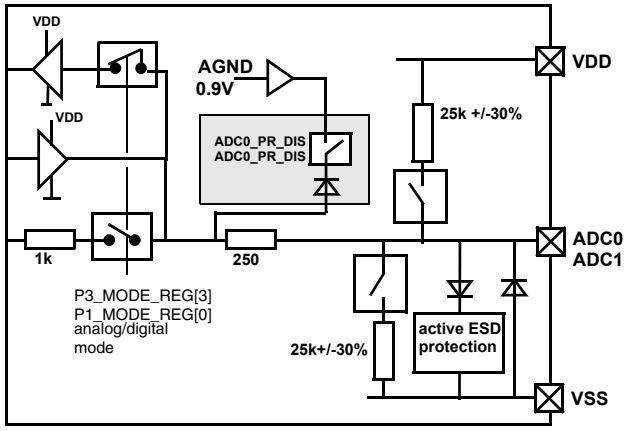


PAD A4

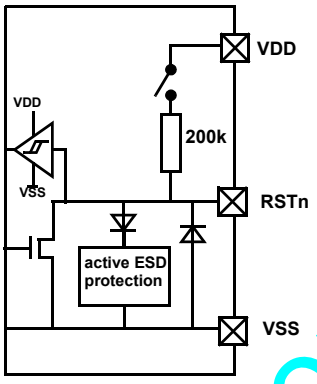
Table 2: PIn type definitions



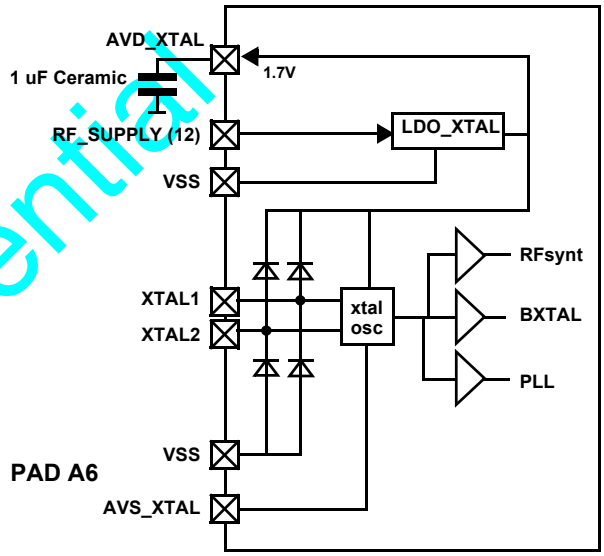
PAD A2S



PAD A4S

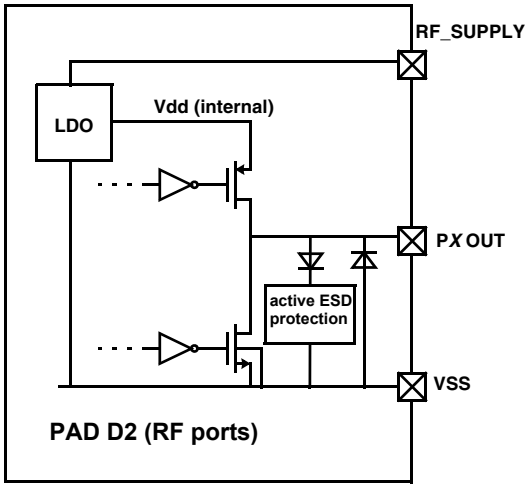


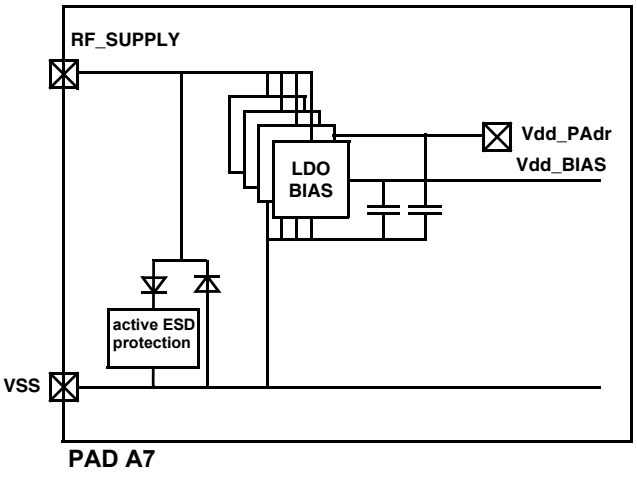
PAD A5

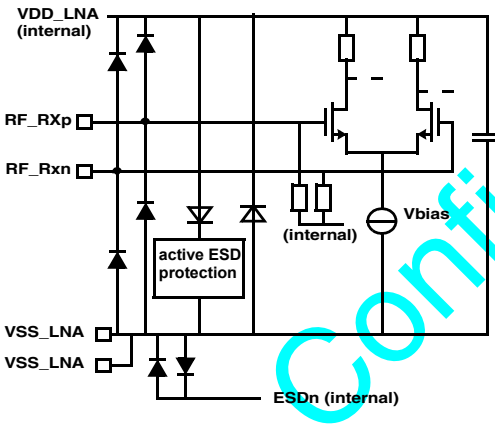


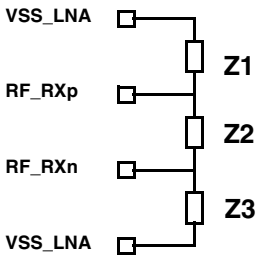
PAD A6

Table 2: PIn type definitions

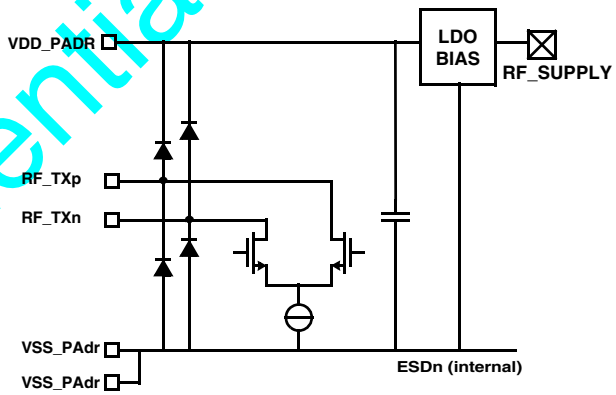


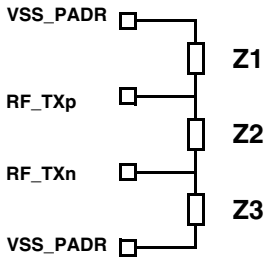






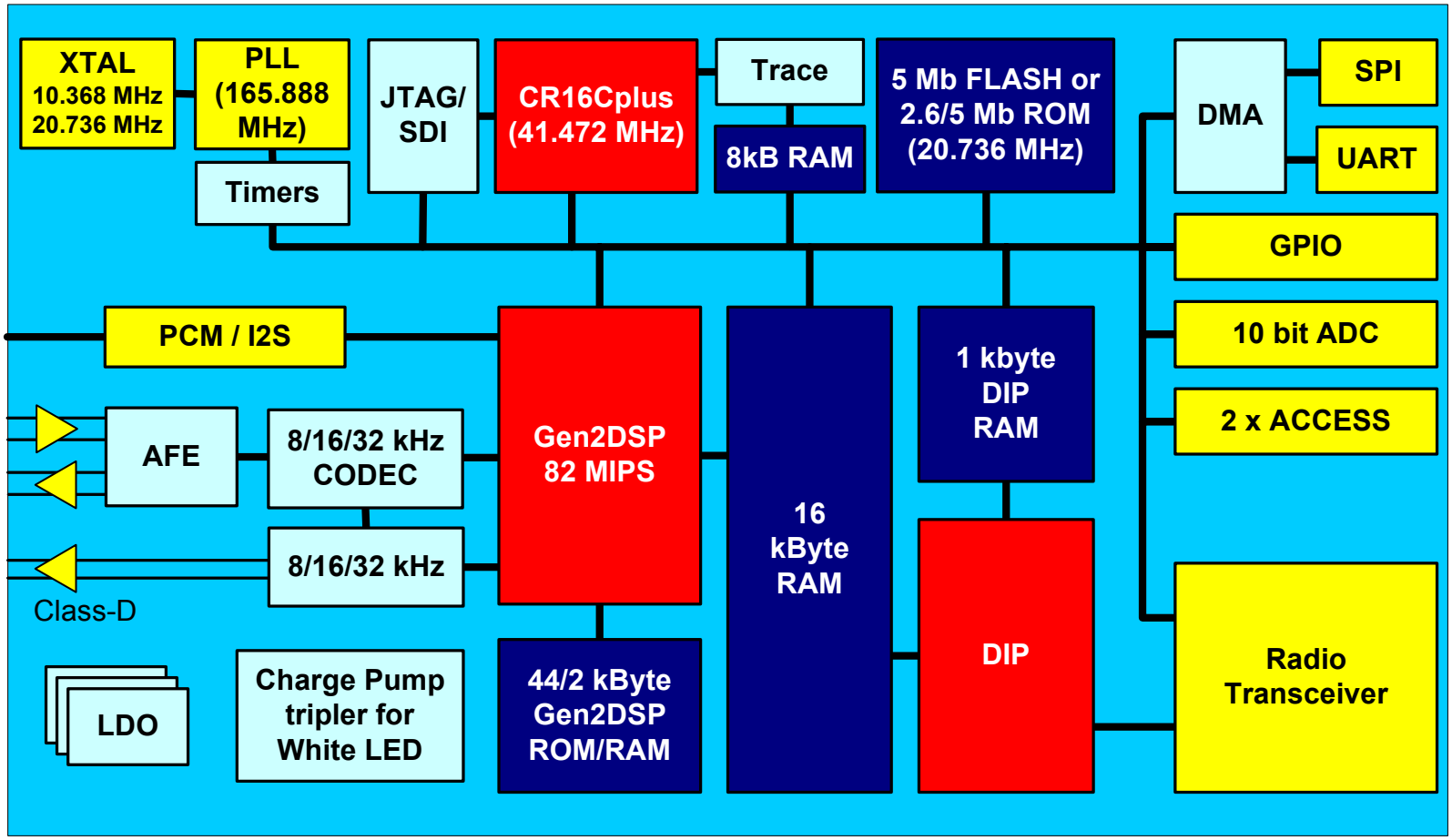
PAD A9





PAD A10

2.0 Functional overview



November 2, 2007

Figure 1 SC14480x5M, x2M6 Block diagram (Refer to family overview for memory size details)

3.0 System Clock generation

3.1 CRYSTAL OSCILLATOR

The Digital Controlled Xtal Oscillator (DXCO) is a Colpitts oscillator designed for low power consumption and high stability. The crystal oscillator frequency can be 10.368 MHz or 20.736 MHz.

Figure 2 shows the xtal connection diagram. **Note that all unnecessary load at the XTAL pins must be avoided. This means that the BXTAL pin must be used for frequency measurement/adjustment.**

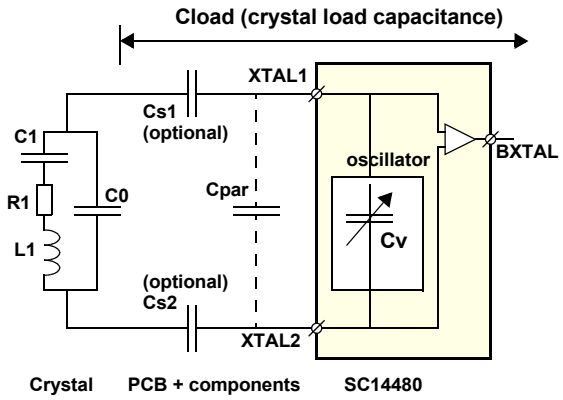


Figure 2 Xtal Equivalent circuit

For best start-up behavior and stable oscillation, it is important to keep Cpar and Co as small as possible. Capacitors Cs1 and Cs2 can be added in series with the crystal terminals to centre the trim-range (one capacitor alone can centre the trim-range, but two is better for symmetry). The capacitance seen by the crystal is given by the following equation:

$$C_{load} = \frac{1}{\frac{1}{C_{s1}} + \frac{1}{C_{s2}} + \frac{1}{C_{par} + C_v}} \quad (1)$$

Table 3: Typical Xtal specification

Parameter	Description	Value
C_L	Load capacitance	**10 pF / 12pF**
C0	Shunt capacitance	1-2 pF
Cpar	Parasitic PCB capacitance between XTAL1 and XTAL2	< few pF
Cs1,2	Optional series capacitor to centre the trim-range	56pF ... 220pF

Table 4: Typical component values

Cpar	XTAL, C_L	Cs1	Cs2
1pF	10pF	short	short
2pF	10pF	220pF	220pF
	10pF	100pF	short
3pF	10pF	100pF	100pF
	12pF	short	short
	10pF	56pF	short
5pF	Parasitic capacitance is to high to guarantee reliable start-up.		

3.2 PCB CONSIDERATIONS

It is very important to minimize the parasitic capacitance between XTAL1 and XTAL2. This parasitic capacitance is caused by the following components:

- Solder pads of the SC14480.
  Differential capacitance between XTAL1 and XTAL2 pins of about 0.15pF
- Wires from crystal to SC14480.
  The capacitance of wires separated by more than 3 times the width is dominated by the capacitance to the layer below. A typical value for this capacitance to the layer below is in the order of 0.11pF/mm (assuming trace width = 0.2mm, Er = 4.5, distance to layer below = 0.138mm). The differential capacitance is composed of the two capacitors to the layer below in series. So the differential capacitance between two wires is half the capacitance to the layer below of a single wire. **Example: the differential capacitance of 10mm long wires will be in the order of 0.55pF. Therefore place the crystal close to the device**.
- Footprint of the crystal.
  For a surface mount crystal, the solder pads can become quite big. When the layer below is used as ground plane or for wires, this can easily result in a differential capacitance of more than 1pF. **Avoid using the area below the footprint of the crystal**.

3.3 FREQUENCY CONTROL

Register CLK_FREQ_TRIM_REG (0xFF400A) controls the trimming of the crystal oscillator. The frequency is trimmed by two on-chip variable capacitor banks. Both capacitor banks are controlled through the same register.

Each of the two variable capacitor banks vary from minimum to max in 2048 equal steps. With CLK_FREQ_TRIM_REG = 00 minimum capacitance and thus maximum frequency is selected. With CLK_FREQ_TRIM_REG = 0x7FF maximum capacitance and thus minimum frequency is selected.

The eight least significant bits of CLK_FREQ_TRIM_REG directly control five binary

weighted capacitors, as depicted in Figure 3. The three most significant bits are decoded according Table 5. Each of the seven outputs of the decoder controls a capacitor (capacitor value is 256 times the value of the smallest capacitor). At least one of these capacitors stays always connected. This gives a guaranteed minimum load for xtal to oscillate. The effect is that CLK_FREQ_TRIM_REG value 0x0.XX has the same varicap value as 0x1.XX (see Figure 4)

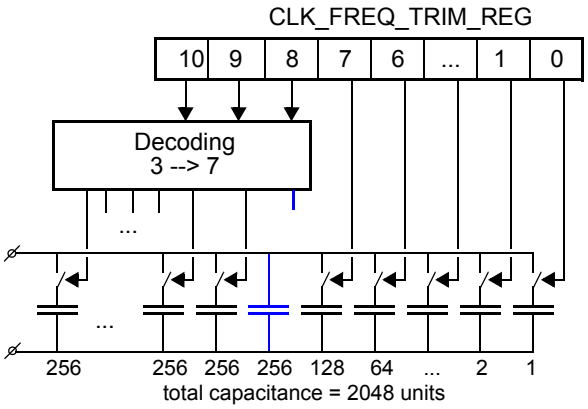


Figure 3 Frequency trimming

Table 5: CLK_FREQ_TRIM_REG (0xFF400A) Decoding 3--> 7

input[2:0]			output[6:0]						
2	1	0	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

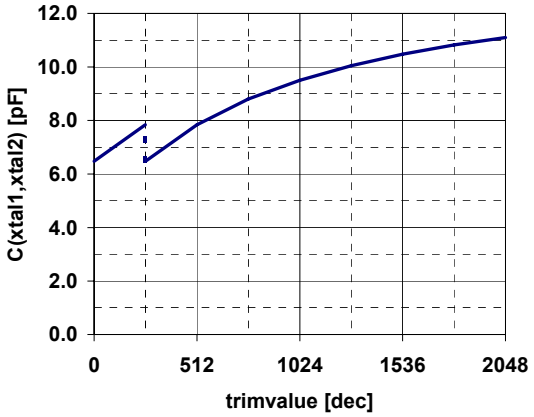


Figure 4 Typical varicap curve

Trimming might cause phase jumps. In order to reduce these phase jumps change only one single switch at a time (this is especially true for the seven largest capacitors). Use bit 10...8 for course adjustment and always increment or decrement this value by 1. Wait approximately 10 msec to allow the adjustment to settle.

Bits 7...0 are used for fine adjustment.

As an example, the recommended way to change the frequency trim register from 0x7FF to 0x100 is first to decrement the value of the three most significant bits by 1 at a time, and then change the least significant bits until the desired frequency is reached:
0x7FF --> 0x6FF -->0x5FF --> 0x4FF --> 0x3FF --> 0x2FF --> 0x1FF --> 0x100.

Adjusting the frequency will not affect the PLL behaviour. The small phase shifts will be followed by the PLL.

The xtal oscillator is supplied from an internal LDO_XTAL with output AVD_XTAL and can not be switched off in the SC14480.

Refer to *AN-D-161 "SC14480 Quartz Oscillator"* for more details.

3.4 XTAL DIVIDER SELECTION

The primary XTAL divider must be changed in CLK_XTAL_CTRL_REG[XTAL_DIV] from '1' (divide by two) in case of 20.736 MHz xtal or kept to '0' to divide by one with a 10.368 MHz XTAL.

3.5 SYSTEM CLOCK GENERATION

The next page shows the SC14480A5M, SC14480A2M6 clock divider overview. The device is clocked from pin XTAL1/XTAL2 with a Xtal frequency of 10.368 or 20.736 MHz.

In case of using a 20.736 MHz XTAL, the application shall set **CLK_XTAL_CTRL_REG[XTAL_DIV]=1** and **RF_PLL_CTRL2_REG[MODE20M]=1** to divide by two. (See "Xtal divider Selection" on page 17). Except for RF blocks PLLDIG, the rest of the clocks are kept to 10.368 MHz base frequency.

For evaluation purposes with an external RF device (e.g LMX4180) the buffered Xtal and use of external TAM/Codec (e.g SC14439), **BXTAL** is available on pin P2[7]. The BXTAL output can be enabled/disabled with DIP command <RFEN>/<RFDIS> or CR16Cplus controlled using bits BXTAL_EN[1-0].

BXTAL is not optimised for use as reference clock for external RF transceivers.

P1, a global 1/16 clock prescaler, used for extreme power saving but requires advanced DIP programming). Lowering the clock also reduces the charge pump performance and requires timers to be compensated. P1 can be enabled by setting DIP_CTRL_REG[PRESCALER] to 1 and CLK_AUX_REG[8] = XDIV to 1 and execution of a <U_PSC> command. Setting the PRESCALER bit back to 0 or generating an DIP interrupt <U_INTx>, <U_VINT> or <U_VNMI> switches P1 back to divide by 1. Refer to *AN-D-152 "SC14480 low power considerations"*

DIV1_CLK provides the PLL or XTAL clock for the RAM interface. In PLL mode DIV1_CLK is 165.888 MHz (max) and allows zero wait state shared RAM access for Gen2DSP and CR16Cplus. (Refer for other PLL values)

P2, DIV2_CLK divides the PLL clock by two and provides the main 82.944 MHz clock for Gen2DSP and 41.472 MHz CR16Cplus (HCLK_DIV=2 required in this case).
With DIV2_CLK_SEL=1, DIV2_CLK is equal to the PLL frequency. If the PLL frequency is reduced, a lower power consumption can be achieved (Refer Table 6 on page 21 for more information).
In XTAL mode DIV2_CLK is equal to the XTAL frequency.

P4, DIVN_CLK divides the PLL clock by N and provides the 10.368 MHz (PLL/16) reference clock for the DIP, Codec and Peripheral. When switching between XTAL and PLL mode this clock stays 10.368 MHz, is spike free and stretches this clock for only 0.5 PLL cycle. This would not affect a pending RF link.

P3, a 1/16 clock prescaler for the CR16Cplus, used in paging mode. To enable P3:

- DIP_CTRL_REG[PRESCALER] is set to 1 and DIP command <U_PSC> is executed.
- or HCLK_PRE =1 (No DIP required with this bit)

The prescaler is disabled:

- Upon a DIP interrupt <U_INTx>, <U_VINT> or <U_VNMI> when the prescaler is enabled or if the PRESCALER bit is set to 0.
- and HCLK_PRE =0

If the <U_PSC> is executed and no DIP interrupt was executed, switching PRESCALER to 0 and 1 will result in switching between 1 and 1/16.

HCLK_DIV, CR16Cplus/DMA/SDI clock divider. Values: 1,2,3,4,5,6,7,8. Maximum HCLK CR16Cplus frequency is 41.472 MHz.

PCLK_DIV, divider for APB bridge to peripherals. Refer to chapter paragraph 26.0. Maximum APB frequency is 41.472 MHz.

CLK_DSP_DIV for reducing Gen2DSP clock frequency. Although the Gen2DSP switches off his clock if finished, the divider may balance Gen2DSP on/off currents for reduced EMC. See also "Power saving" on page 57.

OWI_DIV is used to clock the JTAG_SDI one wire interface.

CLK_CODEC_DIV_REG[CODEC_DIV] divides to 1.152, 2.305 and 4.608MHz frequencies for narrow/wide band audio, while CLK_CODEC_REG multiplexes these outputs to Codec AD and DA and CLASSD blocks. (See Table 6 on page 21)

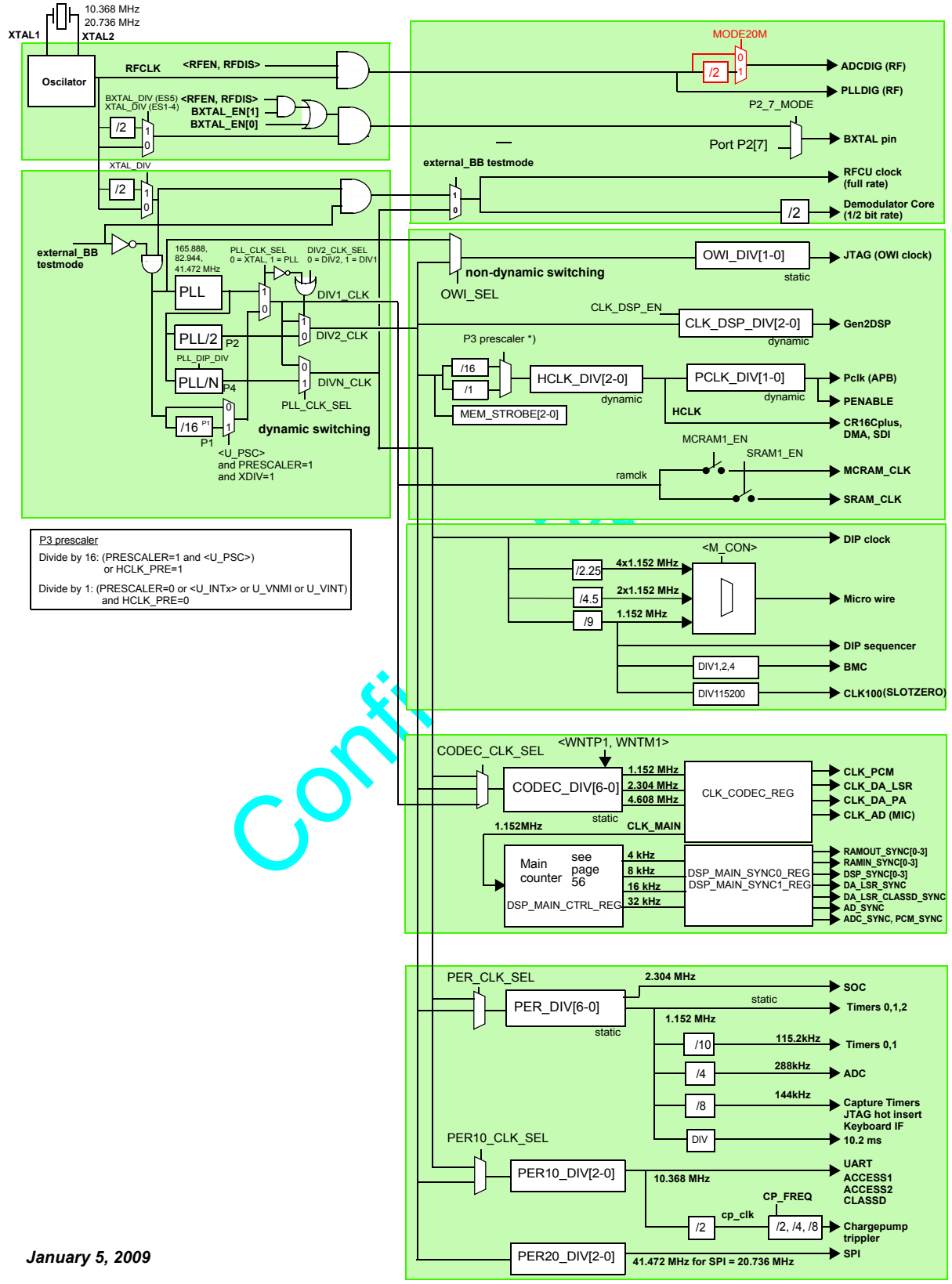
The **DSP_MAIN_CTRL_REG** divides the 1.152MHz main clock to 4kHz, 8kHz, 16kHz and 32kHz sample rates for narrow wide band audio. DSP_MAIN_SYNC0_REG and DSP_MAIN_SYNC1_REG multiplex these sample clocks to DIP, DSP interrupts, CODEC ADC and PCM interface.

PER_DIV divides DIVN_CLK to the basic 1.152 MHz and 2.304 MHz for low speed peripherals.

PER10_DIV divides to 10.368MHz peripherals.

PER20_DIV divides to 20.768 MHz SPI interface

Refer to Table 6 on page 21 for examples on how to set the various dividers.



January 5, 2009

Figure 5 SC14480A5M, A2M6 Clock divider overview

3.6 PHASE LOCKED LOOP (PLL)

The SC14480A5M, SC14480A2M6 contains a Phase Locked Loops (PLL) that is depicted in Figure 6: The PLL generates a clock with a frequency x16, x8 or x4 higher than the Xtal frequency, i.e., 165,888 or 82.944 or or 82.944/2 MHz.

The PLL is not required during a normal voice connection for a basic DECT cordless telephone. However, the PLL can be used if a higher cycle budget on the CR16Cplus or Gen2DSP is required, e.g., for hands-free applications.

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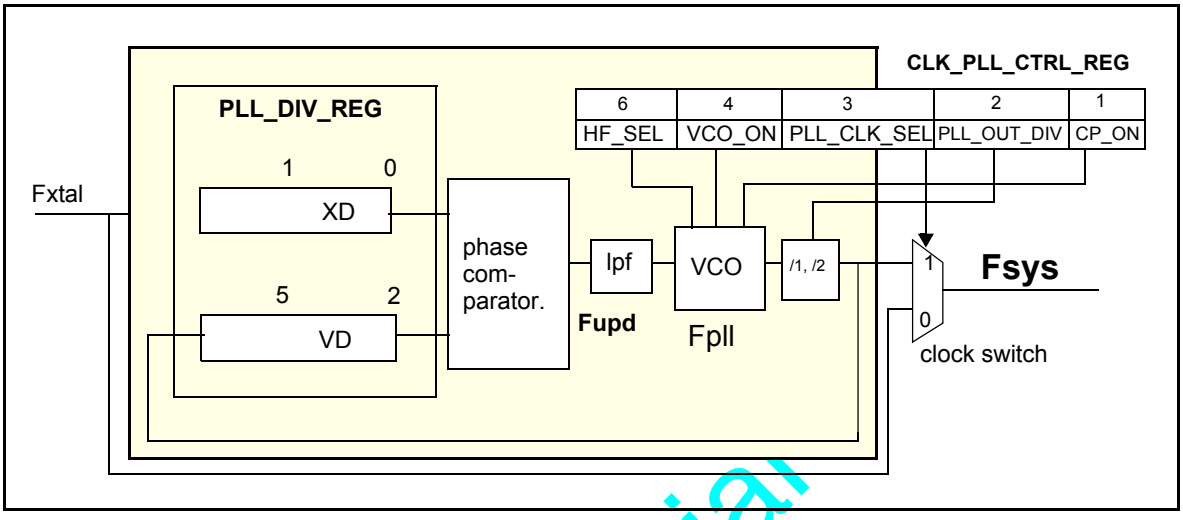


Figure 6 PLL block diagram

3.7 PLL CLOCK SWITCHING

At startup the PLL is bypassed (PLL_CLK_SEL=0) and the xtal frequency clocks the whole IC. The dividers CLK_CODEC_DIV_REG[CODEC_CLK_DIV], PER_DIV_REG[PER_DIV] must be set according Table 6 on page 21 to get the fundamental 1.152 MHz for Codec and peripherals.

If the PLL is switched as system clock Fsys with PLL_CLK_SEL=1, the output frequency of CLKN_DIV is kept constant to the 10.368 MHz DIP frequency FDIP, the 1.152 MHz for peripherals and 10.368 MHz for the UART 230kbaud and SPI.

This seamless dynamic clock switching can be done while a MAC link is active. Switching from xtal to the PLL clock stretches the DECT bitclock with 1 PLL clock cycle. Switching from PLL to xtal clock shortens the DECT bitclock with 1 PLL bitclock.

3.8 PLL CLOCK SWITCHING PROCEDURE

The sequence to enable and disable the PLL is:

- The PLL starts up in the bypass mode with CLK_PLL_CTRL_REG[3] = PLL_CLK_SEL is 0
- For **10.368 MHz XTAL frequency (and 20.736/2)**, Set PLL Xtal divider XD and VCO divider VD:
  CLK_PLL_DIV_REG = 0x1C for 165.888 MHz
  ~~CLK_PLL_DIV_REG = 0x8 for 124.416 MHz~~
  CLK_PLL_DIV_REG = 0x4 (recommended) or 0x1D for 82.944 MHz
  ~~CLK_PLL_DIV_REG = 5 for 41.472 MHz~~
  CLK_PLL1_DIV_REG = 0x4 for 82.944 MHz and set PLL_OUT_DIV for 41.472 MHz output.
- VCO and charge pump can be switched on with CLK_PLL_CTRL_REG[4] = VCO_ON set to 1 and CLK_PLL_CTRL_REG[1] = CP_ON set to 1. CLK_PLL_CTRL_REG[2] = PLL_DIV_OUT must be set to 1 to get 41.472 MHz with VCO 82.944 Mhz
- The firmware must wait at least 500 us before PLL_CLK_SEL may be set to 1. This time is needed for the PLL to settle to the Fpll frequency.
- CLK_PLL_CTRL_REG[3] = PLL_CLK_SEL is 1 to use the PLL clock as system clock

Switching back to xtal mode can be done at any time by setting PLL_CLK_SEL to 0. The CR16 must wait at least 10 PLL cycles (E.g 5xNOP if CLK_DIV=1) if DIP is off or 2 DIP Bit clock cycles (c.q 1.75 us in case of DECT) if PLL is on before the VCO and Charge Pump may be switched off.

Change clock frequency during a link is only possible via XTAL mode (PLLCLK_SEL=0), then the new PLL frequency must be set according to the clock switching procedure described above.

Table 6: Recommended Clock selections for 8kHz and 16 kHz voice applications for 10.368 MHz XTAL, 10.368 MHz DIP with 1.152 MHz data rate.

		XTAL mode	PLL 41.472 MHz		PLL 82.944 MHz		PLL 124.416 MHz		PLL 165.888 MHz	
Register	Applications / Bits	8 kHz Codec	8 kHz Codec	16 kHz Codec	8 kHz Codec	16 kHz Codec	8 kHz Codec	16 kHz Codec	8 kHz Codec	16 kHz Codec
CLK_PLL_DIV_REG	VD1	-	1 (2x4)		1(2x4)		Not allowed		7(4x4)	
	XD1	-	0(1)		0(1)				0(1)	
CLK_PLL_CTRL_REG	DIV2_CLK_SEL[7]	0	0	0	0	0			0	0
	DYN_SW	1	1	1	1	1			1	1
	PLL_DIP_DIV	0	4	4	8	8			16	16
	HF_SEL	0	1	1	1	1			1	1
	VCO_ON	0	1	1	1	1			1	1
	PLL_CLK_SEL	0	1	1	1	1			1	1
	PLL_OUT_DIV	0	1	1	0	0			0	0
	CP_ON	0	1	1	1	1			1	1
CLK_CODEC_DIV_REG	CODEC_CLK_SEL	0	0/1	1	0/1	1			0/1	1
	CODEC_DIV	9	9/18	18	9/36	36			9/72	72
CLK_PER_DIV_REG	PER_CLK_SEL	0	0	0	0	0			0	0
	PER_DIV	9	9	9	9	9			9	9
CLK_PER10_DIV_REG	PER20_DIV	1	1	1	1	1			2	2
	PER10_CLK_SEL	0	0	0	0	0			0	0
	PER10_DIV	1	1	1	1	1			1	1
CLK_CODEC_REG	CLK_PCM_SEL	0-3	0-3	0-3	0-3	0-3			0-3	0-3
	CLK_DA_LSR_SEL	0	0	2	0	2			0	2
	CLK_DA_CLASSD_SEL	0	0	2	0	2			0	2
	CLK_AD_SEL	0	0	2	0	2			0	2
	CLK_MAIN_SEL	0	0	0	0	0			0	0
CLK_AMBA_REG	MEM_STROBE [8]	0 (1)	0 (1)	0 (1)	0 (2)	0 (2)			0 (4)	0 (4)
	HCLK_PRE	0,1	0,1	0,1	0,1	0,1			0,1	0,1
	MCRAM1_EN[7]	0/1	0/1	0/1	0/1	0/1			0/1	0/1
	SRAM1_EN	1	1	1	1	1			1	1
	PCLK_DIV	0-2	0-2	0-2	0-2	0-2			0-2	0-2
	HCLK_DIV (CR16Cplus clock MAX)	0,1-7 10.368	0,1-7 21	0,1-7 21	0,1-7 42	0,1-7 42			0,2-7 42	0,2-7 42
MEM_CONFIG_REG	T_RC	0	0	0	1	1			1	1
CLK_DSP_REG	CLK_DSP_EN	1	1	1	1	1			1	1
	CLK_DSP_DIV Gen2DSP clock MAX	0,1-7 10.368	0,1-7 21	0,1-7 21	0,1-7 42	0,1-7 42			0,1-7 83	0,1-7 83
DSP_MAIN_SYNC0	RAMOUT[3-0]_SYNC	0	0	1	0	1			0	1
	RAMIN[3-0]_SYNC	0	0	1	0	1			0	1
DSP_MAIN_SYNC1	PCM_SYNC	0	0	1	0	1			0	1
	ADC_DA_SYNC	0	0	1	0	1			0	1
	DA_LSR_SYNC	0	0	1	0	1			0	1
	DA_CLASSD_SYNC	0	0	1	0	1			0	1
	AD_SYNC[9]	0,1	0,1	0,1	0,1	0,1			0,1	0,1
	DSP_SYN2	-	-	-	-	-			-	-
	DSP_SYN1	-	-	-	-	-			-	-
	DSP_SYN0	0	0	1	0	1			0	1
DSP_MAIN_CTRL_REG	DSP_MAIN_CTRL[10]	0,1, 2	0,1, 2	0,1, 2	0,1, 2	0,1, 2			0,1, 2	0,1,2
	DSP_MAIN_PRESET	0xF	0xF	0xF	0xF	0xF			0xF	0xF
DSP_MAIN_CNT_REG	DSP_MAIN_REL	0x8F	0x8F	0x8F	0x8F	0x8F			0x8F	0x8F

Note 7: With DIV2_CLK_SEL=1, the PLL frequency can (and must) be reduced to maximum 82.944 MHz. In this mode the GenDSP introduces wait cycles if the CR16Cplus accesses the shared RAM at the same time. DIV2_CLK_SEL=0 is therefore recommended , it saves power because the GenDSP and PLL clock can be set to a lower value.

Note 8: Values show safe reset values, value between brackets are for optimal power saving. When increasing PLL clock speeds make sure that the

MEM_STROBE is not too short for the new frequency. Most save is to change PLL frequency with MEM_STROBE =0 and then adjust MEM_STROBE to the optimal value. The memory strobe shall not be shorter than 48 ns. See also CLK_AMBA_REG (0xFF4000) (table 101, page 159).

Note 9: One or two conversion depends on application. E.g AD_SYNC = 16 kHz, CID opamp read by Gen2DSP @8 kHz + VBAT read by CR16Cplus @8 kHz

Note 10: Value 2 is the reset value. Synchronization starts if an <A_NORM> is received. Each time that a new <A_NORM> is executed to synchronize the DIP to Gen2DSP, DSP_MAIN_CTRL must toggle 2 -> 0 ->2.
Value 1 is for free running if the DIP is still off. To change to DIP synchronisation follow sequence 1-> 0 -> 2. It may take up-to 10 ms before the <A_NORM> is executed. During this time the Gen2DSP processing does not receive start triggers.

Note 11: If MC_RAM or MC_ROM are not accessed (e.g in paging mode), Bit MCRAM1_EN may be set to 0 to reduce power. The RAM contents will not be destroyed if this bit is 0.

4.0 Battery Management

The SC14480A5M, SC14480A2M6 has a complete power management function integrated.

Features:

- On / off control
- Battery voltage measurement ADC
- Temperature measurement.
- On-chip and optional external LDO's
- Constant current/constant voltage or on/off charge control function.
- State of charge (SOC) circuit for accurate battery charge calculation.

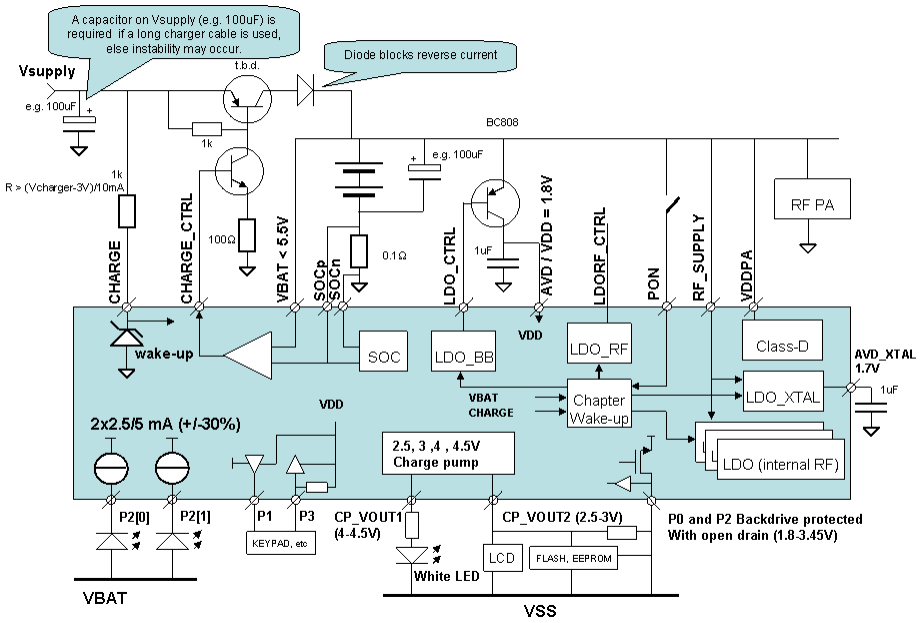


Figure 7 Handset application with 2xNiMH

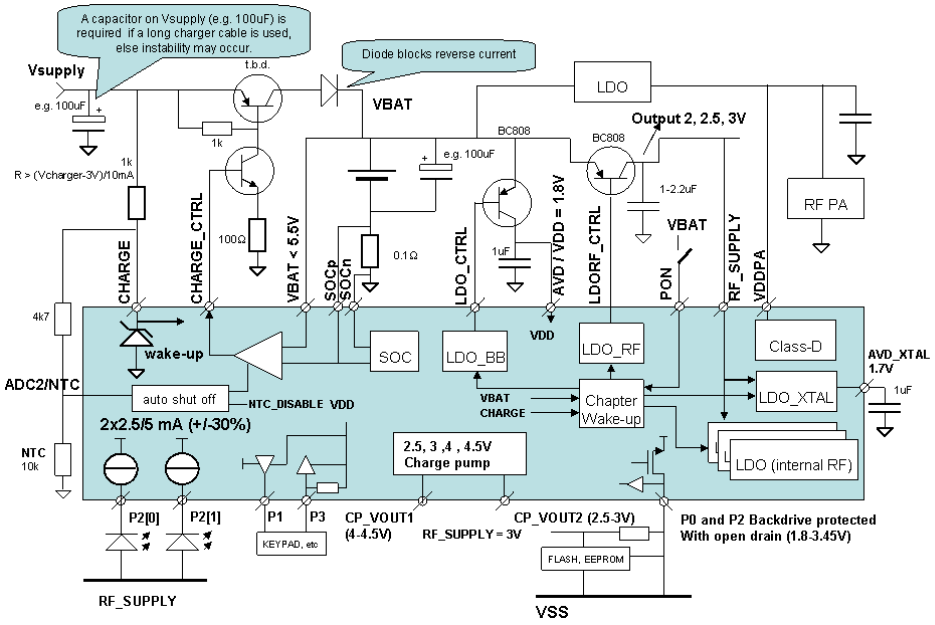


Figure 8 Handset application with Li-Ion battery

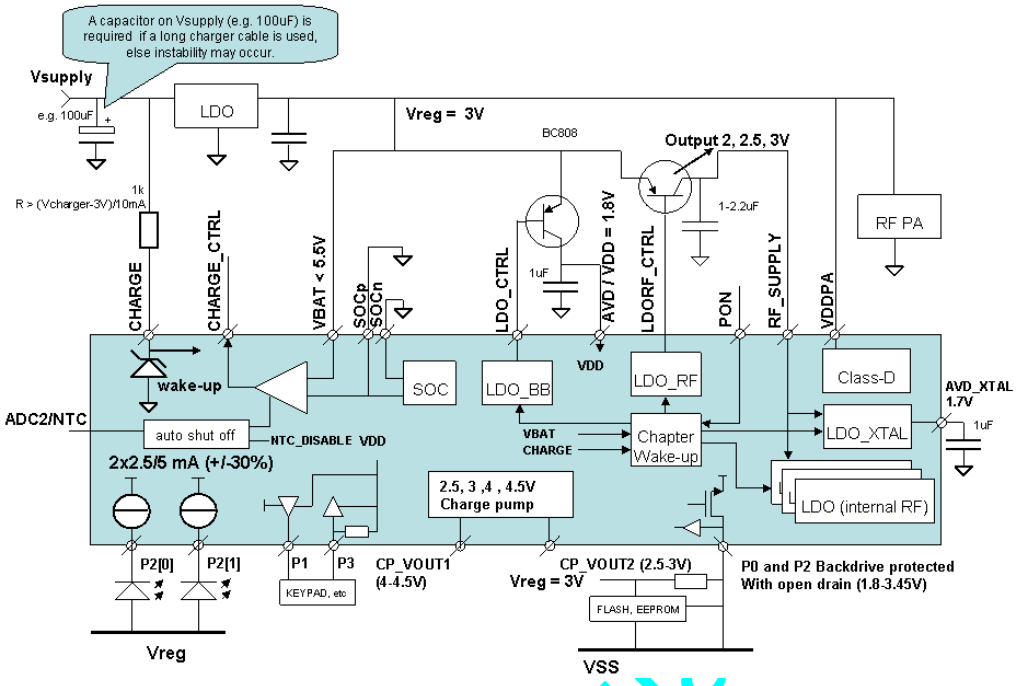


Figure 9 Basestation application using external LDO

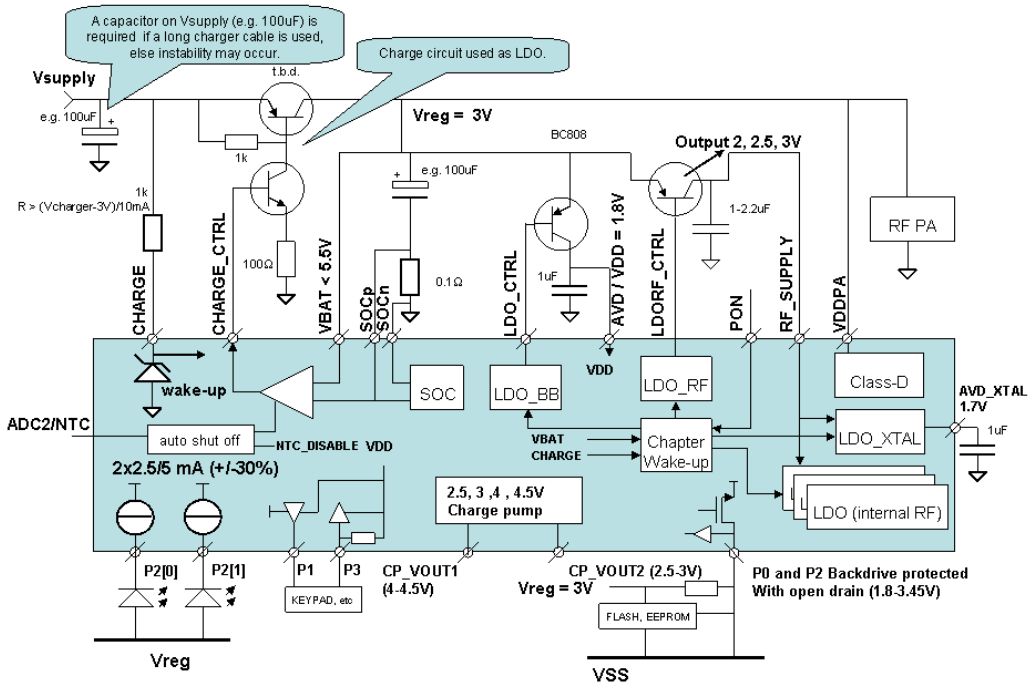


Figure 10 Basestation application using charge regulator as general purpose LDO

4.1 CHARGE CONTROL

See also *"AN-D-139 SC14480 power management"*

The SC14480A5M, SC14480A2M6 contains a constant voltage, constant current charging control circuit. The intended applications are depicted in the application diagrams.

The charge circuit has two modes of operation:

- Continuous current/voltage source mode. The control circuit keeps the charge voltage or the charge current equal to the defined values (whichever of the two is reached first). The values can be changed via BAT_CTRL2_REG. This mode is used when the charger supply adapter has **low output resistance.**
- On/off mode (SC1443x compatible mode). In case of charging via an adapter **with significant output resistance**, it is also possible to use the external pass transistor as a switch. When the charge current is set to "unlimitted", a small hysteresis is added to the charge voltage and the external transistor is either completely open or completely closed. This will significantly reduce the dissipated power in the external transistor (excessive power is now dissipated in the output resistance of the adapter).

The charging control circuit is initially supplied from the CHARGE-pin (after start-up, VBAT will take over). The complete charging circuit is powered down if the CHARGE pin is low for more than 10ms or by setting the BAT_CTRL2_REG[CHARGER_ON]=0. In Li-ion application, the charger is also disabled if the voltage on the NTC pin is in "too hot" region. (See "Charger Auto shut off circuit" on page 26)

Non rechargable batteries

To check for non-rechargable batteries, BAT_CTRL2_REG[bit0] bit is set to '1' (the charge voltage is increased above normal levels) and an ADC conversion can be started. As soon as the conversion is ready, BAT_CTRL2_REG[bit0] is automatically reset to 0 (see Table 79) in order to return to normal charge voltages.

Charge status

If a charger voltage on pin CHARGE pin is high, the CHARGE_STS in BAT_STATUS_REG (0xFF4816) is set to 1. The software has to reset this bit. The actual value of the CHARGE pin can be read from the P1_DATA_REG.

Charge regulator used as general purpose LDO in basestation

In basestation applications the charge circuit can be used as general purpose LDO. See applicatin diagrams. The output voltage is set with the BAT_CTRL2_REG[CHARGE_LEVEL] bits. Vinput ranges depend on the "output voltage" and maximum dissipation of the PNP transistor.

In this application the SOC circuit is used to regulate the start-up current. After start-up the BAT_CTRL2_REG[CHARGE_CUR] bits have no effect anymore.

4.2 CHARGER AUTO SHUT OFF CIRCUIT

The charger auto shut-off circuits for Li-ion batteries automatically switches off the charger circuit if the NTC input voltage goes outside specified voltage ranges as shown in Figure 11

The charge disable function will be activated if the voltage ratio (NTC voltage/CHARGE voltage) is between 1/2 and 1/16 (too hot). (See NTC input shuff-off level (table 279, page 223).

The region 1 to 7/8 (too cold) is not supported by hardware and can be measured using the on-chip "Temperature Sensor" on page 94.

R1 can be dimensioned as follows:
R1 = R_{NTC}@Tcritical, E.g If the NTC if 4k7 at Tcritical ~40 degrees C, charging will stop at the “too hot” limit.

The “too cold” temperature is not so critical and will practically be around 0 deg C and can therefore easily be done by SW.

For using the auto shut off function, after start-up ADC2_PR_DIS must be set to 1 to have the full input detection range upto 3.45V on the NTC pin. See also **“NTC/ADC2 voltage/current limits”** on page 92.

To **disable** the charge auto switch-off feature, either BAT_CTRL2_REG[NTC_DISABLE] must be set within 200ms after power up, or the ADC2/NTC pin must be tied to ground.

See also *“AN-D-138 SC14480 power management, Li-Ion charger”*

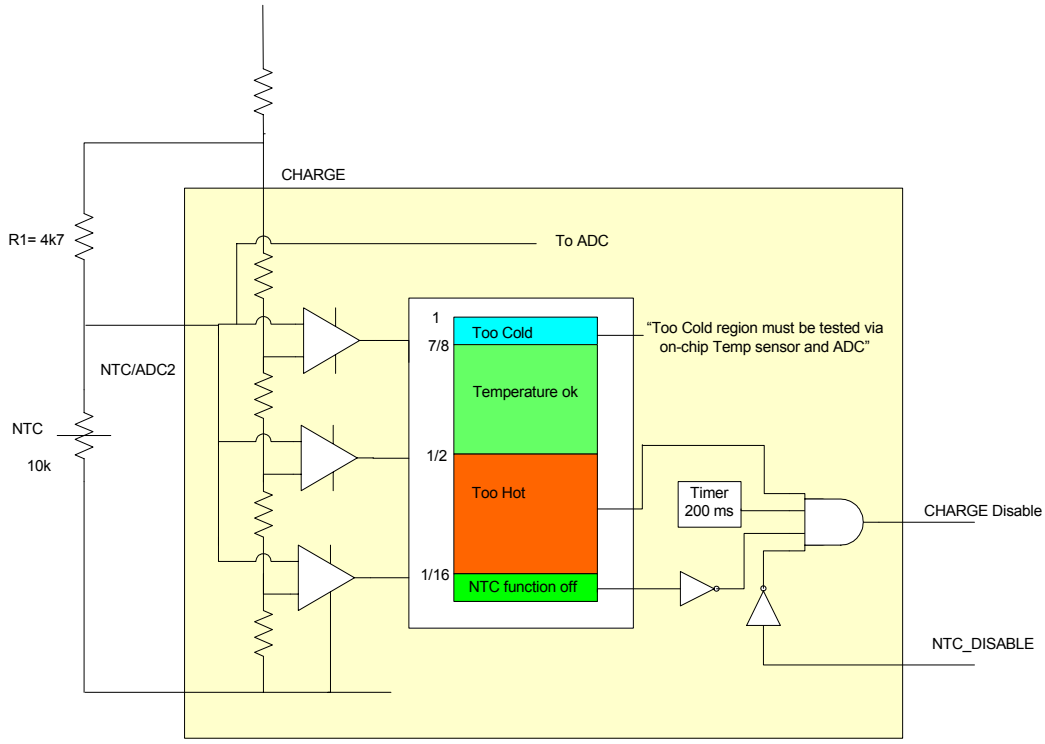


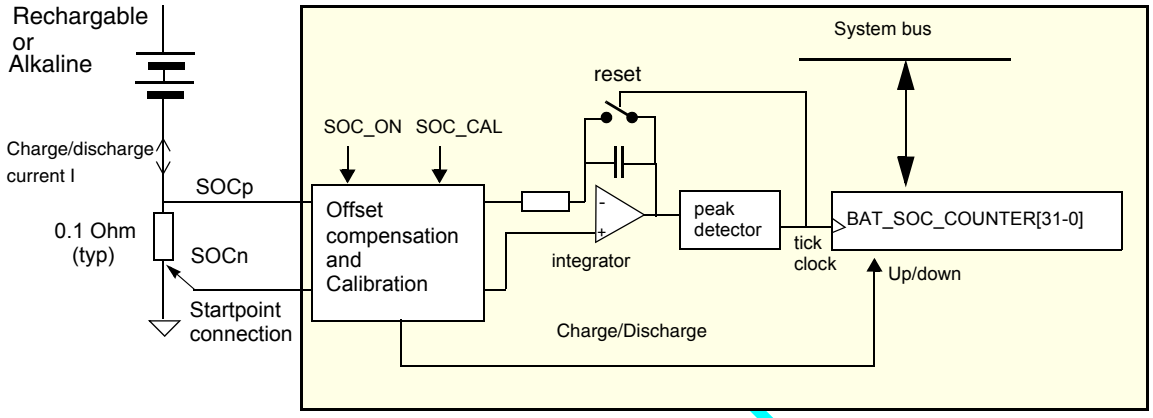
Figure 11 Charger auto shut-off circuit.

4.3 STATE OF CHARGE CIRCUIT (SOC)

The SOC circuit is used to very accurately determine the amount of charge in rechargable batteries as well as the discharge state of Alkaline batteries. This information is essential for the battery charging algorithm and necessary for battery status indication to the user.

Features

- Measures charge and discharge currents.
- Built-in offset compensation, high noise immunity
- Calibration mode for various battery types
- Very low software effort required
- Refer to *AN-D-113* SOC application note



August 26, 2005

Figure 12 State of charge (SOC) circuit blockdiagram

State of charge principle

The current is measured over a 0.1 Ohm external resistor using SOCp and SOCn pins. The SOCn signal should be connected as star point close to the resistor. The resistor could be made with a PCB trace. Its value is not critical if proper calibration is done. During operation (charge or discharge) the SOC continuously integrates the voltage difference. If a certain reference voltage is reached, the BAT_SOC_COUNTER is incremented or decremented and the integrator is reset. Every tick of the counter represents a small defined unit of charge. With 1A current over 0.1 ohm, the typical integration time is 50us, so 1 tick represents 50uAs or ±14nAh of charge. Taking these values as a reference, charging a 1000mAh battery will return a counter state of 72M ticks The maximum value of the 'state of charge' counter is 2^{31}= 2.14E+9

Operation (rechargable battery)

The counter state represents the amount charge Q=I*t. At insertion of a new battery this value is unknown, a temporary reference point has to be determined by doing a VBAT voltage measurement with ADC input 14 in single input mode. An estimation of the charge can be made and a start value needs to be written in BAT_SOC_COUNTER.
Battery status indication will be in-accurate until a new definite reference point is determined. This new point can either be "fully charged" (VBAT=max) or "fully discharged" (VBAT=min). At these events a new counter value is written in the register (high value in case of a full battery, low value in case of an empty battery). A positive voltage difference SOCp-SOCn (charge battery) counts up and a negative value (discharge) counts down.

Operation (non-rechargable battery)

In case of the insertion of non-rechargable Alkaline battery, the counter can be preset to a value equivalent to the (estimated) charge/capacity of the battery and the SOC can be used to measure the discharge process. The estimated charge can be determined by measuring the VBAT voltage with ADC input 14 in single input mode.

Calibration

The integration constant can be determined by setting BAT_CTRL_REG[SOC_CAL] to 1. In this calibration mode, the integrator gets a 100 mV reference voltage. This voltage represents current of 1A over 0.1 Ohm. The integration constant C can be determined by reading out the SOC_COUNTER value after a fixed time controlled by the software. In application production a 1A current through the actual 0.1 Ohm resistor can be used as reference, this way the resistors error is calibrated as well, for even higher accuracy.

Example:

- SW initiates calibration for 10ms
  SOC_COUNTER returns value: $250_{(d)}$
  So, 250 ticks = 1A/10ms => 1 tick = 11.1nAh

Software 'knows' that a full 1000mAh battery is 90 Million counter ticks. after getting a reference point by means of a VBAT measurement (ADC input 14), accurate battery indication can be started.

5.0 ON / OFF control

Switch on procedure

The SC14480A5M, SC14480A2M6 will switch on the LDO_BB, LDO_XTAL and the XTAL oscillator under the following conditions: (see Figure 13 and Figure 14 and paragraph 35.0):

- VBAT> Vbat_on (vbat_ok) and one of the following conditions becomes true:
  - PON pin >Vih_a3pad. (Power on key)
  - CHARGE pin > Vih_a3pad (charger voltage)
  - Connecting a new battery to VBAT pin. (“new bat”)

When the regulated VDD/AVD supply is stable, the internal reset is released and the CR16Cplus is activated. BAT_CTRL_REG[**REG_ON**] must be set to 1 to keep the LDO_BB, LDO_XTAL and XTAL on.

The internal LDO supplying the RF blocks are enabled with their corresponding DCF. (Refer to paragraph 9.6.2)

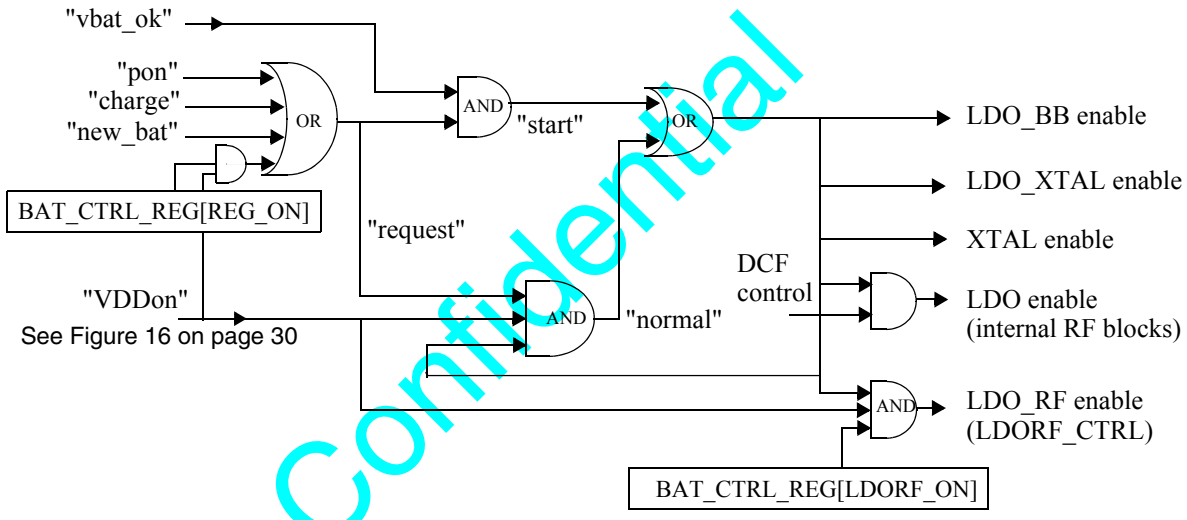
The External LDO_RF LDO can optionally be enabled by setting BAT_CTRL_REG[LDORF_ON]

Switch off procedure

The software can decide to switch off the device, for example when the software gets a PON interrupt signal.

To switch-off, all following conditions must be true:

- PON pin < Vil_a3pad
- CHARGE pin < Vil_a3pad for more than 100 ms.
- BAT_CTRL_REG[REG_ON] =0.



October 9, 2007

Figure 13 Wake-up circuits

5.1 POWER-ON STATUS

The source of the power-on request can be read in the BAT_STATUS_REG. PON_STS indicated the PON pin was pressed, CHARGE_STS that a charger was connected and VBAT3_STS that a rising edge on VBAT occurred. The PON and CHARGE status bits are set on a positive level and must be reset by writing a '0' to the registers. The status bits remain set as long as the "pon" and "charge" conditions are valid.

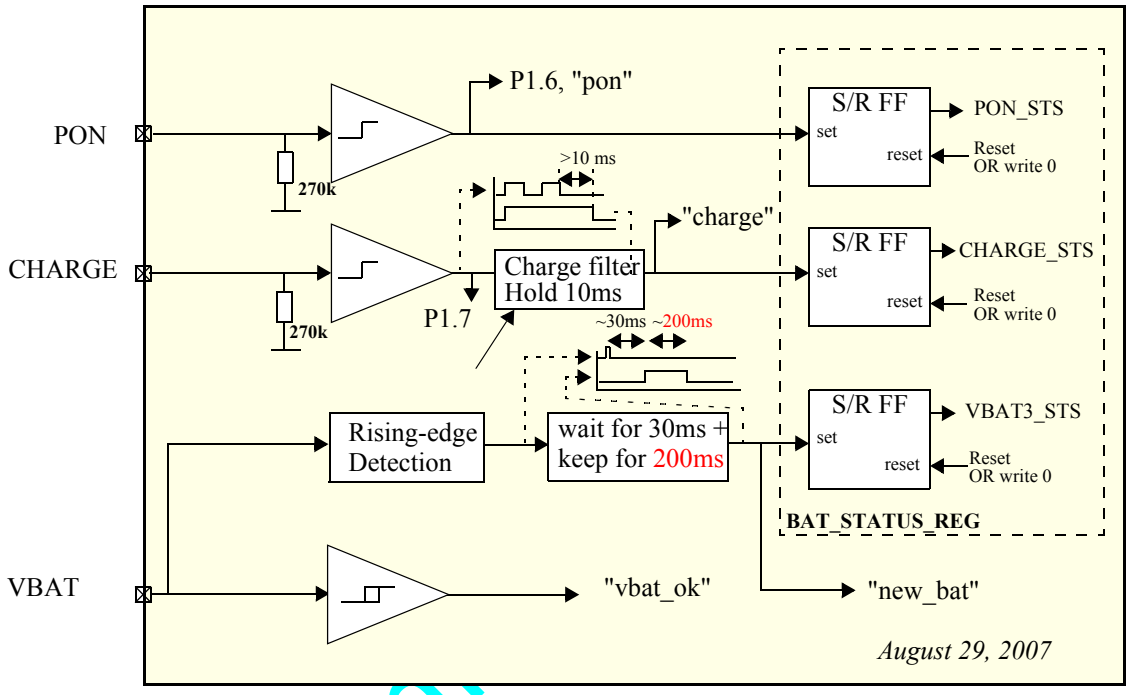


Figure 14 Wake-up status circuit

5.2 BANDGAP REFERENCE

The SC14480A5M, SC14480A2M6 has a bandgap register which is used by the analog codec front-end, Radio frontend Battery management circuitry and ADC as reference voltage.

The BANDGAP_REG has reset value 0xF, resulting in an initial VDD/AVD voltage of 1.8V -0% +10%. This voltage can be tuned in production to 1.8V with BANDGAP_REG bits 3-0 to an accuracy better than 1%.

If VDD/AVDF is trimmed to 1%, VDDIO is 2% accurate.

The trimmed value written to BANDGAP_REG can be saved by the CR16Cplus in the external EEPROM and restored in the BANDGAP_REG register at system startup.

See BANDGAP_REG (0xFF4810) (table 77, page 151) for a registers on how to trim the voltages.

The BANDGAP_REG is only reset by a hardware reset (RSTn)

6.0 Reset circuit

6.1 POWER ON RESET

At AVD=1.8V-2.0V (BANDGAP_REG=0xF, reset value, see also Table 277 on page 222), or the LDO voltage has reached a stable voltage (LDO_BB_stable), the internal signal "VDDon" releases the RSTn pin via an open drain FET. With an external capacitor connected to the RSTn pin, the internal reset is released at Vih_rst and all blocks, including SDI+, the SW reset and HW reset will get inactive, port P0 will be latched in TEST_ENV_REG and the boot program will be started. (See "Boot program" on page 121).

After power-on the RSTn must stay low for at least Trst_low_pu (see Table 316)

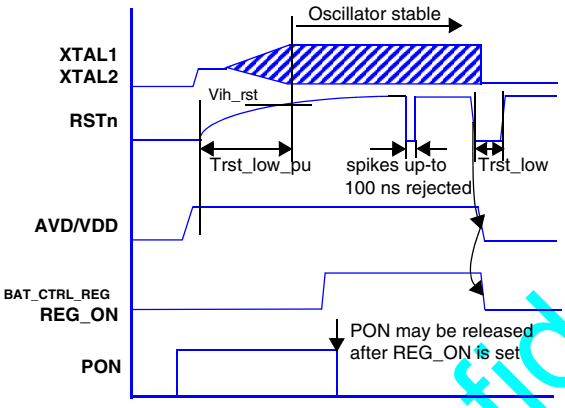


Figure 15 Reset diagrams

The values of the external capacitor Crst is determined is by the RC product with the internal pull-up on the RSTn (Ipu_rst_lo (see Table 280)).

A typical value for **Crst**=Trst_low_pu/R= Trst_low_pu/(U/Ipu_rst_lo(MAX)= 10E-3 /(1.8/20E-6) = **100nF**.

6.2 SYSTEM RESET.

After power on, the following conditions reset the whole SC14480A5M, SC14480A2M6 or parts of it as shown in Figure 16:

- If the RSTn pin is pulled down for at least Trst_low, then the "VDDon" goes LOW. A full device reset is issued. The RAM content is not intentionally reset, but might contain undefined data due to an early termination of a RAM write cycle. Spikes less than 100 ns are suppressed.
- If the AVD drops below Vrst_on-Vhyst (typical 1.65V with trimmed bandgap), the RSTn pin is automatically pulled low.
- If the JTAG_SDI+ issues the command sequence SYSRST_ON/SYSRST_OFF all blocks, excluding JTAG_SDI+ and TEST_ENV_REG, are reset but the RSTn pin is not pulled low. (Note that a JTAG command that sets the internal TRSTn pin, only sets the SDI+ TAP controller in the reset state.)
- If the watchdog timer expires and TIMER_CTRL_REG[WD0G_CTRL] = 1, all blocks excluding JTAG_SDI+ and TEST_ENV_REG, are reset but the RSTn pin is not pulled low.
  If WD0G_CTRL=0, an NMI will be executed and the user has full control over manual reset sequence (e.g setting SW_RESET)

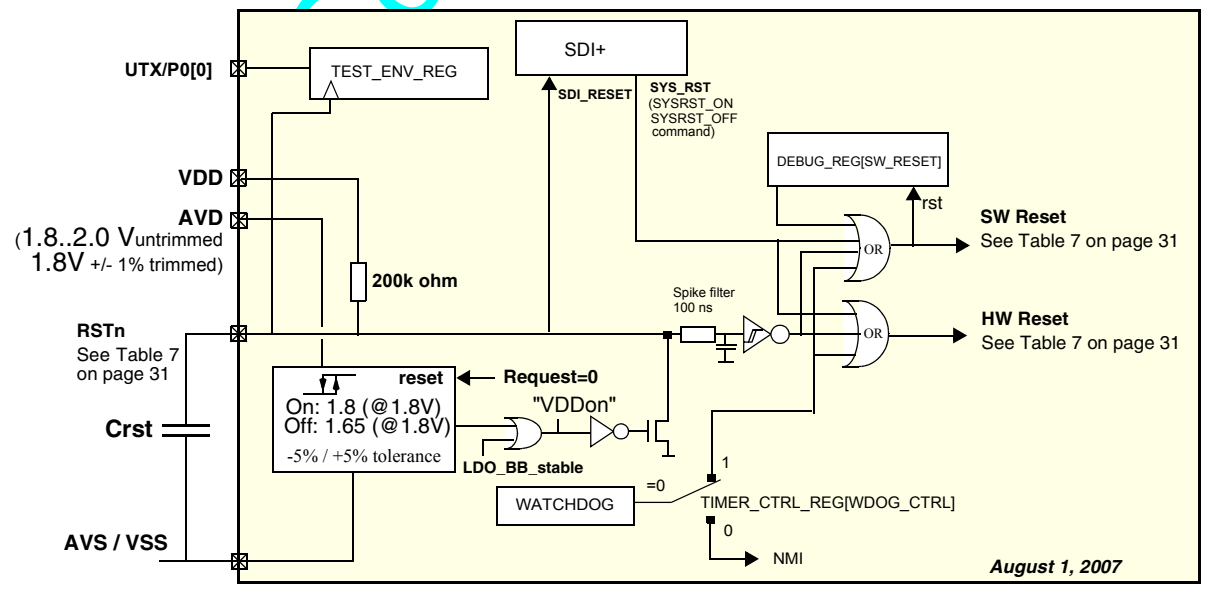


Figure 16 Reset circuit

6.3 SOFTWARE RESET

Purpose of a SW software reset is to reset the chip and jump to a specified start address defined by PC_START_REG. The software reset is a partial reset as shown in **Table 7** and is invoked by setting DEBUG_REG[SW_RESET]=1.

The SW reset can be used in the following cases:

- Enabling the ROM patching feature (**See DEBUG_REG[CR16_DBGM] and AN-D-146**)
- Restart of the application upon a Watchdog time out. In case TIMER_CTRL_REG=0, an NMI will be executed and the ISR may give a SW reset.
- If a program is loaded via the UART boot protocol and SW_RESET is given, the UART boot protocol can be skipped if DEBUG_REG[ENV_B0]1 is set. See **"Boot from internal RAM" on page 121**

Table 7: Registers reset overview

Register	RSTn=0 or AVD< (Vrst_on-Vhyst)	SDI SYS_ RST or Watch-dog	HW reset	SW reset
- JTAG_SDI+	✓	-	-	-
- TEST_ENV_REG	✓	-	-	-
- PC_START_REG	✓	✓	✓	-
- DEBUG_REG[CR16_DBGM]	✓	✓	✓	-
- DEBUG_REG[ENV_B01]	✓	✓	✓	-
- BANDGAP_REG	✓	✓	✓	-
- BAT_CTRL_REG	✓	✓	✓	-
- FLASH_CTRL_REG[10-9]	✓	✓	✓	-
- Px_DATA_REG	✓	✓	✓	-
- Px_DIR_REG	✓	✓	✓	-
- Px_MODE_REG	✓	✓	✓	-
- Other registers	✓	✓	✓	✓

6.4 PROGRAM COUNTER AFTER RESET

See Figure 17. At a hardware reset caused by the RSTn pin, the PC_START_REG is reset to 0xFEF0 (booter ROM address) and the CR16Cplus program counter PC bits 24, 9-0 are set to 0 and bits 23-10 are loaded with PC_START_REG[15-2] (See Figure 17) and the CR16Cplus starts to execute from the boot ROM at 0xFEF000.

At a SW_RESET, PC_START_REG is not reset but the CR16 PC is again loaded with PC_START_REG bit 15-2. This allows to restart from an other address e.g on-chip RAM.

Note that the PC_START_REG can only be set to . boundaries of 1k

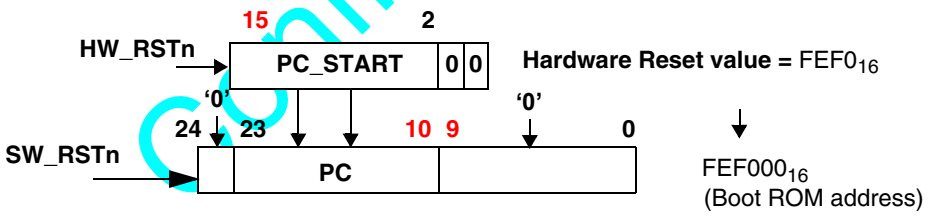


Figure 17 PC_START_REG loading in CR16Cplus Program counter PC

7.0 DIP

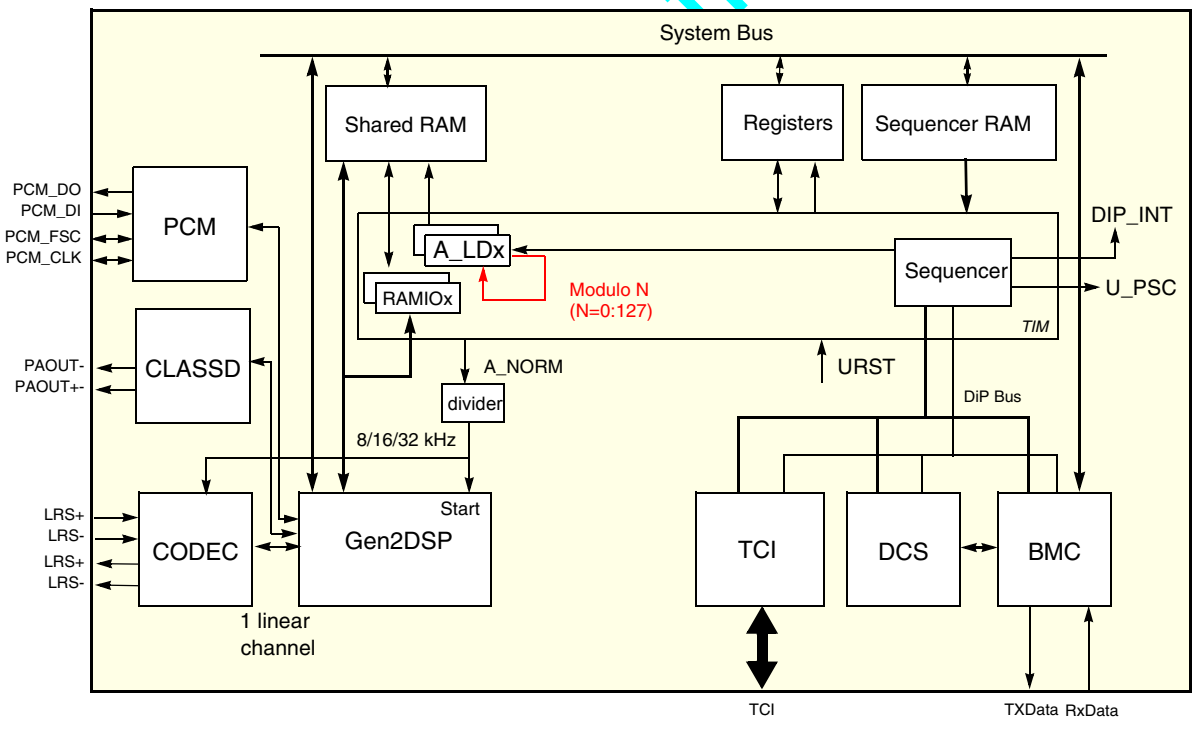
The Dedicated Instruction Processor (DIP) in conjunction with the CR16 takes care of MAC-CSF functions as depicted in Figure 19. The S, A, B, and Z field order is controlled from the sequencer and 16 and 32 bits R-CRC generation is done in the BMC. The DIP handles slot and frame timing to the RF front end interface without CR16 interruption. The instructions for the DIP are stored in the Sequencer RAM. All necessary data and control information can be stored in advance to control a complete (10ms) frame. Consecutive instructions are performed at the symbol clock rate.

The DIP issues instructions to BMC, DCS (Cyphering) and TCI (Transceiver Control Interface) and supports automatic Gen2DSP ADPCM and BMC pointer handling toward shared RAM.

For detailed information refer to "AN-D-140 SC14480A5M, SC14480A2M6 DIP Instruction Processor"

Features

1. Instructions for fix DECT full, long and double slot formats or user programmable Rx and Tx slot with one bit resolution.
2. Instructions for fixed or programmable S-field.
3. Instructions for fixed or programmable A-field with automatic 16 bit R-CRC generation and detection.
4. Instructions for protected and non protected B-field formats with programmable 16 bit R-CRC and 32 bit B-CRC
5. Next generation protected B-fields 8x(64+16)
6. BMC Bit Clock divider factor 1, 2 and 4.
7. Automatic ADPCM and BMC pointer handling (4xRx, 4xTx) to shared RAM for minimum delay of full slots, 640 bits long slots.
8. Flexible slot format with Modulo 0:127 operation
9. Instructions to synchronise the audio path from BMC to Gen2DSP and Codec. (A_NORM)
10. Instructions to synchronize DIP frame to 8kHz PCM slave interface. (WSC)
11. Bit accurate timing control of the Radio transceiver functions over the Transceiver Control Interface (TCI).



August 22, 2006

Figure 18 DIP block diagram

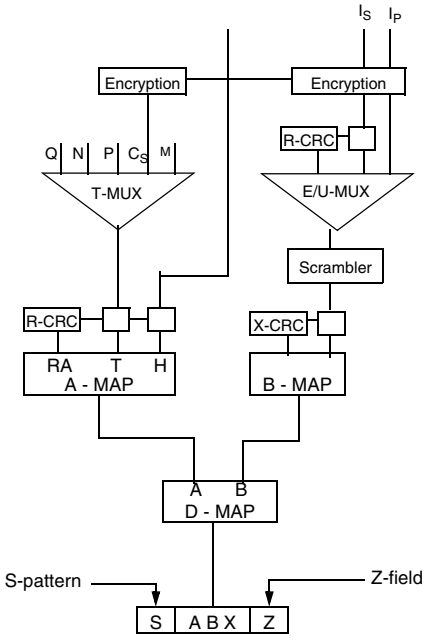


Figure 19 SC14480A5M, SC14480A2M6 MAC functionality

7.1 DIP ON/OFF CONTROL

The SC14480A5M, SC14480A2M6 CR16Cplus controls the DIP with the DIP_CTRL_REG[URST] bit. With URST is set to 0 the DIP executes the instructions stored in sequencer from address 0x0100.0002 at a clock rate of 1.152MHz ~~in case of the DECT mode, 1.024MHz in case of 8/9 mode~~.

7.2 DIP SEQUENCER RAM

The 512 words of internal DIP program RAM contain the DIP executable code. The executable code inside this RAM can be read and written by the CR16Cplus at any time. An internal bus arbiter takes care of bus conflicts if the DIP and CR16Cplus access the sequencer RAM at the same time.

7.3 DIP INTERRUPT GENERATION AND POWER CONTROL

DIP instructions <U_INT0>, <U_INT1>, <U_INT2>, <U_INT3> and <U_VINT> <X> generate a DIP_INT interrupt to the CR16Cplus. The corresponding interrupt vector can be read from register DIP_CTRL_REG[3-0]. <U_VINT> <X> set bits 3 to 0 to value <X>. <U_INT0> set bit 0, <U_INT1> sets bit 1 etc.

If the prescaler mode bit is set to 1 and the DIP executes the <U_PSC> command the SCLK is divided by 16. This clock division remains active after the <U_PSC> command is executed until the DIP executes a <U_INTx> or <U_VINT> command or the prescaler mode bit is set to 0.

The DIP_CTRL_REG[DIP_BRK_INT] bit is set by the DIP if the BRK command is executed. At this time also a DIP interrupt is generated at the CR16Cplus. After execution of the break command the DIP program counter is not incremented until a 1 is written to DIP_CTRL_REG[DIP_BRK_INT]. The CR16Cplus can read the program counter from the time the BRK command is executed until the break bit is cleared.

7.4 INTERFACING TO GEN2DSP

See Figure 18.

Instruction <A_NORM> starts 8/16/32 kHz generation and the Gen2DSP has full access to its own data RAM.

7.5 MINIMUM DELAY

For minimum delay voice applications, the Gen2DSP must use RAMIO registers DSP_RAMx_IN_REG and DSP_RAM_OUTx_REG so that the DIP handles the RAM access.

The <A_LDRx>/<A_LDWx> instructions sets pointers to the buffers in shared RAM were the RAMIO registers will be written or read from. Every 4kHz (for 32kbits/s) or 8 kHz (64kbits/s) the DIP (TIM) reads from DSP_RAMx_IN_REG and writes one byte to DSP_RAM_OUTx_REG. With the same rate the Gen2DSPx must access the RAMIO registers.

The TIM block takes care of copying these registers to circular buffer pointed to by <A_LDWx> pointer and auto increment these pointer with a modulo N (0:127). N=39 for 32kbit/s ADPCM and N=79 for 64kbit/s ADPCM).

For minimum delay the BMC is able to read and write one location after the actual ADPCM pointer using instructions:

- <B_BRFU>, <B_BTFU> with parameter 0xFC for 32kbits/s ADPCM: 32S+64A+320B+4X+4Z (Buffer modulo 40 bytes).
- <B_BRLU>, <B_BTLU> with parameter 0xFC for 64kbits/s ADPCM: 32S+64A+ 640B+(32BCRC)+4X, 4Z. (Buffer modulo 80 bytes). 32 bits CRC can be switched on/off with B_RC3[EN_32B].

7.6 MUTING

The SC14480A5M, SC14480A2M6 can sense the correctness of the A-field CRC by setting the SENSE_A bit to 1. If an erroneous frame is received the new B-field will not be written and the last received B-field will be repeated in order not to disturb the ADPCM sound.

If the SENSE_A bit is kept to 0 and an A-field error is detected, the CR16Cplus can decide to initiate mute sequence to the Gen2DSP.

In case of sync loss the B-field is muted if the SENSE_S bit is set to 1.

Command <B_BTFM> transmits '0's or 1s in the B-field in order to mute the outgoing speech. If BMC control bit MUTE_LEVEL is 0 then '0's are transmitted, else 1s.

7.7 SLOT CONTROL INFORMATION

Receive and transmit burst timing in the radio transceiver is controlled by the DIP over the transceiver control interface. With DIP command <B_RC>, the slot control information can be read from any shared RAM location (see table 8). Control information is read before every received and transmitted slot. With DIP command <B_WRS> the MAC status information on received slots is written into the shared RAM of the SC14480A5M, SC14480A2M6 (see table 9). DIP command <B_WRS d_offset> updates all these parameters. At the end of every received time-slot an interrupt instruction <U_INTx>, <U_VINT> or <U_NMI> can be set in the sequencer RAM to enable the microprocessor to read out the appropriate status data.

Table 8: Slot control information in the shared RAM

NAME	TYPE	FUNCTION
S_err[3..0]	Binary	Maximum number of errors allowed in non-masked bits of S-field pattern S[8..31]
Inv_RDI		Inversion of received data input
Inv_TDO		Inversion of transmit data output
SENSE_A		B field data is not written in the case when the A-field CRC is incorrect
SENSE_S		B field data is not written in the case when the BMC loses synchronisation.
PP/FPn		PP mode selected
Mask[3..0]	Binary	Mask S-field pattern[15..8] in error calculation over pattern [8..31]
Slide[3..0]	Binary	Mask S-field pattern[15..8] in Sliding error calculation over pattern[15..8]
ADP	Binary	Upon A-field CRC error, no phase adjustment will be made
WIN[3..0]	Binary	Defines maximum phase shift. If phase shift is between ±WIN symbols, the IN_SYNC bit will be set
FR_nr[3..0]	Binary	Frame number 0..15
MFR[23..0]	Binary	Multi frame number
IV[28..63]	Code	Encryption unit initialisation vector
CK[0..63]	Code	Encryption unit cypher key
ENC_OFF	Binary	Disable/enable Encryption
SCR_OFF	Binary	Disable/enable Scrambling

Table 8: Slot control information in the shared RAM

NAME	TYPE	FUNCTION
MUTE_ LEVEL	Binary	Used with B_BTFM command. If 1 transmit 1's, 0 transmit 0 in B-field.
EN_32B	Binary	Enable CRC32 in B_BTLU and B_BRLU or Enable Padding in B_BTLP and B_BRLP

7.8 SLOT STATUS INFORMATION

At the end of every received slot the status is updated in the shared RAM.

.

Table 9: MAC Slot status information the shared RAM

NAME	TYPE	FUNCTION
IN_SYNC		Set to 1 when the S-Field pattern falls within the defined window size
A_CRC		Set to 1 when the A-field CRC is correct
X_CRC		Set to 1 when the X-field CRC is correct
ZACK		Set to 1 when the Z-field = X-field
Bn-CRC		Set to 1 when protected B field R-CRC of block n is correctly received. n =0..9
SL_err[3..0]	Binary	Report number of sliding errors over unmasked S-field bits 8 to 15.
TAP[4..0]		S-field phase information, with 1/9 DECT bit accuracy
Phase[7..0]	2's Compl	S-field pattern phase error, with DECT bit accuracy
DC[5..0]	Binary	DC offset information
Offset[15..0]	Binary	Offset counter from <B_SR> command upto received S-field

7.9 SLOT SYNCHRONISATION

The SC14480A5M, SC14480A2M6 BMC is capable of detecting the S-field pattern. To be able to lock to the received frame in the PP mode the microprocessor enables the slot counter to be preset at S-field detection. If the preset of the slot counter occurred once, the preset is disabled. The microprocessor can enable this preset again. If disabled the SC14480A5M, SC14480A2M6 will only search for the S-field pattern in a predefined window repeated every 10ms after the

first S-field pattern has been detected. In lock the SC14480A5M, SC14480A2M6 can accept a packet phase shift up to a programmed maximum window size. This window is programmable with control nibble WIN[3:0] from 0-15 symbol periods. This phase shift information is stored in PHASE[7-0] in two's complement notation in the MAC status bytes. If the phase shift is more than the programmed window the "in_sync" bit will not be set. Once enabled by the microprocessor the SC14480A5M, SC14480A2M6 will automatically adjust the frame timing. If the ADP bit is set 1 then the automatic phase adjustment will only be done if the A-field CRC is correct. If ADP is 0 the phase adjustment will be made regardless of the A-field result. Choosing to write the B-field data depending on the A-field CRC result is selectable using the control bit SENSE_A. If the phase shift between the internally generated frame and received frame is less than 2 symbol periods frame timing is adjusted with ±1 symbol period at the end of the frame. The update will be maximum ±2 symbols if this phase shift is 2 or more symbols. However the microprocessor can take over control and program phase jumps of ±1 symbol period instructions for the next frame if appropriate and disable the automatic phase jumps.

If in an unlocked state an S-field is received, the slot counter is preset and the current WNT is terminated. If a <JMP1> instruction is then executed a jump will be executed.

7.10 S-PATTERN CORRELATOR

With the control bytes it is possible to define the criteria for the S-field to be detected.

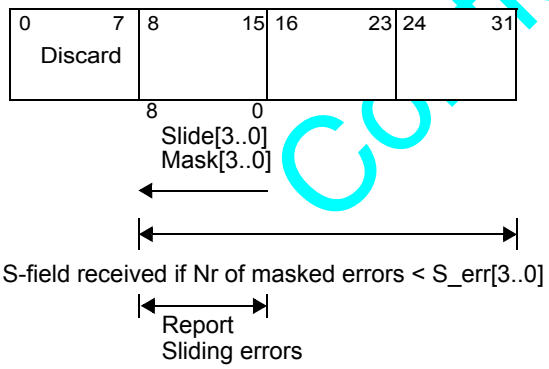


Figure 20 S-field pattern

The first eight bits of the S-field bit sync pattern S[0..7] are ignored. On the next eight bits a mask register Mask[3..0] masks bits 15 to 8. ("0011" unmasks bit 13,14,15.). If the total number of errors in bits 16 to 31 plus the unmasked bits 8 to 15 is less than a number programmed in the shared RAM (S_err[3..0]), the S-field is received correctly and the phase shift can be calculated. S-field bits 15 through 8 are also used to check for sliding errors. These are reported in the MAC unit status register SL_err[3..0]. Mask register Slide[3..0] masks S-field bits 15..8. ("0011" unmasks bits 8,9,10). Only unmasked bits are taken in to account for the sliding error calculation. A sliding error occurs when a neighbouring un-synchronized station sends out a packet that slides into the received packet.

The received S-field is compared with the BMC_RX_SFIELD_REG. The transmitted S-field data can be transmitted as a fixed pattern with <B_ST>, from RAM with <B_ST2> 00, from BMC_TX_SFIELD_REG with <B_ST2> 01 to 04.

7.11 DCS BLOCK ENCRYPTION

The Key Stream Generator (KSG), used to encrypt A and B-field information, can be switched on or off by the microcontroller via instructions in the sequencer RAM. The KSG initial state is stored in the internal data memory. CK[63..0] is the cypher key information. The MAC unit recognizes Cs type messages in the A-field data and encrypts or decrypts only these messages. Encryption can be temporarily disabled with bit ENC_OFF set to 1. The encryption engine remains active but no data is encrypted.

7.12 SCRAMBLER

Scrambling and descrambling, using the frame counter bits FR_nr[3..0] to initialize the scrambler and descrambler, is performed on the B-field.

7.13 R-CRC, X-CRC AND Z FIELD

Generation and checking of the 16-bit CRC is performed on the A-field data (A_CRC will be set if CRC is correct). For the B-field, X-CRC and Z-field are generated and checked for transmission and reception respectively. A, X and Z field results are stored in the internal data memory (A_CRC, X_CRC and ZACK bit). Full slot protected B-field format is supported and 16 bit CRC is calculated for every 64 bits of data.

Instruction <B_RON> and <B_RINV> are used to manually start and stop X-CRC.

<B_NIC> in conjunction with <B_BRFP>/<B_BTFP> supports 16bits R-CRC and <B_NIC> with B_BRDP>/<B_BTDP> supports 32 bits B-CRC calculation. according ETS EN 300 175-3.

7.14 ADPCM SUPPORT

In order to support minimum delay for upto four voice links the following ADPCM commands are used: <A_NORM>, <A_LDWx>, and <A_LDRx>. The other <A_xxx> have no function any more, but can be kept in DIP sequencer code if software reuse requires this. See Table 10.

7.15 DIP COMMANDS

.

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
BR	0x1	Branch Always
BRK	0x6E	Break for CR16Cplus

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
JMP	0x2	Jump to subroutine (4 deep)
JMP1	0x3	Jump conditionally to sub-routine
RTN	0x4	Return from subroutine
WNT	0x8	Wait until start of times-lot(s)
WT	0x9	Wait N time symbols (Immediate or indirect via LD_PTR2)
RFEN	0xB	Enable RF clock
RFDIS	0xA	Disable RF clock
BK_A	0x0E	Set memory bank for ADPCM channel
BK_A1	0x05	Set memory bank for ADPCM channel 1
BK_A2	0x1E	Set memory bank for ADPCM channel 2
BK_A3	0x15	Set memory bank for ADPCM channel 3
BK_MA	0x16	Set main memory bank for ADPCM channels
BK_C	0xF	Set memory bank for burst mode controller, micro wire and encryption unit
BK_MC	0x1F	Set main memory bank for burst mode controller, micro wire and encryption unit
BCPV	0x4B	Programs WNT-enter pre-set value
SLOTZERO	0xD	Reset internal CLK100 timer
EN_SL_ADJ	0x2C	Enable DECT bitclock phase adjustment
WNTP1	0x7	Increment symbol counter
WNTM1	0x6	Decrement symbol coun-ter
WSC	0x48	Wait for external synchro-nisation on PCM IF.
LD_PTR	0xC	Load pointer for indirect shared Ram access
LD_PTR2	0x1C	Load pointer for parame-ters of WT, R_LDH, R_LDL
UNLCK	0x28	Enter “PP unlocked” mode

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
A_NORM	0xC5	Start Gen2DSP main counter and determines start of ADPCM tick.
A_LDR	0xC6	Initialise start of ADPCM channel read buffer
A_LDW	0xC7	Load ADPCM channel write address
A_LDR1	0xCE	Initialise start address of ADPCM channel 1 read buffer
A_LDR2	0xD6	Initialise start address of ADPCM channel 2 read buffer
A_LDR3	0xDE	Initialise start address of ADPCM channel 3 read buffer
A_LDW1	0xCF	Initialise start address of ADPCM channel 1 write buffer
A_LDW2	0xD7	Initialise start address of ADPCM channel 2 write buffer
A_LDW3	0xDF	Initialise start address of ADPCM channel 3 write buffer
A_TX	0x4A	ADPCM channel assign-ment to BMC Tx slots
A_RX	0x49	ADPCM channel assign-ment to BMC Rx slots.
B_ST (B_TX)	0x31	Transmit any data from the shared RAM
B_ST2	0x21	Transmit fixed ETSI S-field in PP or FP mode
B_PPT	0x22	Transmit prolonged pre-amble
B_AT	0x32	Transmit A-field
B_AT2	0x37	Transmit A-field and A-field CRC (R_A)
B_BT	0x34	Transmit B-field
B_BTFU (B_BT2)	0x25	Transmit full slot unpro-tected B-field, B-field CRC (X) and Z-field (Z)
B_BTFM	0x23	Transmit full slot unpro-tected B-field, B-field CRC (X) and Z-field (Z) B-field contains either 0: (Mutelevel=0) or 1: (Mutelevel=1)

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
B_BTFP	0x35	Transmit full slot protected B-field, B-field CRC (X) and Z-field (Z)
B_BTDU	0x71	Transmit double slot unprotected B-field, B-field CRC (X) and Z-field (Z)
B_BTDP	0x72	Transmit double slot protected B-field, B-field CRC (X) and Z-field (Z)
B_BTLU	0x95	Transmit 640 bits slot unprotected B-field: 32S, 64A, 640B, (32BCRC,) 4X, 4Z. (BCRC on/off with B_RC3[EN_32B])
B_BTLM	0x93	Equal to B_BTLU, but B-field contains either 0: (Mutelevel=0) or 1: (Mutelevel=1)
B_BTLP	0x75	Transmit 640 bits slot protected B-field: 32S, 64A, 8x(64B/16CRC), (32bits padding), 4X, 4Z. (Padding bits on/off with B_RC3[EN_32B])
B_SR	0x29	Receive S-field
B_AR	0x3A	Receive A-field
B_AR2	0x3F	Receive A-field and A-field CRC (R_A)
B_RON	0x2F	Transmit A-field CRC or Receive and compare A-field
B_RINV	0x2E	Invert last bit A-field R_CRC
B_BR	0x3C	Receive B-field
B_BRFU (B_BR2)	0x2D	Receive full slot unprotected B-field, B-field CRC (X) and Z-field (Z)
B_BRFP	0x3D	Receive full slot 320 bits protected B-field, B-field CRC (X) and Z-field (Z)
B_BRFD	0x2A	Receive full slot unprotected B-field, B-field CRC (X) and Z-field (Z), No B-field data is stored
B_BRDU	0x79	Receive double slot unprotected B-field, B-field CRC (X) and Z-field (Z)

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
B_BRDP	0x7A	Receive double slot protected B-field, B-field CRC (X) and Z-field (Z)
B_BRLU	0x9D	Receive 640 bits slot unprotected B-field, 32S, 64A, 640B, (32BCRC,) 4X, 4Z. (BCRC on/off with B_RC3[EN_32B])
B_BRLD	0x9A	Equal to B_BRLU but no B-field data is stored
B_BRLP	0x7D	Receive 640 bits slot protected B-field: 32S, 64A, 8x(64B/16CRC), (32bits padding), 4X, 4Z (Padding bits on/off with B_RC3[EN_32B])
B_XR	0x2B	Receive X-field
B_WB_ON	0x65	Write zeroes in B-field receive buffer if A-CRC is 0
B_WB_OFF	0x64	Disable B_WB_ON command
B_WRS	0x39	Write BMC status information to the shared RAM
B_WRS2	0x38	write synchronisation counter to RAM
B_RC	0x33	Load BMC control information from the shared RAM in BMC
B_XOFF	0x26	X-CRC off
B_XON	0x27	X-CRC on
B_XT	0x24	Transmit X-CRC
B_RST	0x20	Set BMC in power down mode.
B_DIV1	0x4F	Set BMC clock to 1.152 MHz. (default)
B_DIV2	0x4E	Set BMC clock to 1.152/2 MHz.
B_DIV4	0x4D	Set BMC clock to 1.152/4 MHz.
D_LDK	0x50	Load encryption data from the shared RAM in DCS unit
D_PREP	0x44	Preprocess encryption data in DCS
D_PREP2	0x45	4 times faster D_PREP
D_WRS	0x5F	Write current encryption status to the shared RAM
D_LDS	0x57	Load intermediate encryption status from the shared RAM

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
D_RST	0x40	Reset keystream generator
M_WR	0xB9	Transfer from the shared RAM to the transceiver control interface
M_RD	0xBC	Transfer to the shared RAM from the transceiver control interface
M_RST	0xA9	Stop the commands M_WR and M_RD
M_INI0	0xA0	Set SK,SO start/end levels to 0, SK falling edge
M_INI1	0xA1	Set SK,SO start/end levels to 1, SK falling edge
M_CON	0xAA	Set Microwire clock speed, edge and level
MEN1n	0xA4	Reset pin LE to 0
MEN1	0xA5	Set pin LE to 1
R_LD0	0x80	Set DCF group 0
R_LDH0	0x81	Set marked bits in DCF group 0
R_LDL0	0x82	Clear marked bits in DCF group 0
R_LD1	0x84	Set DCF group 1
R_LDH1	0x85	Set marked bits in DCF group 1
R_LDL1	0x86	Clear marked bits in DCF group 1
R_LD2	0x88	Set DCF group 2
R_LDH2	0x89	Set marked bits in DCF group 2
R_LDL2	0x8A	Clear marked bits in DCF group 2
U_INT0 U_INT1 U_INT2 U_INT3	0x61, 0x6B, 0x6D, 0x6F	Generate interrupt to CR16Cplus
U_PSC	0x60	Set CR16Cplus SCK prescaler to 16
U_VINT <x>	0x63	Generate Vectored interrupt x=1-0xF
U_VNMI <x>	0x4C	Generate Vectored NMI x=1-0xF
PAG_ON	0x18	Disable Codec clocks and DIP RAM access
PAG_OFF	0x19	Enable Codec clocks and DIP RAM access

Table 10: DIP Commands overview (Continued)

Command	OPCODE	Description
B_NIC	0x9F	Used in conjunction with full slot protected B field commands. This opcode disables the intermediate CRC calculations and transmit resp receive full slot protected B field with only 1X16 bit CRC at the end
JMPF	0x12	JuMP Far to bank 1 of DiP sequencer RAM
RTNF	0x14	ReTurN Far to bank 0 of DiP sequencer RAM
BR_B0	0x10	BRanch to bank 0 of DiP sequencer RAM
BR_B1	0x11	BRanch to bank 1 of DiP sequencer RAM

For more detailed information see ***AN-D-140, "SC14480 Dedicated Instruction Processor"*** .

8.0 MICROWIRE™ interface

The MICROWIRE is a flexible bidirectional serial interface that allows unlimited data transfer between DIP and RF control unit at four different data rates.

The MICROWIRE is mainly used to configure the on-chip RF Dynamic Control Functions (DCFs) (Refer to Section 9.6.2) via the RF control unit with the same DIP software as used for the LMX4180. The alternative way of dynamically controlling the RF blocks is directly via DIP instructions <R_LDx>, <R_LDHx> <R_LDLx> and the CR16Cplus. This is explained in chapter "Transceiver Control Interface" on page 44.

The RF static registers can also be accessed via the APB bus interface. (see Figure 21). The APB bus has priority over Microwire Interface access to the RF registers.

This means that if a Microwire Write (M_WR) or Microwire Read (M_RD) is in progress, the CR16, SDI or DMA may NOT access the RF registers otherwise Microwire access may fail. See also Section 26.0

For SW evaluation purposes the internal MICROWIRE signals and TDOD and RDI can be observed in the **monitor mode** set by setting P1_MODE_REG[RF_BB_MODE] = 01.

An external Radio Transceiver can also directly be controlled by the MICROWIRE in the **external RF mode** by setting P1_MODE_REG[RF_BB_MODE]=10.

Table 11 shows the MICROWIRE and baseband signals and their directions.

Table 11: MICROWIRE and Baseband interface switching

Mode\ Signal	Port pins	Monitor mode	External RF mode	Description
LE	P1[1]	Output	Output	MICROWIRE Load enable active high
SK	P1[2]	Output	Output	MICROWIRE clock with programmable edges and levels.
SIO	P1[3]	Output (RF and BB data)	Input / Output	MICROWIRE data in-output, reset value 3-state, with weak pull-down resistor. The pulldown resistor is automatically switched off if the output is driving.
TDOD	P1[4]	Output	Output	Transmitted Digital Baseband data (external filter required in external RF mode)
RDI	P1[5]	Output	Input	Received Digital Baseband data

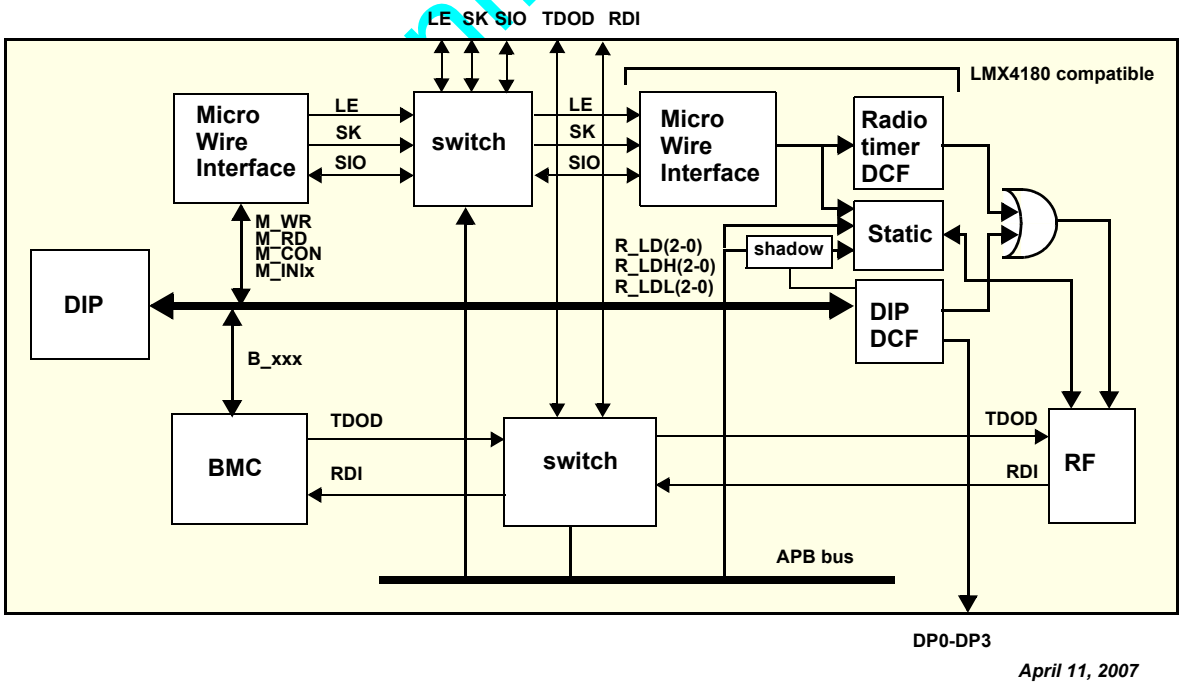


Figure 21 MICROWIRE and baseband interface

8.1 MICROWIRE INTERFACE AT THE BASEBAND SIDE

Table 12: MICROWIRE instruction overview

Instruction	Parameter	Description	
M_INI0	00_{16}	Sets SIO, SK start/end level to 0. SIO data clocked out on rising edge of SK.	
M_INI1	00_{16}	Sets SIO, SK start/end level to 1. SIO data clocked out on rising edge of SK.	
M_WR	<offset> (00_{16}-FF_{16})	SIO is switched to output and the serial clock SK is activated automatically. First the MSB is clocked out on rising edge of SK. (Active edge is programmable, see <M_CON> instruction)	
M_RD	<offset> (0016-FF16)	SIO is switched to input and the serial clock SK is activated automatically. First the MSB is clocked in on falling edge of SK. (Active edge is programmable, see <M_CON> instruction) <M_RD> may also be given before <M_WR>.	
M_RST	00_{16}	Stop <M_WR> and <M_RD> instructions. SIO returns to end level and SK active edge remains unchanged as set by <M_INI0>/<M_INI1>/<MCON> instructions or get default values if none of these instructions were given.	
MEN1	00_{16}	Sets LE pin to 1.	
MEN1n	00_{16}	Sets LE pin to 0.	
M_CON	**Operand Bit**	**Description**	**Reset (Note 13)**
	7-5		0
	4	0 = Bits 3 and 2 disabled 1 = Bits 3 and 2 enabled	0
	3	0 = Sets SIO Start/end level to '0' 1 = Sets SIO Start/end level to '1'	0
	2	0 = SIO data clocked in/out on falling edge of SK. 1 = SIO data clocked in/out on rising edge of SK.	0
	1-0	**Average (Max) Frequency on SK (Note 12)** 00 = 1.152 MHz (default) 01 = 2.3 MHz 10 = 4.6 MHz 11 = 10.368MHz	0

Note 12: SK = 10.368MHz / divider factor. Therefore SK duty cycle varies depending on the divider factor. If divider factor is a whole number then maximum frequency is valid (SK duty cycle is 50%). Otherwise the average frequency will decrease (SK duty cycle is unequal to 50%). For detailed information refer to the SK timing diagrams

Note 13: Reset if DIP_CTRL_REG[URST] = 1. Also <M_INI0> and <M_INI1> are reset: SIO returns to input, pull-down enabled, SIO changes on falling edge of SK.

The MICROWIRE is completely reset if DIP_CTRL_REG[URST] =1. After reset, data on SIO is clocked in and out on the falling edge of SK. LE changes on the DIP bus clock TCK.

Table 12 shows the complete MICROWIRE instruction set. The instructions <M_INI0> and <M_INI1> can be used to set the active edge of SK different to the hardware reset value and the initial/final polarity of the SK and SIO outputs.

When a DIP instruction <M_WR> is used the SIO is switched to output to transfer data from data memory towards RF. In order to transfer data from the RF towards data memory, SIO can be switched to input using a <M_RD> instruction. The offset field within the <M_WR> and <M_RD> instructions denotes the data RAM address.

The data rate in both directions is programmable with the <M_CON> instruction. The parameter field of the <M_CON> instruction refers to the speed (data-rate) of the transfer. Note that the <M_CON> instruction may not be changed during the data transfer.

The data transfers are stopped when the <M_RST> instruction is used. Note that <M_RST> does not affect the end levels of SK and SIO as set by <M_INI0>/<M_INI1>.

The <MEN1> instruction sets the LE pin to 1. This value stays unchanged until the <MEN1n> instruction is executed, which sets the pin to 0. Note that after hardware reset the LE pin is set to 0.

Figure 22 shows a typical MICROWIRE timing with associated instructions. Transfer of data from RF towards data memory starts with the execution of the <M_WR> instruction that instructs the RF to transmit data towards the MICROWIRE. As soon as a <M_RD> instruction is given, the SIO is switched to input. The moment at which the <M_RD> is given depends on the used RF device and can be timed by adding other instructions like the <WT> instruction in this example. In this case the data is clocked out by RF on rising edge of SK and will be clocked in by the MICROWIRE on falling edge of SK.

In case of a sequence with <M_INI0> and <M_INI1> instructions the data is clocked out by RF on falling edge of SK and will be clocked in by MICROWIRE on rising edge of SK.

Instead of using <M_INI0> and <M_INI1>, <M_CON> <PAR> bits 4,3,2 may also be used to set the active edge of SK and start/end level of the SIO signal. If bit 4 is kept to '0', bits 2 and 3 have not effect.

<M_INI0> or <M_INI1> can be used in combination with <M_CON>. As soon as <M_CON> <PAR> bit 4 is set however, bits 3 and 2 determine active edge and level. Note that if bit 4 is reset again, the MICROWIRE reset state (SIO input, pull-down enabled) is active if no <M_INI0> or <M_INI1> were used.

The <M_CON> <PAR> bits may not be changed if the MICROWIRE is active, so changing parameters may only be changed before <M_WR> and <M_RD> instructions or after the <M_RST>.

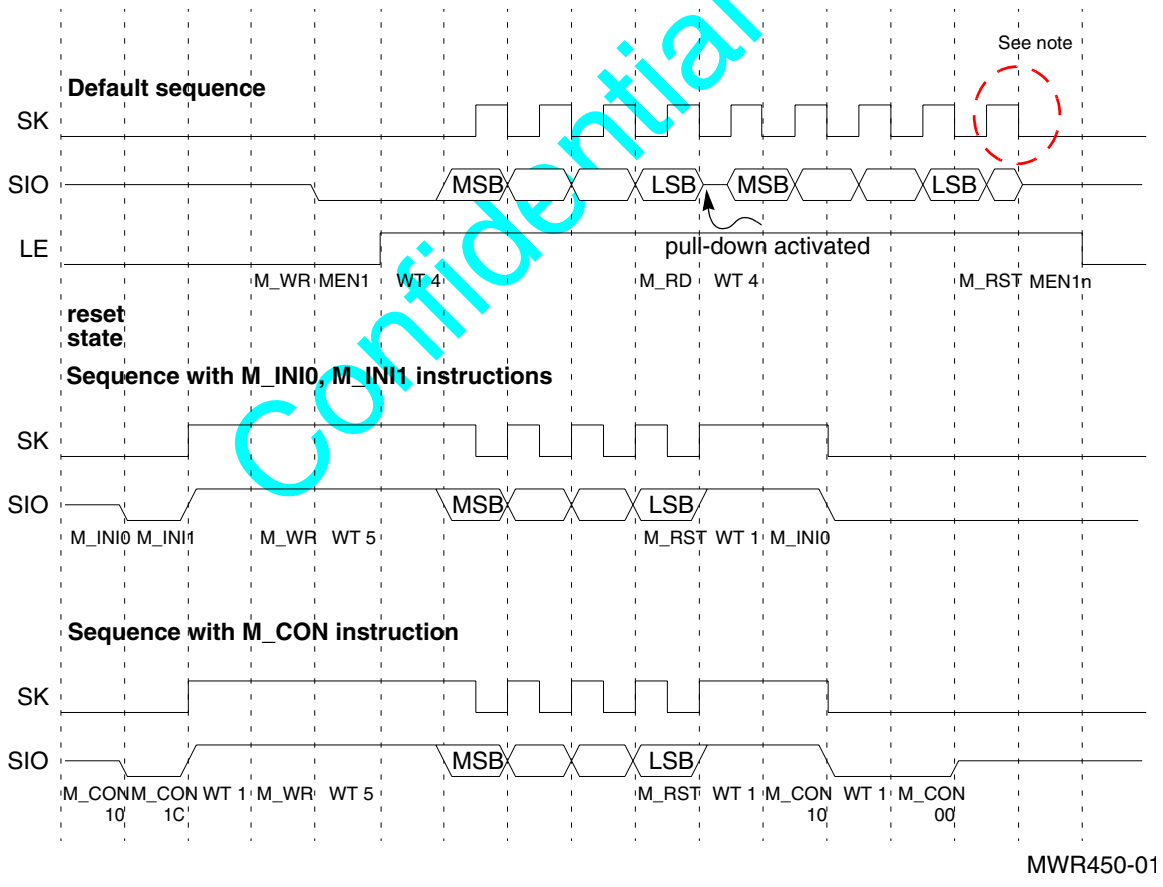


Figure 22 Typical MICROWIRE timing diagrams with 1.152 Mhz SK selection

Note 14: One or more clock pulse are active after the LSB is clocked in with <M_RD> instruction. The number of extra clock pulses depends on the selected SK frequency and the execution timeslot of the <M_RST> instruction. Refer to *AN-D-140 "SC14480 Dedicated Instruction processor* "for application examples and an overview of the extra number of cycles.

8.2 MICROWIRE INTERFACE AT RF SIDE

A Microwire transaction consists of 24 bits (or 8 bits, see Section 9.7):

- The first bit (RW) discriminates between a read (RW = 1) and a write (RW = 0) operation.
- The next 7 bits (A6 to A0) are the address bits A[6:0].
- The final 16 bits (D15 to D0) are the data bits D[15:0].
- The three wires of the interface are:
- LE: latch enable. This is an input to the SC14480A5M, SC14480A2M6. All serial communication with the device is enabled only when this pin is high. When writing, the transferred information is decoded and stored into one of the on-chip registers on the falling edge of LE (no other clock is necessary to be active).
- SK: serial clock. This input controls the bit transfer rate. On the rising edge of SK, incoming serial data is clocked into the Microwire shift register. This signal has only effect when LE is high.
- SIO: data in/data out. This signal carries the bits transferred.

The timing of a write operation is shown in Figure 23 while the diagram for a read operation is given in Figure 24. Note that the read operation has half a clock cycle shift for the data bits.

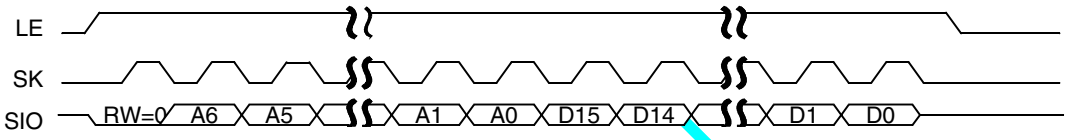


Figure 23 Microwire write timing.

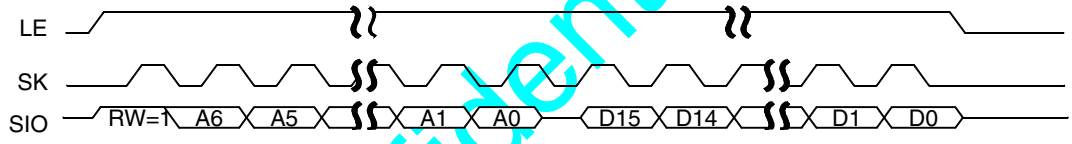


Figure 24 Microwire read timing.

9.0 Radio transceiver

The SC14480A5M, SC14480A2M6 has a complete DECT radio transceiver integrated that is designed to perform the complete receive function in a DECT receiver without requiring an external SAW filter at IF. Furthermore, the device includes a fully integrated fractional-N PLL used for both transmit and receive functions. The device is designed to operate the frequency synthesizer in a closed loop fashion in both transmit and receive mode.

The operation of radio transceiver can be divided into three distinct tasks:

- Set-up of the desired functionality,
- Locking the frequency synthesizer, and
- Performing the desired transmit or receive function.

All functions are controlled by programming the transceiver control interface of the device.

Before transmission or reception of a data slot, the frequency synthesizer is locked to the desired frequency. When locked, the transmit or receive functions are switched on automatically at a predefined (user-configured) time.

During transmit mode, a data signal is provided by a burst mode controller. The PA driver provides the signal to an off-chip matching circuit.

During receive mode, the signal at the Rx input is downconverted to an intermediate frequency (IF = f_XTAL/12) of 864kHz. At IF, blocking signals and noise are attenuated and the wanted signal is amplified to a sufficient level using an AGC amplifier. Thereafter the signal is demodulated, and the data signal is recreated, along with a received signal strength indication (RSSI) signal.

Features:

- Highly integrated 1.9GHz low-IF CMOS transceiver
- Down conversion to half the DECT channel spacing (864 kHz)
- On-chip channel select filter
- On-chip voltage controlled oscillator (VCO)
- On-chip low noise amplifier (LNA)
- Closed-loop modulation
- < 70 μs PLL lock time
- On-chip timing control
- Six digital output ports (including two for fast antenna diversity switching)
- 2 dBm PA driver RF output
- -96 dBm receiver sensitivity

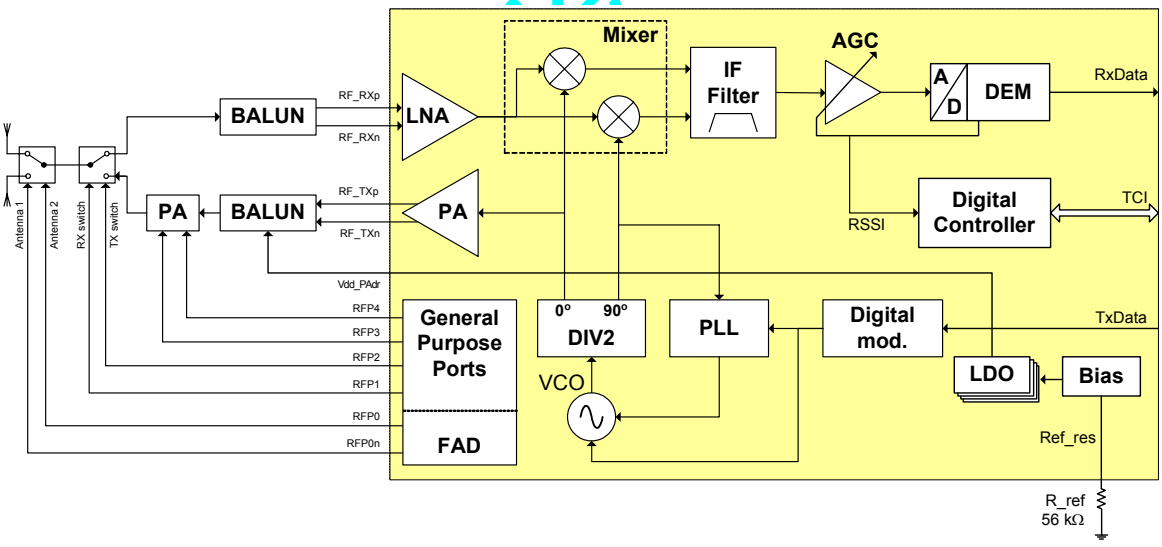


Figure 25 Radio Transceiver Block Diagram

9.1 FREQUENCY SYNTHESIZER

The fractional-N frequency synthesizer embodies an automatic VCO calibration and tuning mechanism. The VCO Calibration can be performed on a slot to slot basis, preceding phase lock. It is also possible to perform VCO calibration beforehand and providing the calibration information along with the desired channel.

9.1.1 PLL

The fractional-N synthesizer is implemented using a multi-modulus prescaler, a tri-state phase-frequency detector a high performance active loop filter and digital control circuitry. For convenience (refer to the Block Diagram) these blocks are indicated with the term *PLL*. The complete loop including the VCO, frequency divider and loop filter is indicated with the term *synthe-*

sizer.

9.1.2 VCO

The VCO is fully integrated and operates at twice the required frequency. An automatic calibration mechanism is implemented to compensate fabrication tolerances. The VCO is powered by an internally regulated supply.

9.1.3 Frequency Divider

A frequency divider (DIV2) is implemented to allow the VCO to run at a different frequency than the incoming/outgoing RF signal frequency and hence prevent load pulling due to activation of the external PA. In receive mode it provides the I/Q generation of the LO signal that is used in the quadrature down converter.

9.2 RADIO TRANSMITTER

Transmission is accomplished by closed-loop modulation. The frequency deviation can be programmed in software. The modulated output frequency of the VCO is divided by 2 in order to down convert to the required transmit frequency. The PA driver is enabled just before the transmit slot becomes active, providing the necessary isolation for a good transmit mask.

9.2.1 PA driver

The RF transmit output is differential and typically connected to the antenna via a power amplifier (PA) and a Tx/Rx switch. The PA driver provides a suitable output level to drive external PA circuitry. Its output matching circuit needs a DC bias point that is provided by Vdd_PAdr. Note that this pin is an output.

9.3 RADIO RECEIVER

The receiver consists of an LNA and a quadrature downconversion mixer converting the desired channel to IF. At IF the signal is filtered and an automatic gain control (AGC) circuit adjusts the gain to allow the full dynamic range of the receiver to be utilized. After the amplification, the signal is converted to the digital domain and is demodulated.

9.3.1 LNA

The on board LNA is a fully differential structure integrated with the mixer providing low noise performance and good immunity from blocking signals.

9.3.2 Mixer

The quadrature down converter is an image reject type mixer.

9.3.3 Polyphase Filter

The polyphase filter provides the required channel selectivity and recombines the quadrature signal to a single differential output. It also serves as an anti-aliasing filter for the ADC which is part of the demodulator.

9.3.4 IF Amplifier

The gain controlled IF amplifier automatically adapts the wanted signal to the maximum input range of the demodulator.

9.3.5 AGC

A digitally realized automatic gain control is implemented as part of the demodulator to adjust the gain of the IF amplifiers.

9.3.6 Demodulator

The demodulator consists of an ADC and digital circuitry. Digital signal processing is used to extract the phase from the IF signal. The derivative of the phase over one symbol results in the demodulated data symbol. Automatic frequency control is used to maintain good sensitivity for IF frequency offsets up to ±100kHz.

9.4 DIGITAL CONTROLLER

A digital controller is provided to operate the chip by timed control sequences, so called dynamic control functions (DCFs, see Section 9.6.2). The set and reset times of DCFs will be defined by programming register banks. Two groups of control sequences can be defined. One for the receive mode and one for the transmit mode of the chip. By use of a control word, the chip is brought into either the receive or the transmit mode. Dependent on the selected mode of operation, one of the two groups of control sequences is started.

9.5 DIGITAL OUTPUT PORTS

Four logic output ports are available for general switching purposes. The signals provided at the ports can be used to control a Tx/Rx switch and/or the external PA. The logic level and the relative timing of the logic signals at the ports can be programmed. Any of these four ports can be used for setting the power level of an external PA.

Two additional ports (RFP0 and RFP0n) are meant for fast antenna diversity (FAD) switching. The FAD functionality is implemented on-chip.

9.6 TRANSCEIVER CONTROL INTERFACE

The transceiver register set can be accessed directly via the APB interface as well as through the MicroWire transceiver control interface. (See Section 8.0)

The APB bus has priority over Microwire Interface access to the RF registers.

This means that if a Microwire Write (M_WR) or Microwire Read (M_RD) is in progress, the CR16, SDI or DMA may NOT access the RF registers otherwise Microwire access may fail. See also Section 26.0

SC14480A5M and A2M6 have no clock gating in the RFCU (see clock diagram). In other SC1448x device the RFCU is clock gated. If the FLASH device is used as development version for SC1448x devices, (e.g. SC14480A2L) the <RFEN> must be set before:

- Before any RX or TX slot is start in the

RF_BURST_MODE_CTRL_REG (paragraph 9.6.1)

- Any RF_ALW_EN_REG bit is set. (paragraph 9.6.3)
- Before any calibration (See also AN-D-136 V1.4) and RF LDO precharge.(paragraph 9.6.7

The transceiver control interface is controlled with the DIP instructions M_RD (read), M_WR (write) and M_RST. A transceiver control interface transaction consists of 24 bits (or 8 bits, see Section 9.6.1):

- The first bit (RW) discriminates between a read (M_RD: RW = 1) and a write (M_WR: RW = 0) operation.
- The next 7 bits (A6 to A0) are the offset address bits A[6:0].
- The final 16 bits (D15 to D0) are the data bits D[15:0].

9.6.1 Burst-Mode Control WORD

Writing to the special 18-bit register RF_BURST_MODE_CTRL_REG initiates most of the activities related to processing a TX or RX slot. In particular, the dynamic control functions (DCFs), the behavior of which can be configured in advance by static register settings (see Section 9.6.2) are activated by means of a single transceiver control interface transaction.

RF_BURST_MODE_CTRL_REG is also called burst-mode control word (BMCW) for historical reasons.

For the BMCW, the information in A[1:0] should be interpreted as the data symbol RX_TX:

- RX_TX = 1: 'transmit'; the transceiver will initiate the processing of a "TX slot" and activate those blocks associated with transmitting according to a programmable sequence.
- RX_TX = 2: 'receive'; the transceiver will initiate the processing of an "RX slot" and activate those blocks associated with receiving according to a programmable sequence.
- RX_TX = 3: 'general calibration'; an autonomous calibration procedure is executed in the hardware (see Section 9.8).
- RX_TX = 0, all blocks that have been activated by a DCF are switched off. This is known as the stop-word.

A BMCW transfer may consist of 8 bits only (M_RST is executed after 8 bits are transferred rather than 24 bits). If 24 bits are sent, the data bits contain various settings that are likely to change from slot to slot (See RF_BURST_MODE_CTRL_REG).

9.6.2 Dynamic Control Functions

The processing of a burst, i.e. a receive (RX) or transmit (TX) slot, is characterized by a sequence of activations and deactivations of transceiver blocks that obey a specific timing at the resolution of one DECT symbol. The waveform that indicates the moment of activation and deactivation for one block, is called that block's *dynamic control function* (DCF).

A collection of counters have been implemented to realize the DCFs. These counters are called the *radio timers*. The mechanism is explained in detail in the next section.

The SC14480 also has dedicated DIP instructions to generate DCFs. They are explained in Section 9.6.5.

9.6.3 DCF Generation with Radio Timers

When the transceiver needs to process a transmit or receive slot, various blocks on the SC14480A5M, SC14480A2M6 will be activated in some specific order according to programmable timing settings. The settings related to one block define the block's dynamic control function (DCF).

A DCF is characterized by a time instant when activation starts and an instant when activation terminates. These instants are specified relative to seven so-called switch instants (SIs). They are listed in Table 13. Each of them, except SO_SLOT which is fixed to time 0, can be programmed with a value between 0 and 1984 DECT bit periods, in multiples of 8. The values are programmed in the registers RF_PORT_RSSI_SI_REG, RF_TX_SI_REG and RF_RX_SI_REG. The values are programmed as the actual switch instant in DECT bit periods divided by 8 (= 8 most significant bits). The offsets from the SIs can be specified using a granularity of a single DECT bit period within a range of 0 to 63.

Table 13: List of switch instants

switch instant	description
SO_SLOT	start of slot (fixed at time 0)
SO_PORT	start of port (programmable)
EO_RSSI	end of RSSI measurement (programmable)
SO_TX	start of transmit (programmable)
SO_RX	start of receive (programmable)
EO_TX	end of transmit (programmable)
EO_RX	end of receive (programmable)

The SIs with respect to which the programmable set and reset times are specified, are hard wired. In addition, the control of activation by either TX, RX or either of the two is hard wired as well. For each DCF <B>, there is a register RF_<B>_DCF_REG. The DCFs and their associated SIs are listed in Table 3. The registers have the following fields (port DCFs are slightly different and are discussed later on):

- SET_OFFSET: limited-range offset in DECT bit periods for the start time of the DCF measured from start SI.
- RESET_OFFSET: limited-range offset in DECT bit periods for the stop time of the DCF measured from stop SI.
- DIS: disable block activation.

In addition, a bit called ALW_EN is associated with each block controlled by a DCF. Setting this bit to '1' activates the block irrespective of any other condition that causes the activation or deactivation of the DCF. All ALW_EN bits of the SC14480A5M, SC14480A2M6 have been collected in a single register called RF_ALW_EN_REG such that any combination of blocks or ports can be turned on or off with a single transceiver control interface transaction. The timing of DCFs is illustrated in Figure 26.

Table 14: List of DCFs

DCF	description	controlled by	start SI	stop SI
PADR	power-amplifier driver	TX or TRX[15)16)]	SO_TRX[17)], SO_PORT[18)] or SO_SLOT[19)]	EO_TRX[21)]
LNAMIX	low-noise amplifier and mixer	RX	SO_RX or SO_SLOT[20)]	EO_RX
IF	intermediate-frequency filter	RX	SO_RX or SO_SLOT[20)]	EO_RX
ADC	analog-to-digital converter	RX	SO_RX or SO_SLOT[20)]	EO_RX
DEM	demodulator	RX	SO_RX or SO_SLOT[20)]	EO_RX
RSSIPH	RSSI peak-hold computation[22)]	RX	SO_DEM[23)]	EO_RSSI or EO_RX[25)]
BIAS	bias circuit	TRX	SO_SLOT	EO_TRX
SYNTH	synthesizer	TRX	SO_SLOT	EO_TRX
PLLCLOSED	PLL closed loop	TRX	SO_SLOT	EO_TRX or SO_TRX[20)]
PORT1 PORT2 PORT3 PORT4	general-purpose output ports	TX, RX or TRX[26)]	SO_TRX, SO_PORT[27)]or SO_SLOT[28)]	EO_TRX
FAD_WINDOW	fast antenna diversity window	RX	SO_DEM	SO_DEM

Note 15: TRX is the Boolean OR of TX and RX.
Note 16: PADR is sensitive to both TX and RX when RF_BURST_MODE_CTRL_REG[RX_SENSITIVE] = '1'.
Note 17: SO_TRX means SO_TX when in a TX slot and SO_RX when in an RX slot.
Note 18: The start SI becomes SO_PORT when RF_PADR_DCF_REG[PADR_SSI] = '1'.
Note 19: The start SI becomes SO_SLOT when RF_PADR_DCF_REG[PADR_SSI] = '2' or '3'
Note 20: The start SI becomes SO_SLOT when RF_*xxx*_DCF_REG[SSI] = '1'
Note 21: EO_TRX means EO_TX when in a TX slot and EO_RX when in an RX slot.
Note 22: While the RSSIPH_DCF and the DEM_DCF are active, reading the RF_RSSI_REG[RSSI_VAL] resets peak-hold computation.
Note 23: SO_DEM is the absolute time instant where the demodulator is started: SO_RX + RF_DEM_DCF_REG[SET_OFFSET].
Note 24: The stop SI becomes SO_TRX when RF_PLLCLOSED_DCF_REG[SSI] = '1'
Note 25: The stop SI becomes EO_RX when RF_BURST_MODE_CTRL_REG[RSSI_PA_MODE] = '1'.
Note 26: The sensitivity of the ports for either TX, RX or both is programmable with RF_PORTx_DCF_REG[EN_BY_TX | EN_BY_RX].
Note 27: The start SI becomes SO_PORT when RF_PORT_CTRL_REG[SSI] = '1'.
Note 28: The start SI becomes SO_SLOT in a TX slot, when RF_BURST_MODE_CTRL_REG[RSSI_PA_MODE] = 1 and RF_PORT_CTRL_REG[PA_PS] = '1'.

All times (in DECT symbol periods) are counted with respect to a moment $T_{start} + \Delta T_{start}$, where T_{start} is the moment when a TX or RX setting in the BMCW was received and ΔT_{start} is a delay related to the processing of the BMCW. There exists also a delay ΔT_{alw_en} from the moment of receiving RF_ALW_EN_REG until it results in activation or deactivation of a block (not shown in the figure).

Port DCFs have four control bits instead of the DIS bit:

- EN_BY_TX: 'enable by transmit'; when '1', the port is activated in a TX slot'; the offsets are taken with respect to a progammable Start SI and EO_TX.
- EN_BY_RX: 'enable by receive'; when '1', the port is activated in an RX slot; the offsets are taken with

respect to a progammable Start SI and EO_RX.

- SSI: ‘select the Start SI’; when ‘0’, the port is activated relative to SO_TRX, when ‘1’, relative to SO_PORT.
- PA_PS: ‘enable activation as PA power control’: When ‘1’, the port is activated relative to SO_SLOT irrespective of SSI and gated with RSSI_PA_MODE in the BMCW. (refer to Section 9.7). In an RX slot, this setting has no effect.

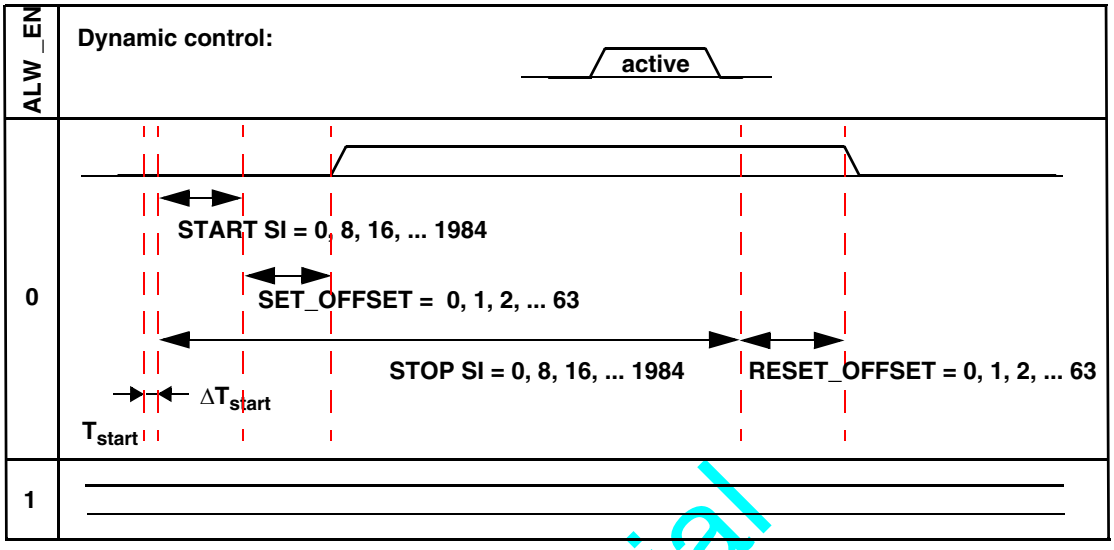


Figure 26 DCF timing

The dynamic control of the PA driver is identical to any other block, with the exception of 2 extra control bits. The function of PADR_SSI is similar to that of the port DCF’s, giving more freedom of the absolute time at which the PA driver switches on. Furthermore, the PA driver can also be activated during a receive slot.

Note that the combination of SIs and offsets allows to control block activation within a range of 0 to 2047 DECT symbol periods at a single symbol resolution. Controlling the blocks by programming RF_ALW_EN_REG allows block activation with an arbitrary duration at a single symbol resolution but with the restriction that two consecutive changes are at least three symbols apart. The two mechanisms can be mixed at wish leading to a very flexible control of block activation.

9.6.4 Re-Triggering and Stop Word

When an 8-bit BMCW is programmed with RX_TX=’1’ or ‘2’, the transceiver will process TX or RX slots without activating the synthesizer. This mode is useful if relatively short slots are to be transmitted or received on the same RF channel with a small guard space in between.

All DCFs that have a start SI = SO_SLOT will retain their values. All DCFs that have a start SI = SO_TRX, will be started relative to SO_SLOT and stopped relative to their own stop SI - SO_TRX.

Effectively, this re-triggers the FAD, active slice and RSSI peak-hold computation for the next receive slot. Otherwise it allows the PA to be temporarily switched off during the guard space between two transmit slots, while leaving the PLL in open loop. Note that the 8-bit BMCW must be programmed before the end of the initial slot, such that the synthesizer blocks are in the correct setting for endured operation.

9.6.5 DCF Generation with DIP Instructions

Integration of the RFIC and BBIC has made it possible to control DCFs directly from the DIP. The DIP instruction set of the SC14480 has been extended with the following 9 commands for this purpose.

- R_LD*x*, with *x*=0, 1, or 2;
- R_LDH*x*, with *x*=0, 1, or 2;
- R_LDL*x*, with *x*=0, 1, or 2;

x identifies a DCF group of potentially 8 members per group, where the maximum of 8 is a direct consequence of the fact that a DIP command can be accompanied by an 8-bit parameter field.

The division of DCFs across the 3 groups, as specified in Table 15. Note that some DCFs (SO_SLOT, MODCAL, DP0 to DP3) can only be controlled by DIP commands. They do not exist in the LMX4180 and no provisions have been taken to implement them with the radio timers. The SO_SLOT DCF is a special DCF that indicates the start of a slot. This trigger is used by the shadowing mechanism discussed in Section 9.6.6.

Table 15: DCFs parameter positions in R_LD(H/L)*x* commands

Bit	<R_LD0> <R_LDH0> <R_LDL0>	<R_LD1> <R_LDH1> <R_LDL1>	<R_LD2> <R_LDH2> <R_LDL2>
7	DP0	DP3	DP1
6	-	DP2	-
5	-	-	RSSIPH
4	MODCAL	PORT4	FAD_WINDOW
3	PLLCLOSED	PORT3	DEM
2	SYNTH	PORT2	ADC
1	BIAS_DCF	PORT1	IF
0	SO_SLOT	PADR	LNAMIX

The R_LD*x* command will turn on a DCF when its corresponding bit in the DIP parameter is 1 and will turn off the DCF when the bit is 0. The R_LDH*x* command will turn on the DCFs corresponding to 1s in the parameter and will leave the other DCFs as is. The R_LDL*x* command does the opposite and turns off the DCFs for which the bit in the parameter is 1 and leaves the others untouched.

A special situation occurs when the parameter for either the R_LDH*x* or R_LDL*x* is zero. This would imply that nothing happens. Instead, the value of "load pointer 2" is used as parameter for these commands.

Here are a few examples of the R_LD-family DIP commands:

- `R_LD1 0x12` (turn on PORT4 and PORT1; turn off all other DCFs in Group 1; 0x12 is "0001 0010 in binary; the pattern selects bit positions 4 and 1).
- `R_LDH2 0x02` (turn on IF; leave all other DCFs in Group 2 unchanged).
- `LD_PTR2 0x08; R_LDH0 0x00` (assign value 0x08 to load pointer 2; turn off PLLCLOSED DCF while leaving all other DCFs in Group 0 unchanged).

Where DCF programming based on the radio timers needs to obey all kind of restrictions with respect to e.g. SIs to which a DCF is related, DIP-based DCFs can be programmed with much more freedom. Any DCF can be turned on or off anytime with the restriction that DCFs belonging to different groups cannot be changed within the same DECT symbol period. There should, of course, be neither a conflict with other DIP commands that need to be issued.

The increased flexibility makes it for example possible to turn on and off a DCF multiple times during a slot. Such a programming can be applied during a long RX slot in which the RSSI is measured multiple times in search for interferers by repeatedly turning on and off the RSSIPH DCF (the RSSI value can be read in a synchronized way by means of the B_WRS DIP command).

Note: the actual control of a DCF is the result of ORing the two ways to control DCFs (by means of radio timers or DIP commands).

To aid debugging, the SC14480 has a mechanism to map DCFs on the externally available signals DP0 to DP3, irrespective of the way the DCFs have been generated. One needs to appropriately program register RF_DCF_MONITOR_REG for this purpose.

9.6.6 Shadowed Register Fields

The SC14480 has a so-called *shadowed registers* to be able to change parameters for the next slot while the current slot is still active. Parameter values that are likely to change from slot to slot are stored in two locations. The location to which a user writes is called the *shadow* register. The value at that location is not directly used. Instead, at the start of a slot, the shadow value is copied to a new location called the *foreground* register. The foreground value is used for slot processing while the shadow register becomes directly available for rewrite. This concept is illustrated in Figure 27.

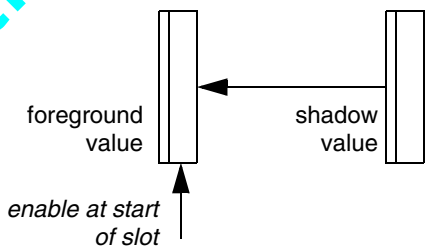


Figure 27 The principle of shadow registers.

The start of a slot is indicated in either of the two ways:

- Writing the RF_BURST_MODE_CTRL_REG at address 0x1 or 0x2 of the Microwire memory space (see Section 9.6.1).
- Turning on SO_SLOT with the R_LD family of DIP commands (see Section 9.6.4).

There are actually two register fields that have been implemented using the scheme of Figure 27:

- RF_TX_SI_REG[EO_TX_VAL]
- RF_RX_SI_REG[EO_RX_VAL]

Fields in RF_BURST_MODE_CTRL_REG are also shadowed, but following a slightly more complex mechanism. This is due to the fact that writing this register triggers the start or end of a slot. Therefore, the fields of this register have an alternative location where shadow values can be written. They are located in RF_BURST_MODE_SHADOW1_REG and RF_BURST_MODE_SHADOW2_REG.

When bit RF_BURST_MODE_SHADOW2_REG[SHADOW_EN] has value 1, the alternative values for the fields in RF_BURST_MODE_CTRL_REG are used according to the mechanism depicted in Figure 28. The mechanism applies to all fields:

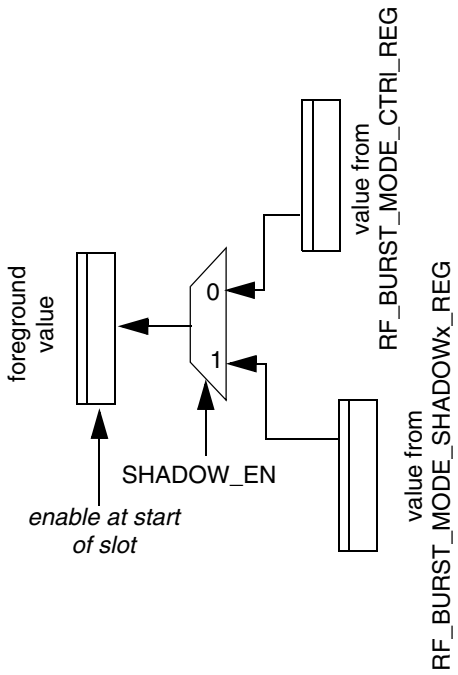


Figure 28 Shadowing for fields in RF_BURST_MODE_CTRL_REG.

- CN, with alternative value CN_SHW. Note that CN_SHW has 8 bits whereas CN has 7. The foreground value has 8 bits. Its MSB is zero when SHADOW_EN is 0.
- RFCAL, with alternative value RFCAL_SHW.
- RSSI_PA_MODE, with alternative value RSSI_PA_MODE_SHW.
- FAD, with alternative value FAD_SHW.

The fields RX_ASSERT and TX_ASSERT in RF_BURST_MODE_SHADOW2_REG are only meaningful when the R_LD family of DIP commands are used. During the period that the SO_SLOT DCF is active, they indicate whether the slot should be designated as receive or transmit slot. The value of RX_ASSERT or TX_ASSERT prior to the rising edge of the SO_SLOT DCF determines the type of slot. After the rising edge the values can be overwritten to indicate the situation in the next slot.

The correct programming of RX_ASSERT and TX_ASSERT matters in the following situations:

- The correct channel selection by the synthesizer (receive channel is offset by IF w.r.t. the transmit channel).
- The correct functioning of the antenna selection (including FAD) when two antennas are used (see Section 9.11).

Even when the Microwire is used for burst-mode control, shadowing makes it possible to shorten the activity in the guard space. One can program all settings for the next slot before the end of the previous slot in RF_BURST_MODE_SHADOW1_REG and RF_BURST_MODE_SHADOW2_REG (with SHADOW_EN = 1). Then, an 8-bit write instead of 24-bit write to address 0x1 or 0x2 is sufficient to start the next slot with the correct parameters.

9.6.7 LDO Refresh

The LDOs that control the power supplies in the transceiver need to be refreshed regularly, from slot to slot. This is taken care of automatically based on the value of the BIAS_DCF, both when radio-timer or DIP DCFs are used. The minimum refresh time is 4 symbols as shown in Figure 29.

When starting the **radio DCFs** via the MicroWire RF_BURST_MODE_CTRL_REG, the refresh takes automatically place when BIAS_DCF=0 and a MicroWire transaction (LE=1) takes place. To start the DCFs in time, <RFEN> must be given before <MEN1n> is given, preferably before <MEN1> is given. For a correct refresh, the user should therefore reset (terminate) BIAS_DCF at the end of a slot or force termination by sending the stop word.

When using **DIP DCFs**, refresh takes place when the transceiver has been turned on by means of the RFEN DIP command and BIAS_DCF is inactive. The user should therefore turn off BIAS_DCF between slots to force a refresh. During calibration this timing is applicable. (See AN-D-136).

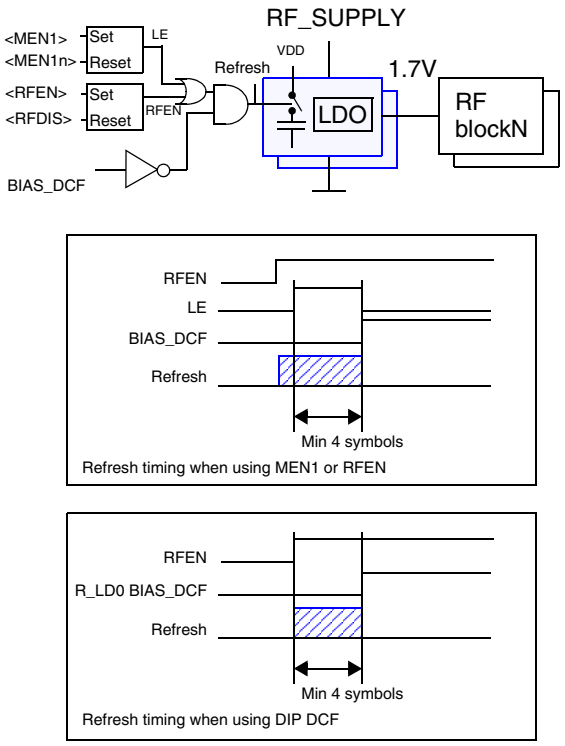


Figure 29 LDO Refresh sequence

9.7 BURST MODE PROGRAMMING

Programming the BMCW will bring the SC14480A5M, SC14480A2M6 in/out receive or transmit mode. It causes the relevant circuit blocks to switch on and off using the predefined DCFs (refer to Section 9.6.2).

This register contains 5 symbols using a total of 18 data bits (at the expense of 2 address bits).

The symbol RX_TX sets the transceiver in RX or TX mode. When the value RX_TX = '3' a general calibration is performed (refer to Section 9.8).

The symbol FAD sets the behavior of the *fast antenna diversity* algorithm (refer to Section 9.11).

The function of RSSI_PA_MODE depends on the mode of operation.

When in RX mode, it defines the behavior of the RSSI computation. The RSSI value is computed constantly during a complete RX slot. Its maximum is available for read after the slot is processed. In some cases it is desirable to measure the maximum of the RSSI during only the first part of a slot. RSSI_PA_MODE = '1' enables the STOP_SI of RSSIPH_DCF to be changed to EO_RSSI instead of EO_RX.

In TX mode, RSSI_PA_MODE can be used to switch an external PA to low power mode, instead of its default high power mode. Any of the ports RFP1 through RFP4 can be used for this purpose. The port is enabled when RSSI_PA_MODE = '1' and disabled when it is '0'. The port is configured for this functionality by setting PA_PS = '1' in register PORT*x*_DCF_REG. Instead of its programmed Start SI, the port will start relative to SO_SLOT, making sure that the port has its value for as long as any of the analog blocks is enabled. The polarity of the ports can be programmed with the symbols PORT*x*_INV in RF_PORT_CTRL_REG.

The symbols RFCAL and CN specify the functionality of the synthesizer.

The desired local oscillator frequency can be programmed with a 7 bit channel number (*CN*) and is given by

$$f_{LO} = [CH0 + SGN(CS \times CN) + RX]f_{IF} \quad (2)$$

In this equation, f_{IF} means the intermediate frequency of 864kHz or more general, f_{IF} is fixed at f_REFCLK/12. All local oscillator frequencies are therefore given as multiples of f_{IF}. The parameters *CH0*, *SGN* and *CS* are multipliers that are constant in a given application. The variables *CN* and *RX* are programmed on a slot to slot basis.

CH0 defines the frequency of channel 0. In the DECT system that is 1897.344MHz, so *CH0* = 2196. The channels in the DECT system count from high to low frequency, so the sign of the additional term is negative (*SGN* = -1). The DECT channel spacing is 1728kHz, so *CS* = 2.

The channel numbers (*CN*) can now simply be programmed between 0 and 9 as defined in the DECT specification. The additional parameter *RX*, the MSB of the RX_TX symbol in the BMCW, is either 1 (in RX mode) or 0 (in TX mode) indicating that the local oscillator frequency is higher than the wanted channel frequency in receive mode.

For the DECT system, the parameters *CH0*, *SGN*, *CS* are given by the reset values, thus need not be programmed. For other applications, these parameters can be redefined at wish. The value of *CN* can vary between 0 and 127 enabling all kinds of applications with up to 128 channels. The channel spacing parameter *CS* can vary from 1 to 4 and the sign can be either positive or negative (*SGN* = -1 or +1).

The parameter *CS* should be changed to 0 for full-rate applications and to 0 for half-rate applications.

Due to the limited frequency range of the integrated VCO, not all possible programming combinations yield valid local oscillator frequencies.

The symbol RFCAL is used for VCO calibration. There are 3 ways in which the synthesizer can start up. The choice is programmed in the symbol RFCAL_MODE in the RF_RFCAL_CTRL_REG. Refer to Section 9.10 for a description of the algorithms.

9.8 GENERAL CALIBRATION PROGRAMMING

There are three ways to start calibration:

- By writing to address 0x3 using the Microwire (setting RX_TX to 3 in the BMCW).
- By writing to APB address 0xFF7006 (which amounts to the same as the above).
- By activating SO_SLOT using the R_LD family of DIP commands while both RX_ASSERT and TX_ASSERT in RF_BURST_MODE_SHADOW2_-REG are set to 1.

The IF filter center frequency and bandwidth, the IF amplifier DC offset voltage, the start value for the VCO calibration and the bandwidth of the internal loop filter are all calibrated sequentially.

The start value for the VCO calibration depends on the selected channel number (CN). The base band IC may perform multiple calibrations sequentially to build a table of start values, or simply choose CN in the center of the frequency band and calibrate only once. Note that although the RX-bit from RX_TX is '1' when RX_TX='3', that during general calibration only the TX channel frequency can be programmed (RX = 0 in Eq. (2)). The channel number used for VCO calibration is either CN or CN_SHW depending on the value of SHADOW_EN.

This general calibration is recommended to be performed once per telephone call. The results are kept in on-chip registers.

Note that during calibration the reference clock must be present, DIP <RFEN> must be executed.

9.9 MODULATION GAIN CALIBRATION PROGRAMMING

The SC14480A5M, SC14480A2M6 features a novel synthesizer architecture enabling closed loop modulation. This has the advantage that the base band TDO output level no longer needs to be trimmed in production. This trimming is replaced by an automatic alignment. This Modulation Gain Calibration is recommended to be performed once per telephone call. It involves a combination of CR16 and DIP code that is described in Sitel Semiconductor Application Note AN-D-136.

9.10 RF CALIBRATION PROGRAMMING

The synthesizer tunes the local oscillator to the desired frequency. It consists of a coarse tuning (RFCAL) and a fine tuning (PLL in closed loop) action. The coarse tuning action is needed to optimize the amount of fixed capacitance in the VCO tank circuit, by means of a binary scaled calibration capacitance (C_{cal} = C_{LSB}×RFCAL_CAP). The coarse tuning range is large to cover all fabrication tolerances. During operation, however, the coarse tuning only uses a limited range around its preset value.

For this reason, the VCO calibration is split up into 2 parts. Initially, during general calibration (Section 9.8), the process tolerances are eliminated and a start value for RFCAL_CAP (CC_{start}) is established.

During normal operation a linear search algorithm optimizes the limited range (CC_δ) to suit the given channel. In the given slot the value for RFCAL_CAP = CC_{start} + CC_δ.

Depending on the application the range of CC_δ can be chosen by varying the number of measurements (RFCAL_STEPS in RF_RFCAL_CTRL_REG) that are performed by the algorithm. For DECT the variation is small and thus 3 steps is default.

Each measurement step can have one of 3 results: correct, too high or too low. The resulting range of CC_δ is thus $[-2^{RFCAL\_STEPS}+1, 2^{RFCAL\_STEPS}-1]$, which turns out as $CC_\delta \in [-7, 7]$ for RFCAL_STEPS = '3', as shown in Figure 30.

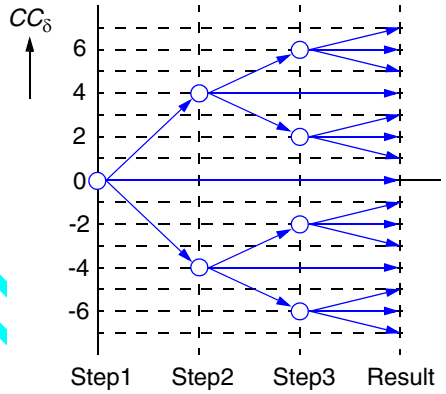


Figure 30 RF Calibration range for 3 steps

Note that the value of RFCAL_CAP can be anywhere in the range [0, 63], but only the range [25, 55] is effective in the VCO. Therefore the value of CC_{start} and the range of CC_δ must be chosen accordingly.

Calibrating only in 3 steps rather than 6 (1 step for every bit in RFCAL_CAP) saves half the time needed for calibration. This allows the PLL to operate in closed loop condition longer and hence more accurate tuning. There are 3 ways in which the calibration can be initiated. This is programed in the symbol RFCAL_MODE in RF_RFCAL_CTRL_REG.

RFCAL_MODE = '0': VCO calibration is omitted altogether, enabling the synthesizer to operate in closed loop for the maximum amount of time. In this case the value of RFCAL from the BMCW is used to preset the VCO. For this mode to work, the base band must keep record of the proper values per channel. These values can be obtained by using one of the other calibration modes first and reading the final value of RFCAL_CAP at the end of the slot from RF_RSSI_REG.

RFCAL_MODE = '1': VCO calibration is performed. The value of CC_{start} is provided by RFCAL in the BMCW. When the base band provides the previous value that was used for the given channel, the number of measurements may be restricted to RFCAL_STEPS = '1'.

RFCAL_MODE = '2': VCO calibration is performed. The previous value of RFCAL_CAP is used for CC_{start}. This value may be derived at a different channel frequency, but only moments earlier. Aging and operating temperature effects are already represented by CC_{start}, and the number of measurements may therefore be restricted to RFCAL_STEPS = '2'.

9.11 FAST ANTENNA DIVERSITY

The SC14480A5M, SC14480A2M6 allows *fast antenna diversity* (FAD), the possibility to select the best of two available antennas. This choice is determined in an RX slot, based on the RSSI information during the (prolonged) preamble. It is described in this section in conjunction with the behavior of the ports RFP0 and RFP0n that are dedicated for switching antennas.

When FAD is to be used, and two antennas are therefore present, the following port connections need to be used:

- RFP1 controls the RX switch
- RFP2 controls the TX switch
- RFP0 controls Antenna 1
- RFP0n controls Antenna 2

There is a special DCF for FAD called FAD_WINDOW (See RF_FAD_WINDOW_DCF_REG). Note that the set and reset offsets are relative to the start instant of the demodulator, rather than SO_RX.

The FAD algorithm is activated when the symbol FAD = '3' and RX_TX = '2' in the BMCW. Initially, Antenna 1 is selected and the RSSI starts to settle. At the switch instant FAD_SWAP, Antenna 2 is selected and a new value for the RSSI becomes available. At the switch instant FAD_DECIDE, the antenna that gave the highest RSSI_VAL is selected and can be read from RF_RSSI_REG as the symbol FAD_CHOICE.

The symbol FAD_CHOICE remains valid, until the next RX slot evaluates it again. When the first slot after evaluation is a TX slot, as is generally true in a hand set, the symbol FAD in the BMCW can be left at '3', and the same antenna is used for this TX slot.

In a base station, the RX slot is usually succeeded by another RX slot, since in DECT all hand sets transmit one after the other in the first half frame and receive one after the other in the second half frame. In this case, each hand set can be identified by its channel number *CN*. In order to use the best antenna for transmitting to a given hand set, the base band IC must record the value of FAD_CHOICE per channel and use it in a TX slot on the same channel ($FAD_{TX,CN}$ = $FAD\_CHOICE_{RX,CN}$). Note that FAD is a 2-bit symbol and FAD_CHOICE is 1-bit.

The combination of control settings leads to the behavior of RFP0 and RFP0n as given in Table 16.

Table 16: FAD and RFP0/RFP0n switching

FAD	RFP0/RFP0n behavior
0	RFP0 follows RFP1 in RX slot and RFP2 in TX slot; RFP0n = ANT_INACTIVE_VAL.
1	RFP0 = ANT_INACTIVE_VAL RFP0n follows RFP1 in RX slot and RFP2 in TX slot.
2	Do not use FAD, RFP0/RFP0n inactive RFP0 = ANT_INACTIVE_VAL; RFP0n = ANT_INACTIVE_VAL.
3	If FAD_CHOICE = '0': RFP0 follows RFP1 in RX slot and RFP2 in TX slot; RFP0n = ANT_INACTIVE_VAL. If FAD_CHOICE = '1': RFP0 = ANT_INACTIVE_VAL RFP0n follows RFP1 in RX slot and RFP2 in TX slot. Note that FAD_CHOICE dynamically changes during an RX slot, resulting in the wanted FAD behavior.

A typical example of the behavior of RFP0 and RFP0n during an RX slot is shown in the timing diagram of Figure 31(a). For all signals, it is assumed that a DCF is high when active (ANT_INACTIVE_VAL = '0' in RF_PORT_CTRL_REG). As can be seen in the figure, the timing of RFP0 and RFP0n is derived from the DCFs of RFP1 and DEM and the preamble delay. Figure 31(b) shows typical behavior in a TX slot where RFP0 and RFP0n only depend on the DCF of RFP2.

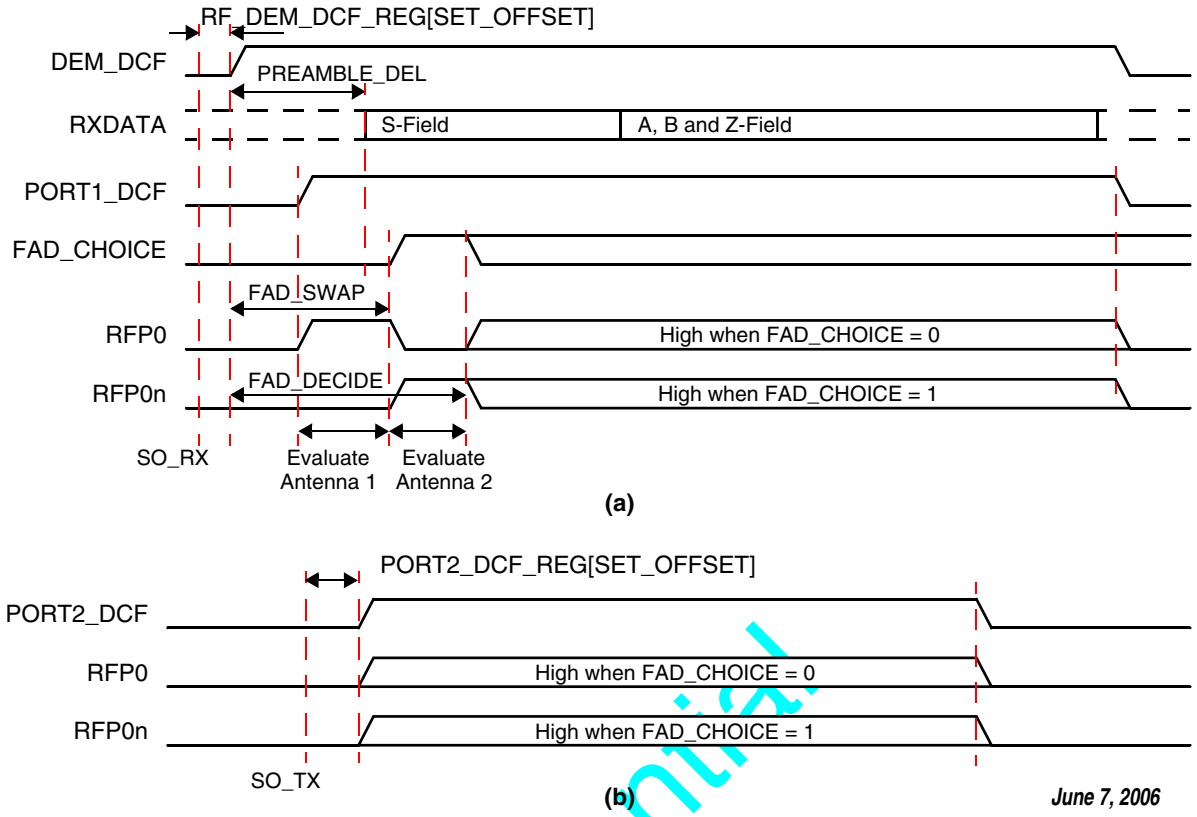


Figure 31 Example of typical timing of RFP0 and RFP0n when performing FAD in an RX slot (a) and a TX slot (b)

10.0 Gen2DSP

The SC14480A5M, SC14480A2M6 has a user programmable Gen2DSP (Generation 2, Generic DSP), for sample and block based algorithms. A fixed set of routines are available in the microcode ROM and a micro code RAM which can execute user defined routines **(Note 29)**. The user defined algorithms can be compiled with a C-compiler/assembler.

The input data as well as the algorithm parameters are stored in the shared RAM.

The Gen2DSP has full zero wait state access to the shared RAM for accessing algorithms parameters.

Features

- Micro code ROM with fixed audio, telecom and voice compression/decompression routines in ROM compatible with SC1443x.
- Micro Code RAM availabe in FLASH version for custom DSP algorithm development.
- Shared parameter RAM for zero wait state access, no wait states due to CR16Cplus/DMA memory access (PLL on), extra wait state for DIP access.
- Parallel transcoding between sample processing (e.g. G.722/G.726) and block processing is possible.
- Interrupt capability e.g. for interrupting block based algorithms.
- Sample rates 8/16 and 32 kHz supporting standard, wide band Codec and Hi-Fi tone generation.
- Programmable clock frequency from up-to 82.944 MHz.

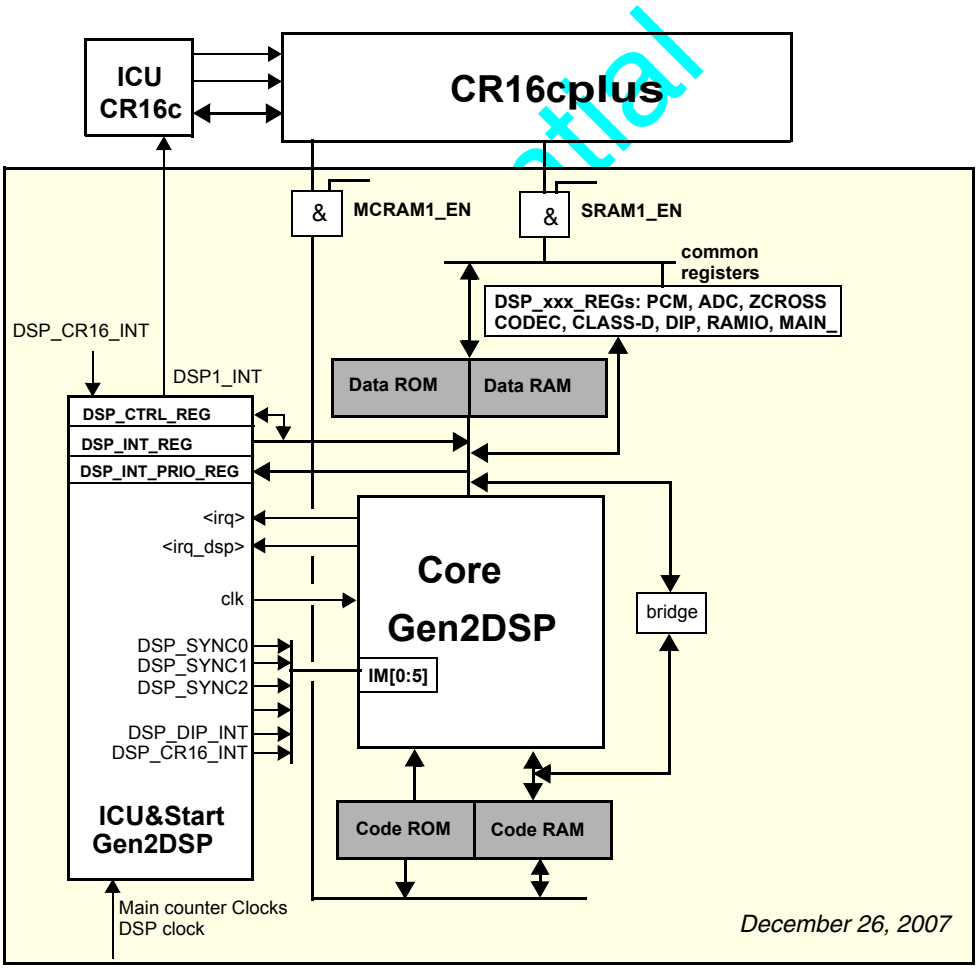


Figure 32 Gen2DSP block diagram

Note 29: The micro RAM is only available on the FLASH version.

Note 30: Shared Data ROM is not available in A2.6M versions, constants must be stored in shared RAM.

10.1 START-UP AND INTERRUPTS

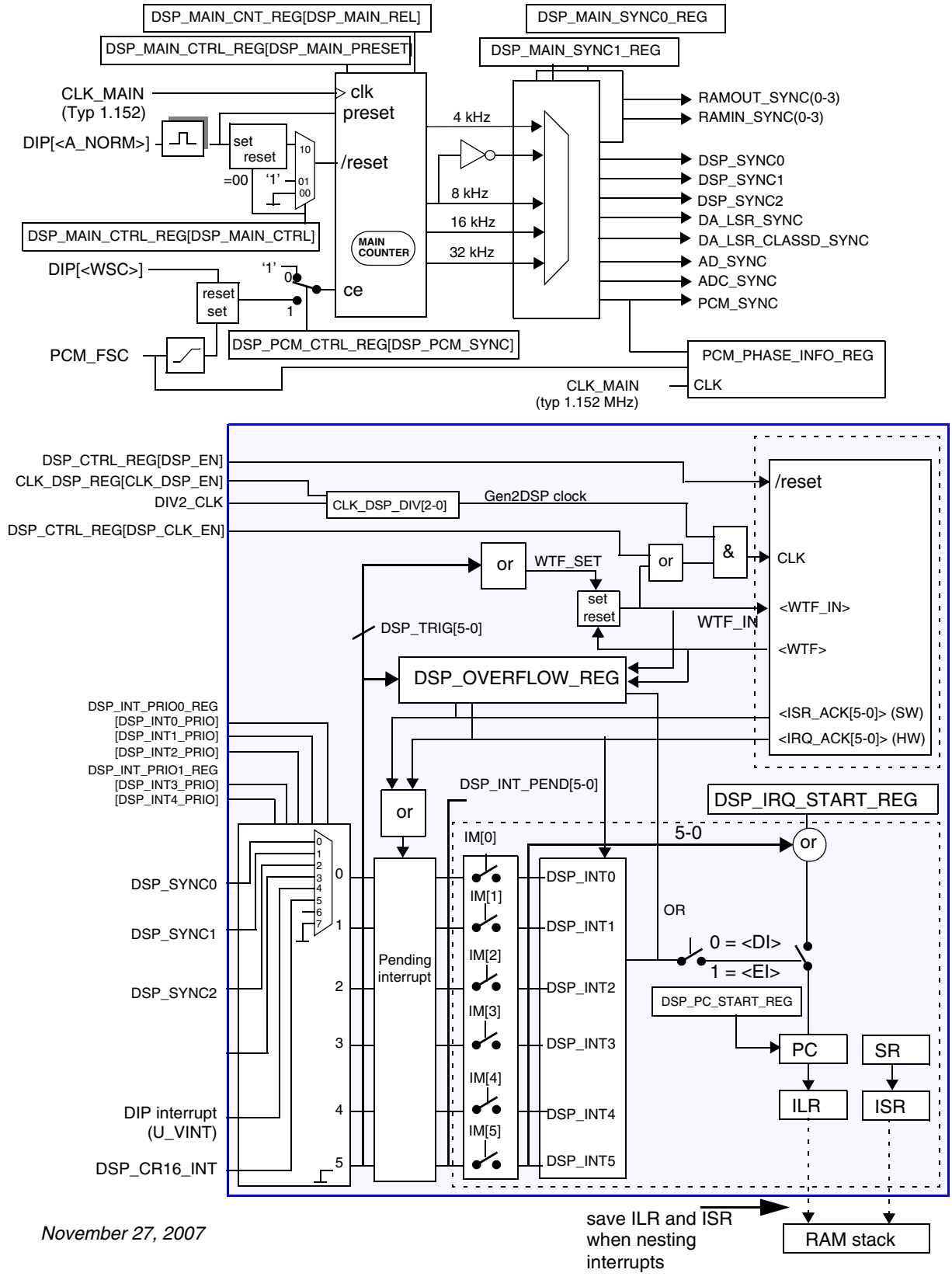


Figure 33 Gen2DSP main counter, start-up and Interrupts

Gen2DSP start-up

The Gen2DSP is started as follows:

- DSP_PC_START_REG must be set
- CLK_DSP_REG[CLK_DSP_DIV] must be set to required clock frequency
- DSP_CTRL_REG[DSP_EN]=1. This bit sets Gen2DSP out of reset.
- Start triggers must be enabled in the DSP_INT_PRIOx_REG and/or DSP_INT_PRIOx_REG. The priority level is only important with interrupts (See next chapter)
- One of the start triggers must be given:
  1. DSP_MAIN_SYNC1_REG[DSP_SYNC0] set for e.g. 8 kHz interrupts,
  2. DSP_MAIN_SYNC1_REG[DSP_SYNC1] set for e.g. 16 kHz interrupts
  3. DSP_MAIN_SYNC1_REG[DSP_SYNC2] set for e.g. 32 kHz interrupts
  4. CR16 interrupt DSP_CR16_INT for e.g non-synchronized block processing (e.g JPEG)
  5. DIP interrupt. DIP executes <U_VINT> with operand=0001. 0000 to interrupt the Gen2DSP
- For triggers 1-3, the main counter must be enabled:
  - DSP_MAIN_CNT_REG[DSP_MAIN_REL] reload value to 0x8F (default for 8/16/32 kHz operation)
  - CLK_CODEC_REG[CLK_MAIN_SEL] main counter clock to “0x” for 1.152 MHz. (default for 8/16/32 kHz operation)
  - DSP_MAIN_CTRL_REG[DSP_MAIN_CTRL] set to
    - 01 = Main counter out of reset, free running. (Non DIP synchronised start-up for tone generation)
    - 10 = If Main counter was running single preset on <A_NORM>, else single start-up on <A_NORM> (DIP synchronised start-up for voice connection, SC14xxx compatible mode)
    - 11 = Reserved
  - If DSP_MAIN_CTRL is started up with values 01 for e.g tone generation, the value must be changed to 00 -> 10 to allow a resync by the DIP. For voice connections DSP_MAIN_CTRL_REG [DSP_MAIN_PRESET] must be set to 15 for Sc14430 to get a compatible <A_NORM> ADPCM start-up timing. (See also AN-D-140)

If no interrupts are enabled (see next chapter), the Gen2DSP clock will be enabled by the WTF_SET condition which is the or of DSP_TRIG[5-0] (see will Figure 33) and starts executing.

For further details on synchronization refer to *AN-D-140 SC14480 DIP Instruction manual, chapter synchronisation.*

10.2 POWER SAVING

Gen2DSP clock disabling

The Gen2DSP can be kept running e.g for block processing or can be put in power down after it has completed a certain processing task. To power down Gen2DSP, <WTF> instruction must be executed, which disables its clock.

If any 8/16/32 switching noise on VDD affects RF performance the Gen2DSP clock can be kept on all the time by setting DSPx_CTRL_REG[DSP_CLK_EN]=1. This has negative effect on power consumption however. In this case the <WTF> will only clear the “Start” synchronization bit and the <WTF_IN> instruction shall be used to poll the “Start” synchronization bit which will be set by one of the interrupt sources. In case the Gen2DSP starts up from power-down, the <WTF_IN> need not to be polled.

RAM/ROM interface clock disabling

The CR16 interface to shared RAM and Gen2DSP registers and micro code RAM can be disabled in order to save power. To enable the shared RAM, ROM and Gen2DSP registers, CLK_AMBA_REG[SRAM1_EN] must be set to ‘1’ (reset value). For Micro Code RAM and ROm access, MCRAM1_EN=1. Access to disabled shared RAM and registers returns 0, while the microcode RAM and ROM return the NOP opcode (0xDFFF.FFFF).

RAM/ROM interface clock frequency reduction

For zero wait cycle shared RAM/ROM/Registers access and micro code RAM of CR16plus and Gen2DSP, CLK_PLL_CTRL_REG[DIV2_CLK_SEL] must be set to 0 and the RAM/ROMs are clocked with the PLL clock (Max 165.888 MHz). With DIV2CLK_SEL set to 1, the CR16plus, Gen2DSP and RAMs/ROMs are all clocked with the PLL clock (Max 82.944 MHz), which gives a power reduction. Upon a simultaneous RAM/ROM read or write access of CR16/Gen2DSP however the Gen2DSP is held one cycle. This SC1443x compatible mode might reduce power, but also reduces the available cycle budget.

10.3 PCM SLAVE SYNCHRONISATION

In PCM slave mode all initialization is equal to the PCM master mode. DSP_PCM_CTRL_REG [DSP_PCM_SYNC] must be set to ‘1’ to stop the main counter at 7/8 of DSP_MAIN_CNT_REG[DSP_MAIN_REL] (typ 126) after DIP<WSC> instruction. At the rising edge of PCM_FSC, the main counter is resumed again (See also 11.5 on page 68) and AN-D-140.

10.4 INTERRUPTS

The Gen2DSP can also use the six start-up triggers to interrupt other running processes as depicted in Figure 33. The interrupts can be used to interrupt:

- Block based algorithms
- Other interrupt routines

The Gen2DSP IM[5-0] (Interrupt Mask) register, masks the six interrupt sources. From start-up this mask is zero.

Interrupts are processed in order 0 to 5. However, the priority can also be changed in the DSP_INT_PRIOx_REGs, which switches the interrupts triggers DSP_SYNC0 to DSP_CR16_INT to any of the interrupt inputs DSP_INT0 to DSP_INT5. If an interrupt occurs and the corresponding IM[x] mask bit is set, the Gen2DSP jumps to address DSP_IRQ_START+ 2x of ISRnr (Interrupt Source number) 0..5. The priority mechanism is only valid if more than one DSP_INTx is '1' at the same time. (see also "Nesting interrupts")

If an interrupt is serviced, the Status Register, SR (== CND, LF, IE, ISRnr[x]) bits are saved in ISR register, the global interrupt IE is disabled automatically, corresponding IM[x] is set '0' and the interrupt source is cleared. E.g. the DSP_CTRL_REG [DSP_CR16_INT] is cleared. No other IM[x] are saved in the ISR.

At the end of a Interrupt Service Routine, the <RTI> (return from interrupt) restores register ISR in SR (CND, LF, IE, ISRnr). So IE and IM[x] are restored to '1', allowing interrupts again. The other IM[x] are unchanged. Next the PC is reloaded from the ILR register.

If a IM[x] is '0' or is set to '0', the corresponding interrupt DSP_INT_PEND[x] stays pending. The pending interrupt is cleared if the ISR is serviced by signal IRQ_ACK[x] "or" if the <ISR_ACK[x]> instruction is given. Although the <ISR_ACK[x]> instruction is mainly used to detect an overflow (See also 10.6 on page 58), this instruction can also be given outside the Interrupt Service Routine to clear old pending interrupts.

Interrupt address "DSP_IRQ_START+ 2*ISRnr[0..5]." may contain either the interrupt routine itself (in case of a single interrupt) or it may contain a <jump> to the interrupt routine.

The interrupt routine is responsible for the whole context save, like registers

Note: Interrupt detection is done with the clock of the receiving Gen2DSP. Therefore the interrupt rate shall not exceed the frequency of the receiving Gen2DSP.

10.5 NESTING INTERRUPT

To allow nested interrupts, the ILR (interrupt link register) containing the saving PC, must be explicitly saved on stack and the <EI> (enable interrupt) must be executed. Recursive interrupts, interrupts from the same source, are not recommended, so the Interrupt mask IM[x] for the current interrupt shall be kept to '0' during an interrupt. To prevent interrupts with lower priority to interrupt a higher priority process who's IM mask bit is set to '0', IM mask bits of lower priority inputs shall also be set to '0' in the interrupt service routine.

When the Gen2DSP is in power down after execution of <WTF>, any of the interrupt sources will power-up the Gen2DSP and the interrupt is handled. At the end of the interrupt routine, after the <RTI> is executed, the background program will resume. Note that the <WTF> shall be placed in the background process (main loop) and not in the interrupt routine in order to avoid interrupt latency overhead and early clock disabling.

10.6 OVERFLOW

The Gen2DSP has the following overflow status and mask bits in register DSP_OVERFLOW_REG. If both Status bit and corresponding mask register bits are set, a CR16 DSP_INT is generated.

- INT_OVERFLOW[x],M_ INT_OVERFLOW]x].
  This overflow indicates that a new DSP_TRIG[x] occurred before instruction <ISR_ACK[x]> was executed. DSP_TRIG[x] sets one of the internal signal bits TRIG_WIN[x] . (E.g. at 8kHz interrupt for sample processing). The <ISR_ACK[x]> resets internal signal TRIG_ WIN[x] and must be executed after sample IO is done and before the next DSP_TRIG[x] occurs, else INT_OVERFLOW[x] is set. Note that only the sample IO must be done before the next DSP_TRIG[x]. The rest of the ISR may run longer but make sure that the next sample is copied before the next DSP_TRIG arrives. This is useful if an interrupt routine uses more cycles and temporarily goes over the DSP_TRIG[x] boundary. If interrupts are disabled in the Gen2DSP core with IM[5-0]=0, the INT_OVERFLOW bits are also set if the main SCP program does not execute the <ISR_ACK[x]>.
- WTF_OVERFLOW, M_WTF_OVERFLOW.
  This bit is set if one of DSP_TRIG[x] start conditions occurs before <WTF> is executed. This is the 43x compatible overflow condition without interrupts.
- IRQ_OVERFLOW, M_IRQ_OVERFLOW
  This overflow is set if a new DSP_TRIG[x] occurs while the previous interrupt request DSP_INT[x] was not acknowledged, so the ISR has not yet started. (IRQ_ACK still '1'). This overflow indicates that one of the enabled interrupts (With IM[x] =1) is not serviced.

Figure 34 shows the examples of the overflow cases.

Signal 1 to 4, Regions:

1. No INT_OVERFLOW.
2. INT_OVERFLOW. <ISR_ACK[x]> not yet given before new DSP_TRIG[x] occurs.

Signal 5 to 8, Regions:

1. No WTF_OVERFLOW
   <WTF> set in time.
2. WTF_OVERFLOW. WTF too late, WTF_IN still '1' while new WTF_SET occurs.

Signal 9 to 11, Regions:

1. No IRQ_OVERFLOW.
2. IRQ_OVERFLOW. One of DIP_INT[x] not serviced.

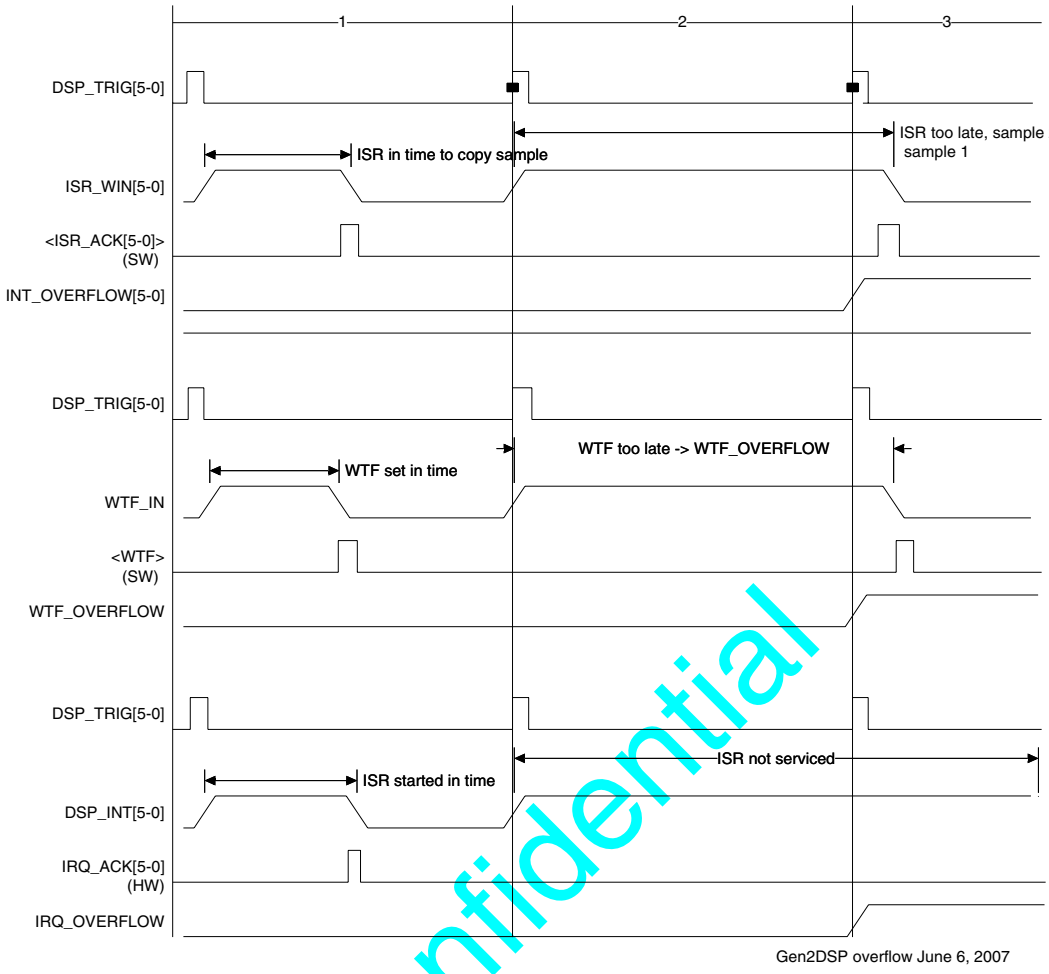


Figure 34 Gen2DSP overflow cases

10.7 REGISTERS

The registers are memory mapped Gen2DSP registers, therefore DSP_CTRL_REG[SRAM1_EN] must be set to '1'. The Gen2DSP can access all the registers starting with DSP_xxx_REG as shown in Table 64.

For debugging purposes the Gen2DSP program counter can be observed by the CR16 in the DSP_PC_REG.

10.8 ECZ1, ECZ2 USAGE AND PORT MAPPING

For diagnostics or control purposes, the Gen2DSP can directly set port pins P2[0] and P2[1] using ECZ1 and ECZ2 signals as shown in Figure 35:

The Gen2DSP may copy any shared RAM location to internal registers DSP_ZCROSS1_OUT_REG and/or DSP_ZCROSS2_OUT_REG. Only bit 15 of the RAM is used. These register outputs are the ECZ1 resp ECZ2 signals which can be directly mapped on P2[0] resp P2[1] by setting P2_MODE_REG multiplexer as shown above.

The ECZ1 and ECZ2 usage and names originate from the Gen2DSP ZCROSS function which requires a single bit hardware register to store output parameter "zcrossout" sign bit 15. These register outputs ECZ1 and ECZ2 are used by the "Capture timers/counters" on page 106 for frequency measurement of line interface signals.

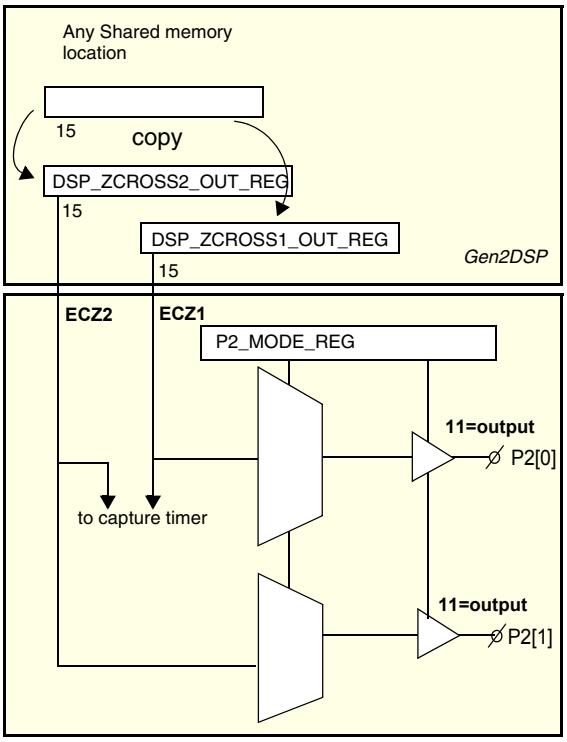


Figure 35 ECZ1 and ECZ2 port mapping

10.9 RAMIO REGISTERS

The RAMIO registers DSP_RAM_OUTx_REG, DSP_RAM_INx_REG, are special registers used for minimum delay I/O to the DIP. Refer to paragraph 7.5 for more information on minimum delay.

10.10 SHARED RAM/ROM

The Gen2DSP has access to the memory at full speed for data transfers. The DIP has always zero wait cycle access, in order to guarantee slot timing.

With simultaneous access the priority in the RAM is: DIP, DSP shared RAM access, DSP SCP access, CR16 access.

Refer also to chapter "Power saving" on page 57 for disabling the shared RAM to save power.

10.11 SUBROUTINE CONTROL PROGRAM (SCP)

The SCP has been redefined to be the main program loop from which the algorithms in micro code ROM are called. The SCP runs in the shared RAM with one wait state or from Micro Code RAM with 0 wait states. The SCP can be also be placed in a interrupt routine.

The SCP main programs calls Gen2DSP algorithms a jump table entry. The start of the jump table is the start of the Micro Code ROM.

10.12 MICRO CODE RAM

The Micro Code RAM is mainly intended to run user defined algorithm from, but can also be used to run the SCP from or used from storage by the CR16.

The Micro Code RAM has two sections: See also “Detailed micro code RAM and ROM Memory map for DIP, CR16Cplus and Gen2DSP (t63,p132)”

- One section mapped in Shared Data RAM used for the SCP main program. The shared RAM can also be used to executed user defined algorithms from. The Gen2DSP needs one extra cycle to execute from this RAM.
- One section mapped parallel to the Micro Code ROM used for algorithm development and only available in the FLASH version.

Both Micro Code RAMs are accessible by the CR16Cplus and can be updated while the Gen2DSP is executing.

Refer also to chapter "Power saving" on page 57 for disabling the micro Code RAM/ROM to save power.

10.13 MICRO CODE ROM

The Micro Code ROM contains predefined DSP algoritms which are accessible via the jump index table as shown on the next page.

For detailed information on Gen2DSP instructions refer to *AN-D-129 “SC14450/SC14480 Gen2DSP programming manual”.*

Table 17: Standard Gen2DSP algorithms in Micro Code ROM (Note 31)

Jump table index	Symbol	Algorithm Name	A5M ES8 FLASH/ ROM	A5M ES7 FLASH/ ROM	A5M ES6 FLASH/ ROM
0	ABS	Absolute value	✓	✓	✓
1	AEC	Acoustic Echo Canceller (428 compatible)	✓	✓	✓
2	AGC	AGC	✓	✓	✓
3	ANAGC	Analog AGC	✓	✓	✓
4	AND	AND	✓	✓	✓
5	BLKMINMAX	Block Min/max value	✓	✓	✓
6	BLKNORM	Block normalisation	✓	✓	✓
7	BUF_PACK	Bit, Nibble and Byte swap and data storage in a circular buffer	✓	✓	✓
8	BUF_UNPACK	Bit, Nibble and Byte swap and retrieving data from a circular buffer	✓	✓	✓
9	CASDET	CAS Detector	✓	✓	✓
10	CASDET2	CAS Detector with separate inputs for low and high tone	✓	✓	✓
11	CBUFFER	Versatile Buffer (delay line)	✓	✓	✓
12	CFFT	FFT and IFFT		✓	✓
13	CONF	Conference	✓	✓	✓
14	COPYB2B	Copy Block to Block	✓	✓	✓
15	COPYP2B	Copy Pointer to Block	✓	✓	✓
16	COPYP2P	Copy Pointer to Pointer	✓	✓	✓
17	COUNTER	Programmable counter	✓	✓	✓
18	DBLLAW2LIN	A/u law to linear for INTERP	✓	✓	✓
19	DCT	Discrete Cosine Transform	✓	✓	✓
20	DEC	Decrement	✓	✓	✓
21	DIVF	Fractional Division	✓	✓	✓
22	DIVI	Integer Division	✓	✓	✓
23	DSCRTGAIN	Discrete gain function	✓	✓	✓
24	DTMFDET	DTMF detector (improved)	✓	✓	✓
25	DTMFRU	DTMF for Russia	✓	✓	✓
26	EDGEDET	Edge Detector	✓	✓	✓
27	EXP	Gives number of significant bits	✓	✓	✓
28	FMOPERATOR	FM operator block	✓	✓	✓
29	FSKDECOD	FSK decoder with data recovery	✓	✓	✓
30	FSKGEN	FSK Generation	✓	✓	✓
31	G722_RX	G722 ADPCM Decoder	✓	✓	✓
32	G722_TX	G722 ADPCM Encoder	✓	✓	✓
33	G726	G726 ADPCM Encoder and decoder	✓	✓	✓
34	G726_VQI	G726 ADPCM Encoder and decoder with VQI	✓	✓	✓
35	GETREVISION	Gen2DSP HW and SW revision number	✓	✓	✓
36	GRAY_SCALE	JPEG Gray scale pixel saturation	✓	✓	✓
37	HAGC	Handsfree AGC	✓	✓	✓
38	HFREE	Handsfree/ half duplex switch	✓	✓	✓

Table 17: Standard Gen2DSP algorithms in Micro Code ROM (Note 31)

Jump table index	Symbol	Algorithm Name	A5M ES8 FLASH/ ROM	A5M ES7 FLASH/ ROM	A5M ES6 FLASH/ ROM
39	IDCT	JPEG Inverse Discrete Cosine Transform	✓	✓	✓
40	INC	Increment	✓	✓	✓
41	INTERP	Interpolator for pitch shift of wave tables	✓	✓	✓
42	LAW2LIN	A/u law to linear	✓	✓	✓
43	LEC	Line Echo Canceller	✓	✓	✓
44	LIN2LAW	Linear to A/u law	✓	✓	✓
45	LIN2LOG	Linear to logarithmic(^{2}logN)	✓	✓	✓
46	LOG2LIN	Logarithmic to Linear ($2^{\wedge N}$)	✓	✓	✓
47	MATRIX3X3	3x3 Matrix multiplication	✓	✓	✓
48	MIXER	Sound mixer	✓	✓	✓
49	MONITOR	Monitor	✓	✓	✓
50	NC100HZ	100 Hz noise canceller	✓	✓	✓
51	NSHL	Nibble Switch (shift left)	✓	✓	✓
52	NSHR	Nibble Switch (shift right)	✓	✓	✓
53	ORB	OR	✓	✓	✓
54	PFILT	Prog. filter (biquad)	✓	✓	✓
55	PFIRFLT	Prog. FIR filter	✓	✓	✓
56	PLEVDET	Power Level Detector	✓	✓	✓
57	PNLEVDET	Noise detection	✓	✓	✓
58	POLY	Polynomial	✓	✓	✓
59	RGB2YCC_420	RGB to YCC color conversion and downsampling	✓	✓	✓
60	RNDGEN	Random generator	✓	✓	✓
61	RS_PARSYN	R-S Parity and Syndrome calculation		✓	✓
62	SHIFT	Shift left/right	✓	✓	✓
63	SINGLETONEDET	SIngle tone detector	✓	✓	✓
64	SUB	Subtract	✓	✓	✓
65	SUMM	Summator	✓	✓	✓
66	SUPP	Suppressor	✓	✓	✓
67	TONEDET	Tone detector	✓	✓	✓
68	TONEGEN	Triple Tone Generation	✓	✓	✓
69	UPSAMPLE420	Graphic Data upsampling 4-2-0	✓	✓	✓
70	UPSAMPLE422	Graphic Data upsampling 4-2-2	✓	✓	✓
71	UPSAMPLE422V	Graphic Data upsampling 4-2-2V	✓	✓	✓
72	WINDOWADD	FFT Window function	✓	✓	✓
73	XORB	Exclusive or	✓	✓	✓
74	YCC2RGB	YCC to RGB color conversion	✓	✓	✓
75	ZCROSS	Zero cross detection	✓	✓	✓
76	-	Reserved			
77	-	Reserved			
78	TEST	Reserved		✓	✓
79	SVC_ENC	SiTel Voice Compression encoder	✓	✓	✓
80	SVC_DEC	SiTel Voice Compression decoder	✓	✓	✓

Table 17: Standard Gen2DSP algorithms in Micro Code ROM (Note 31)

Jump table index	Symbol	Algorithm Name	A5M ES8 FLASH/ ROM	A5M ES7 FLASH/ ROM	A5M ES6 FLASH/ ROM
81	MIDI_SYNTH	Midi synthesizer is a configurable mix of FM melodic, FM percussion and wavetable voices - include wavetable 'chorus' option - includes Mixer, LFO's, timer - support 32 voices when DSP runs at 80MHz - generate configurable interrupt vector when the timer expires	✓	✓	✓
82	PAEC	Perceptual Acoustic Echo canceller.	✓	✓	✓
83		Reserved	✓	✓	✓
84	-	Reserved	✓	✓	✓
85	USER0	Jump to user defined function in MC RAM address 0, 2, 4, 6, 8,10, 12, 14 (FLASH) MC ROM address <tbd> (Customer ROM code)	✓	✓	✓
86	USER1		✓	✓	✓
87	USER2		✓	✓	✓
88	USER3		✓	✓	✓
89	USER4		✓	✓	✓
90	USER5		✓	✓	✓
91	USER6		✓	✓	✓
92	USER7		✓	✓	✓
93	RFFT	Real input FFT	✓	✓	
94	RiFFT	Real outputFFT	✓	✓	
95	RFFTD	Dynamic Scaling real-to-complex FFT	✓		
96	RiFFTD	Dynamic Scaling complex-to-real iFFT	✓		
97	RESAMPLE	Audio buffer resampler (for USB/PCM resampling)	✓		
98	POLYPHASE	Sample rate resampler (for SVC)	✓		
99	CBUFIRQ	Rec/play buffer with programmable frame-interrupt generation	✓		
100	WIDEBAND	Artifical voice enhancement	✓		

Note 31: For SC14480A2M6 Micro Code ROM content see SC1448x family overview. With FLASH to ROM migration, mention CHIP_TEST1_REG to indicate which Gen2DSP ROM is used for development.

11.0 PCM interface

The PCM interface is a 8/16/32kHz synchronous interface to external audio devices, ISDN interface circuits and serial data interfaces.

Features

- PCM_CLK in Master mode Nx512, Nx576kHz (N=1,2,4,8) and Nx1.536 MHz
- Programmable strobe output 1,8,16,32 bits and Programmable strobe output before or on the first bit. (Master mode)
- PCM_CLK in Slave mode upto 4.608 MHz 1 bit strobe input on or before first bit.
- 4x16bits channels.
- Programmable inversion of PCM_CLK, PCM_FSC
- I2S mode (Left/Right channel selection)

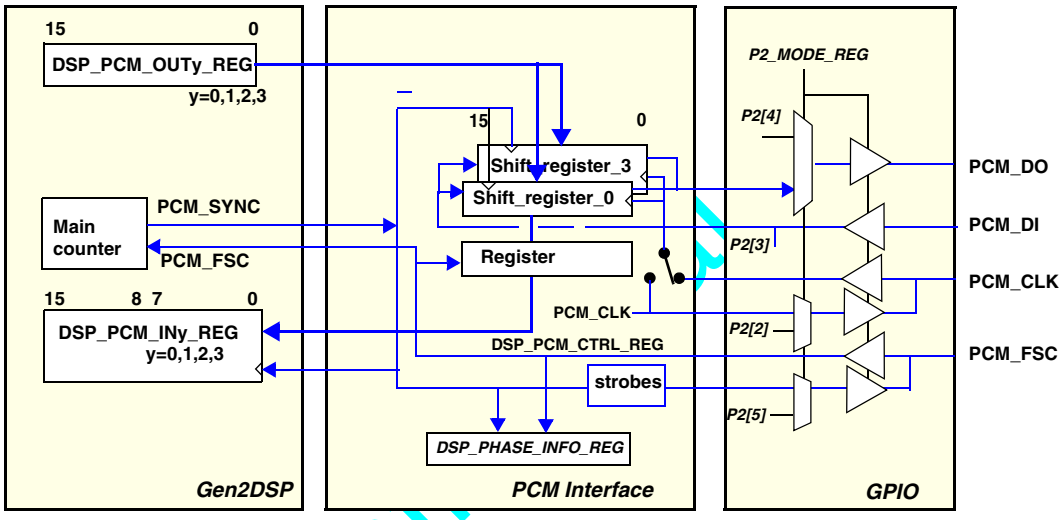


Figure 36 PCM interface

11.1 INTERFACE SIGNALS.

- PCM_FSC, strobe signal input, output. 8/16/32 kHz. Can generate an interrupt to Gen2DSP
- PCM_CLK, PCM clock input, output push pull or open drain with external pull-up resistor.
- PCM_DO, PCM Data output, push pull or open drain with external pull-up resistor.
- PCM_DI, PCM Data input

Pin assignment is done using P2_MODE_REG bits P2_2_MODE, P2_3_MODE, P2_4_MODE, P2_5_MODE.

DSP_PCM_CTRL_REG (0x1027FB6) bit PPOD = 1 sets PCM_DO to **open drain** configuration. This bit can be set if external IO device voltage is 1.8V and the bus is shared with other devices.
PADS_CTRL_REG[P234_OD, P225_OD] **forces** PCM_DO and PCM_CLK, PCM_FSC **to open drain** configuration for interfacing to external IO voltage up-to 3.45V.

If PPOD is 0, PCM_DO is 0 after transmission of the last channel. With PPOD is 1, PCM_DO is Hi-Z if a '1' is transmitted and after the last channel.

The PCM interface is in power down if DSP_MAIN_SYNC1_REG[PCM_SYNC] is "11" and CLK_CODEC_REG[CLK_PCM_EN] = '0'.

11.2 CHANNEL ACCESS

The PCM interface has 4 channels of 16 bits which are byte and word wise accessible by the CR16C and only word wise by the Gen2DSP. The channels are accessible through 16 bits registers DSP_PCM_OUT0_REG, DSP_PCM_OUT1_REG, DSP_PCM_OUT2_REG, DSP_PCM_OUT3_REG(0x1027FA6, 0x1027FA8, 0x1027FBA, 0x1027FAC) and DSP_PCM_IN0_REG, DSP_PCM_IN1_REG, DSP_PCM_IN2_REG, DSP_PCM_IN3_REG (0x1027FAE, 0x1027FB0, 0x1027FB2, 0x1027FB4).

The first channel is mapped on bit 15-0, etc. Channels are shifted in and out at the same time with the MSB first.

11.3 CLOCK GENERATION

Figure 37 shows the PCM clock generation.

The SC14480A5M, SC14480A2M6 has a common divider for the PCM_CLK. This allows operation of PCM_CLK at Nx512kHz PCM_CLK frequencies with Codec off or Nx1.152MHz with both PCM and Codec active.

The PCM_CLK frequencies are derived from the DIV1_CLK, DIV2_CLK, DIVN_CLK selected with CLK_CODEC_REG[CLK_PCM_SEL] and divider CLK_CODEC_DIV_REG[CODEC_DIV].

If CODEC_DIV is set to generate frequency X, automatically 2X and 4X are generated. (see table 18 and register description).

PCM_FSC strobes of 4, 8, 16 and 32 kHz PCM_FSC are derived from CODEC_DIV and the main counter divider through DSP_MAIN_CTRL_REG. Duration and position is selected in DSP_PCM_CTRL_REG bits.

Table 18: PCM clock divider examples

PLL (MHz)	CLK_CODEC_DIV_REG [CODEC_CLK_SEL]	CLK_CODEC_DIV_REG [CODEC_DIV]	CLK_CODEC_REG[CLK_PCM_SEL] generating PCM_CLK (MHz)		
			0x	10	11
41.472 82.944 124.416 165.888	2 (DIV1_CLK) 1 (DIV2_CLK) - -	81 81 - -	0.512	2.048 [32]	4.096 [32]
41.472 82.944 124.416 165.888	- 2 (DIV1_CLK) - 1 (DIV2_CLK)	- 81 - 81	1.024	2.048 [32]	4.096 [32]
165.888	2 (DIV1_CLK)	81	2.048	4.096 [32]	4.096 [32]
Off	0, 1 or 2	9	1.152	2.304 [32]	4.608 [32]
41.472 82.944 165.888	2 (DIV1_CLK) 1 (DIV2_CLK) 1 (DIV2_CLK)	36 36 72	1.152	2.304 [33]	4.608 [33]
41.472 82.944 165.888	2 (DIV1_CLK) 1 (DIV2_CLK) 1 (DIV2_CLK)	27 27 54	1.536	3.072 [32]	6.144 [32]

Note 32: Derived 2x, 4x clocks are automatically available but have no constant duty cycle because CODEC_DIV can not be divided by 2 (first higher) and not by 4 (second higher).

Note 33: Derived clocks are automatically available with constant duty cycle if CODEC_DIV for the base frequency can be divided by 2 (first higher) and by 4 (second higher)

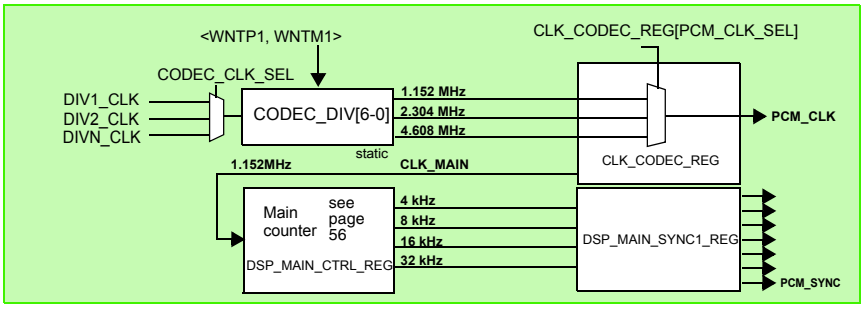


Figure 37 PCM clock generation

Duty cycle jitter

The PCM clock divider generates three frequencies being the base frequency DIVx_CLK/CODEC_DIV and the base frequency x2 and x4.

Figure 38 shows an example of the PCM_CLK derived from DIVx_CLK = 10.368 MHz and CODEC_DIV=9.

- Base frequency 10.368/9 = 1.152 MHz
- Base frequency (10.368/9)*2= 2.304 MHz
- Base frequency (10.368/9)*4= 4.608 MHz

If CODEC_DIV can not be divided by 2 or 4, then the derived clocks (x2 and x4) have a duty cycle jitter determined by the DIVx_CLK of as shown below. If CODEC_DIV can be divided by 2, reps 4 (see Table 18) x2 and x4 clocks have no jitter.

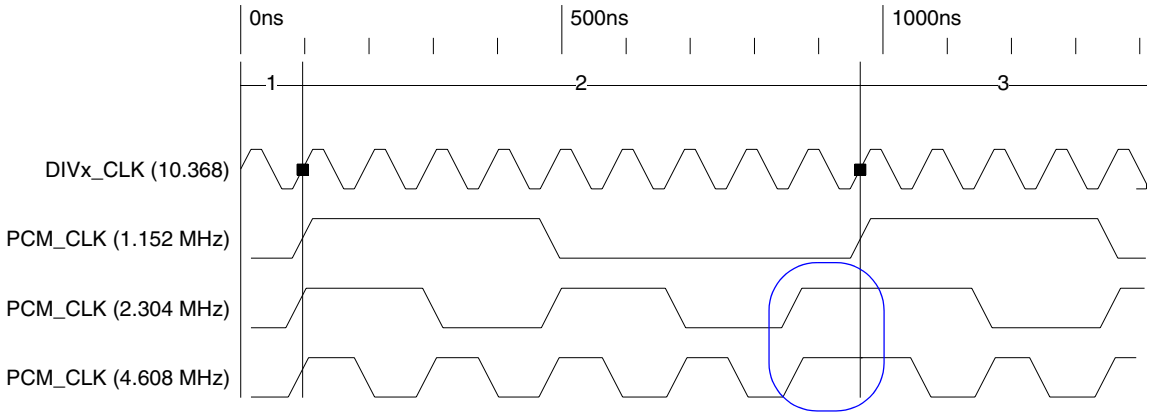


Figure 38 Duty cycle variation with CODEC_DIV

Clock stretching/shortening

In **portable** applications If PCM master, upon the execution of DIP <WNTP1>, <WNTM1> or <EN_SL_ADJ> the PCM_CLK and PCM_FSC are automatically stretched/shortened with 1 DECT bit of 1.152 MHz in order to maintain a constant phase to the received DIP frame. This stretching/shortening happens every 1.152 MHz with the selected clock DIVx_CLK (DIVN_CLK, DIV2_CLK or DIV1_CLK) until the 1.152 MHz bit is corrected.

11.4 DATA FORMATS

The various PCM data formats are shown on the next pages. "PCM Interface timing diagram" on page 252 show timing details of the PCM interface timing

Master mode

Master mode is selected if DSP_PCM_CTRL_REG (0x1027FB6) bit [MASTER] = 1.

In master mode **PCM_FSC** is output and falls always over Channel 0. The duration of PCM_FSC is programmable with **PCM_FSC0LEN**: 1, 8, 16, 32 clock pulses high. The start position is programmable with PCM_FSC0DEL and can be placed before or on the first bit of channel 0. The repetition frequency of PCM_FSC is programmable in DSP_MAIN_SYNC1_REG (0x1027F82) bits PCM_SYNC between 8,16, 32 kHz.

If master mode selected, **PCM_CLK** is output. The polarity of the signal can be inverted with bit PCM_CLKINV.

The PCM_CLK frequency selection is described in paragraph 11.3.

Slave mode

In slave mode (bit MASTER = 0) **PCM_FSC** is input and determines the starting point of channel 0. The repetition rate of PCM_FSC must be equal to PCM_SYNC (8, 16 or 32 kHz) and must be high for at least one PCM_CLK cycle. Within one frame, PCM_FSC must be low for at least PCM_CLK cycle.
Bit PCM_FSCDEL sets the start position of PCM_FSC **before or on** the first bit (MSB).

In slave mode **PCM_CLK** is input. The minimum received frequency is 256 kHz, the maximum is 4.608 MHz.

In slave mode DSP_PCM_CTRL_REG (0x1027FB6) bit [DSP_PCM_SYNC] must be set to 1 to resume the main counter on a rising edge of PCM_FSC.

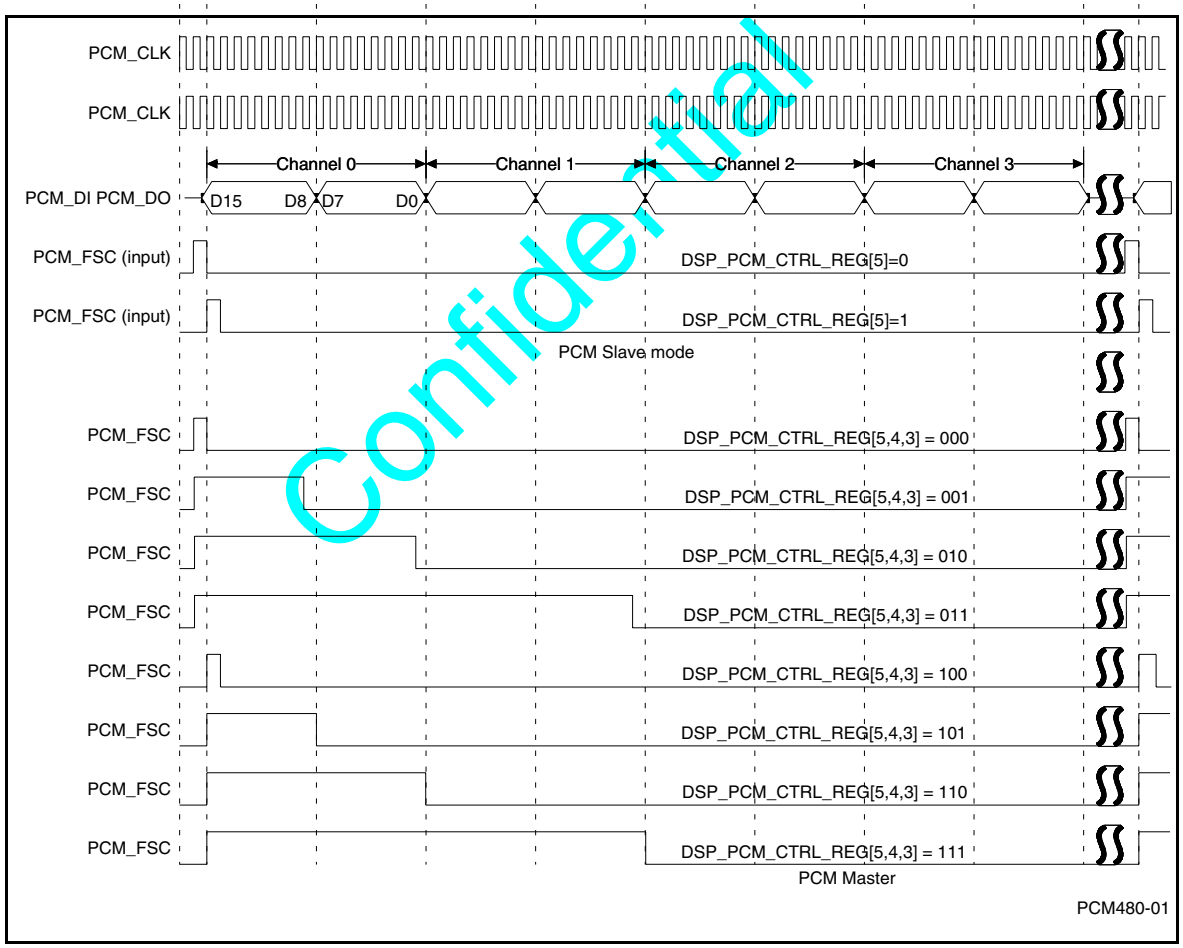


Figure 39 PCM interface formats

I2S format

In I2S mode, the PCM clock can be inverted. In **master** mode the PCM_FSC strobe length can be selected using PCM_FSC0LEN. This allows 0, 1 or 2 channels for left/right. In **slave** mode all data is shifted in into the shift registers.

To support I2S mode PCM_FSC0DEL and PCM_CH0_DEL must be 0. PCM_CLKINV must be 1.

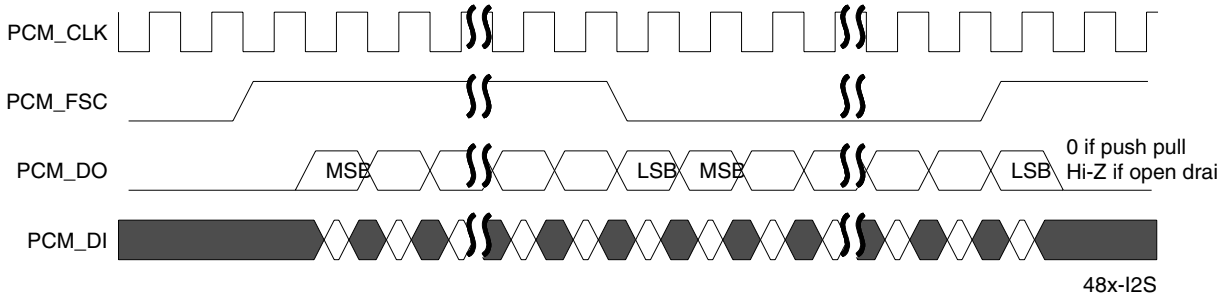


Figure 40 I2S format

11.5 EXTERNAL SYNCHRONISATION

With the PCM interface in slave mode, the DIP can be started at an external PCM_FSC and the phase difference between the internal and external PCM_FSC can be monitored in DSP_PHASE_INFO_REG (0x1027FB8) in units of main counter clock (typically 1.152 MHz).

To maintain a constant phase the following parameters may be changed by extending/shortening the DIP frame using <WT> instructions in combination with DIP instructions <WNTP1> and <WNTM1>, which stretches/shortens the CODEC_DIV derived clocks.

Initial synchronisation

Initial Phase synchronisation between PCM_FSC and the DIP frame can be done by executing DIP command <WSC> which halts the DIP processor and main counter. The next PCM_FSC rising edge resumes DIP operation and main counter after 16x4 channel = 64x PCM_CLK cycles.

Refer to *AN-D-140 "SC14480 DIP Instruction Manual"* for detailed application information on synchronisation.

12.0 CODEC and Analog frontend

The SC14480A5M, SC14480A2M6 contains a 1.8 Volt CODEC and a full differential Analog Front End which can be configured for handset or basestation applications including on-caller-id, ring detection and voice activity detection for baby phone applications.

Features

- 8, 16 and 32 kHz operations
- Separate AD and DA clocks can be selected for improved out-of-band noise performance.
- Optional Low Pass Filter in DA path
- Very low microphone amplifier offset eliminated any digital offset compensation.
- Internal buffer circuit eliminates VBUF pin
- Integrated headset detection
- Single ended or differential microphone and loudspeaker connections
- Loudspeaker gain adjust in 8 steps of 2 dB
- Microphone gain 15 steps of 2 dB from 0 to +30 dB
- CLASSD Buzzer mode can be used by connecting LSRp/n pins to PAOUTp/n (short cicuit protection using CODEC_TEST_CTRL_REG[CODEC_PROT]

12.1 LOUDSPEAKER CONNECTION

The loudspeaker stage can be fully configured through register **CODEC_LSR_REG.** The LSRN_MODE, and LSRP_MODE bits are used to select differential or single ended (see Figure 44 and Figure 45)

Dynamic loudspeakers with an impedance as low as 28 Ω can be connected as well as ceramic loudspeakers with an equivalent resistance of 600 Ω and 30 µF capacitance can be connected without additional circuitry. The loudspeaker gain can be controlled with CODEC_LSR_REG[LSRATT] from plus 5 to minus -9 dB in 8 steps of ~2dB/step.

In basestation applications (see Figure 44) the LSR+ or LSR- can be configured as single output to the line interface. The unused LSR+ or LSR- pin can be configured as a voltage reference pin (REF) with 0.9V output voltage.

12.2 MICROPHONE CONNECTION

The microphone stage can be fully configured through register **CODEC_MIC_REG.** The MIC_MODE bits are used to select differential or single ended modes.

Several types of microphones can be used. The supply current for the microphone is fed through differential reference voltages independent of the supply voltage. The microphone gain can be adjusted in the CODEC_MIC_REG[MIC_GAIN] from 0 dB upto plus 30 dB in steps of 2dB.

For active microphones a voltage source with high supply voltage rejection ratio is provided on supply pins VREFp/VREFm. Filtering of internal and external reference voltages is provided with internal capacitor on the VBUF only. The time constants can be set with internal resistors. With VREF_INIT set to '1' (reset value), 200k ohm resistors are selected. If VREF_INIT is '0' (recommended), 1M ohm series resistance is selected.

If using VREFp, make sure CODEC_TONE_REG [CID_PR_DIS]=1 in order to disable the CID protection diodes on the shared VREFp /CIDINp pin.

12.3 HEADSET CONNECTION

The AFE can be configured to handle two single ended microphones, one normal and one headset microphone. (see Figure 45) Both microphones are supplied from **VREFp**. The optional headset microphone, if connected to **MICh**, can be enabled by setting CODEC_MIC_REG[MICH_ON] to '1'. This disables the MICn input. The normal microphone signals is connected to **MICp**.

The headset loudspeaker is connected to the LSRn pin. By setting LSRp in power down, the normal loudspeaker can be muted.

In order to prevent a buzzer tone on the headset speaker the buzzer tone must only be put on LSRp (or LSRn) only (single-ended) when the headset speaker is plugged-in. The headset loudspeaker, if connected, can be muted by switching LSRn to AGND level.

This implies a -6 dB level reduction compared with the differential mode buzzer level (the case when the headset speaker is not plugged-in)

12.4 CODEC OFFSET COMPENSATION

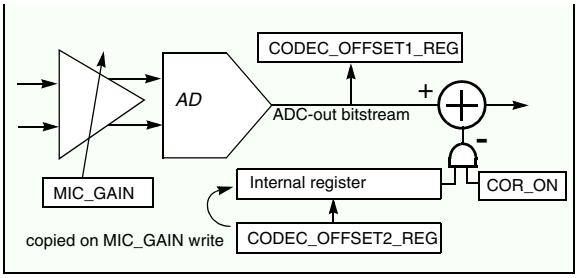


Figure 41 Codec offset compensation

The MIC_GAIN amplifier offset error can be compensated in the digital domain. Therefore the offset error for each gain setting must be measured at start-up by reading out CODEC_OFFSET1_REG while the MIC_MUTE is set to '1'.

For an applied MIC_GAIN setting, the corresponding offset error value must then be written to CODEC_OFFSET2_REG to compensate the offset error. The value in this register becomes active in a seamless way after the new MIC_GAIN value is written to the CODEC_MIC_REG.

This synchronisation process guarantees simultaneous activation of the new MIC_GAIN and corresponding CODEC_OFFSET2_REG value. During synchronisation, which takes about 156 us,

CODEC_TEST_CTRL_REG[COR_STAT] becomes '1'. As soon as COR_STAT is '0', CODEC_OFFSET2_REG may be loaded with new value. The COR_ON bit must be switched on **before** the initial load of CODEC_OFFSET2_REG and MIC_GAIN.

12.5 FILTERING

In the DAC path of the codec has been extended with some extra features which can be used to reduce noise. An extra low-pass filter with a programmable cut-off frequency via CODEC_ADDA_REG[LPF_BW] in the range from 5.5 kHz to 30 kHz can be selected prior to final amplification. Depending on the pole frequency of this filter extra droop will occur in the pass-band. It is up to the application what is acceptable an desirable. The high-frequency poles for instance are useful to reduce out-band-noise (basestation application) without affection the pass-band transfer function too much.

To reduce near-band noise, say from 4 kHz to 10 kHz when for instance loudspeakers are used with a larger bandwidth, extra filtering is normally necessary to meet the integrated idle channel noise specification. In this case the extra filter can be operated at a lower pole frequency.

As extra feature the DAC reconstruction filter double-pole (standard 2 x 8 kHz) can be halved by setting CODEC_ADDA_REG[DA_HBW] to '1'. This will give some droop in the pass-band (0 to 4 kHz). The HBW-mode can be used with or without the extra LPF. The passband-droop can be corrected by the DSP when necessary.

Also new in the codec is the fact that the sample clocks of the ADC (transmit path) and DAC (receive path) can be set to separate rates (1x, 2x, or 4x).

In order to increase DAC the audio quality it is possible for instance to operate the DAC at 2x or 4x the ADC clock (2x or 4x larger oversampling ratio) in combination with the HBW an extra LPF. The extra oversampling will reduces the (inband) noise density. This mode however will come with a cost: the DSP has to interpolate 2x or 4x at the DA-side in order to match the basic sample rate of 8 kHz.

Notice that the pole frequencies of the DAC en LPF are connected with the clock rate (standard 1.152 MHz). Doubling the clock doubles the pole frequencies and the bandwidth.

12.6 PROGRAMMABLE CLOCKS

The SC14480 has three separate clocks whos frequency can be set CLK_CODEC_REG with bits:

- CLK_DA_LSR_SEL for DA path to loudspeaker.
- CLK_DA_CLASSD_SEL for DA path to CLASSD.
- CLK_AD_SEL for AD path from microphone.

Bit values unequal to 00, enables the digital parts of the codec paths.

For **narrow band 32kbit/s ADPCM (G.726)**, the AD and DA shall be set 1.152 MHz resulting in sample rate of 8 kHz. If improved out-of-band noise is required in DA direction one or more of following measures can be taken:

- The sample Codec DA clock rate can be increased to 16 kHz by setting DA_LSR_SYNC to 1 while the AD sample rate can stay at 8 kHz. The Gen2DSP shall process at 8 kHz and interpolate the 8 kHz samples to 16 kHz, using an interpolation filter. The interpolated samples are stored by the SCP program in a two word software FIFO and the 16 kHz Gen2DSP interrupt routine copies these samples to the DSP_CODEC_OUT_REG. The Codec DA reads the FIFO at a 16 kHz rate.
- CODEC_ADDA_REG[DA_HBW] can be set to 1, divides the DA fIlter bandwidth by two.
- CODEC_ADDA_REG[LPF_BW] can be set to enable addition Low pass filters after the DAC.

For **wide band 64kbit/s ADPCM (G.722),** the AD and DA shall be set 2.304 MHz resulting in sample rate of 16kHz. No noise reduction is required in this mode, because the out-of-band noise contributes from 20 kHz which is not audible.

In case of **32 kHz MP3**, the out-of-band noise is hardly audible and the DA clock stays at 4.608 MHz for 32 kHz sample rate.

12.7 CALLER-ID OPAMP

The opamp can be used in three configurations:

- On-hook Caller-id detection, CIDOUT is internally switched via MICn to the Codec. MICp input to the Codec is disabled.
- On-hook ring detection, the CIDOUT goes via 10 bit ADC input and is sampled with 8 kHz. The digital output samples can be read by either Gen2DSP for further signal processing. See "ADC" on page 91.
- Off-hook caller-id detection, the opamp can be disabled and the in-band caller-id information goes straight via MICh to the Codec.

12.8 RINGING AND PARALLEL SET DETECTION

Furthermore, two separate opamps are used for ring frequency detection and parallel set detection. The outputs are multiplexed to the 10 bit ADC. The digital output samples are transferred to shared RAM. The GenDSP can access the samples for further signal processing.

The output of the RING opamp RINGOUT is also input for the RINGING comparator and capture timer. Note that the capture timer accuracy has been enhanced by counting on both edges of the ringing signal compared

to rising edge in the previous generations.

Table 19: SC14480A5M, SC14480A2M6 Analog frontend supply, reference voltage and power down and recomended values overview

AFE functions AFE register	MICp/n	VREFp	LSRp/n REF	TONE (CID, Para, Ring)	RINGING (comparator)	CODEC ADC/DAC
CODEC_VREF_REG						
BIAS_PD	**0**	**0**	**0**	**0**	**0**	**0**
VREF_BG_PD	**0**	**0**	**0**	**0**	**0**	**-**
AMP1V5_PD	**0**	**0**	**0**	**0**	**0**	**0**
VREF_PD	**0**	**0**	**0**	**0**	**0**	**0**
VREF_INIT	**0**	**0**	**0**	**0**	**0**	**0**
CODEC_MIC_REG	**Appl**	**-**	**-**	**-**	**-**	**-**
CODEC_LSR_REG	**-**	**-**	**Appl**	**-**	**-**	**-**
CODEC_TONE_REG	**-**	**-**	**-**	**Appl**	**Appl**	**-**
RING_CMP_PD	**-**	**-**	**-**	**Appl**	**Appl**	**-**
PARA_PD	**-**	**-**	**-**	**Appl**	**Appl**	**-**
RNG_PD	**-**	**-**	**-**	**Appl**	**1 (off)**	**-**
CID_PD	**-**	**-**	**-**	**Appl**	**Appl**	**-**
CODEC_ADDA_REG	**-**	**-**	**-**	**-**	**-**	**Appl**
REFINT_PD	**-**	**-**	**-**	**-**	**-**	**0**

Appl = Application specific setting,
'-' = don't care, preferably in power down to save power

12.9 INTEGRATED HEADSET DETECTION

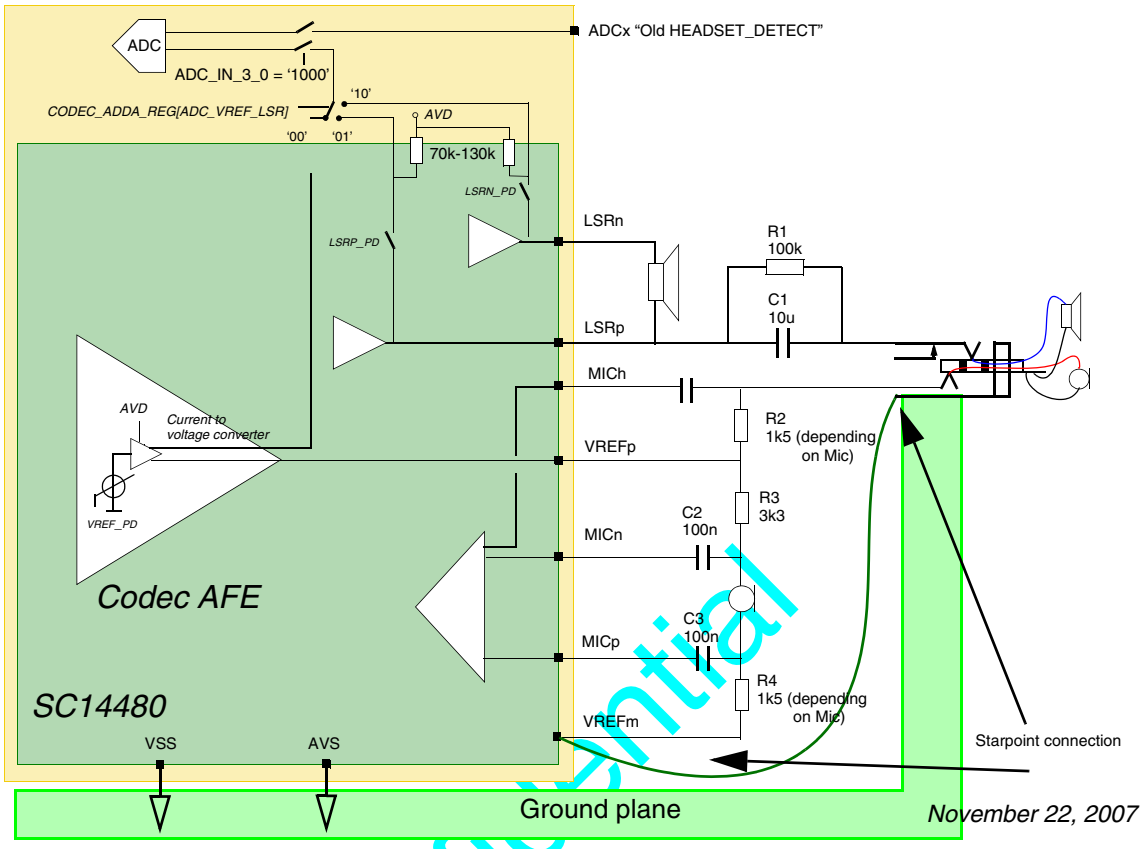


Figure 42 Integrated earphone and microphone detection

The LSRp/LSRn output driver and VREFp buffer circuits can be configured to detect presence/absence of an earphone and none, one or two microphones using the on-chip ADC. See **Figure 42 on page 72**

Earphone detection.

Earphone detection is done with the LSRx_PD=1, which configures the LSRp/LSRn driver as a voltage source with 100k output resistance. The output at LSRp/LSRn is measured full scale with the ADC if no loudspeaker connected and will drop to less than 1.2V if a low ohmic loudspeaker with 100 k series resistor over the AC capacitor is connected.

The voltage on the LSRp/LSRn pins can be measured if CODEC_ADDA_REG[ADC_VREF_LSR] =01/10 and ADC_CTRL_REG[ADC_3_0] = 0011

Table 20: ADC values for earphone detection

LSRx_PD	Earphone	ADC value
1	Not connected	V = 1.8V
1	Connected	V < 1.2V
0	Not connected	not defined
0	Connected	not defined

Microphone detection. (ES5 and up)

Detection of none, one or two microphones is done by measuring the difference in current driven by the VREFp buffer. For this purpose the VREFp driver has a current to voltage converter which can be switched to an ADC input. The characteristics of the converter is shown in **Figure 43 on page 73** with bandgap trimmed to 1.8V.

Due process tolerances and microphone bias current variations, it is obvious that calibration of the thresholds for none, one and two microphones is required:

- Disable CIDIN pad protections CODEC_TONE_REG[CID_PR_DIS] = 1
- Set reference voltages for VREFp according to Table 19: CODEC_VREF_PD[BIAS_PD, VREF_BG_PD, AMP_1V5_PD, VREF_PD] =0
- Disconnect VREFp buffer from VREFp pin by enabling CID opamp: CODEC_TONE_REG[CID_PD] = 0
- Measure “Not connected” value with ADC.
- Reconnect VREFp buffer to VREFp pin by disabling CID opamp: CODEC_TONE_REG[CID_PD] = 1

- Measure ADC with one and two microphones connected

Note that microphone detection can not be done while VREF_PD =1.

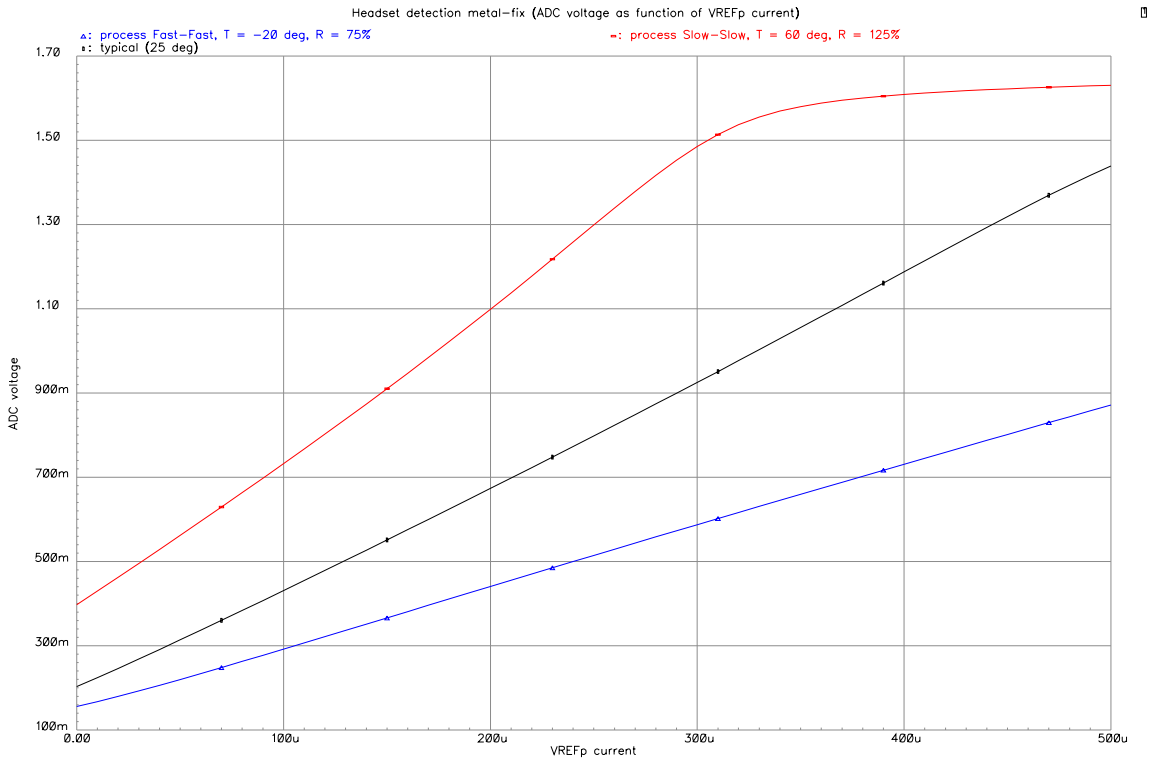


Figure 43 VREFp Current to Voltage converter characteristics. Best (bottom), typical (middle) and worst case (top)

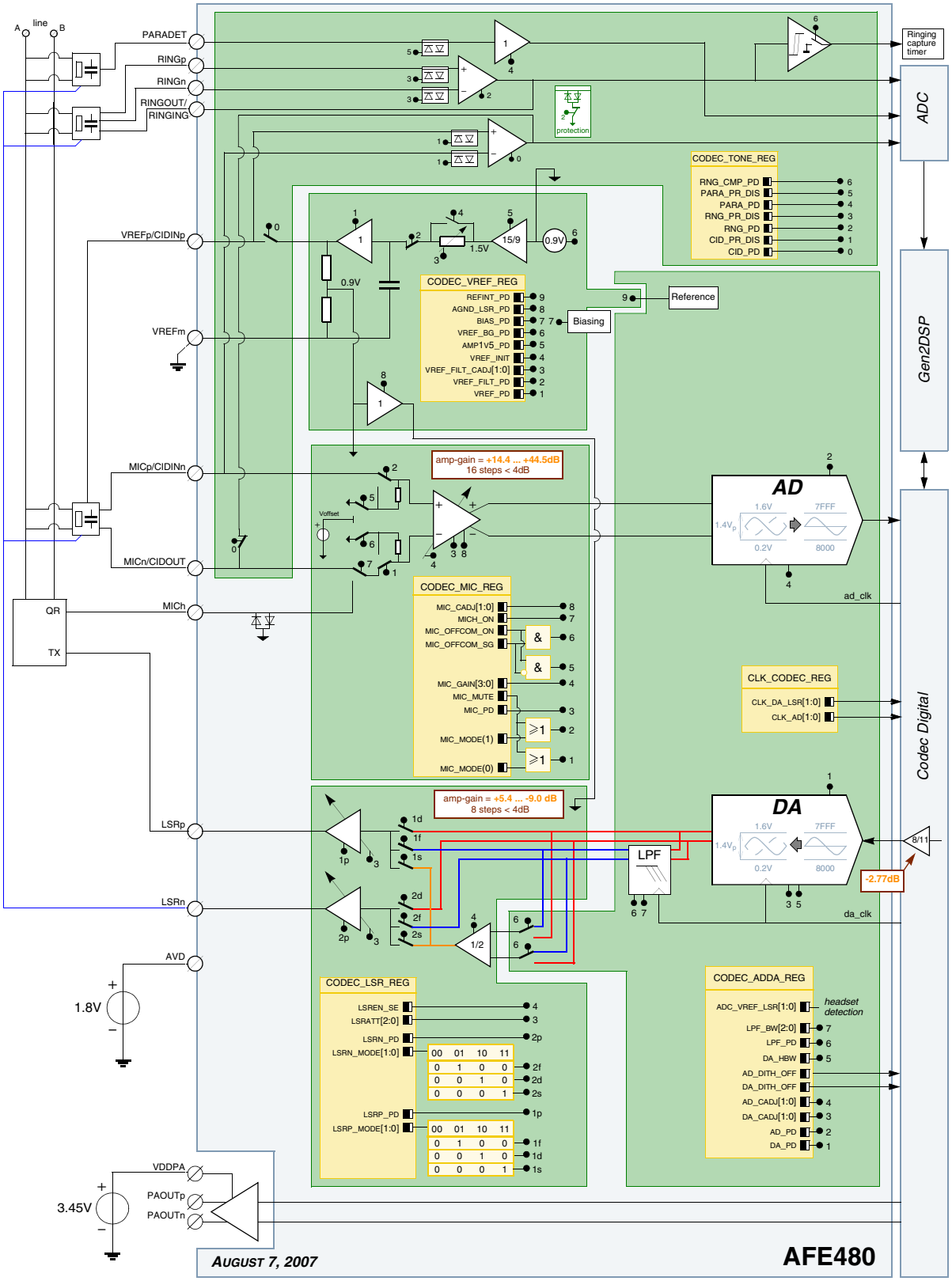


Figure 44 AFE480: fixed part (base) application

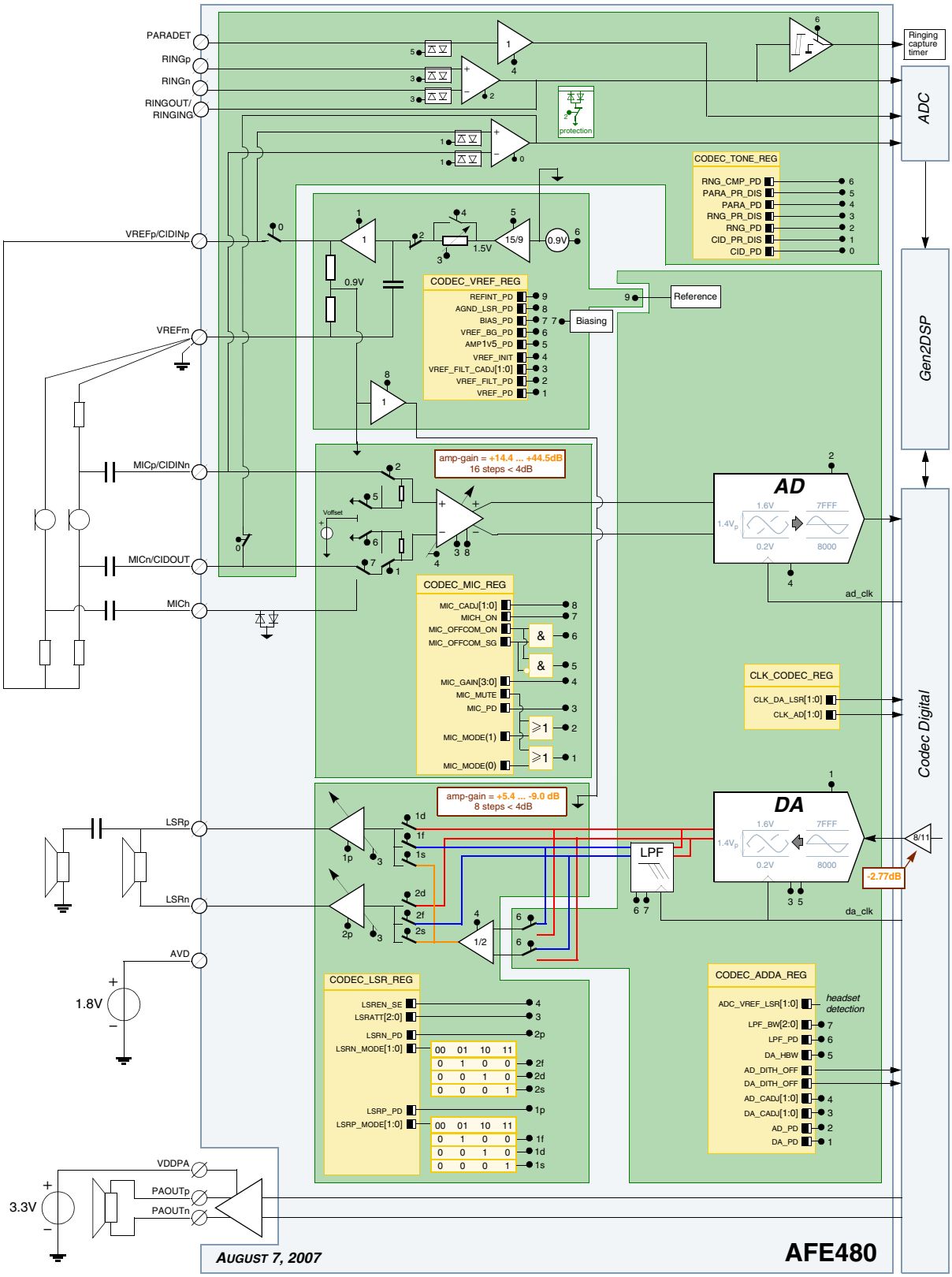


Figure 45 Analog Front End Portable part

13.0 CLASSD Amplifier

The SC14480A5M, SC14480A2M6 has a fully integrated single-supply high efficiency switching “Class-D” type audio amplifier as shown in Figure 46.

Features

- Efficiency at 300mW@2V, 500mW@2.5V into 4 ohm transducer 75%.
- Improved noise reduction.
- Buzzer mode with programmable attenuation
- Digital input mode.
- Separate supply pins for analog drivers
- The output gain and filtering characteristics of the audio signals is performed by the Gen2DSP.
- Anti-plop circuit and output disable mode.
- Independent audio path for CODEC and CLASS-D.
- Outputs can be used as general purpose digital outputs.

13.1 DIGITAL AUDIO MODE PATH SELECTION

See Figure 46.
For CLASS-D access via DSP_CLASSD_REG, set CLK_CODEC_REG[CLK_DA_CLASSD_EN] =1.

For CLASS-D access via DSP_CODEC_OUT_REG, set CLK_CODEC_REG[CLK_DA_CLASSD_EN]=1 and CLK_CODEC_REG[CLK_DA_LSR_EN]=1.

CLK_CODEC_REG[CLK_DA_CLASSD_SEL] must be set to 00 for 1.152MHz/8kHz, 10 for 2.304/16kHz, 11 for 4.608/32kHz operation

13.2 ANTI-PLOP CIRCUIT

In power-down state (CLASSD_PD=1), the PAOUTp and PAOUTm are connected to ground. This mid-level state suppresses a “plop” sound during power-up.

Setting CLASSD_POPEN/ CLASSD_MOPEN to 1, disables the outputs in order to avoid noise pick-up in idle state. In this mode an internal output load of 6k stays connected from the output to VSSPA.

13.3 CLIP DETECTION

The CLASS-D amplifier has a clip detection by monitoring the output signal. When output is high (or low) for a number of periods, programmable between 32 and 2048 with bits CLASSD_CLIP, a CLASSD_INT interrupt is generated. This interrupt must be cleared with CLASSD_CLEAR_INT. Clipping can be stopped by adjusting the gain in Gen2DSP. (See **Note 113: on page 235)**

13.3.1 Buzzer mode

For CLASSD buzzer mode the following bits must be set:

- Gen2DSP: DSP_CLASSD_BUZZOFF_REG[15] = ‘0’ to enable the buzzer mode, or ‘1’ to mute the buzzer. This register must be set to mute the buzzer output without audible side effects.
- CLASSD_BUZZER_REG[CLASSD_BUZ_MODE] =1 to switch from audio to buzzer mode.
- CLASSD_BUZZER_REG[CLASSD_BUZ_GAIN] can be set as desired.
- Depending on the selected audio path, either DSP_CLASSD_REG or DSP_CODEC_OUT_REG is used as audio output register for the GenDSP.

13.4 DIGITAL OUTPUTS

The PAOUTp and PAOUTm outputs can also be used as GPO ports by setting P3_MODE_REG. The output level can be set with P3_DATA_OUT_REG[1-0].

13.5 POWER SAVING

Enabling the CLASSD output stage will consume power, also in “digital output port mode”. Refer to Supply currents (Indicative value) (table 275, page 221). For power saving, it is recommended to set CLASSD_PD to 1 if the CLASS-D amplifier is not used. If only the CLASS-D amplifier is used without the CODEC, the CLASS-D audio path selection is recommended to disable all not used analog block (MIC_PD, LSRN_PD, LSRP_PD, AD_PD, DA_PD all set to 1). In general, only blocks that are needed must be switched on.

13.6 NOISE REDUCTION CIRCUIT

The noise reduction circuit combines good PSSR at high signal levels with low noise at low signal levels.

When the level of the input signal is below a certain level (programmable with CLASSD_NR_LVL) for at least a certain time (programmable with CLASSD_NR_TON), the "noise reduction" is enabled.

When the input level comes above the threshold level plus an optional offset (programmable with CLASSD_NR_HYST), the "noise reduction" is disabled.

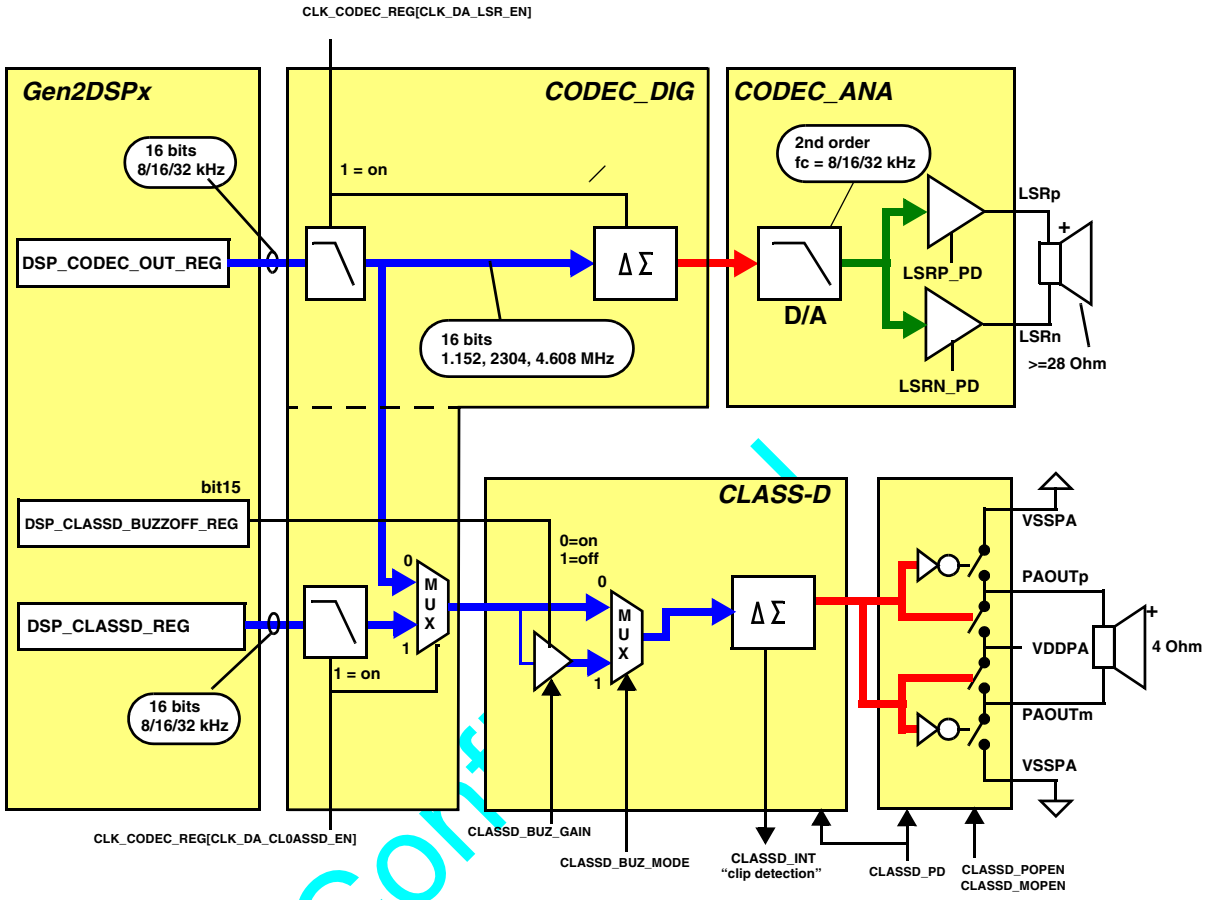


Figure 46 CLASS D amplifier

14.0 Input/Output ports

The SC14480A5M, SC14480A2M6 has software-configurable I/O pins, organized into six 8-bits ports. The ports are named Port 0, Port 1, Port 2 and Port 3, Port4, Port5.

In addition to their general-purpose I/O capability, the I/O pins of the ports have alternate functions for use with on-chip peripheral modules such as the UART or the Access bus. The alternate functions of all I/O pins are shown in Table 21.

Table 21: Alternate functions of the I/O pins

Bit	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5
7	SPI_DI/PWM1	CHARGE **(Note 34)**	INT7/BXTAL	RINGp		
6	SPI_DO	PON **(Note 34)**	INT6/WTF_IN	RINGn		
5	SPI_CLK	INT5/RDI/VDDE	PCM_FSC/SF	RINGING/RINGOUT		
4	SPI_EN	INT4/TDOD	SCL1/PCM_DO/DP3 **(Note 35)**	PARADET		
3	SCL2 **(Note 35)**	INT3/SIO/INT8	SDA1/PCM_DI/DP2 **(Note 35)**	ADC0	SPI2_DI	
2	SDA2 **(Note 35)**	INT2/SK/INT7	CLK100/PCM_CLK		SPI2_DO	
1	URX/PWM0	INT1/LE/INT6	ECZ2/PWM1/LED4	PAOUTp/DP1 **(Note 36)**	SPI2_CLK	
0	UTX	INT0/ADC1	ECZ1/PWM0/LED3	PAOUTn/DP0 **(Note 36)**	SPI2_EN	

Note 34: Input only and with a fixed pull-down resistor (270 kΩ)

Note 35: The output can be push-pull or open-drain.

Note 36: Output only and with a fixed pull-down resistor to discharge loudspeaker coil.

The I/O pin characteristics are programmable. The pins can be configured to operate as a push-pull output, pull-up input, pull-down input or high-impedance input. Furthermore, the pins P0[2-3] and P2[3-4] can either be push-pull or open-drain outputs. Different pins within the same port can be individually configured. Figure 47 and Figure 48 are diagrams showing the I/O port pin logic. The register bits, multiplexer, and buffers allow the port pin to be configured into the various operating modes. The pull-up or pull-down, if used, prevents the port pin from going to an undefined state when it operates as an input.

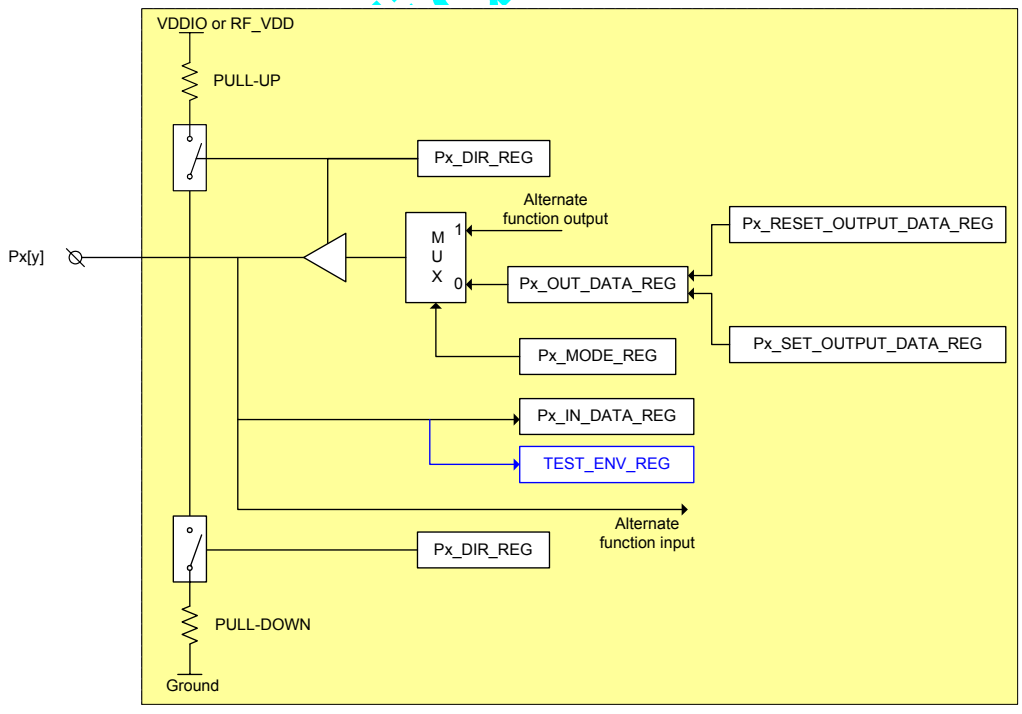


Figure 47 Port Pin Logic (push-pull output only)

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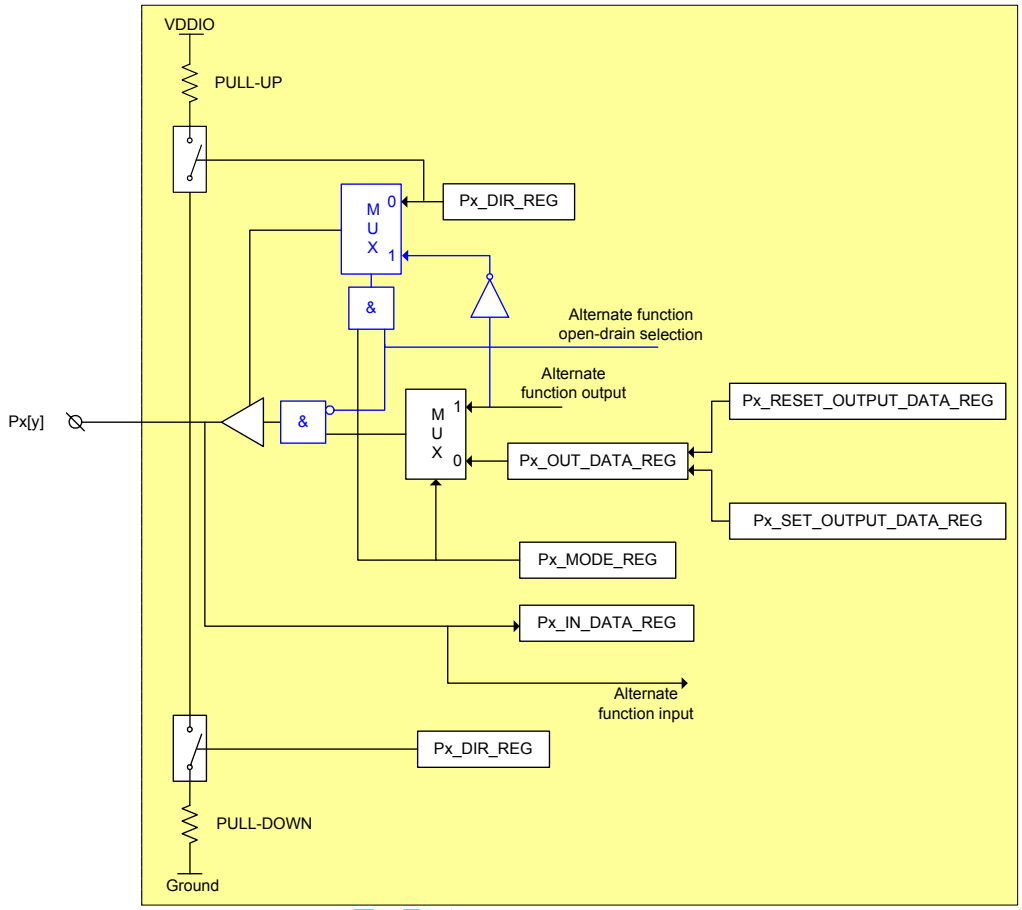

Figure 48 Port Pin Logic (push-pull and open-drain outputs)

14.1 PORT REGISTERS

Each port has an associated set of memory-mapped registers used for controlling the port and for holding the port data:

- Px_MODE_REG: Port alternate function register
- Px_DIR_REG: Port direction and pull-up/down selection register
- Px_IN_DATA_REG: Port data input register
- Px_OUT_DATA_REG: Port data output register
- Px_SET_OUTPUT_DATA_REG: Port set output register
- Px_RESET_OUTPUT_DATA_REG: Port reset output register

14.1.1 Port Mode Register (Px_MODE_REG)

The Px_MODE_REG registers control whether the port pins are used for general-purpose I/O or for their alternate function. Each port pin can be controlled independently.

The selection between the general purpose I/O's and the alternate functions is described in the port alternate function registers P0_MODE_REG (0xFF4838) to P5_MODE_REG (0xFF4868)

A reset operation clears the port alternate function registers, which initializes the pins as general-purpose I/O ports. This register must be enabled before the corresponding alternate function is enabled.

The port pins P1[3] and Port P1[4] can also be configured as current source for driving the base of an external NPN transistor without series resistance.

14.1.2 Port Direction Register (Px_DIR_REG)

The port direction register (Px_DIR_REG) determines whether each port pin is used for input or for output, and whether a pull-up or pull-down resistor is used.

All pins, expect P1[5]/VDDE, P3[0]/PAOUTn and P3[1]/PAOUTp operate as an input after a reset. The port P1[5] is output from start-up and can be used as a supply for an external **EEPROM**.

The direction and the pull-up/pull-down resistor selec-

tion is described in the port direction registers Px_DIR_REG.

14.1.3 Port Data Input Register (Px_IN_DATA_REG)

The data input register (Px_IN_DATA_REG) is a read-only register that returns the current state on each port pin. The CR16Cplus can read this register at any time even when the pin is configured as an output.

The registers Px_OUT_DATA_REG and Px_IN_DATA_REG are mapped on the same address.

14.1.4 Port Data Output Register (Px_OUT_DATA_REG)

The data output register (Px_OUT_DATA_REG) holds the data to be driven on output port pins. In this configuration, writing to the register changes the output value.

The registers Px_OUT_DATA_REG and Px_IN_DATA_REG are mapped on the same address.

14.1.5 Port Set Data Output Register (Px_SET_OUTPUT_DATA_REG)

Writing a 1 in the set data output register (Px_SET_OUTPUT_DATA_REG) sets the corresponding output pin. Writing a 0 is ignored.

14.1.6 Port Reset Data Output Register (Px_RESET_OUTPUT_DATA_REG)

Writing a 1 in the reset data output register (Px_RESET_OUTPUT_DATA_REG) resets the corresponding output pin. Writing a 0 is ignored.

14.2 OPEN-DRAIN OPERATION

The port pins P0[2-3] and P2[3-4] can be configured to operate as an open-drain output buffer when the alternate function (ACCESS or PCM bus) is selected. The open-drain mode is selected in the control register for the alternate functions.

Notes: PAD_CTRL_REG[P234_OD] bit overrules the ACCESS1_CTRL_REG bits SDA_OD and SCL _OD

PAD_CTRL_REG[P023_OD] bit overrules the ACCESS2_CTRL_REG bits SDA_OD and SCL _OD

PAD_CTRL_REG[P234_OD] bit overrules the DSP_PCM_CTRL_REG bit PCM_PPOD.

Open drain mode using ACCESSx_CTRL_REG[SDA_OD, SCL_OD] and DSP_PCM_CTRL_REG[PPOD] bits will reach the 'HIGH' pull-up output voltage in two steps. First step is 1.8V + 0.6V for the duration of about 10 to 20 usec. In the second step, the output stage is fully open drain and the output voltage reaches the pull-up voltage.

The problem does not occur if SDA_OD=0, SCL_OD=0 resp PCM_PPOD=0 and corresponding PAD_CTRL_REG[Pxx_OD] = 1.

In devices were this problem is solved, (see SC14480_buglist.xls), the alternative method by setting PAD_CTRL_REG[xx_OD] only, can also be used here, This guarantees compatible SW between the FLASH and ROM device.

(See **Note 43: on page 148)** (See **Note 69: on page 182)**

14.3 BACK DRIVE PROTECTION

Backdrive protected pins allow interfacing with devices using VDDIO upto 3.45 V.

If PAD_CTRL_REG[xxx_OD] bit is set then

1) The internal Pull-up resistors are always disabled to prevent currents from 1.8V< Vin <3.45 to VDD.

2) If port is set to output, the output is always configured as open drain to allow the output level to reach VDDIO >1.8V. The external pull-up resistor value determines the rise time of the signal.

Refer to pinning which pins have backdrive protection

15.0 Keyboard interface

A **keyboard** function can be made using P0 as output and P1 as input. Six port input pins can be programmed to generate a KEYB_INT interrupt. Three of the six pins can be configured as general purpose interrupt input. PON and CHARGE pins can also be “ored” together with the P1 port to generate a keyboard interrupt. The PON and CHARGE pins can be programmed to bypass the debounce filter.

Features

- Up-to 6 maskable interrupt pins
- Trigger on the positive or negative edges with or without debounce timer
- Separate PON, CHARGE (rising, falling) interrupts
- 3x edge/level interrupts shared with keyboard interrupt.
- Keyboard interrupt on key release.
- The debounce timer is programmable from N x 1ms N=0-63.
- Automatic keyboard interrupt on key pressed condition. The repeat time is programmable from N x 1ms N=1-63.
- Keyboard Status register with interrupt vector.

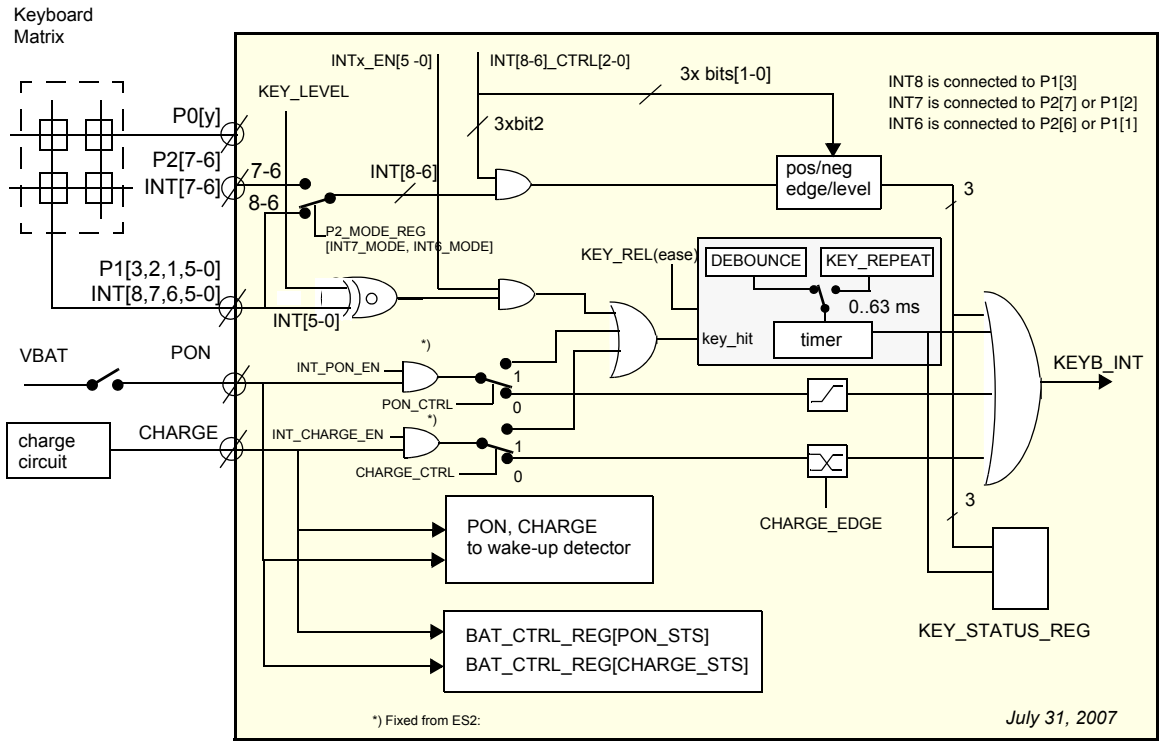

Figure 49 Interrupts, PON, CHARGE block diagram

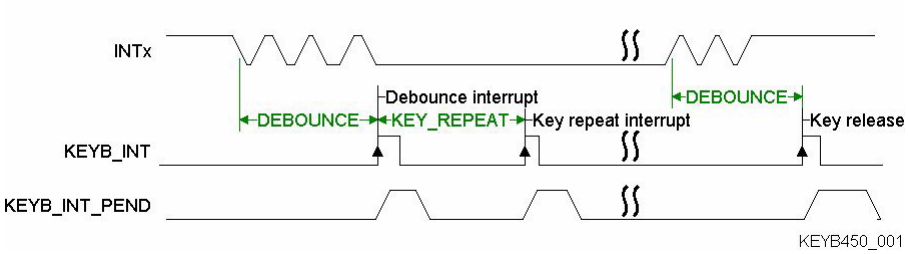

Figure 50 Basic Keyboard debounce and key repeat timing

Keyboard debounce timer and key repeat interrupt

(see Figure 50) A high to low level transition on one of the port inputs INTx, while bits KEY_LEVEL =0 and INTx_EN =1, sets internal signal “key_hit” to 1. This signal triggers the keyboard interface state machine as depicted in Figure 51. The debounce timer is loaded with value KEY_DEBOUNCE_REG[DEBOUNCE]. The timer counts down every 1ms. If the timer is 0 and the “key_hit” signal is still ‘1’, the timer is loaded with value KEY_DEBOUNCE_REG[KEY_REPEAT], generating a repeating sequence of interrupts every time the timer reaches 0.

If the key is released (key_hit = 0) and bit KEY_REL (key release) is set, a new debounce sequence is started and a KEYB_INT is generated after the debounce time.

The debounce timer can be disabled if DEBOUNCE is set to 0. Similarly, the key repeat function can be disabled if KEY_REPEAT is set to 0.

The low to high or high to low level change is programmable with bit KEY_BOARD_INT_REG[KEY_LEVEL], the key release function can be disabled with bit KEY_BOARD_INT_REG[KEY_REL] set to 0. One or more interrupts can be enabled by setting the corresponding KEY_BOARD_INT_REG[INTx_EN] to ‘1’.

The keyboard interrupt routine can distinguish which INTx has caused the interrupt by reading the P0_DATA_REG or P1_DATA_REG.

General purpose interrupts

Three of the six interrupt signals can be configured to generate an interrupt on a rising or falling edge or on a positive or negative level. Refer to KEY_GP_INT_REG[INT8-5_CTRL] bits. The edge detection is done with a frequency of 1.152 MHz, so will introduce a latency of appr 3us before the ICU is triggered.

Status registers

The status of the PON and CHARGE signals is described in "Power-on status" on page 29 and status bits can be found in BAT_STATUS_REG (0xFF4816) (table 80, page 153). The value of the CHARGE pin after 100 Hz filter, can best be read from the BAT_STATUS_REG[CHARGE_STS]. If this bit returns ‘1’ after it is cleared, the CHARGE pin is still high.

The status of the INT8, INT7, INT6 and keyboard timer can found in KEY_STATUS_REG (0xFF49B6) (table 179, page 189). The status bits can only be cleared by writing a ‘1’. Bits not set to ‘1’, shall be written with a ‘0’. This prevents unwanted interrupt clearing while monitoring this register via JTAG interface.

New interrupts on the same input will not be remembered until the interrupt is cleared.

Typical programming sequence to read and clear the interrupt vector bits:

```
key_vector = KEY_INT_STATUS_REG;
KEY_INT_STATUS_REG = key_vector;
```

Interface to interrupt control unit (ICU).

The KEYB_INT only generates an interrupt the ICU if the INT3_PRIORITY_REG[KEYB_PRIO] is set unequal to 0. If an interrupt is set, the interrupt must be cleared by writing RESET_INT_PENDING_REG[KEYB_INT_PEND]= ‘1’.

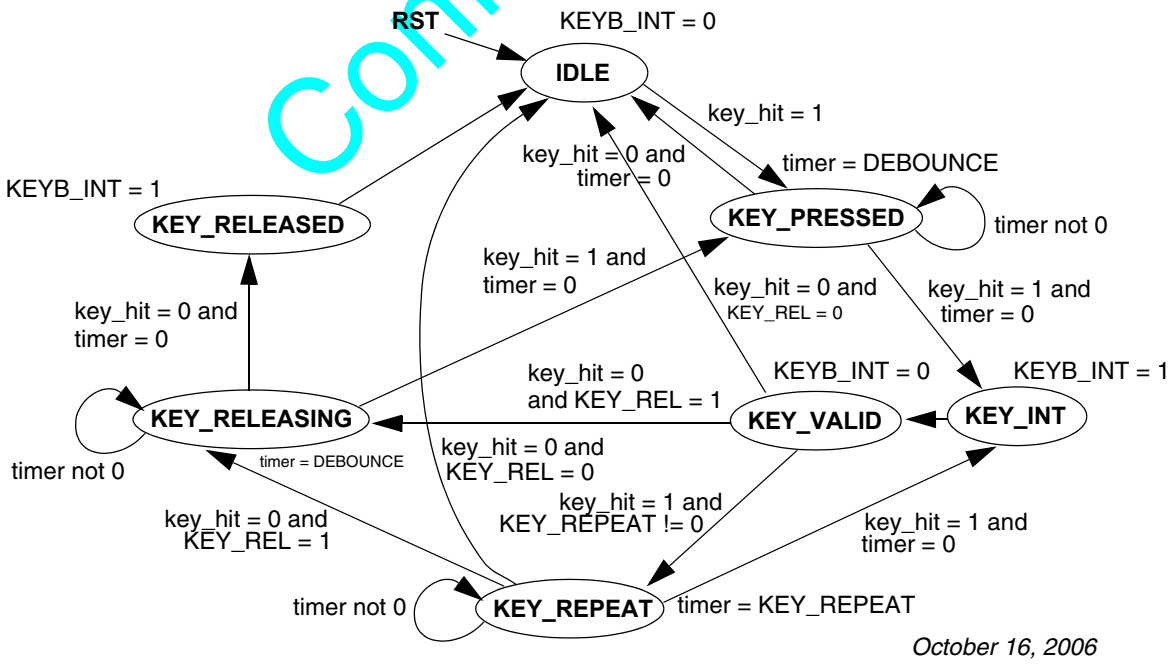

Figure 51 Keyboard interface state machine

16.0 UART

The SC14480A5M, SC14480A2M6 has one full duplex Universal Asynchronous Receiver Transmitter (UART) which interfaces through pins URX and UTX.

Features:

- Full/half duplex operation
- 1 start bit, 8 data bits (LSB first), 1 stop bit
- Baudrates 230.4k, 115.2k, 57.6k, 192000 or 9600 Baud with no parity. 10.125 kBaud with even parity. (Frequencies are based on PER10_DIV output frequency of 10.368 MHz.)
- Maskable receive and transmit interrupts
- DMA operation
- IRDA mode

The baudrates can be selected with UART_CTRL_REG. After reset the baudrate is 9600 baud.

Data loaded in the UART transmit register UART_TX_REG is transmitted on pin UTX. This register is loaded into the TX shift register only if the start bit, 8 data bits and stop bit are transmitted and the TI bit is 0 (no UART interrupt pending). After the shift register is reloaded the UART interrupt pending bit is set to 1. The RI/TI interrupt source can be read in UART_CTRL_REG bit 6 and 5. Data received on pin URX is copied from the RX shift register in UART_RX_REG after detection of the stop bit. After transferring the data to the UART_RX_REG the UART interrupt pending bit is set to 1. After (10 * Rx/Tx Clock) the data received in the UART_RX_REG is overwritten by the next received data bit.

Note: UART_RX_REG and UART_TX_REG are two registers mapped on the same address.

Pull-up resistors are enabled as specified in the pin description.

Additionally 10.125 kbaud can be selected with even parity check on 8 data bits. In case the number of 1s in the received data including the parity bit is not even, the parity error UART_ERROR_REG[PAR_STATUS] is set. In transmit mode the parity bit makes the number of transmitted 1's even.

Transmitter and receiver operation are enabled with bits UART_CTRL_REG[TEN] and REN. If TEN is set to 0 during a transmission of the UART, the transfer is finished normally.

The UART RI and TI interrupts sources must be cleared by writing any value to UART_CLEAR_RX_INT_REG, resp UART_CLEAR_TX_INT_REG. During DMA operation these bits are cleared automatically.

The UART functional behaviour is not affected by the DMA.

For multiplexing UART pins to port pins, refer to P0_MODE_REGs.

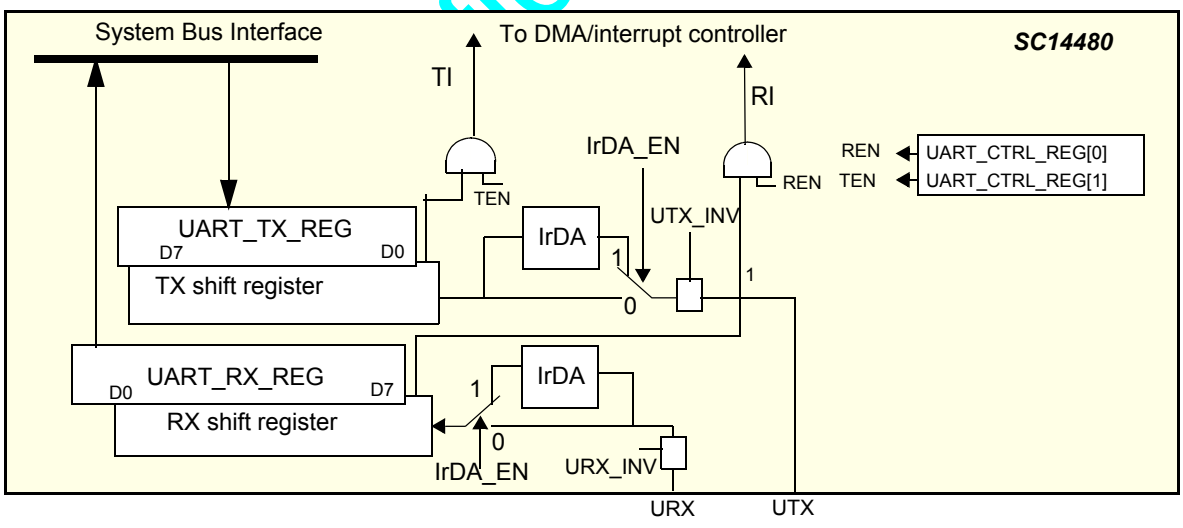

Figure 52 UART blockdiagram

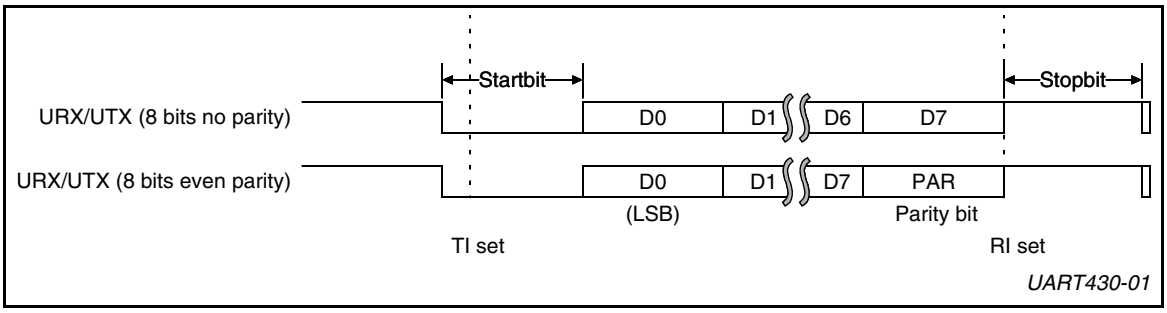

Figure 53 UART data transfer

16.1 IRDA MODE.

The UART (See also 16.0 on page 83) supports bidirectional IrDA data transfer with 1 start bit, 8 data bits and 1 stop bit (LSB first) and no parity. The supported bit rate are 9600, 19200, 57600 and 115200 baud with RZI modulation type.

The UART can be switched to IrDA mode with UART_CTRL_REG bit IRDA_EN=1. The timing signals of a IrDA Frame is shown in Figure 54.

Refer to Table 320 for accurate timing of bit time and pulse width.

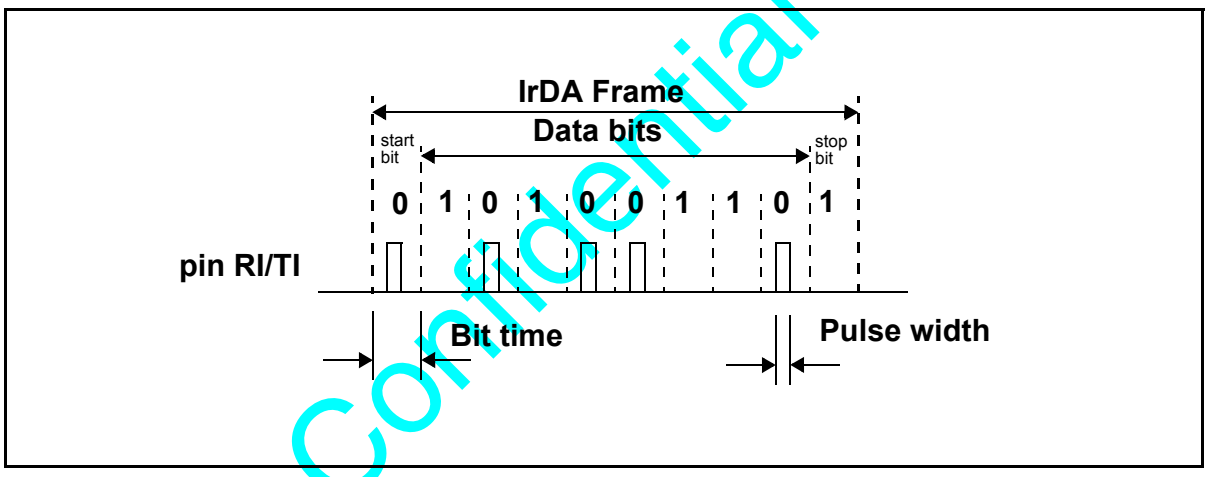

Figure 54 IRDA frame

17.0 ACCESS BUS

The SC14480A5M, SC14480A2M6 has two serial two wire ACCESS Bus interfaces (AB) for communication to a variety of peripheral devices.

Features

- Master transmitter and master receiver mode
- 100kHz, 400 kHz and 1.152 MHz bus clocks.
  (With PER10_DIV output = 10.368 MHz
  100kHz: PER10_DIV output / 104,
  400kHz: PER10_DIV output / 26
  1.152 MHz: PER10_DIV output /9)
- 8 bits (master transmitter only) or 9 bits (8 + acknowledge) transfers
- Open drain or push pull outputs on clock and data
- Clock bit and byte stretching for flow control.
- Both blocks shared the same Interrupt

Interface signals

- SDA = Serial data in/out.
  Selectable push-pull or open drain.
- SCL = Serial clock in/out
  Selectable push-pull or open drain.
  In opendrain mode SCL is is also input to support clock stretch

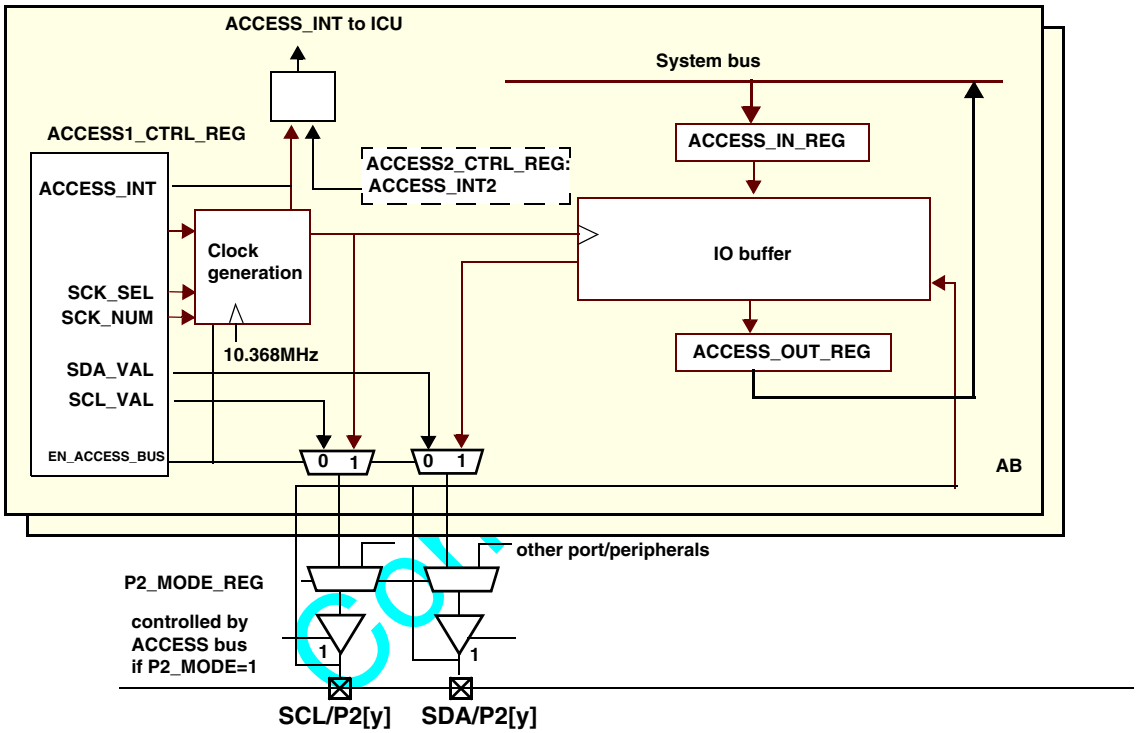

Figure 55 ACCESS bus 1 and 2 block diagram

Port configuration

To enable ACCESS bus operation, the port output multiplexer must be correctly set in P2_MODE_REGs to switch SDA and SCL to the port pins.

If ACCESS bus mode is selected, the driving output state (Hi-Z, Push-pull or Open drain) is fully controlled by the ACCESS bus blocks depending on the state and SCK_NUM, SCL_OD bits. Note that bit SDA_OD and SCL_OD must be correctly set to push-pull or open drain.

Master transmitter mode

Prior to enabling the ACCESS bus interface (ACCESSx_CTRL_REG[EN_ACCESS_BUSx]= 0), the Start condition must be programmed by software with a sequence of ACCESSx_CTRL_REG[SDA_VAL, SCL_VAL] bits: 11->01->00.

Next the ACCESS bus can be enabled with ACCESSx_CTRL_REG[EN_ACCESS_BUSx]= 1. Both SCLx and SDAx are set to 0. After a byte is written in the ACCESSx_IN_OUT_REG, 8 bits are shifted out on SDA (MSB first) and an interrupt is generated.

The interrupt is cleared by writing anything to ACCESSx_CLEAR_INT_REG. If a new byte is loaded the next transfer is started.

In 9 bits mode, (SCK_NUM=1), the received <ACKn>

bit will be stored in the control register ACCESSx_CTRL_REG[ACKn] and interrupt bit ACCESSx_CTRL_REG[ACCESS_INT] is set.

Master receiver mode (9 bits mode only)

Like the master transmitter mode but with <R/Wn> bit D0 set to 1 the ACCESS bus is switched to receiver mode for the next byte(s). More bytes can be consecutively received. When in receive mode, the value of ACCESSx_CTRL_REG[ACKn] will be transmitted in the <ACKn> bit.

Once a complete byte has been received and the <ACKn> bit is transferred an interrupt bit is set in the ACCESSx_CTRL_REG[ACCESSx_INT] (if enabled with EN_ACCESSx_INT) and the SCK is halted until the interrupt bit is cleared by writing anything to CLEAR_ACCESSx_INT_REG. Note that bit SDA_OD must be set to 1 to configure SDA as open drain.

Stop condition

Once one or more bytes are transferred, the ACCESS bus can be disabled again with ACCESSx_CTRL_REG[EN_ACCESS_BUSx]= 0 and a Stop condition must be programmed by software with a sequence of ACCESSx_CTRL_REG[SDA_VAL, SCL_VAL] bits: 00->01->11.

Clock stretching

Clock stretching on SCLx for each bit clock cycle is supported. As soon as the SCLx is set to 1 by the master (transmit or receive mode), the SCLx level is read back. If the level is kept low or pulled low by a slave within 40 ns after the rising edge, the master waits forever until the SCLx line goes high again. As soon as SCLx has reached the value '1', clock stretching is ignored until the next rising edge of SCLx.

Note that SCL must be configured as open drain by (SCL_OD set to 1) in order to avoid conflicts on SCL. If a slave does not support clock stretching, the push-pull mode can be selected to save the pull-up resistor.

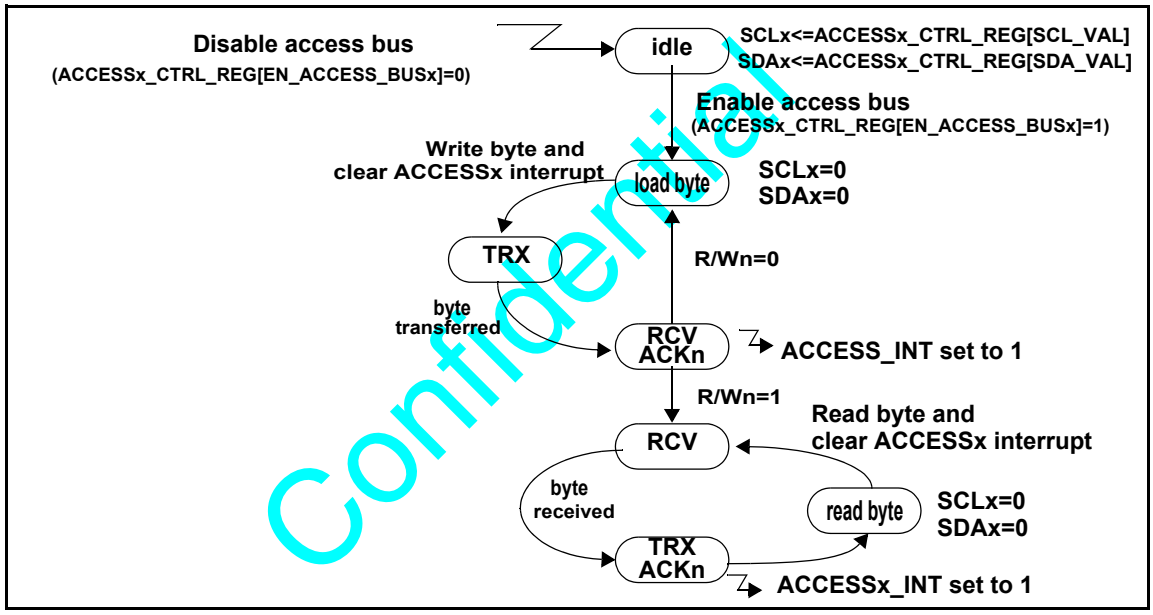

Figure 56 Access bus state machine

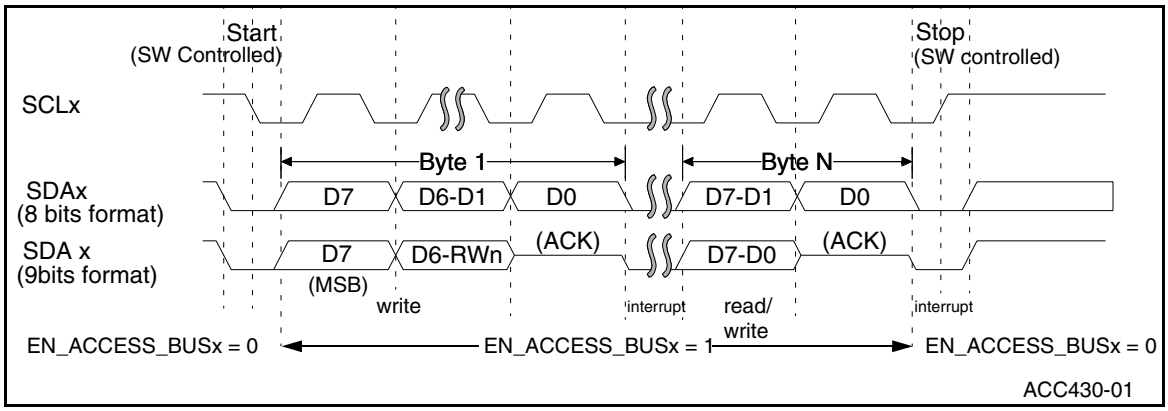

Figure 57 ACCESS bus master write/read access

18.0 SPI™ interface

The SC14480A5M, SC14480A2M6 has a serial synchronous interface to support a subset of the Serial Peripheral Interface SPI™. The serial interface can transmit and receive 8,16 or 32 bits in master/slave.

SPI™ is a trademarks of Motorola, Inc

Features

- Slave and Master mode
- 8 bit, 16 bit or 32 bit operation
- Clock speeds
  Master/slave mode 20.736 MHz Max.
  Programmable frequencies Output of PER20_DIV divided by 2, 4, 8, 14.
- SPI mode 0,1,2,3 support. (clock edge and phase)
- Programmable SPIDO idle level
- Maskable Interrupt generation
- DMA support

Refer to *AN-D-117* for known SPI limitations.

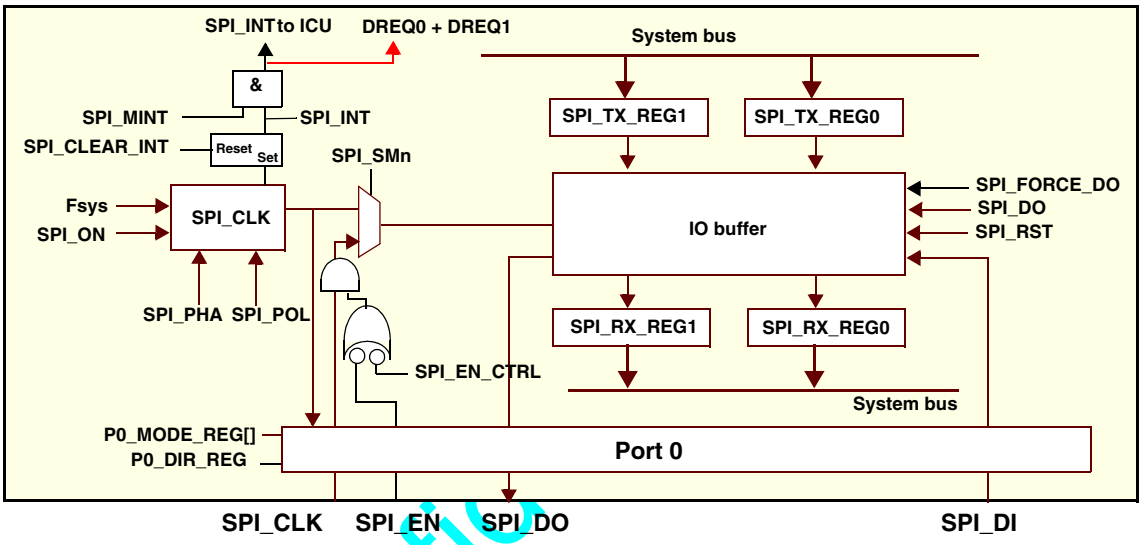

Figure 58 SPI blockdiagram

Master mode

To enable SPI™ operation, first Ports P0 must be configured with P0_MODE_REG, P0_DIR_REG[] must be 1 to enable the SPI_CLK, SPI_DO and SPI_EN outputs. For SPI_DI the respective port pin must be set to input. Next the SPI must be configured in "SPI_CTRL_REG, SPI2_CTRL_REG (0xFF4940, 0xFF4950)" on page 199 for the desired mode. Finally bit **SPI_ON** must be set to 1.

A SPI transfer cycle starts after writing to the SPI_RX_TX_REG0. In case of 32 bits mode, the SPI_RX_TX_REG1 must be written first. Writing to SPI_RX_TX_REG0 also sets the SPI_TXH. As soon as the holding register is copied to the IO buffer, the SPI_TXH is reset and a serial transfer cycle of 8/16/32 clock-cycles is started which causes 8/16/32 bits to be transmitted on SPIDO. Simultaneously data is received on SPIDI and shifted into the IO buffer. The transfer cycle finishes after the 8th/16th/32nd clock cycle and SPI_INT_BIT bit is set in the SPI_CTRL_REG and SPI_INT_PEND bit in INT_PENDING_REG is set. The received bits in the IO buffer are copied to the SPI_RX_TX_REG0 (and SPI_RX_TX_REG1 in case of 32 bits mode) were they can be read by the CR16 in any order.

Interrupts to the ICU can be disabled using the SPI_MINT bit. To clear the SPI interrupt source, any value to SPI_CLEAR_INT_REG must be written.

Slave mode

The slave mode is selected with **SPI_SMn** set to 1 and the SPI_CLK and optionally SPI_EN must be set to input in P0_DIR_REG[]. The SPI has an active low clock enable SPI_EN which can be enabled with bit SPI_EN_CTRL=1. The functionality of the IO buffer in slave and master mode is identical. The SPI module clocks data in on SPI_DI and out on SPI_DO on every active edge of SPI_CLK. As shown in Figure 59 to Figure 62.

SPI_POL and SPI_PHA

The phase and polarity of the serial clock can be changed with bits SPI_POL and SPI_PHA in the SPI_CTRL_REG.

SPI_DO idle levels.

The idle level of signal SPIDO depends on the master or slave mode and polarity and phase mode of the clock.

In master mode pin SPI_DO gets the value of bit SPI_DO if the SPI is idle in all modes. Also if slave in SPI modes 0 and 2, SPI_DO is the initial and final idle level.

In SPI modes 1 and 3 however there is no clock edge after the sampled lsb and pin SPI_DO gets the lsb value of the IO buffer. If required, the SPI_DO can be forced to the SPI_DO bit level by resetting the SPI to the idle state by shortly setting bit **SPI_RST** to 1**.** (Optionally **SPI_FORCE_DO** can be set, but this does not reset the IO buffer). The following diagrams show the timing of the SPI™ interface.

DMA operation

The SPI supports DMA in the 16 bits mode. By triggering two DMA channels simultaneously upon a SPI_INT interrupt, Rx Data can be transferred to memory by using e.g DMA0 channel and Tx data can be transferred from memory to the SPI using DMA1 channel. So the Rx and Tx buffers have the same size.

To enable SPI_INT to DMA0_REQ,
DMA0_CTRL_REG[DREQ_MODE] must be set to 1.
To enable SPI_INT to DMA1_REQ,
DMA1_CTRL_REG[DREQ_MODE] must be set to 1.

To start DMA operation, the first word must be written to SPI_INOUT_REG by the CR16.
Next the SPI_INT triggers both DMA channels and data is copied automatically. DMA0 and DMA1 priorities may **not** have the same priority.

After a DMA supported Tx or Rx burst, the DMA channel can generate an interrupt if DMAx_CTRL_REG[DINT] was set to 1.

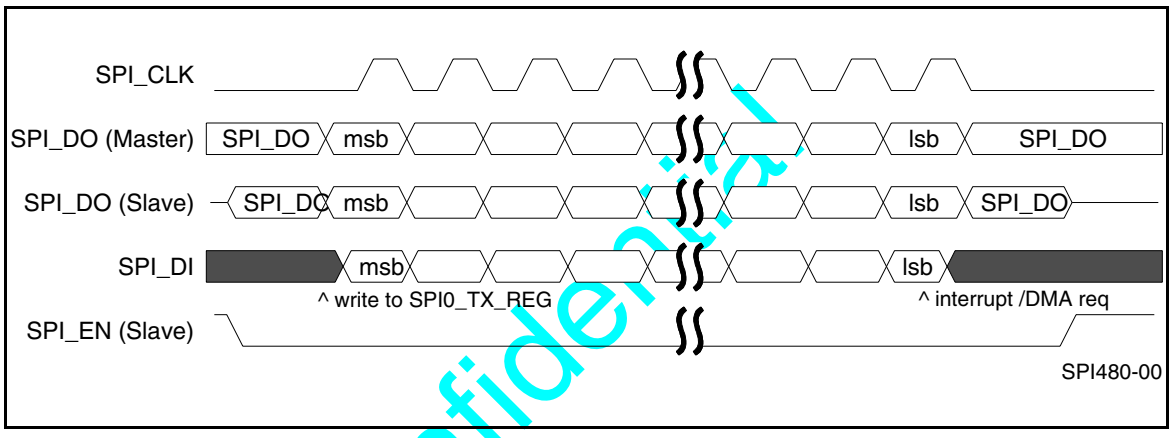

Figure 59 SPI Master/slave, mode 0: SPI_POL=0 and SPI_PHA=0

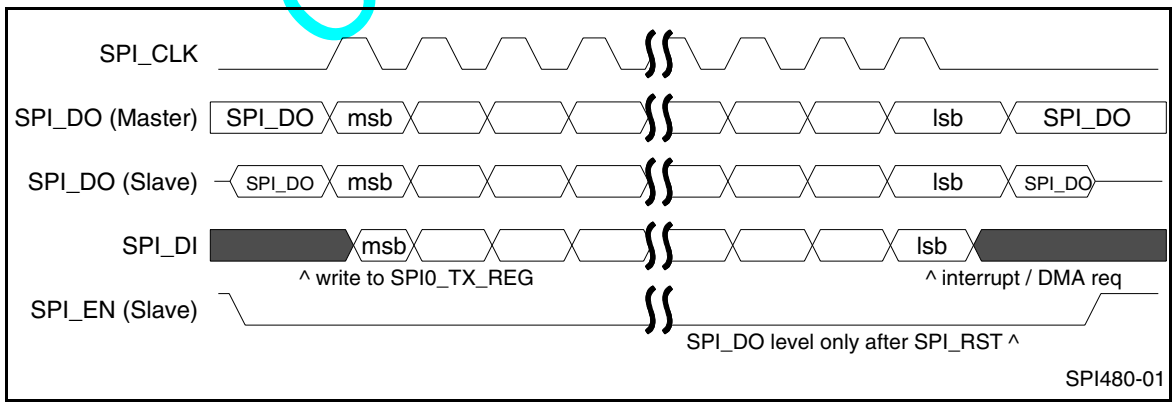

Figure 60 SPI Master/Slave, mode 1: SPI_POL=0 and SPI_PHA=1

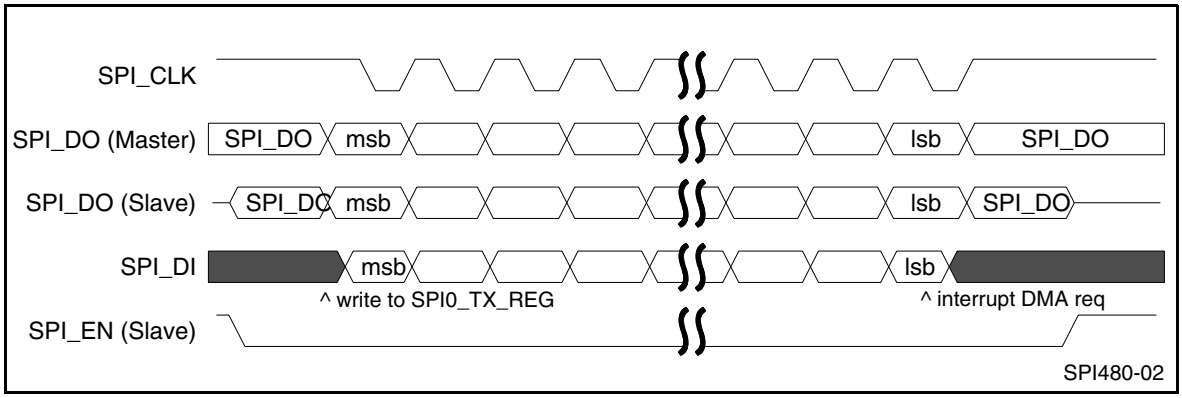

Figure 61 SPI Master/Slave, mode 2: SPI_POL=1 and SPI_PHA=0

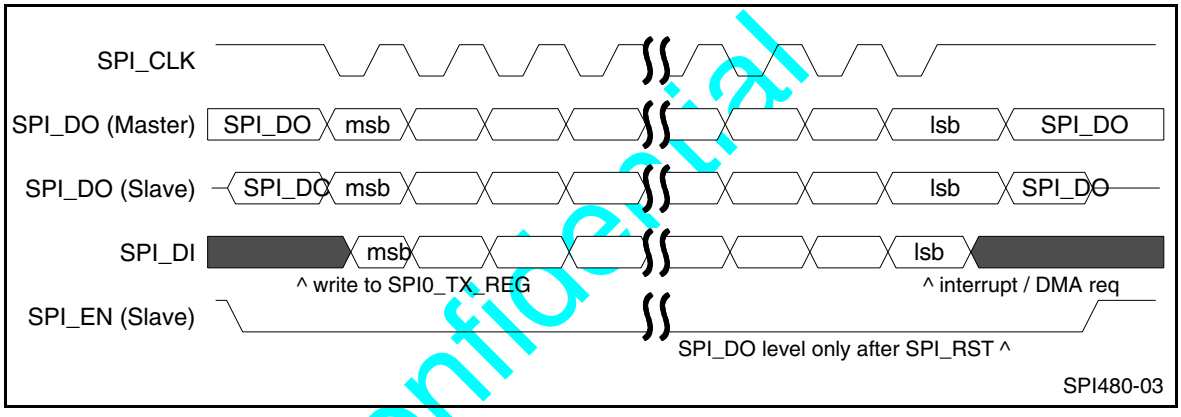

Figure 62 SPI Master/slave, mode 3: SPI_POL=1 and SPI_PHA=1

19.0 ADC

The SC14480A5M, SC14480A2M6 has an 10-bit successive approximation Analog Digital Converter. This ADC is optimized for portable applications for battery and battery temperature applications and fixed part applications to monitor line voltages and measure ring frequencies.

For line interface application protection circuits can be enabled on ADC0, ADC1, ADC2, CIDINp/CIDINn, RINGp/RINGn and PARADET

The temperature sensor is described in "Temperature Sensor" on page 94.

Features

- 10 bits resolution
- Conversion time 55 µs
- External Inputs: ADC0, ADC1, ADC2, Parallel set opamp, ringing opamp, Caller-id opamp (also input of the CODEC) and VBAT monitoring.
- Switchable protection circuits for line application. (See Table 271 on page 218 for characteristics)
- Internal input: temperature sensor.
- Internal input: Codec headset detection
- Manual and automatic mode for real time 8/16 kHz signal processing on the Gen2DSP.

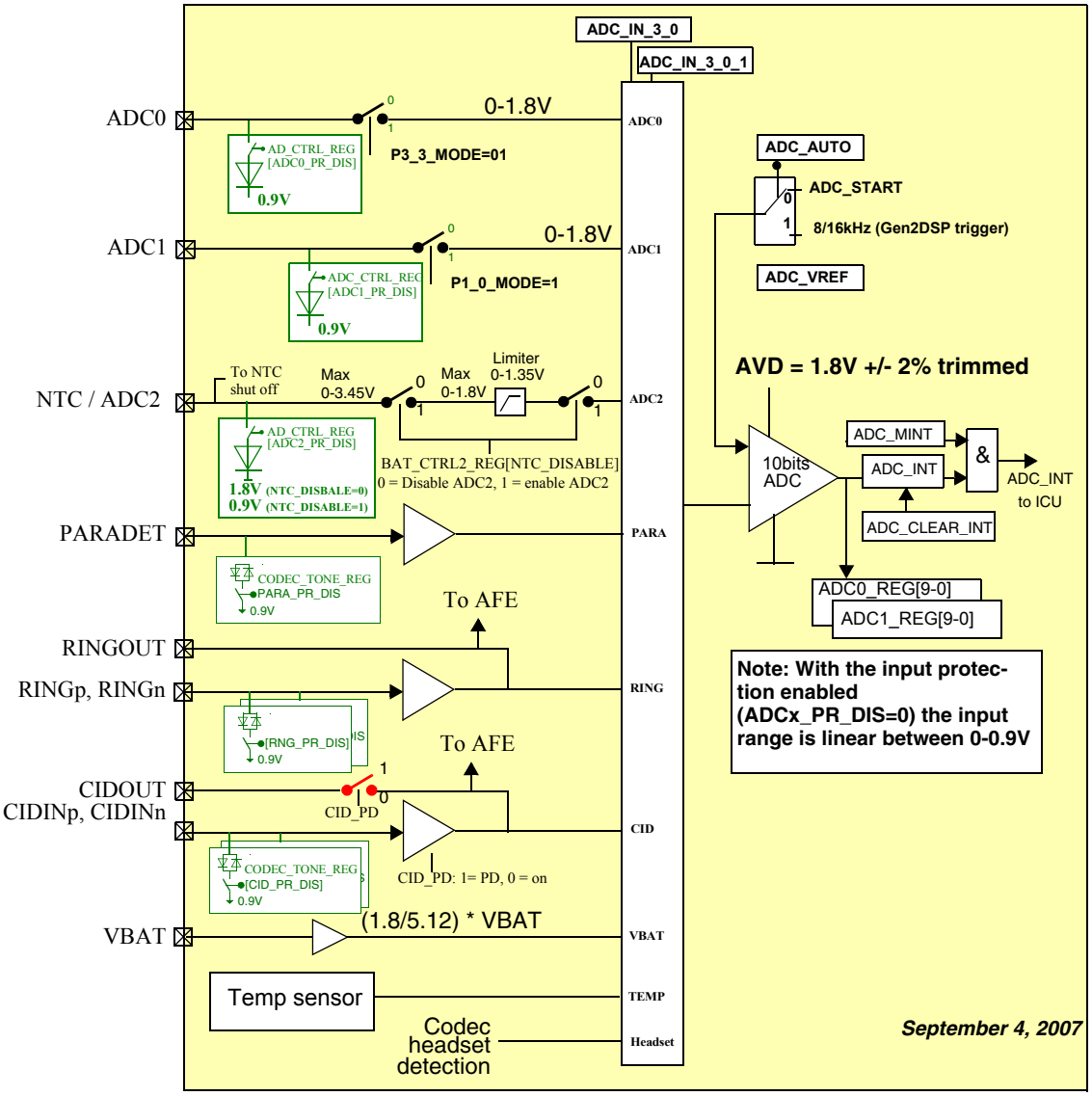

Figure 63 ADC Blockdiagram

Manual ADC conversion

The ADC_CTRL_REG[ADC_IN_3_0] determines which input is selected. An ADC conversion is started by setting ADC_CTRL_REG[ADC_START] equal to 1. After 10 µs the input is sampled for 7µs. During this time an internal capacitive load of 2pF is charged or discharged from AVD/2 to the value of the input pin. The source impedance determines this time constant (See Table 285). After a total conversion time of 50 µs bit ADC_START is automatically cleared to 0 and bit ADC_INT is set. This must be cleared by SW by writing to register ADC_CLEAR_INT. An interrupt to the ICU is only generated if ADC_MINT bit is also set to 1.

Automatic AD conversion

Automatic AD conversion can be used for:

- 8 kHz sampling of in band signals like ringing signal via CID opamp and signal processing by the Gen2DSP.
- Relief of the CR16 from repetitive starting the AD converter and handling interrupts.

Automatic conversion is started by setting ADC_CTRL_REG[ADC_AUTO] to 1, while the automatic conversion is started on the rising edge of signal ADC_SYNC which can be set in DSP_MAIN_SYNC1_REG[ADC_SYNC] (See Figure 64). This signal can be 8/16 kHz.

Input selection

In automatic conversion mode, two separate ADC input can be selected for conversion, e.g ADC0 and Caller-id input by settings ADC_CTRL_REG[ADC_IN_3_0] resp ADC_CTRL1_REG[ADC_IN_3_0_1]. Both ADC_IN_3_0 and ADC_IN_3_0_1 may have the same value.

The output of the ADC is stored always ADC0_REG if ADC_CTRL_REG[ADC_ALT] = 0. If ADC_ALT = 1, samples selected by ADC_IN_3_0 are stored in ADC0_REG and samples selected by ADC_IN_3_0_1 are stored in ADC1_REG. Table 22 shows the maximum sample rate of ADC_SYNC if ADC_ALT =1.

Output format

The converted values stored in ADC0_REG and ADC1_REG in an 10 bits linear format. The Gen2DSP reads these value as 16 bits 2's complement in DSP_ADC0S_REG and DSP_ADC1S_REG for signal processing. In 2's complement notation, bits D9-D0 are converted to 7x(not)D9, D8-D0. The CR16 can read both linear and 2's complement registers. The ADC0_REG and ADC1_REG can not be read by the Gen2DSP but only by CR16Cplus.

Table 22: ADC0_REG and ADC1_REG sample rate

ADC_AUTO	ADC_ALT	ADC0_REG	ADC1_REG
0	0	Manual	-
0	1	Manual	-
1	0	ADC_SYNC	
1	1	ADC_SYNC/2	ADC_SYNC/2

In automatic mode, no ADC_INT is generated. If switching from automatic to manual mode, the current conversion is correctly finished. However a new conversion may only be started after the ADC_START has become 0, otherwise the ADC0_REG may have an unpredictable result for one conversion. Switching from manual to automatic mode may be done at any time without data loss.

Using the caller-id input

To use CID input as general purpose ADC input, CIDOUT must be connected to CIDINn and CIDINp must be used as input.

NTC/ADC2 voltage/current limits

Depending on PP or FP application, the NTC/ADC2 has different requirements which are listen in Table 23.

Li-Ion application

With NTC_DISABLE=0, the input path to the ADC is disconnected allowing up-to 3.45V on the NTC/ADC2 pin for applications to automatically switch off the charger circuit. (see "Charger Auto shut off circuit" on page 26). From start-up the ADC2_PR_DIS is 0 (to be prepared for the ADC2 used in a FP) and must be set to 1 in order not to limit the input voltage.

FP application

With NTC_DISABLE=1, the normal ADC2 path is enabled and he maximum allowed voltage on the ADC2 pin is 1.8V. In FP applications with high line voltages, the ADC2_PR_DIS is set and an external resistor must be used to limit the current 1 mA. (see also Table 271 on page 218). This guarantees the maximum allowed voltage of 2V on the ADC2 input.
(See **Note 97: on page 219)**

Table 23: NTC/ADC2 voltage/current limits

NTC_ DISABLE	ADC2_ PR_DIS	NTC/ADC2 Voltage/ Current limits	Guaran_ teed linear ADC range	Appli_ cation
0	0	3.45V / 1 mA	undefined	Reset
0	1	3.45V / -	undefined	Li-Ion
1	0	- / 1 mA	0-0.9V	FP line
1	1	1.8V / -	0-1.35V	Normal

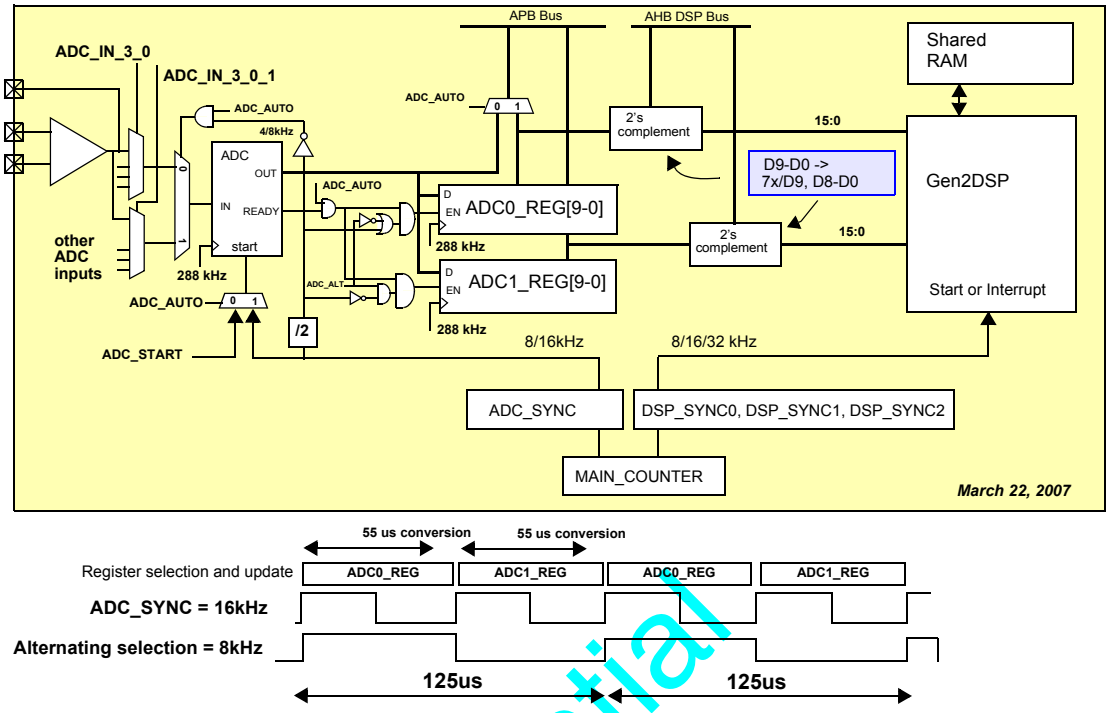

Figure 64 Automatic AD conversion

20.0 Temperature Sensor

The SC14480A5M, SC14480A2M6 contains an on-chip temperature sensor for measuring temperatures between 5 degrees and 55 degrees Celsius. The temperature sensor has a negative temperature coefficient α which must be determined during equipment production by measuring the ADCout value at room temperature and solving the equation ADCout = $\alpha * T + 2960$. (T in Kelvin, ADCout is decimal value of ADC) Refer to Temperature sensor (table 284, page 227) for the minimal and maximal ranges of α.

Figure 65 shows transfer characteristic of the temperature sensor.

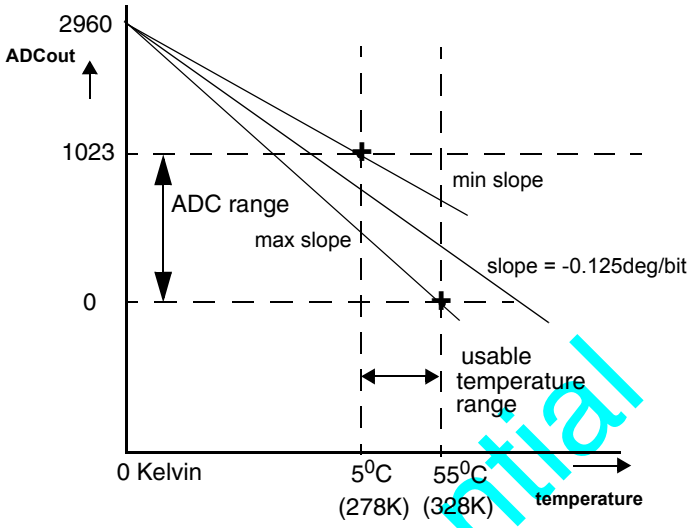

Figure 65 Temperature sensor

21.0 Charge pump

21.1 CHARGE PUMP TRIPLER

The Programmable Charge pump **tripler** provides two programmable output voltages of 2x 4.5V max at pins CP_VOUT1/LED1, CP_VOUT2/LED2. White LEDs can be connected to the outputs, but the generated voltage also provide an auxiliary supply voltage of 2.5/3V for external devices.

Features

- Simple charge pump for cheap 1 uF external capacitors.
- Direct connection to 2 cells battery
- 2 independent outputs groups with programmable CP_VOUTx voltage 2.5, 3.0, 4.0, 4.5 V
- Automatic low power mode selection in case of low load.
- Each output can be dimmed by a separate PWM timer T2. If PWM is 100%, the intensity is maximum.
- Parallel mode for high current applications

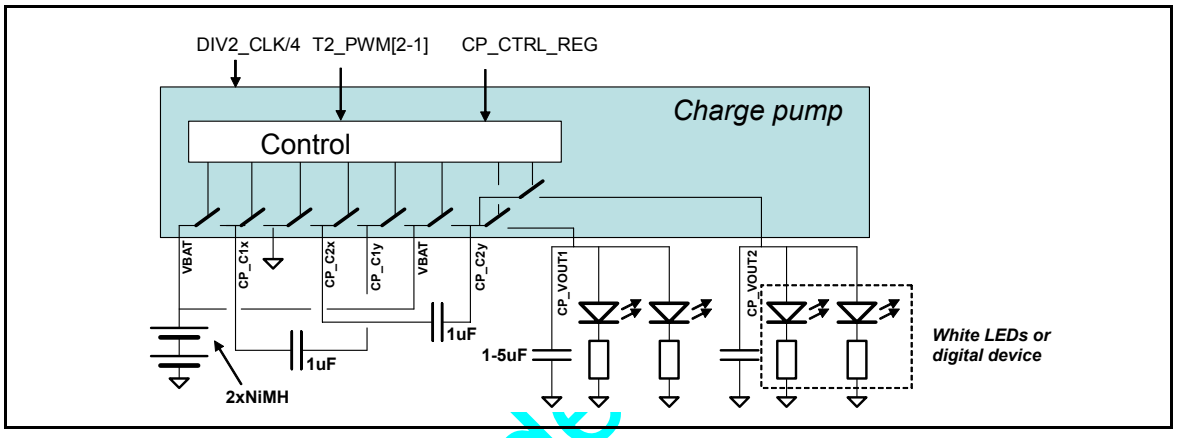

Figure 66 Charge pump blockdiagram

Operation

The charge-pump performs a 3x operation. When the voltage becomes higher then the programmed output voltage (2.5/3/4/4.5V), the charge-pump is stopped until the voltage drops below the wanted level.

The maximum total output **current** depends on the battery voltage, the required output voltage and the internal resistance Rcp of the charge pump and selected frequency in CP_FREQ, see Figure 67. Refer to **Table 278 on page 223 for the charge pump specification**

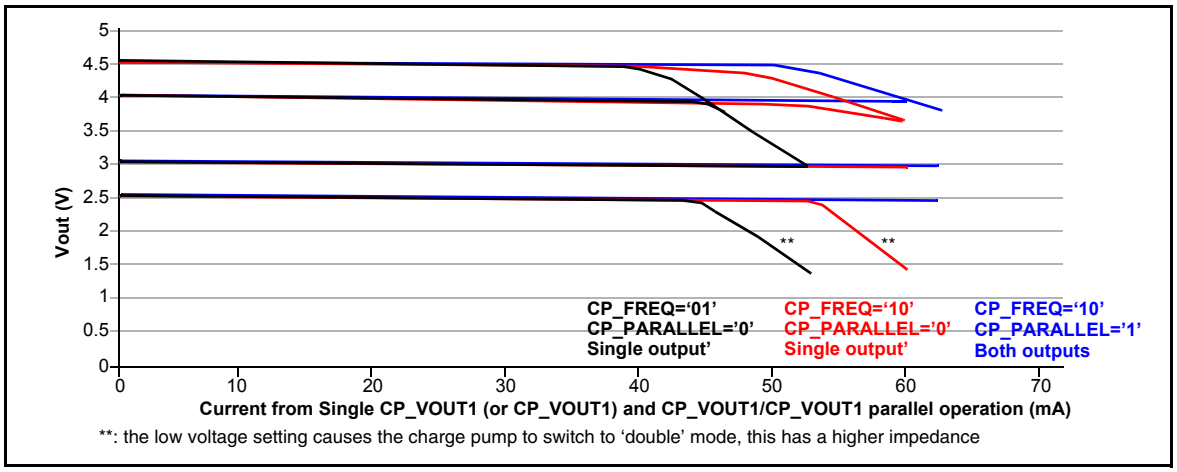

Figure 67 Typical Charge pump output characteristic (Vbat = 2.1V)

Typically 50 mA for CP_VOUT1 and 10mA for CP_VOUT2 is feasible. (CP_VOUT1 and CP_VOUT2 may be interchanged but the booter assumes that CP_VOUT2 is used for a SPI FLASH)

The voltage difference (3xVBAT-Vcp_out) is dissipated in the switches of the charge-pump. With 4.5V output voltage the lowest on-chip dissipation achieved, but the maximum allowed current is limited **(see Figure 67)**. With 4V output voltage, the maximum current is higher but the LED currents must have a better match because the series resistors have a lower value. External series resistors are used to adjust the currents and to balance to currents over the LEDs.

Output Ripple

The ripple depends on the output capacitor, output current and the selected frequency. Each output has a current limiter of approx. 300mA +/- 30%.
The output ripple can be calculated with the following formula.

$$\text{Vripple} = \frac{\text{(current limit - output current) x output period}}{\text{output capacitor}}$$

The output period for the three CP_FREQ settings are:

- '00' -> 384ns (PER10_DIV clock / 4)
- '01' -> 768ns (PER10_DIV clock / 8)
- '10' -> 1536ns (PER10_DIV clock / 16)

For the lowest ripple settings this results in the following:

Vripple = (300mA - 0mA) x 384ns) / 1uF = 115mV

To reduce the ripple, increase the output capacitor or increase the frequency. Also refer to *AN-D-159 "SC14480 Charge pump voltage tripler"* for more details about using the charge pump in low current applications

Single output/Parallel operation

In cases were the lowest output resistance Rcp is required, CP_CHARGE[CP_PARALLEL] must be set and CP_VOUT1 and CP_VOUT2 must connected to each other. In this parallel operation the output resistance is reduced by approx. 10%, and the output voltage is controlled with CP_VOUT1 only.

Voltage/intensity control

The two charge-pump output voltages on CP_VOUT1 and CP_VOUT2 can be controlled independently. The outputs can be programmed at different output voltages. For example one output can be used for 3V supply voltage for an external SPI FLASH and the other for e.g 4.5V white LED. The LED voltage/intensity be controlled in the following ways:

- CP_CTRL_REG[CP_LEVELx] sets the maximum CP_VOUTx voltage to 2.5, 3.0, 4 or 4.5V.
- The CP_VOUTx voltage can be reduced by switching on/off the Charge pump output using the **PWM** outputs of timer 2. To enable this feature, CP_CTRL_REG[CP_PWMx] must be set. The Timer 2 duty cycle ranges from 0 to 100%. If CP_VOUT2 is used for the **supply of external devices, this bit shall be kept to 0**. The charge-pump/Timer2 control can also be temporarily suspended to suppress switching noise this feature is useful during an RF Rx or Tx burst. Refer **"PWM timer2" on page 102** for this feature.

Low power mode

The charge pump has a low power mode which is automatically activated at low load currents. So when supplying e.g and LCD display at 3V, the charge-pump's low power mode has a positive effect on power consumption.

General Purpose Output

Refer to *AN-D-155 "SC14480 Using the tripler as General Purpose Port"*

22.0 LED drivers

Two currents sources of are available on P2[0]/LED3, P2[1]/LED4 for small (red) LEDs **(see Figure 68):**

- 2x 2.5/5 mA

These port are backdrive protected can handle up-to 3.45V. The anode of these LEDs can be directly connected to the two cells battery voltage **without resistors**.

In analog mode there is no Timer0 PWM control on these PADs.

Using P2[0] and P2[1] to control LEDs in digital mode with external resistors and the Timer0 PWM should be avoided in order not to affect RF performance.

The use white LEDs refer to chapter “Charge pump”.

Controlling the current sources

To enable the current sources set

- PAD_CTRL_REG[P20_OD/P21_OD] = ‘1’ in order to disable the pull-up resistor to VDD permanently. P20_OD/P21_OD = ‘0’ would not damage the PAD but would cause a small current via the pull-up resistance to VDD.
- P2_MODE_REG[P2_0_MODE/P2_1_MODE] = 11 to select LED3/LED4 mode and **switch on** the LEDs
- P2_MODE_REG[P2_0_MODE/P2_1_MODE] = 00 to **switch off** the LEDs
- P2_DIR_REG[P2_0_DIR/P2_1_DIR] = 00
- PAD_CTRL_REG[LED3_CUR/LED4_CUR] 0 = 2.5 mA, 1 = 5 mA

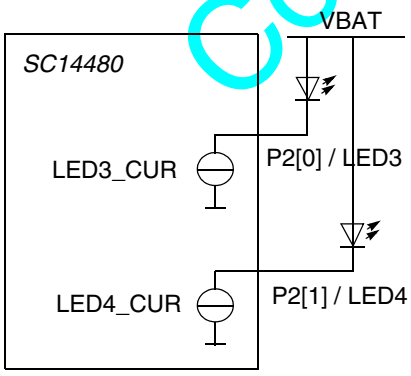

Figure 68 LED3 and LED4 connections

23.0 Timers

23.1 TIMER0

Timer 0 generates the Pulse Width Modulated signals PWM0 and PWM1 and the CR16C interrupt.

Features

- Programmable output Frequency = (1.152 MHz or 115.2 kHz) / (M+1)+(N+1) N=0..(2**16)-1, M=0..(2**16)-1
- Programmable duty cycle: (M+1)/((M+1)+(N+1)) *100%
- Separate Programmable interrupt timer (1.152MHz or 115.2 kHz)/ (ON+1)

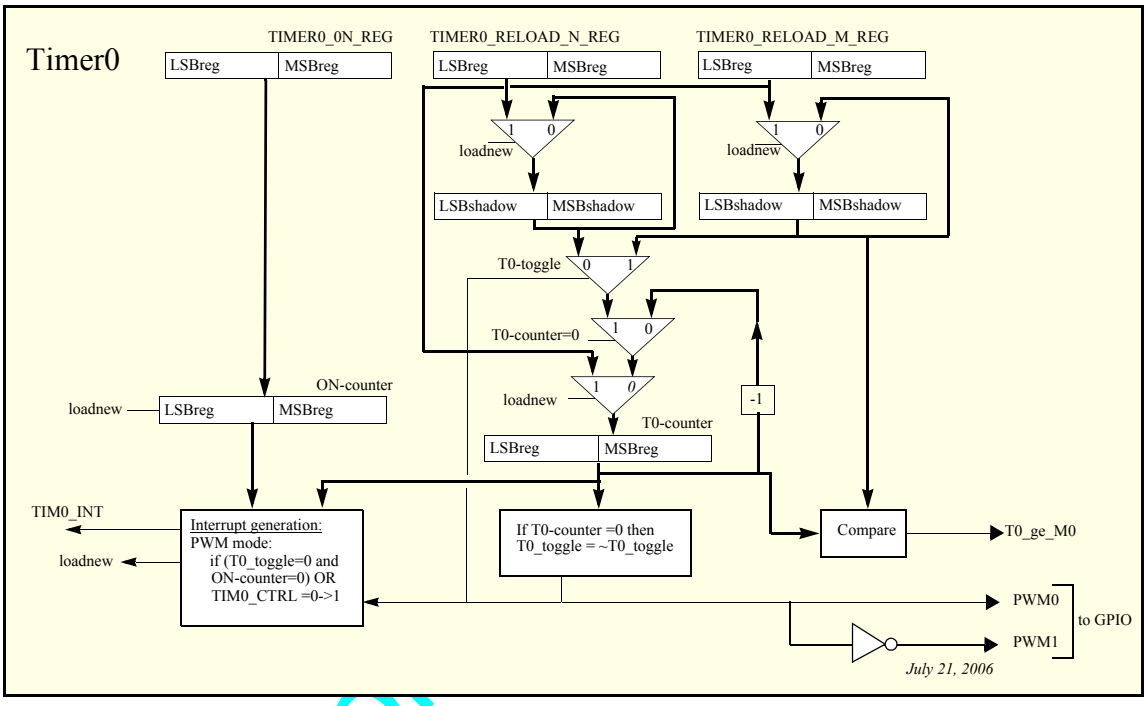

Figure 69 Timer0 block diagram

Figure 69 shows the block schematic of Timer0. The 16 bits timer consists of two counters: T0-counter and ON-counter, and three registers: TIMER0_RELOAD_M_REG, TIMER0_RELOAD_N_REG and TIMER0_ON_REG. On reset the counter and register values are 0000. Timer0 will generate a Pulse Width Modulated signal PWM0. The frequency and duty cycle of PWM0 are determined by the contents of the TIMER0_RELOAD_N_REG and the TIMER0_RELOAD_M_REG.

The timer can run at two different clocks: 115.2 kHz and 1.152 MHz. The clock speed can be selected by bit 2 of the timer control register TIMER_CTRL_REG. The ON-counter only runs at 115.2 kHz.

Timer0 operates in PWM mode. The Signals PWM0 and PWM1 can be switch to ports pins.

Timer0 PWM mode

If TIM0_CTRL bit (bit 0) in the TIMER_CTRL_REG is set, Timer0 will start running. TIM0_interrupt will be generated and the T0-counter will load its start value from the TIMER0_RELOAD_M_REG, and will decrement on each clock. Also the ON-counter loads its value from the TIMER0_ON_REG and decrements with a fixed clock of 115.2 kHz. When the T0-counter reaches zero the internal signal T0-toggle will be toggled and now selects the TIMER0_RELOAD_N_REG of which its value will be loaded in the T0-counter. Each time the T0-counter reaches zero it will alternately be reloaded with the values of the M0- and N0-shadow registers. If the ON-counter reaches zero it will remain zero until the T0-counter also reaches zero when it was decrementing the value loaded from the TIMER0_RELOAD_N_REG (PWM0 is low). The counter will then generate an interrupt (TIM0_interrupt). The ON-counter will be reloaded with the value of the ON-register. The T0-counter as well as the M0-shadow register will be loaded with the value of the TIMER0_RELOAD_M_REG. At the same time the N0-shadow register will be loaded by the

TIMER0_RELOAD_N_REG.

Both counters will be decremented on the next clock again and the sequence will be repeated.

During the time that the ON-counter is not zero, new values for the ON-register, M0-register and N0-register can be written, but they are not used by the T0-counter yet. The newly written values in the TIMER0_RELOAD_M_REG and TIMER0_RELOAD_N_REG are only stored into the shadow registers when the ON-counter and the T0-counter have both reached zero and the T0-counter was decrementing the value loaded from the TIMER0_RELOAD_N_REG (see Figure 70).

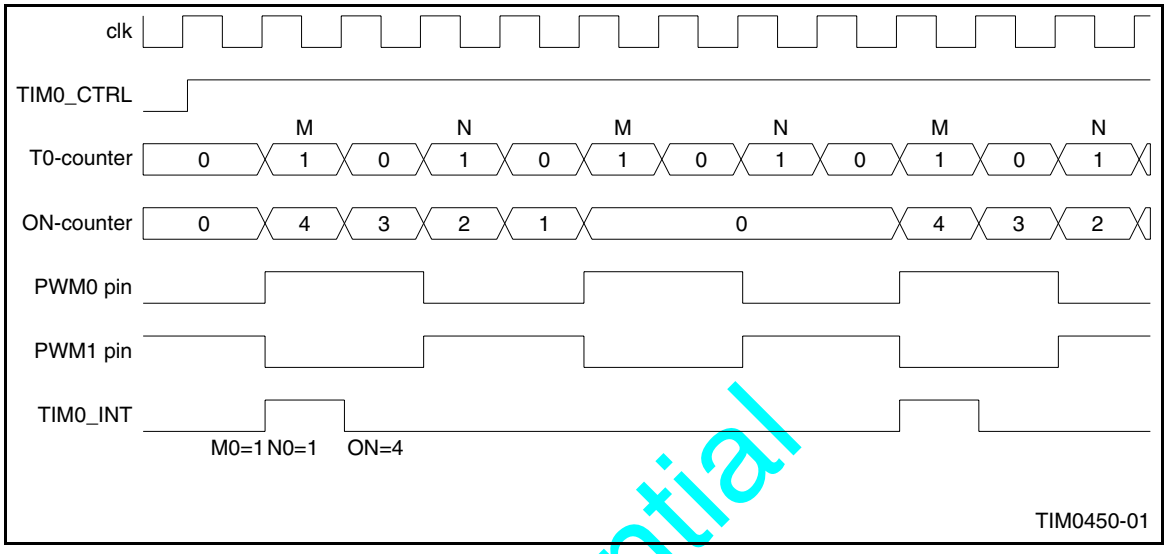

Figure 70 Timer 0 Pulse PWM mode

At start-up both counters and the PWM0 signal are low so also at start-up an interrupt is generated. If Timer0 is disabled all flipflops and outputs are in reset state except for the ON-register, TIMER0_RELOAD_N_REG and the TIMER0_RELOAD_M_REG. In 115.2 kHz mode however, the timer is not reset if switched off. If resetting is required, the timer must switched to 1.152 MHz mode, next reset and switched to 115.2 MHz mode. This way these registers can be programmed before the timer is activated.

The timer input registers ON-register, TIMER0_RELOAD_N_REG and TIMER0_RELOAD_M_REG can be written and the counter registers ON-counter and T0-counter can be read. If read from the address of the ON-register, the value of the ON-counter is returned. If read from the address of either the TIMER0_RELOAD_N_REG or the TIMER0_RELOAD_M_REG, the value of the T0-counter is returned.

It is possible to freeze the timer0 with bit 1 of the register SET_FREEZE_REG. When the timer is frozen the timer counters are not decremented. This will freeze all the timer registers at their last value. The timer will continue its operation again when FREEZE is cleared (bit 1 of register RESET_FREEZE_REG).

If the timer is switched off, all registers are switched into the reset state.

23.2 TIMER1

Timer1 generates a system clock tick interrupt to the CR16.

Features

- Programmable timer Frequency Mode 1
  (1.152MHz or 115.2 kHz) / (M+1)+(N+1)
  N=0..(2**16)-1, M=0..(2**16)-1
- Programmable timer Frequency Mode 2
  (1.152MHz or 115.2 kHz) / N+1
  (N=M shifting in time)
  N=0..(2**16)-1, M=0..(2**16)-1

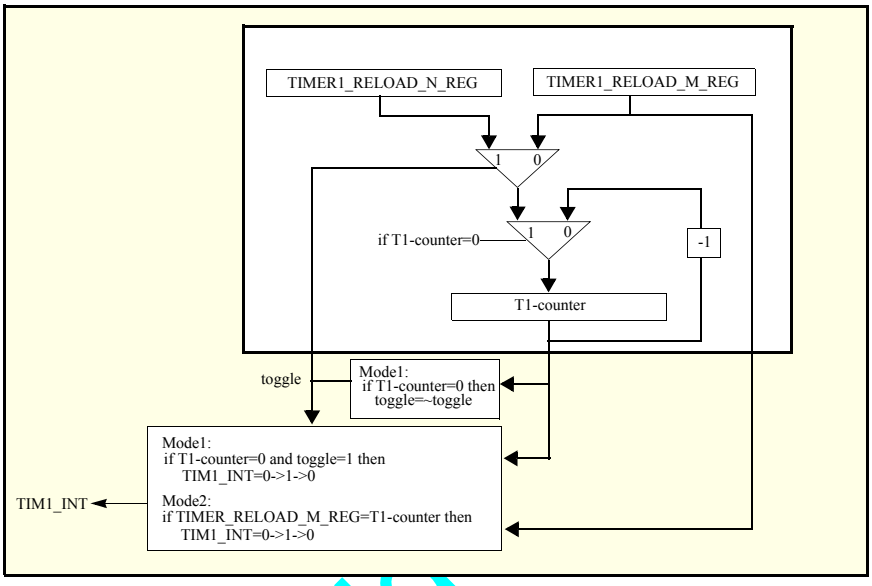

Figure 71 Timer1 block diagram

Figure 71 shows the timer 1 block diagram. The 16 bits timer consists of a counter, and two registers: TIMER1_RELOAD_N_REG and TIMER1_RELOAD_M_REG. On reset the counter and register values are 0000. Timer1 can be used as a general purpose timer.

The timer can run at two different clocks: 115.2 kHz and 1.152 MHz. The clock speed can be selected by TIMER_CTRL_REG bit CLK_CTRL1. The timer can be switched on and off with bit TIM1_CTRL. With bit CLK_DIV8 of the TIMER_CTRL_REG a divider of 8 can be selected.

The timer input registers TIMER1_RELOAD_N_REG and TIMER1_RELOAD_M_REG can be written and the counter register T1-counter can be read. If read from the address of the TIMER1_RELOAD_N_REG, the value of the T1-counter is returned. If read from the address of the TIMER1_RELOAD_M_REG, the value of the M1-register is returned.

It is possible to freeze the timer with bit 2 of the register SET_FREEZE_REG. When the timer is frozen the timer counters are not decremented. This will freeze all the timer registers at their last value. The timer will continue its operation again when FREEZE is cleared (bit 2 of register RESET_FREEZE_REG).

If the timer is switched off, all registers are switched into the reset state.

If Timer1 is disabled all flipflops and outputs are in reset state except for the TIMER1_RELOAD_N_REG and the TIMER1_RELOAD_M_REG. This way these registers can be programmed before the timer is activated.

Timer1 mode1

After enabling this timer T1-counter is loaded with the value of the TIMER1_RELOAD_M_REG. The counter is then decremented until it reaches zero. Then the counter is loaded with the value of the TIMER1_RELOAD_N_REG and decremented again. Each time it reaches zero the counter is alternately loaded with the values of the TIMER1_RELOAD_M_REG and the TIMER1_RELOAD_N_REG.

The TIM1_INT interrupt is activated when the TIMER1_RELOAD_M_REG is loaded into the counter, except for the first time when the timer is switched on.

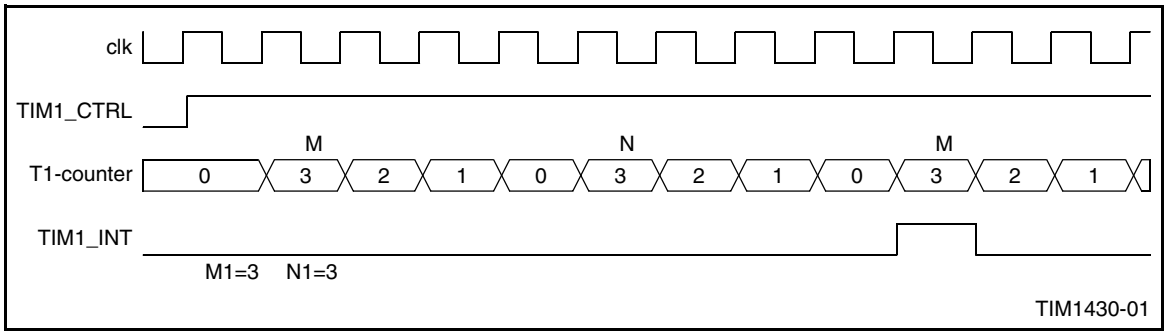

Figure 72 Timer 1 mode 1

Timer1 mode2

In this mode only the TIMER1_RELOAD_N_REG is repeatedly loaded into the counter when this reaches zero. A TIM1_INT interrupt will be generated each time the counter value is equal to the TIMER1_RELOAD_M_REG value. This mechanism provides a constant interrupt repetition rate and the possibility to shift (fine tune) the interrupt trigger in time.

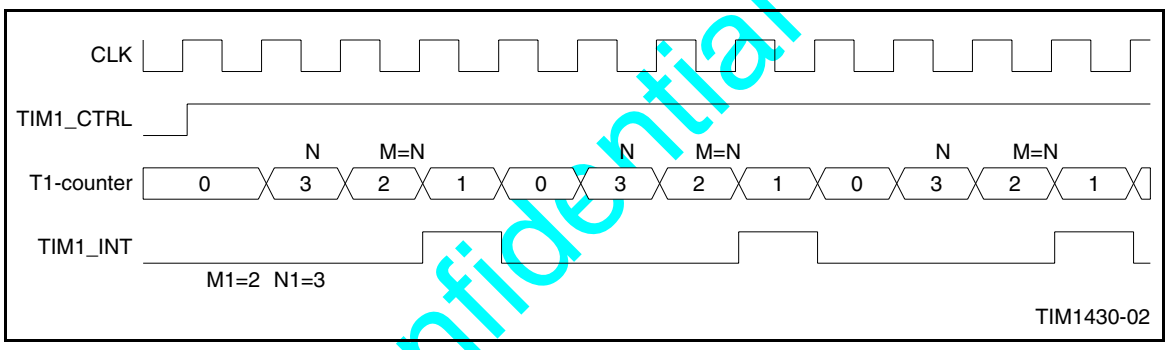

Figure 73 Timer 1 mode 2

23.3 PWM TIMER2

Timer2 has two Pulse Width Modulated (PWM) outputs used for intensity control of the white/amber LEDs connected to the "Charge Pump Tripler" on page 95)

Features

- Clock frequency 1.152 MHz
- Programmable output frequency
  F = 1.152MHz/2 to 1.152MHz/((2**14)-1)
- Two outputs with Programmable duty cycle 0-100%
- Used for charge pump on/off control
- DIP controlled freeze function using BIAS_DCF

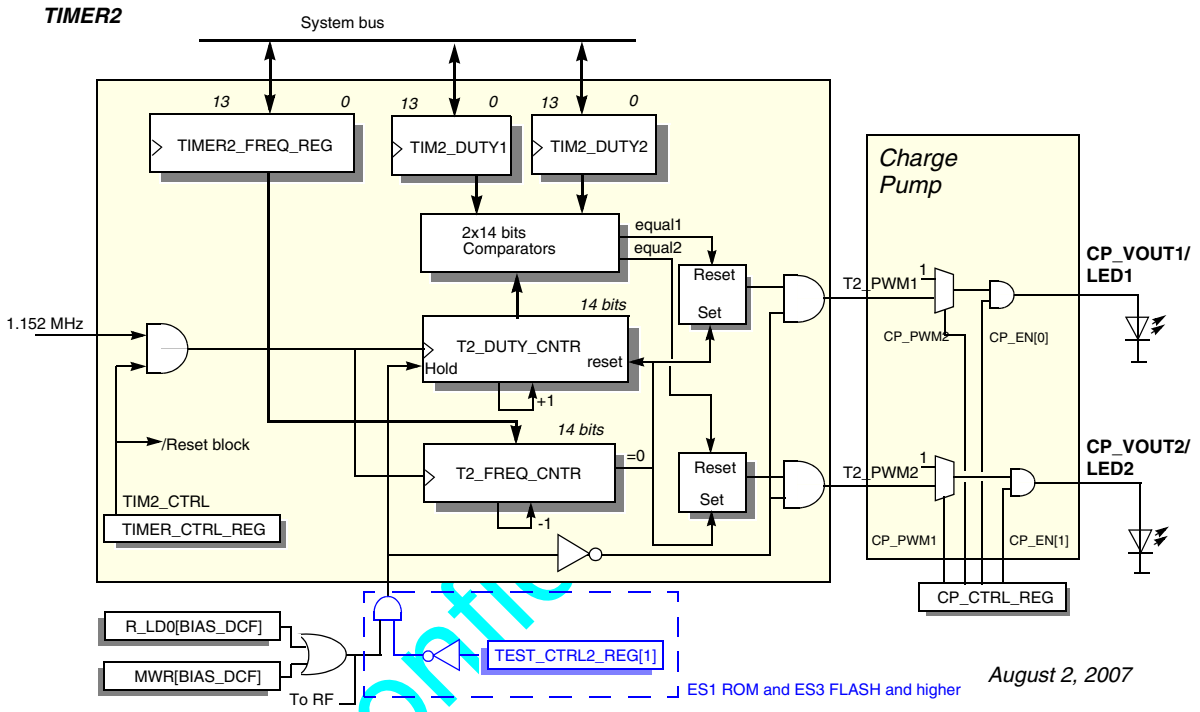

Figure 74 PWM Timer T2 block diagram

Figure 74 shows the PWM timer T2 block diagram.

The timer 2 is clocked with 1.152 MHz and can be enabled with TIMER_CTRL_REG[TIM2_CTRL].

T2_FREQ_CNTR determines the output frequency of the T2_PMWn output. This counter counts down from the value stored in T2_FREQ_REG. At counter value 0, T2_FREQ_CNTR T2_PWMn output to 1 and the counter is reloaded again.

T2_DUTY_CNTR is an up-counter that determines the duty cycle of the T2_PWMn output signal. After the block is enabled, the counter starts from 0. If T2_DUTY_CNTR is equal to the value stored in the T2_DUTY_REG[T2_DUTYn], “equal1” resp “equal2” resets the T2_PWMn output to 0. T2_DUTY_CNTR is reset if T2_FREQ_CNTR is 0.

The Timer 2 timing diagram is shown in Figure 75.

Charge pump on/off control and freeze function.

For LED intensity control, T2_PWMx can be used to reduced the average output voltage of the charge pump outputs CP_VOUTx. For this function CP_CTRL_REG[CP_PWMx] must be set to ‘1’.

During RF activity it is desirable that the charge pump can be switched off temporarily in order to reduce the switching noise. If BIAS_DCF is set to ‘1’ (either by MWR or R_LD0) at the start of a burst, T2_DUTY_CNTR is frozen and T2_PWMx output is switched to ‘0’ to disable the selected charge pump output. As soon as BIAS_DCF is set ‘0’, T2_DUTY_CNTR resumes and finalizes the remaining part of the PWM duty cycle.

During searching for basestation when BIAS_DCF is high for more slots, TEST_CTRL2_REG[1] can be set to ‘1’ to disable the freeze function of duty counter and keep the duty cycle constant. Once the PP is locked to FP, TEST_CTRL2_REG[1] must be set back ‘0’.

If the charge pump is used for continuous VDDIO voltage source, PWM control is undesired and

CP_CTRL_REG[CP_PWMx] is set to '0'.

Refer also to "Charge Pump Tripler" on page 95

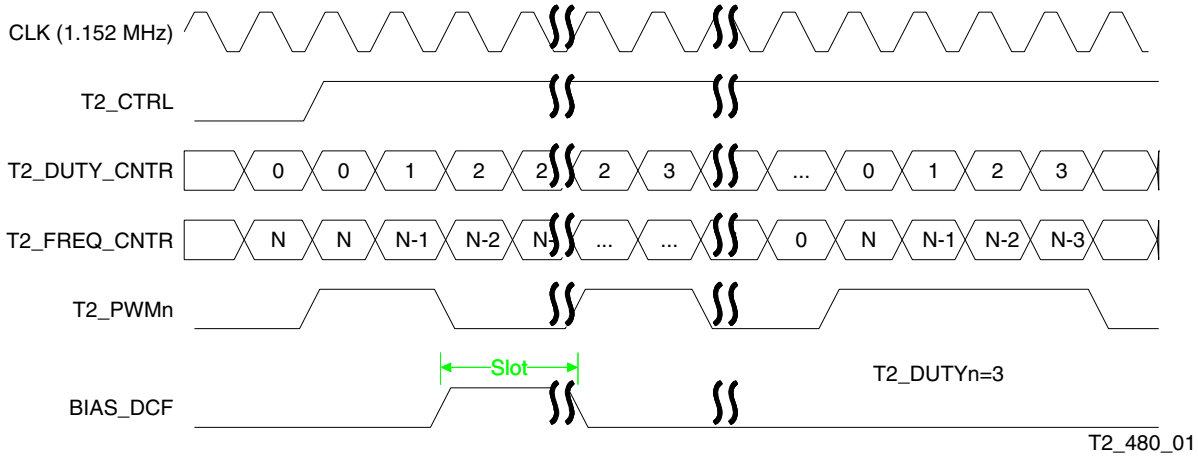

Figure 75 Timer 2 PWM timing diagrams

Example:

- T2_PWMx frequency 5ms = 200 Hz (1/2 DECT frame)
- T2_FREQ_CLK = 1152000/200 = 5760 -1
- For duty cycle 80%
  -> T2_DUTY_REG = 0.8×5760 = 4608. (= 4 ms)

During a slot of 654 bits (Between BIAS_DCF on/off), T2_PWMn is holded for 654/1.152MHz = 0.57 us

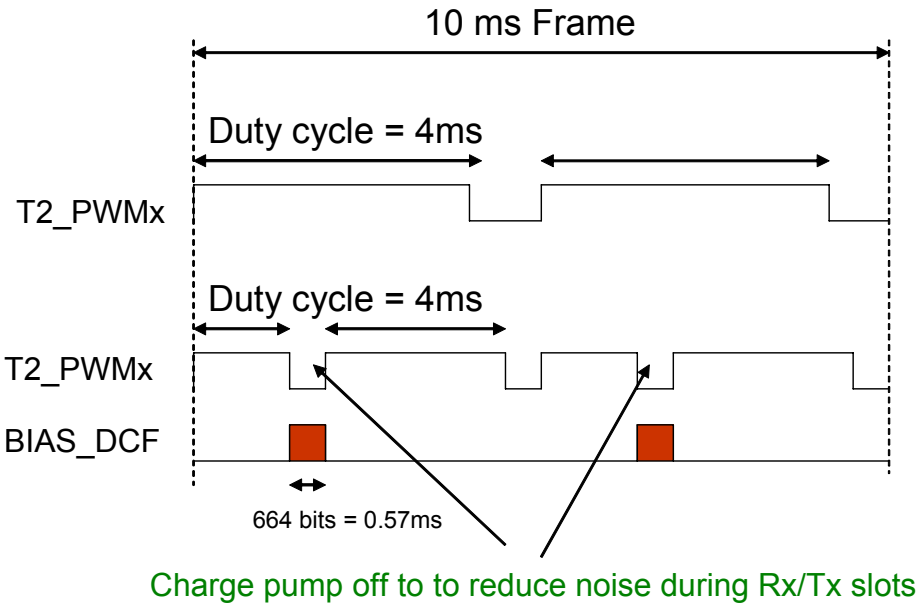

Figure 76 Timer 2 Example timing

23.4 WATCHDOG TIMER

The watchdog timer is an 8-bit timer that can be used to detect an unexpected execution sequence caused by a software run-away.

The watchdog timer consists of 8 bits, its contents is decremented by 1 every 10.66 msec. The WATCHDOG_REG is set to 0xFF at reset. This results in the maximum watchdog time of 2.56 seconds. If the watchdog reaches 0 the WATCHDOG_REG is set to 0xFF again. TIMER_CTRL_REG [WDOG_CTRL] can be set to either generate an NMI (default) or an internal HW reset + SW reset if the watchdog timer reaches 0. In the latter case everything is reset but the RSTn pin is not pulled low and the TEST_ENV_REG is not reloaded. Bit WDOG_CTRL can only be set and will only be reset on a HW reset. See also Figure 16 on page 30 for an overview of the reset circuit.

Note that the NMI is shared with a DIP <U_VNMI> interrupt. Reading DIP_STATUS_REG determines whether the DIP generated the interrupt or not.

For debugging purposes, the watchdog timer can be froozen if SET_FREEZE_REG[FRZ_WDOG] is set and resumes if RESET_FREEZE_REG[FRZ_WDOG] is set again.

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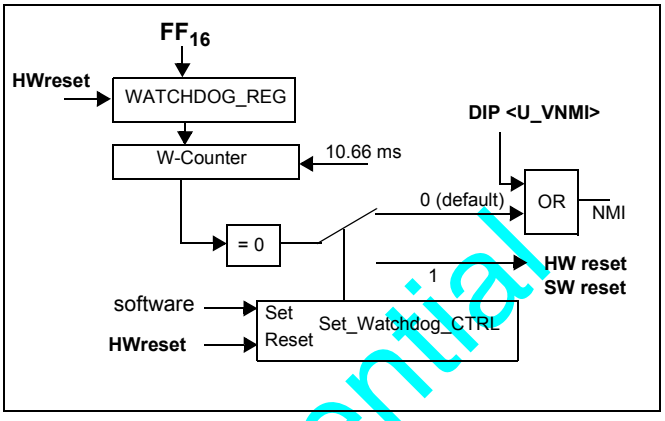

Figure 77 Watchdog timer

23.5 CLOCK 100 TIMER

If CLK100_SRC bit in the DEBUG_REG is 0 then the clock 100 timer has a time period of 10 msec, synchronised to the execution of a DIP timer. If CLK100_SRC is 1 the clock 100 is a continuous signal with a time period of 10.66 msec. The clock 100 timer (10msec) is started if the sequencer program is started (URST = “0”). The clock 100 timer rising edge is synchronised to the DIP SLOT_ZERO command. The clock 100 interrupt pending bit is set on every rising edge and/or falling edge of clock 100 depending on the DEBUG_REG[CLK100_POS, NEG] values. The active edge value can be read back with CLK100_EDGE. When the sequencer program is stopped (URST = “1’) the clock timer is also stopped.

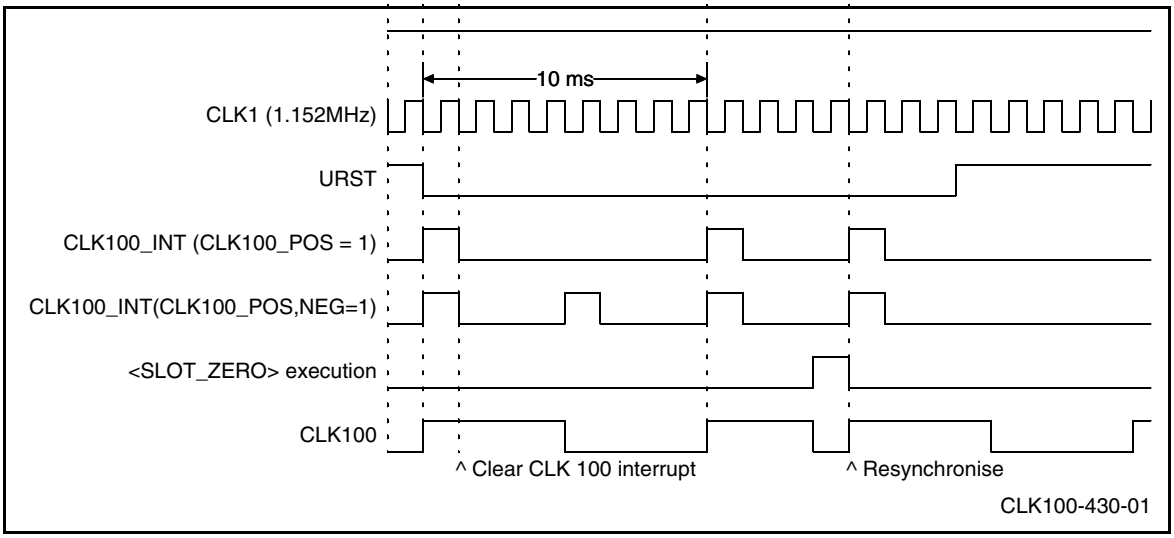

Figure 78 Clock 100 Timing

23.6 CAPTURE TIMERS/COUNTERS

The SC14480A5M, SC14480A2M6 has two programmable capture timer/counters (CT1 and CT2) to relief Gen2DSP measure frequencies of tones coming from the PSTN line or from the microphone. Figures 79 show the on-hook and off-hook basestation applications to detect ringing pulses with CT1 or CT2.

Table 24 shows the applications and how to select the multiplexers GATESRCx and CLKSRCx as shown in figure 80.

Table 24: Gate and clock selection

Application	GATESRC	CLKSRC
RINGING pin comparator	01	00
Call progress, ringing (ECZ via MICp/MICn pins and Gen2DSP)	10/11	00
Call progress, ring High Accuracy, high interrupt rate (ECZ via MICp/MICn pins and Gen2DSP)	00	10/11

The capture timer can either measure the time between two zero crossings (timer operation) or measure the number of zero crossing during a programmable time interval (counter operation).

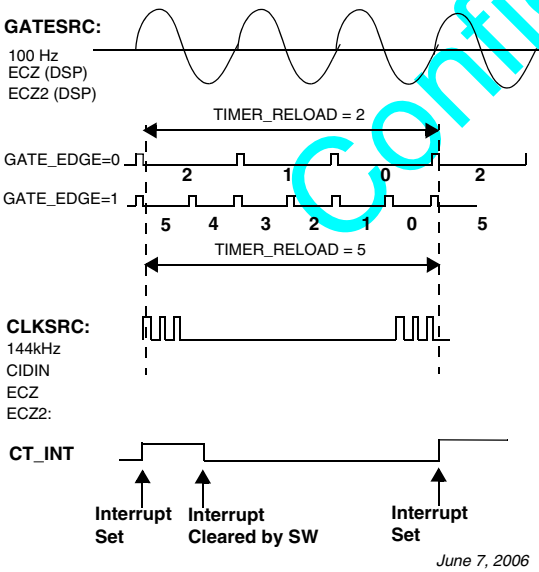

Figure 79 Timer/counter operation

The sources to measure the time between the zero crossings are selected with GATESRCx. The clocks that count the number of cycles are selected with CLKSRCx in counter TONE_COUNTERx. (see Figure 80)

- GATESRC selection:
  - 00 = 100 Hz, the internal clock DECT frame clock
  - 01 = RINGING Comparator.
  - 10 = ECZ1, from Gen2DSP Zero crossing det 1 (optionally behind echo canceller)
  - 11 = ECZ2, from Gen2DSP Zero crossing det 2 (optionally behind echo canceller)

- CLKSRC selection:
  - 00 = 144 kHz, an internal clock
  - 01 = Reserved
  - 10 = ECZ1, from Gen2DSP Zero crossing det 1 (optionally behind echo canceller)
  - 11 = ECZ2, from Gen2DSP Zero crossing det 2 (optionally behind echo canceller)

The ECZ1 and ECZ2 signal are outputs of the single bit Gen2DSP internal register DSP_ZCROSS1_OUT_REG and/or DSP_ZCROSS2_OUT_REG. Refer to chapter "ECZ1, ECZ2 usage and port mapping" on page 69 for more information.

The TONE_TIMERx determines the actual time interval for the measurement. It counts down from value determined by TIMER_RELOADx on every transition positive edge of GATESRCx. On value 0 the TONE_COUNTERx value is latched in TONE_LATCHx and the CTx_INT is set. If the mask interrupt bit MCT1x_INT is set to 1, an CT_INT interrupt in the ICU is set.

CTx_INT must be cleared by writing to TONE_CLEAR_INTx_REG. This resets also the TONE_LATCHx_REG automatically. CT_INT must be cleared using the RESET_INT_PENDING_REG.

With GATE_EDGEx=0, only the rising edge of GATE_SRC is used to clock the TONE_TIMER. With GATE_EDGEx =1, both edges are used. This feature gives higher resolution with e.g ringtone detection.

The formula below shows the value of the TONE_LATCHx register if a CT_INT interrupt is generated as function of frequencies of CLKSRC, GATECLK input signals and TIMER_RELOADx value.

GATE_EDGE=0:
TONE_LATCHx = (TIMER_RELOADx+1).*$F_{CLKSRCx}$/$F_{GATESRCx}$
GATE_EDGE=1:
TONE_LATCHx = (TIMER_RELOADx+1).*$F_{CLKSRCx}$/2x$F_{GATESRCx}$

Example Figure 79
FCLKSRC=144kHz, FGATESRC = 4 kHz

TONE_LATCH = (2+1)*144/4=108

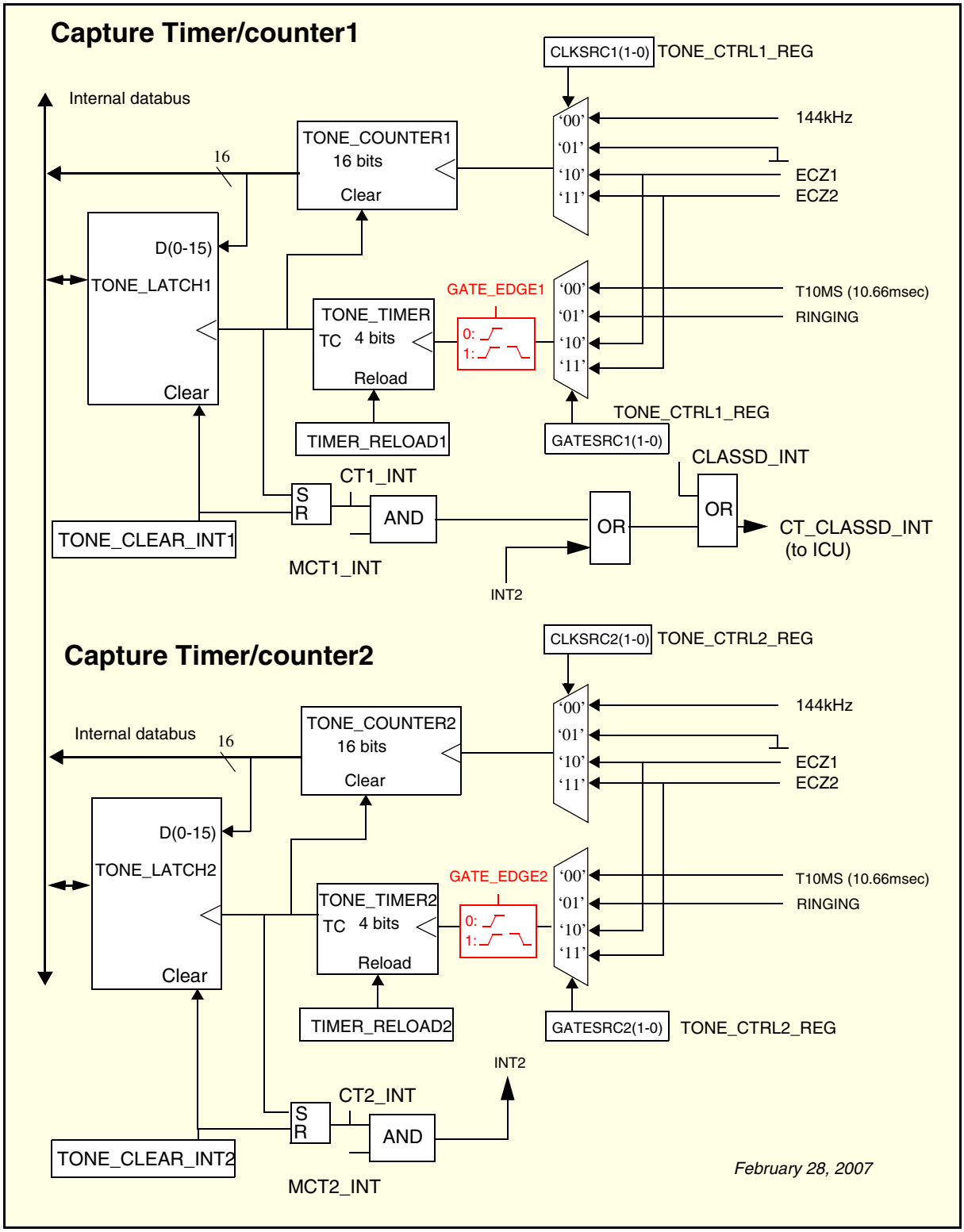

Figure 80 Capture timers block diagram

24.0 CR16Cplus

Refer to CR16CPlus Core Architecture Specification Revision 1.0.

25.0 Rom Patching

The CR16 hardware debug logic makes is possible to jump to and execute alternative code in RAM instead of the ROM code. The code patch in RAM contains the corrected code. So the ROM patching is used to fix bugs in the program ROM. The alternative code is copied to RAM at start-up from Eeprom or SPI FLASH.

Refer to *AN-D-146 "ROM patching manual"* for details

The table shows the ROM patch register overview for the SC14480A5M, SC14480A2M6 device.

Table 25: Debug control and status register overview

Registers
DBS[15-0]
DSR0-DSR3
DCR0-DCR3
CAR0 - CAR7
Number of breakpoints (code patches): 8

Table 26: Debug control and status register overview (A2M6)

Registers
DBS[15-2] = 0, DBS[1-0]
DSR0
DCR0
CAR0 -CAR1
Number of breakpoint (code patches) : 2

26.0 APB Bridge

The AMBA Peripheral Bus (APB) bridge interfaces the high speed system bus to low speed peripherals registers of:

- GPIO ports registers
- ADC registers
- ACCESS bus registers
- SPI registers
- UART registers
- DMA registers
- RF registers
- Charge pumps

The peripheral cores run on a different clock as explained in "System Clock generation" on page 18.

The purpose of this bridge is to reduce the system bus load and therefore saving power. Because the CR16Cplus or DMA access to the peripherals is infrequent, the peripherals are designed for a lower frequency in order to save power and area.

The APB bus peripherals are mapped from 0x00FF.0000 to 0x00FF.FBFF

APB Bus speed

The maximum frequency of the APB interface is 41.472 MHz and can be set in register CLK_AMBA_REG[PCLK_DIV]. The frequency depends on the system bus clock HCLK which is set with CLK_AMBA_REG[HCLK_DIV].

For lowest power the PCLK_DIV should be set to its maximum value 4 which divides the HCLK to 4. If more performance during peripheral I/O is required, e.g. DMA/SPI transfers, the PCLK_DIV may be set to 1, giving a maximum APB frequency of 41.472 MHz, equal to the maximum HCLK of 41.472 MHz.

In order to avoid internal timing problems, **HCLK_DIV and PCLK_DIV values may never be modified at the same time.** Make sure that PCLK always stays equal to or below 41.472 MHz if HCLK_DIV is changed first to get a higher HCLK frequency. (See **Note 52: on page 159)**

Register access

Because the APB bus is a 16 bits bus, **all APB peripheral register write access must be WORD wise**. Read access may be BYTE wise, but the not selected byte in the register will return 0. Writing BYTE wise to the registers will result undefined data in the not selected 8 bits in the 16 bits registers.

Accessing two successive 16 registers in a single 32 bits access gives incorrect results.

DSP registers

The DSP registers are not accessible via the APB bridge. Therefore they can be accessed BYTE or WORD wise, except for DSP_MIC_CODEC_GAIN_REG and DSP_OVERFLOW_REG. Like the APB registers, these registers must be accessed WORD wise.

FLASH info block selection.

After selecting FLASH info block with MEM_CTRL_REG[PROG_INFO_SELx]=1, the info block may be accessed after one dummy instruction cycle. This is also after selecting the main block again. Reason for this is the pipeline latency between AHB and APB.

Accessing RF Registers

The APB bus has priority over Microwire Interface access to the RF registers.

This means that if a Microwire Write (M_WR) or Micro-

wire Read (M_RD) is in progress, the CR16, SDI or DMA may NOT access the RF registers otherwise Microwire access may fail.

Example: If a debugger (e.g DCTmon) is monitoring RF registers, Micro Wire access to the RF registers may fail. So the RF peripheral register window must always be close during an active RF link.

27.0 DMA Controller

The SC14480A5M, SC14480A2M6 has four identical Direct Memory Access (DMA) channels for fast data transfers between the shared memory and the peripheral devices. All channels can copy up to 64k bytes/ Halfwords or Words of data within the 32 Mbyte address range.

The following devices have DMA support:

- DMA0_REQ: SPI (Rx)
- DMA1_REQ: SPI (Tx).
- DMA2_REQ: UART Rx
- DMA3_REQ: UART Tx

The channels can operate in one mode:

- **Indirect, dual address mode**. In this mode data from the source is read from the source, temporarily stored in a register and written to a destination address.

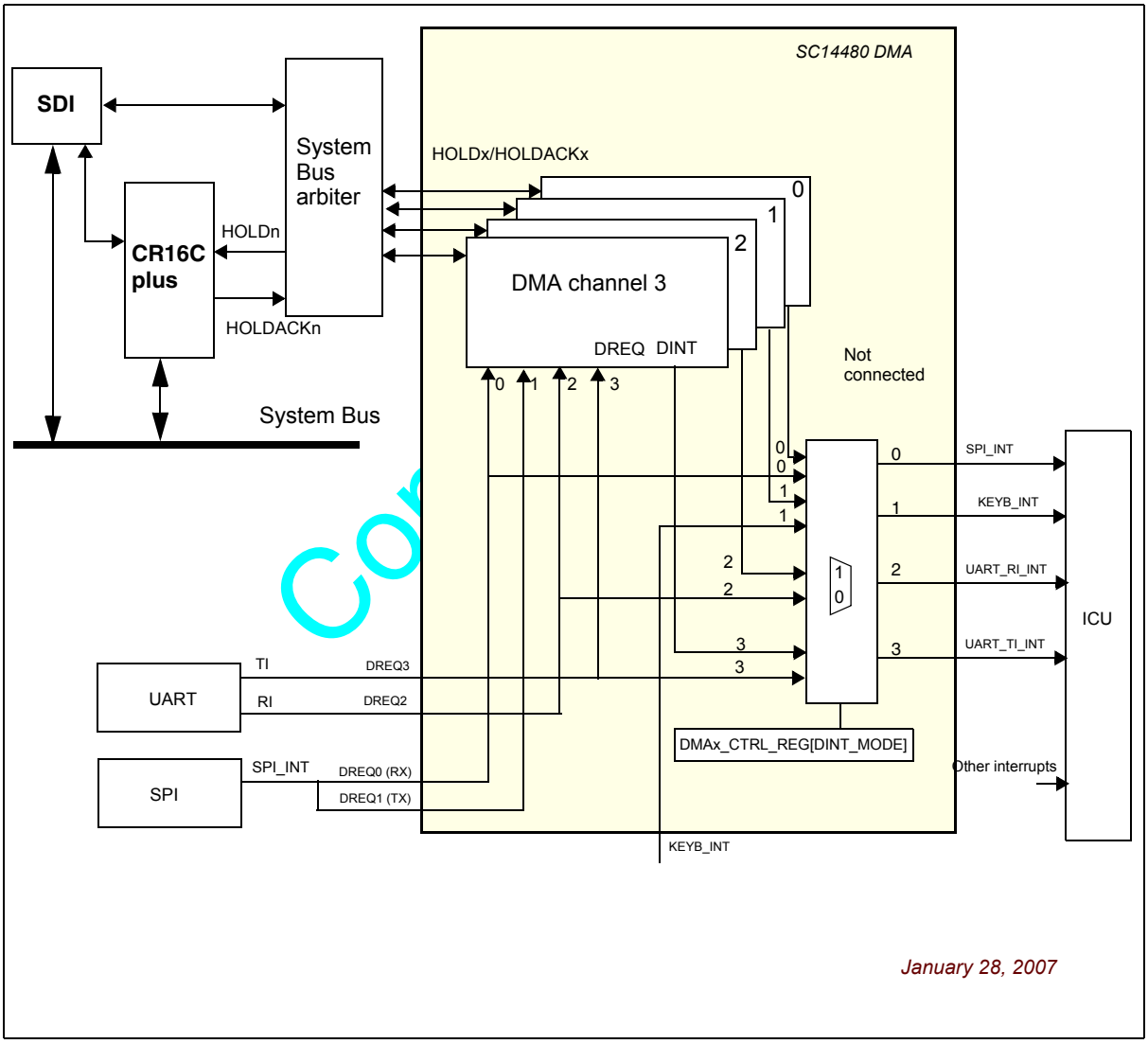

Figure 81 DMA controller block diagram

If a DMA transfer starts the DMA channel request the system bus with HOLDn and waits for an acknowledge signal HOLDACKn. If granted, the **DACKn** signal goes low.

27.1 DMA CHANNEL OPERATION

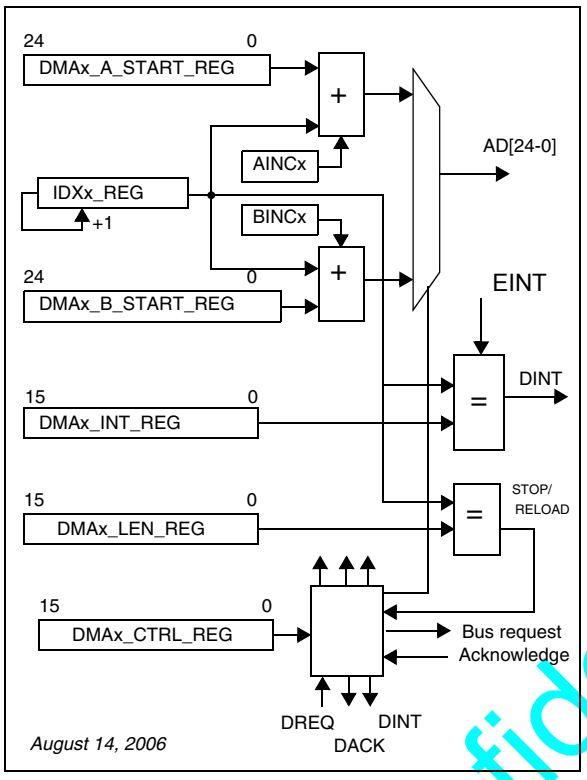

Figure 82 DMA channel diagram

A DMA channel is switched on with bit **DMA_ON.** This bit is automatically reset if the dma transfer is finished. The DMA channels can either be triggered by software or by an hardware interrupt source. If **DREQ_MODE** is 0, then a DMA channel is immediately triggered. If DREQ_MODE is 1 the DMA channel can be triggered by an Hardware interrupt.

If DMA starts, data is transferred from address **DMAx_A_START_REG** to address **DMAx_B_START_REG** for a length of **DMAx_LEN_REG**, which can be 8, 16 or 32 bits wide. The address increment is realized with an internal 16 bits counter **DMAx_IDX_REG,** which is set to 0 if the DMA transfer starts and is compared with the DMA_LEN_REG after each transfer. The register value is multiplied according to the **AINC** and **BINC** and **BW** values before it is added DMA_B_STARTL/H_REG and DMA_B_STARTL/H_REG. **AINC** or **BINC** must be 0 for register access.

Either the DMA channels or the interrupt sources can generate an interrupt to the ICU. This can be by bit **DINT_MODE**. (see also "Interrupt Control Unit (ICU)" on page 119)

If at the end of a DMA cycle, the DMA start condition is still true (DREQ in Figure 81), the DMA continues. The DMA stops if DREQ is low or if **DMAx_LEN_REG** is equal to internal index register. This condition also clears the **DMA_ON** bit.

If bit **CIRCULAR** is set to 1, the DMA controller automatically reset the internal index registers. and continues from its starting address without intervention of the CR16. If the DMA controller is started with **DREQ_MODE** =0, the DMA will always stop, regardless of the state of CIRCULAR.

Each DMA channel can generate an interrupt if **DMAx_INT_REG** if equal to DMAx_IDX_REG. After the transfer and before DMAx_IDX_REG is incremented, the interrupt is generated.
Example: if DMA_x_INT_REG=0 and DMA_x_LEN_REG=0, there will be one transfer and an interrupt. ~~If **DMAx_INT_REG** is zero, never an interrupt is generated.~~

27.2 DMA ARBITRATION

The priority level of a DMA channel can be set with bits **DMA_PRIO[1-0]**. These bits determine which DMA channel will be activated in case more than one DMA channel requests DMA. Once the DMA channel is active, it can not be interrupted.

Note that during DMA operation, the CR16 is stopped. Therefore the DMA transfer length must be taken into account.

27.3 FREEZING DMA CHANNELS

Each channel of the DMA controller can be temporarily disabled by writing a 1 to bits FRZ_DMA_CH0,1,2,3 in the SET_FREEZE_REG.
To enable the channels again, a 1 to bits FRZ_DMA_CH0,1,2,3 in the RESET_FREEZE_REG must be written.

There is no hardware protection against miss programming the DMA registers.

DMA transfers will take place over the system bus, so they can be traced by a In Circuit Emulator.

The CR16 CLK divider register must be set such that the system clock is minimum 1.152 MHz.

28.0 SDI-JTAG

The JTAG Serial Debug Interface (SDI+) is an on-chip debug interface, compliant to the Nexus 5001 Forum™ Standard for Global Embedded Processor Debug Interfaces (Revision 1.0, 15th December 1999), Class 1+. It implements all basic functions to allow application development and testing with the chip already installed in the final target application.

The SDI+ has the following features:

- Communication via One Wire Interface (OWI) through pin JTAG.
- Upto eight hardware breakpoints/watch points, triggered upon instruction execution or data access.
- Single-Stepping of instructions.
- Access to memory mapped resources by holding the CR16.
- Access to CR16Cplus internal registers.
- Client break support for the DIP and Gen2DSP

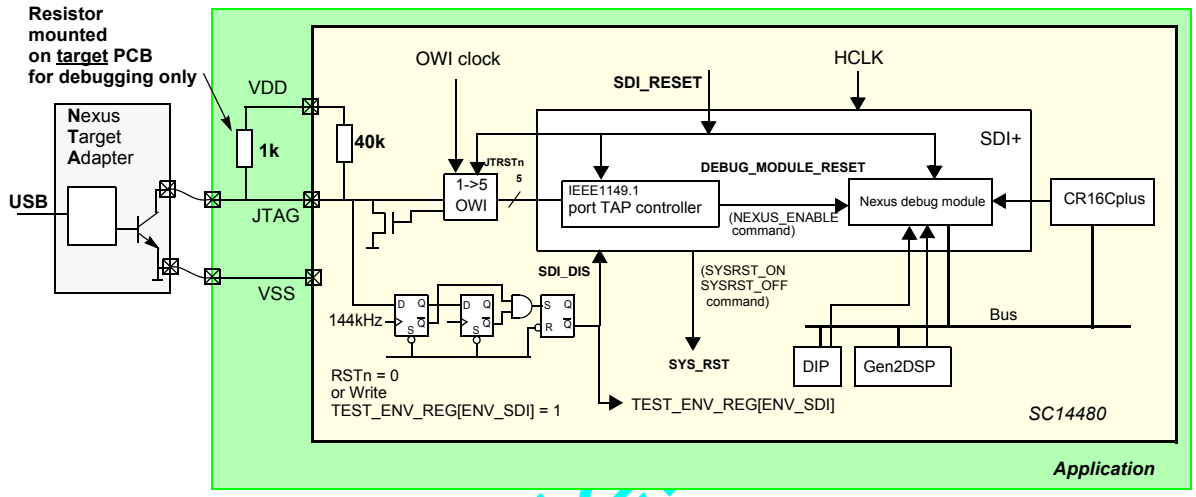

Figure 83 SDI debug module

On-chip communication to standard IEEE1149.1 (JTAG) TAP controller through signals TMS, TDI, TDO, TCK, TRSTn, TEVOn, RDYn

The SDI can take over the CR16Cplus or DMA execution at any time. The SDI has the highest priority in bus arbitration over DMA and CR16 operation. See also "DMA arbitration" on page 111.

Enabling the SDI, Hot insertion

The SDI can be enabled at any time when the CR16 or DMA is running, by pulling the JTAG pin low for at least 15 us. This hot insertion feature is useful when debugging is required after the application has ran for a long time and software problems show up.

Enabling the SDI consumes power and must therefore be avoided in a normal application by keeping the JTAG pin either unconnected and/or pull-up to VDD

Due to the hardware structure of the CR16Cplus, either the JTAG/SDI or the program counter patch module can invoke the CR16C debug feature. Default the JTAG/SDI hot insertion feature is enabled. To enable the program counter patch module, the CR16C must set DEBUG_REG[CR16_DBGM] to 0 and issue a SW_RESET. The side effect is that the JTAG/SDI hot insertion feature will be disabled and the JTAG/SDI can not be used. Program patches e.g. in ROM devices can be stored in EEPROM and loaded in RAM after start-up. For more information refer to the CR16Cplus programmer manual.

Disabling SDI

The SDI can be disabled in two ways:

- JTAG pin is disconnected or kept '1' during and after the RSTn pin is pulsed low.
- Writing a '1' to TEST_ENV_REG[ENV_SDI] followed by an inactive '1' state of the JTAG pin within 5 us. The JTAG SDI+ is enabled again if the JTAG pin is kept '0' for at least 15 us.

Start-up with no program loaded.

If no program is loaded in internal FLASH or RAM, then the JTAG must be kept low while RSTn is low and kept low for 20 us after the RSTn pin is set to '1'. This prevents uncontrolled program execution, since the booter will enter the "right" branch of the booter flow diagram (See "Boot from UART" on page 121) because TEST_ENV_REG[ENV_SDI] is 0. Because no external UART is connected, the CR16Cplus waits in an endless loop which allows the SDI to become bus master by setting the DGCR[DBR] bit in the SDI+.

From this point CR16Cplus program execution can be directed to execute the boot procedure from internal FLASH or ROM

Clock selection

The OWI clock can be selected with CLK_AUX_REG[OWI_SEL] and OWI_DIV. The default value (xtal selected divide by 1) shall only be modified by the DCTmon.exe tool. The SDI clock is equal to the CR16 clock HCLK and is application dependent.

29.0 Trace control unit

The on chip Trace controller is able to trace discontinuous program counter values (jumps, calls), data read and write operations and Events, like change of Bus Grant, entry or exit of the trace region, or change of an external signals. All trace information is written in a cyclic buffer in internal, non shared RAM. The size of the trace buffer is scalable from 0 to 8kbyte.

All trace actions take place in real time, i.e. no wait states will be added when data is written into the trace buffer. Only when the CR16Cplus or another bus master wants to read or write in the same non shared RAM, one or more wait cycles will be generated when a trace record is written at the same time.

Features:

- Trace of discontinuous program counter values (jumps, calls) within programmable ranges.
- Trace of data read and write operations
- Trace of Events, free running or triggered by external events:
  - Change of Bus Grant
  - Exit of the trace region
  - Change of Gen2DSP WTF_IN and ECZ2
  - Change DIP ports signals DP0, DP1
  - Change of two external signals P2[2], P2[5]
- All Event traces contain timing information using a 32 bits counter which is clocked with the CR16Cplus clock.
- Scalable trace buffer sizes 0, 1, 2, 4 or 8 kbyte in non-shared memory.

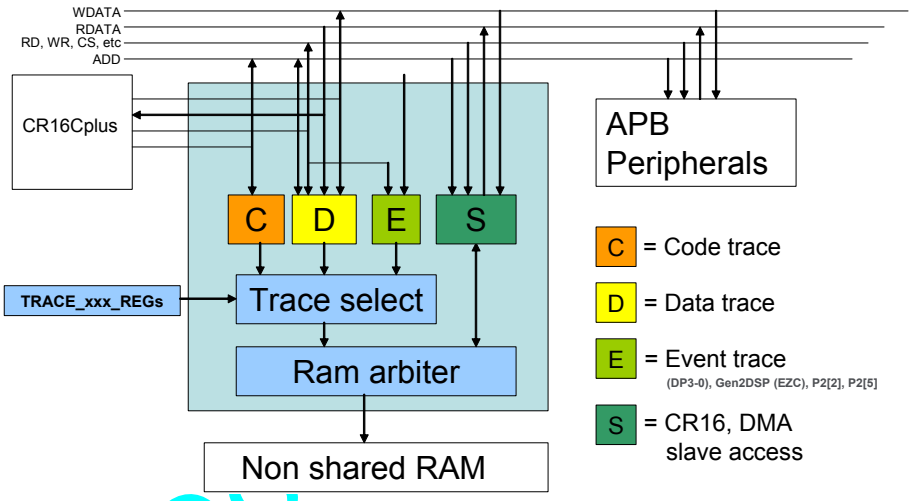

Figure 84 Trace control unit blockdiagram

29.1 GENERAL

The trace unit can trace:

- Instruction fetches
- Data read and write actions
- Events.

With the trace start and length registers, the user can define two independent address areas, where instruction and data trace will be active.
When the address of an instruction fetch to a data read or write cycle is outside these area's, no trace record will be written

For instruction and data trace, the user can select between:

- trace with an event record with timing information
- trace without an event record with timing information
- no trace

Tracing of events does not depend on the contents of trace start and length registers, but only on the contents of the Trace Control Register.

29.1.1 Trace control

Instruction/data tracing is enabled if TRACE_CTRL_REG[I_TRACE_ON] resp. TRACE_CTRL_REG[D_TRACE_ON] are set.

Tracing of instruction fetches or data read/write events takes only place if:

If TRACE_CTRL_REG[TRACE_COND]=0 then
(if TRACE_CTRL_REG[TRACE_COND_EXT]=0-7
and (Trace address range 0 or trace address range 1))

If TRACE_CTRL_REG[TRACE_COND]=1 then
(if TRACE_CTRL_REG[TRACE_COND_EXT]=0-7
or (Trace address range 0 or trace address range 1))

If TRACE_COND_EXT =0, the P2[2], P2[5] are don't care else the trace can also be started/stopped as a

result of a logical function on pins P2[2] and P2[5]. (or, xor, and, nand, xor, xnor). The logical function is evaluated one, every clock cycle.

Active trace address ranges are determined by:
(TRACE_START0_REG to
TRACE_START0_REG+ TRACE_LEN0_REG
or
TRACE_START1_REG to
TRACE_START1_REG+ TRACE_LEN1_REG)

29.1.2 Trace buffer

All trace information is written to a cyclic buffer in on-chip non-shared RAM. The buffer size is scalable in sizes 0, 1, 2, 4 or 8 kByte. The remaining part of the non-shared memory can be used by the application

If TRACE_CTRL_REG[TRACE_MODE] = 0 (Default) the trace buffer is a cyclic buffer, with TRACE_MODE =1, the trace buffer is filled only once.

29.1.3 Types of trace records

To prevent stalling of the CR16Cplus by the trace unit, the trace unit can write only one primary trace record for every bus cycle. A primary trace record is a record that is written real time, without any delay.

Primary trace records are:

- Instruction trace records
- Data trace records with 8 bits wide data
- A limited set of data trace with 16 data bits wide data

Not all data can be traced in this way, but it is a known fact that the CR16Cplus generates a lot of IDLE bus cycles.
During an IDLE cycle and cycles where sequential instructions are executed and no data is read or written, optional trace records can be written by the trace unit. Such records are:

- Data trace records with 16 bits wide data
- Data trace records with 32 bits wide data
- Extended Instruction trace records
- Event trace records

Since these optional records are only written when no primary records have to be written, it is always possible that an optional trace record cannot be written in time.

29.1.4 Priority in memory

Trace records are written in a part of the non shared ram. Other parts of the non shared ram can also be read or written by a CR16Cplus program or by a DMA transfer via the AHB slave port of the trace unit.
Writing Trace records has a higher priority then reading or writing data via the AHB slave port. This means that wait states may be generated when data is read or written via the AHB slave port.

29.1.5 Format of trace records

In order to use the available trace memory as efficient as possible, different formats are defined for trace records. Especially in case of data trace where an address and data must be traced every bit is needed.

29.2 INSTRUCTION TRACE

The instruction trace record is generated during the data phase that belongs to the address phase of the bus cycle. One cycle later, the memory arbiter writes the trace record in non shared ram.

Table 27: Instruction trace record

ID(31.28)	Address(27-5)	Count(4-0)
0001	A23-A1	0..31

The layout of an instruction trace record is given above. Bits 31.28 contain the unique ID for its record.
Bits 27.5 contain the value of the Program Counter, i.e. Address bit 23.1. Note that Address bit 0 is not part of the program counter, since all instruction fetches are done on even addresses.
Every time when a non-sequential instruction is executed and the program will not continue with the next instruction, the new program counter value will be stored in bits 27.5. of the trace record. The 5 bits Count indicator contains the number of executed sequental instructions, that followed the previous instruction trace record.

Table 28: Instruction trace extension record

ID(31-24)	Count(23-0)
0000 0010	0..16777215

If the count value exceeds 30, the next Instruction trace record will be generated with the count value 31 and an extra Instruction trace extension record will be written as well. When this record cannot be written immediately, because other records like data trace are written, this record will be written later, as soon as possible. In the exceptional case when writing cannot take place at all, because the next instruction trace record has to be written already, instruction synchronisation is lost, and the Trace User Interface software can generate a message about this.

Table 29: Instruction trace exit region record

ID(31-24)	Count(23-0)
0000 0011	0..16777215

If the select region is exited, an instruction trace exit region record will be generated.

29.3 DATA TRACE.

The data trace record will be sent to the memory arbiter as soon as the data, belonging to this memory read or write cycle, is available on the AHB bus. One cycle later, the memory arbiter writes the trace record in non

shared ram.

Table 30: Data trace read byte record

ID(31-28)	27-24	Address(23-8)	D(7-0)
0010	Base	A15-A0	D7-D0

Table 31: Data trace read half word record

ID(31-28)	27-24	Address(23-8)	D(7-0)
0100	Base	A15-A0	D7-D0

Table 32: Data trace read word record

ID(31-28)	27-24	Address(23-8)	D(7-0)
0110	Base	A15-A0	D7-D0

Table 33: Data trace write byte record

ID(31-28)	27-24	Addr(23-8)	D(7-0)
0011	Base	A15-A0,	D7-D0

Table 34: Data trace write half word record

ID(31-28)	27-24	Addr(23-8)	D(7-0)
0101	Base	A15-A0	D7-D0

Table 35: Data trace write word record

ID(31-28)	27-24	Addr(23-8)	D(7-0)
0111	Base	A15-A0	D7-D0

Three different formats are defined for a data trace record. Bits 31.29 contain the unique ID for the BYTE, HALF WORD or WORD wide data trace record. Bit 28 indicates a data read action(0) or a data write action(1). To avoid the generation of extra wait states, only one record can be written worst case for every instruction. For this reason, not the full absolute address is displayed in the trace record, but a dedicated address format, defined as a base and an offset.

Table 36: Base address ranges for data trace

B(27-28)	Base Address	Description
0000	0x0000.8000	non-shared RAM
0001	0x0001.0000	shared RAM
0010	0x00FF.0000	Peripherals
0011	0x0100.0000	DIP
0100	0x0102.0000	Gen2DSP peripherals
0101	0x0103.0000	Gen2DSP memory
0110	0x0yyy.0000	TRACE_START0_REG yyy = bits 6..14.

Table 36: Base address ranges for data trace

B(27-28)	Base Address	Description
0111	0x0yyy.0000	TRACE_START1_REG yyy = bits 6..14
1000	Unknown	Not in regions above
1xxx	Undefined	Undefined

Bits 27-24 define an address base, and bits 23-8 define the offset upon this base region. The table above shows the defined base addresses.

Bits 7-0 contain the 8 least significant data bits that are read or written..

Table 37: Data trace read half word extension record

ID(31-24)	Address(23-8)	Data(7-0)
0000 0100	A31-A16	D15-D8

Table 38: Data trace read word extension record

ID(31-24)	Data(23-0)
0000 0110	D31-D8

Table 39: Data trace write half word extension record

ID(31-24)	Address(23-8)	Data(7-0)
0000 0101	A31-A16	D15-D8

Table 40: Data trace write word extension record

ID(31-24)	Data(23-0)
0000 0111	D31-D8

When a half word or word wide data record is traced, and the next slot is empty, an extended data trace record will be written, as defined above. The missing data is now traced as well. When no time slot is available, the missing data will not be available for the user.

When the address is not in one of the ranges of the defined base addresses, the base will be 1000.
In case of a 16 bits read or write, the higher address bits will be incorporated in the Data trace extension record for that instruction.
In case of a 8 bits read or write, there is no Address Extension record and in case of a 32 bits read or write, the extension record is already full.
So in these cases, an extra Address extension record will be generated, as defined below..-

Table 41: Data trace read byte Address extension record

ID(31-20)	19-9	Address (8-0)
0000 0000 1000	0	A24-A16

Table 42: Data trace read word Address extension record

ID(31-20)	19-9	Address(8-0)
0000 0000 1001	0	A24-A16

Table 43: Address write byte Address extension record

ID(31-20)	19-9	Address(8-0)
0000 0000 1010	0	A24-A16

Table 44: Data trace write word Address extension record

ID(31-20)	19-9	Address(8-0)
0000 0000 1011	0	A24-A16

An important feature is the data trace of peripheral registers. To avoid that data will be missed to often, extra trace record formats (Table 45, Table 46) are defined that guarantees that no data will be missed.

Table 45: Data trace read half word alternative record

ID(31-30)	Address(29-16)	Data(15-0)
10	A14-A1, offset	D15-D0

Table 46: Data trace write half word alternative record

ID(31-30)	Address(29-16)	Data(15-0)
11	A14-A1, offset	D15-D0

The unique ID bit 31 has the value 1. Bit 30 indicates a data read action(0) or a data write action(1). The address bits 29-16 will contain the offset with respect to address value 0x0yyy.0000, where yyy = bits 14-6 of TRACE_START1_REG (0xFF5028) value. So the trace region for this data trace is limited to 15 bits.

The 25 bit address of this trace record is composed of two parts. The upper part, bits 24-15 is defined in the TRACE_START1_REG, bits 14-5 The lower part, bits 14-1 can be found in the trace record. Since only 16 bit data accesses in a 32 kbyte region defined by TRACE_START1_REG will generate these alternative data trace records, bit 0 will always be zero. So there is no need to store this bit.

Note that address bit 0 is no part of the address offset, since peripheral registers are bound to even addresses.

Also note that the use of this trace record is not limited to peripheral registers only, but it is applied in the whole address map wherever it fits for HALF WORD accesses on an even boundary.

29.4 EVENT TRACE

Event trace records (Table 45) are generated when one or more Events change from polarity and the corresponding Event Enable Bits in the TRACE_CTRL_REG bits 9-4. is set. Event records will be generated, but only in empty slots.,

Table 47: Event trace record

ID(31-27)	(26-20)	ID(19-16)	(15-0)
00001	events# (6-0)	overflows	TRACE_TIMERL

The following event are defined

Table 48: Event ID definition

Event#	Name
1000000	Bus grant for CR16Cplus
0100000	Gen2DSP event 0 (ECZ2)
0010000	Gen2DSP event 1 (WTF_IN)
0001000	DIP event 0 (DP0_OUT output **(Note 37)**)
0000100	DIP event 1 (DP1_OUT output **(Note 37)**)
0000010	External event 0 (P2[2])
0000001	External event 1 (P2[5])

Note 37: RF_DCF_MONITOR_REG[DP0_SEL][DP1_SEL] multiplexer outputs are used.

Overflows

When individual event bits have changed twice or more since the last event record was traced, one or more of the overflow bits 19-16 will be set:

- Bit 19: a bus grant (bit 7) change is not reported in time.
- Bit 18: a change of events 5 or 4 are not reported in time.
- Bit 17: a change of events 3 or 2 are not reported in time.
- Bit 16: a change of events 1 or 0 are not reported in time.

Trace timer

The trace unit has a real time TRACE_TIMER timer which is clocked with CR16C HCLK and starts to run from 0 as soon as one of the TRACE_CTRL_REG(9-4) is set to 1

Bits 15-0 (TRACE_TIMERL) of event trace record are the LSBs of TRACE_TIMER. If TRACE_TIMER changes from 0xFFFF to 0, an extended event record is written that contains the most significant bits 31-16

TRACE_TIMERH..

Table 49: Event extension record

ID(31-24)	Bits(23-16)	MSB timer value(15-0)
0000 0001	reserved	TRACE_TIMERH

30.0 Interrupt Control Unit (ICU)

The SC14480A5M, SC14480A2M6 has 8 non-maskable interrupt, maskable interrupts and 6 exception vectors. If an interrupt source becomes active the ICU generates an interrupt address. In case of a maskable interrupt source the ICU determines whether this interrupt source has the highest priority before the CR16Cplus is forced to terminate the current instruction. In case of a non-maskable interrupt source the CR16Cplus is always forced to terminate the current instruction. After saving the stack pointer and processor status register, the CR16Cplus executes interrupt service procedure at

INTBASE + [vector * 2] if CFG.ED=0
INTBASE + [vector * 4] if CFG.ED=1

The INTBASE can be stored with CR16Cplus instruction <LPR> or <LPRD>.

The vector addresses are shown in Table 50.

The NMI is shared between the watchdog timer and the DIP <U_VNMI> interrupt. Reading DIP_STATUS_REG determines whether the DIP generated the interrupt or not.

Interrupt priorities

The CR16Cplus has six fixed exception priorities as shown in Table 50. The DBG_TRAP has priority 1, IAD_TRAP has priority 2. The NMI is non maskable with priority 3. The ISE and exception vectors have the lowest priorities 5 and 6.

The non maskable interrupts with priority 4 have a programmable sub priority level which can be set in registers INTx_PRIORITY_REG (Table 172 to Table 175). Writing priority value '000' will disable these interrupts. If more than one interrupt request occurs the one with the highest priority is accepted, the others stay pending.

At the end of an interrupt service routine, the pending interrupt must be cleared by software by writing a 1 to register RESET_INT_PENDING_REG (0xFF5402) (table 194, page 196). This register also gives the status of the pending interrupt if read. If maskable interrupts have the same interrupt level the inherent priority scheme is used.

The maskable interrupts can also be set by software by writing a 1 to register SET_INT_PENDING_REG (0xFF5400) (table 196, page 197). This register also returns the status of the pending interrupt.

The watchdog timer will generate an NMI in case the TIMER_CTRL_REG[WDOG_CTRL] = 0, else a reset is generated.

Some interrupts are "ored" ; the interrupt routine must read the status registers is the connected sources to determine which interrupt has occurred. Next one or more service routines must be executed. Finally the active interrupt sources must be cleared and the RESET_INT_PENDING_REG can be set.

Four interrupts can also be generated by either DMA channels or other sources. DMAx_CTRL_REG[DINT] can be set to make this selected. Table 50 column "Secondary function with DINT" indicates which interrupts are selectable. See also Figure 81 on page 110.

See also AN-D-027 "Interrupt handling with SC144xx"

Table 50: SC14480A5M, SC14480A2M6 Interrupt Vectors

Interrupt source	Vector	Exception priority	Inherent sub priority	Description	Secondary function with DINT
Reserved	00	-	-		
NMI_INT	01	3	-	Non maskable interrupt from DIP <VNMI> and Watchdog timer	
Reserved	02	-	-		
Reserved	03	-	-		
Reserved	04	-	-		
SVC_TRAP	05	6 (exceptions)	-	Supervisor Call Trap	
DVZ_TRAP	06			Divide by zero Trap	
FLG_TRAP	07			Flag Trap	
BPT_TRAP	08			Breakpoint Trap	
TRC_TRAP	09			Trace Trap	
UND_TRAP	10			Undefined Instruction Trap	
Reserved	11	-	-		
IAD_TRAP	12	2	-	Illegal address Trap	
Reserved	13	-	-		
DBG_TRAP	14	1	-	Debug Trap	
ISE_INT	15	5	-	In System Emulator Interrupt caused by ISE pin or SDI	
ACCESS12_INT	16	4	Lowest	Access bus 1 and 2 interrupt	
KEYB_INT	17	4		Keyboard Interrupt or vectored level/edge interrupt	DMA1_INT
RESERVED_INT	18	4		Reserved	
CT_CLASSD_INT	19	4		Capture timer 1,2 interrupt or CLASSD clipping interrupt	
UART_RI_INT	20	4		UART RI interrupt	DMA2_INT
UART_TI_INT	21	4		UART TI interrupt	DMA3_INT
SPI_INT	22	4		SPI Interrupt	DMA0_INT
TIM0_INT	23	4		Timer 0 interrupt	
TIM1_INT	24	4		Timer 1 interrupt	
CLK100_INT	25	4		CLK100 interrupt	
DIP_INT	26	4		DIP Interrupt	
AD_INT	27	4		ADC interrupt	
SPI2	28	4		SPI2 interrupt	
DSP_INT	29	4		Gen2DSP Interrupt	
Reserved	30	4	Highest	Reserved	

Refer to Figure 81 on page 110 for an overview of interrupt multiplexers.

31.0 Boot program

31.1 BOOT PROCEDURES

The boot program is located at 0xFEF000 in ROM and is always executed after the RSTn pin is pulled low.

The boot program flow is shown afte Figure 88. The boot program may boot from the following sources in this order:

1. Boot from internal RAM at 0x10080 see paragraph 31.2
2. Boot from JTAG pin see paragraph 31.3
3. Boot from UART see paragraph 31.4
4. Boot from ACCESS2 par 31.5
5. Boot from SPI see paragraph 31.6
6. Boot from internal FLASH paragraph 31.7.
7. Boot from ROM see paragraph 31.8.

Note that the PC_START_REG is not modified in the booter. Jumps to any address location are possible. A SW_RESET restarts using PC_START_REG which can only be set at boundaries of 1 kByte.

31.2 BOOT FROM INTERNAL RAM

If DEBUG_REG[ENV_B01] = 1, the booter will execute from on chip RAM at 0x10080. Bit ENV_B01 is mostly set in a loader program and provides a jump to the loaded program after a SW_RESET.

31.3 BOOT FROM JTAG

If pin **JTAG=0** on the rising edge of RSTn, the JTAG one wire interface is enabled and the booter waits in an endless loop. After loading a program in on-chip or off-chip memory, the PC_START_REG may be changed to the desired start address and a software reset (DEBUG_REG [SW_RESET]=1) can be executed to start the loaded program. The JTAG interface can be disabled and invoked again at any time during program execution. See "SDI-JTAG" on page 112.

31.4 BOOT FROM UART

If **UTX=0** and URX=1 on the rising edge of RSTn, the UART boot protocol as shown in Table 52 is executed and the UART ports are set according Table 52:

Table 51: UART interface assignment at start-up

Pin name	Port number
UTX	P0[0] output
URX	P0[1] input with 10k pull-up

PAD_CTRL_REG[P001_OD] = 0, so no opendrain selected.

UART Configuration

The UART is configured for 9600 baud with 10.368 MHz Xtal and 19200 baud with 20.736 MHz Xtal.

No parity bits are added from start-up.

After sending the STX character, the watchdog is started and the boot program starts to wait for Byte 1 on URX. If no character is receives, the watchdog times out after 2.5s, generates an NMI and SW reset and the boot program restarts to boot from UART again.

If parameters LEN and CRC are both ACKnowledged, the loaded program is executed by a jump to 0x10080.

The boot protocol still supports one wire UART mode.

Table 52: UART boot protocol

Port	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte5..N	ByteN+1	ByteN+2
UTX	STX=02				ACK=0x6 NACK=0x15		CRC (XOR over CODE)	-
URX		SOH=01	LEN_LSB	LEN_MSB		CODE		ACK=06

31.5 BOOT FROM ACCESS BUS 2

See Figure 85**.** On the rising edge of RSTn, P0[0, 7] is latched into TEST_ENV_REG[0, 7]. If TEST_ENV_REG[0]=0 the booter polls the P0[1]/URX for 1ms. If P0[1]/URX='1' or becomes '1' within this time, the UART booter is invoked immediately as explained in "Boot from UART" on page 121. If P0[1]/URX='0' for 1 ms (BREAK condition), the ACCESS bus 2 boot protocol is invoked.

In both cases, BAT_CTRL_REG[REG_ON] is set. The allows starting a debug session without holding the PON button. In "normal" boot from ROM, the user application sets the REG_ON bit.

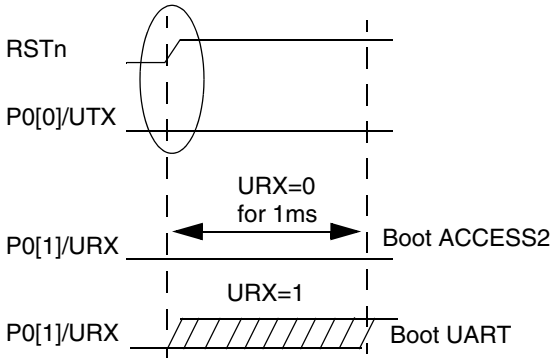

Figure 85 UART or ACCESS 2 boot selection

Table 53 shows the ACCESS bus 2 configuration and when the charge pump is switched on.

Table 53: ACCESS bus boot configuration for EEPROM

Pin name	Port	P0[7] = 1 CP_VOUT2 = off VDD = 1.8V	P0[7] = 0 CP_VOUT2 = 3V
SDA2	P0[2]	Open drain	Open drain
SCL2	P0[3]	Push pull	Open drain

ACCESS2 Register Configuration

- ACCESS2_CTRL_REG[SCK_SEL] = 00 (100 kHz)
- ACCESS2_CTRL_REG[SCK_NUM] = 1 (8 +ACK)
- ACCESS2_CTRL_REG[SDA_OD] = 1 (Open drain)
- ACCESS2_CTRL_REG[SCL_OD] = 1 (Open drain) if charge pump switched on ACCESS2_CTRL_REG[SCL_OD] = 1 (push pull) if charge pump off

Device address

The protocol accesses the EEPROM device at sub address (A2-A0) = 0

If the EEPROM responds with the format shown in Table 54, the ACCESS loader is copied to on-chip RAM address indicated by Bytes 2 to Byte 5.

Loading to on-chip RAM above 0x1F.FFF is not allowed. But doing so, the response bytes 0-7 are copied to address 0x10000 in on-chip memory and the boot program will wait in an endless loop.

If no EEPROM is connected, the booter continues booting form UART.

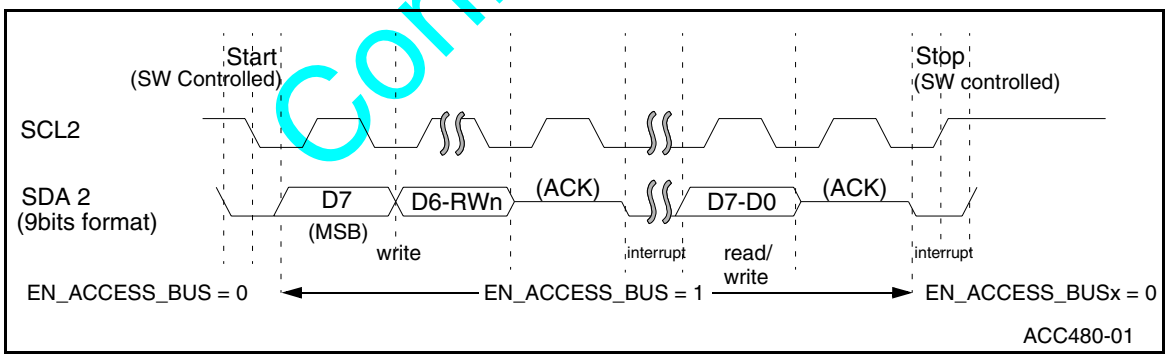

Figure 86 ACCESS bus master write/read access

Command format

S = ACCESS bus start condition

P = ACCESS bus stop condition

ACK = Acknowledge

NACK = Not Acknowledge

Table 54. The protocol starts by writing EEPROM slave address <A0 + sub address 0 + write bit> followed by EEPROM start addresses (0x00, 0x00) were the loader parameter are stored. Next the read command <A0 + sub address 0 + read bit> is given. The first two bytes in the DataFLASH must consist of a unique string. The

string (“pP”) must be recognized to continue

Table 54: Command sequence to EEPROM

									Byte 0		Byte 1	
S	SLAVE ADDR_W	ACK	Address byte 0	ACK	Address byte 1	S	SLAVE ADDR_R	ACK	Unique character	ACK	Unique character	ACK
	0xA0		0x00		0x00		0xA1		‘p’ (0x70)		‘P’ (0x50)	

Table 55. The following bytes 2 to 7 are interpreted as start address and length of the loader which must be an address in shared RAM or non Shared RAM below 0x20000. The booter uses addresses 0x10000 to 0x10007F, so 0x00010080 is a practical value for S3-S0.

.

Table 55: Response on Sequential READ on SDA from EEPROM address 0.

Byte 2		Byte 3		Byte 4		Byte 5		Byte 6		Byte 7		
Loader Start Address Bits31-24	ACK	Loader Start Address Bits23-16	ACK	Loader Start Address Bits15-8	ACK	Loader Start Address Bits 7-0	ACK	Loader Length Bits15-8	ACK	Loader Length Bits 7-0	NACK	P
S3		S2		S1		S0		L1		L0		

Table 56 The loader contents B0 to BN, starts from byte 8 and is copied for length L(1-0) to the specified location S(3-0) in on-chip RAM.

Table 56: Response on Sequential READ on SDA from EEPROM address 0.

									Byte8		Byte N		
S	SLAVE ADDR_W	ACK	Address byte 0	ACK	Address byte 1	S	SLAVE ADDR_R	ACK	Loader Byte 0	ACK	Loader Byte N	NACK	P
	0xA0		0		8		0xA1		B0		BN		

31.6 BOOT FROM SPI

The boot program tries to access a SPI DataFLASH through the following pins:

Table 57: SPI interface assignment for DataFLASH

Pin name	Port	Configuration for attempt 1,2 assumed SPI VDD = 1.8V	Configuration for attempt 3,4 assumed SPI CP_VOUT2 = 3V
SPI_DO	P0[6]	Output push-pull	Output open drain
SPI_DI	P0[7]	Input	Input
SPI_CLK	P0[5]	Output push-pull	Output open drain
SPI2_EN	P0[4]	Output push-pull	Output open drain

SPI Configuration

- SPI MODE 3 timing is used.
- The selected speed is XTAL/4
- Byte mode is selected.

Initially the boot program configures the SPI interface as shown in Table 57 and assumes the SPI is supplied from VDD=1.8V. Two attempts are done to find one of the three FLASH types, by sending three different OPCODES (Table 58) and watch their responses as shown in Table 58. If no valid responses are found, the SPI interface outputs are switched to open drain by setting PAD_CTRL_REG[P4567_OD] to 1 and the Charge pump output CP_VOUT**21** is enabled and set to 3V. Another two attempts are done to read the FLASH loader.

If no programmed SPI is found, the charge pump is disabled, the SPI interface is switched back to the port reset values, the SPI block is disabled and the booter continues with the next boot source. If the FLASH responds with the format shown in Table 58, the SPI loader is copied to on-chip RAM address indicated by Bytes 2 to Byte 5.

Loading to on-chip RAM above 0x1F.FFF is not allowed. But doing so, the response bytes 0-7 are copied to address 0x10000 in on-chip memory and the boot program will wait in an endless loop.

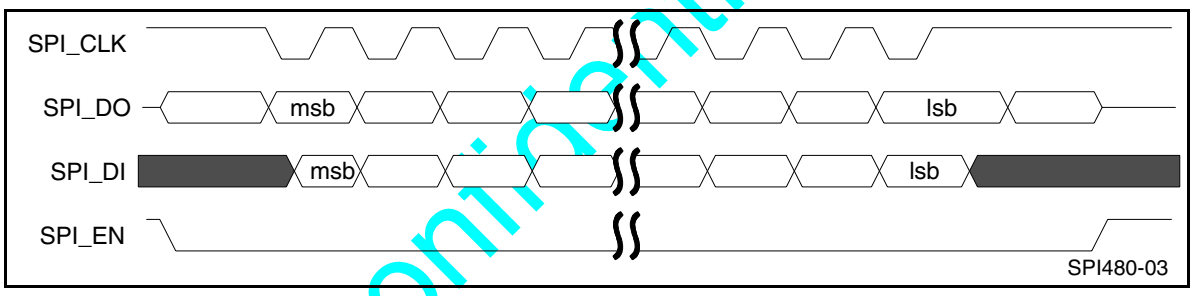

Figure 87 SPI master mode 3

Command format

The commands shown in Table 58 are executed two times in order to get the booter loader parameters from DataFLASH. Three commonly used read command opcodes are used: 03h, 0Bh, E8h. With these commands the majority of DataFLASH devices can be accessed. Each command has a corresponding number of dummy bytes.

Table 58: Command format to access various types of DataFLASH

Signal	Byte 0	Byte1	Byte 2	Byte 3	ByteN..	ByteM...
SPI_D0	OPCODE	Address byte 0	Address byte 1	Address byte 2	Dummy bytes	-
	03	0	0	0	-	-
	0B	0	0	0	0	-
	E8	0	0	0	0,0,0,0	-
SPI_DI	-		-		-	Response (See Table 59)

DataFLASH command response

See Table 59. The first two bytes in the DataFLASH must consist of a unique string. If this string (“pP”) is recognized, the following bytes are interpreted as start address and length of the loader. The loader contents B0 to BN, starts from byte 8 and is copied for length L(1-0) to the specified location S(3-0) in on-chip RAM.

The loader must be located between 0-16M, being the maximum code address space of the CR16.

Table 59: Response on SPI_DI from SPI DataFLASH

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte8	Byte N
Unique String		Loader Start Address f Bits31-24	Loader Start Address Bits23-16	Loader Start Address Bits15-8	Loader Start Address Bits 7-0	Loader Length Bits15-8	Loader Length Bits 7-0	Loader Byte 0	Loader Byte N
'p' (0x70)	'P' (0x50)	S3	S2	S1	S0	L1	L0	B0	BN

31.7 BOOT INTERNAL FLASH

If non of the boot sources is selected If FLASH available and the START parameter in the FLASH info block equals the string "sS", then the boot address is read from the PC_START parameter in the FLASH info block. The boot address is otherwise 0xF0000.

31.8 BOOT INTERNAL ROM

If non of the boot sources is selected and ROM is available, the boot program jumps to program ROM at 0xF0000.

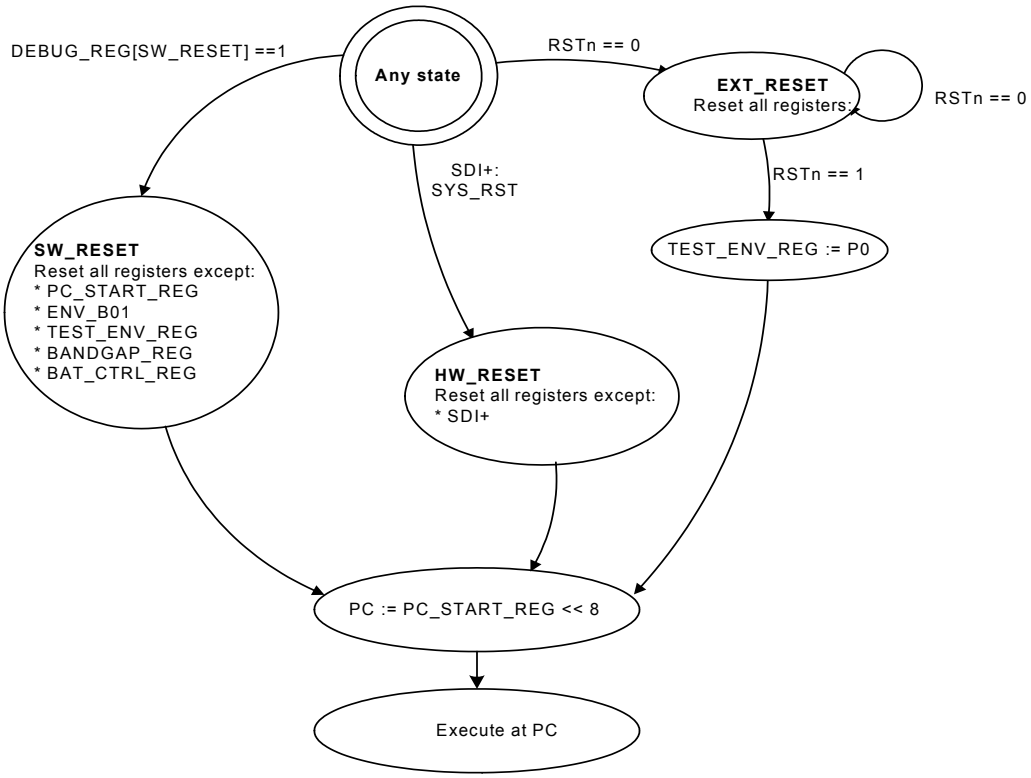

Figure 88 SC1448x Startup state machine (hardware)

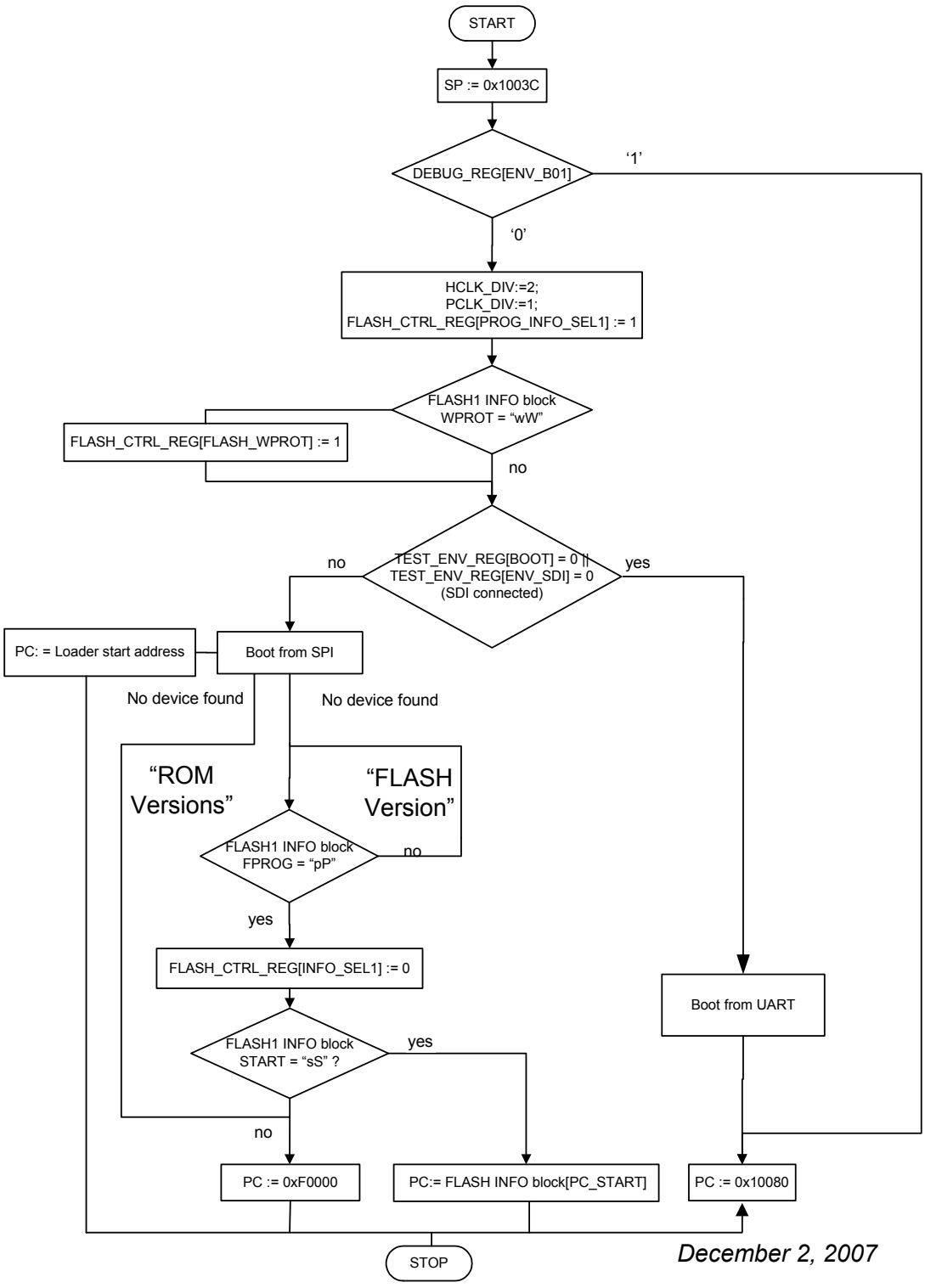

Figure 89 Boot ROM program at 0xFEF000 (A5M)

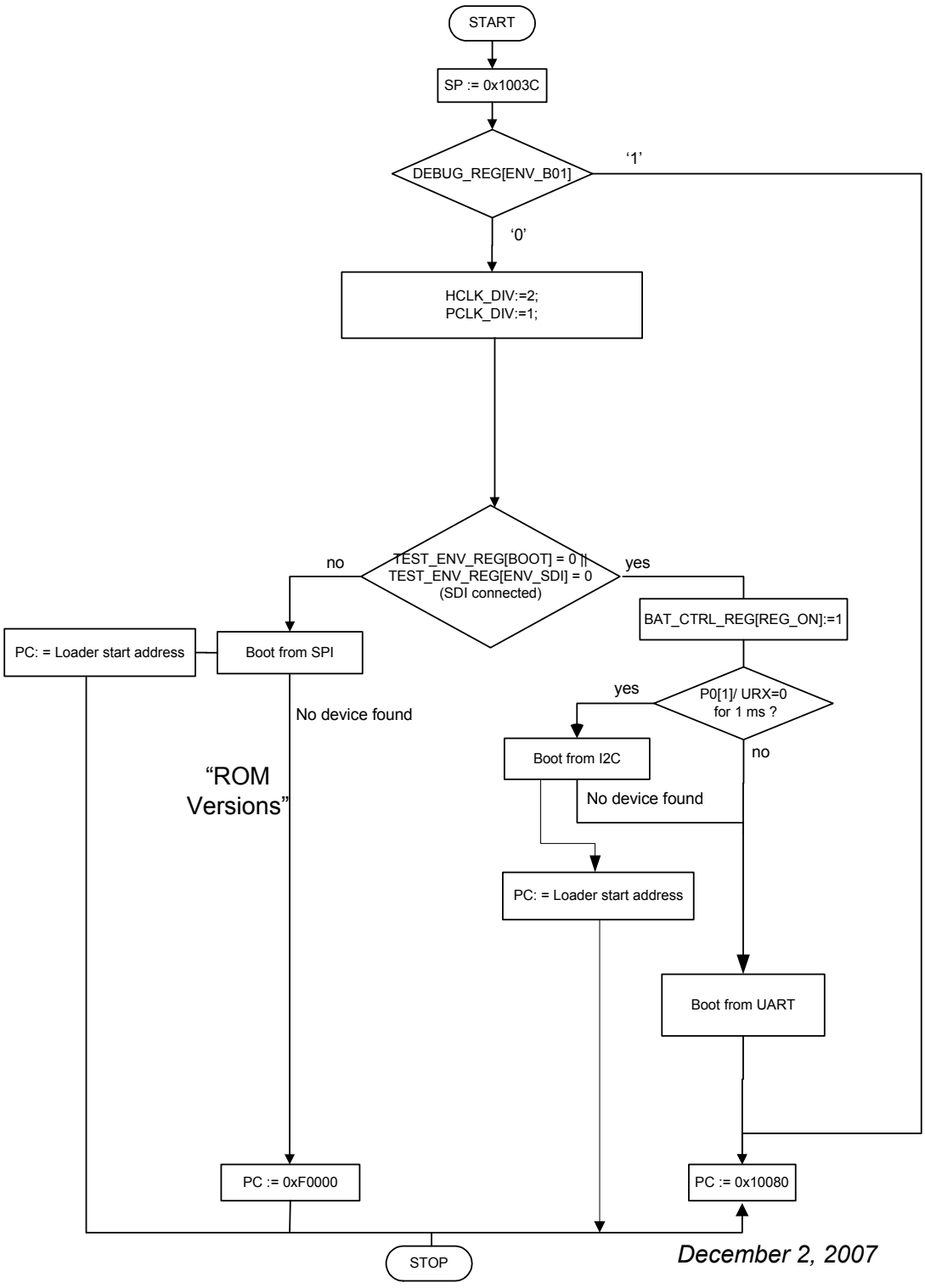

Figure 90 Boot ROM program at 0xFEF000 (A2M6)

32.0 Memories

32.1 BOOT ROM

The SC14480A5M, SC14480A2M6 has a boot ROM that is always executed when the chip starts up after the RSTn is asserted. Refer to "Boot program" on page 121 for the system startup procedure.

32.2 INTERNAL NON-SHARED RAM

The internal non-shared memory (if available) can be only accessed by CR16Cplus and is also used by the trace unit. (if available)

32.3 INTERNAL SHARED RAM

The internal shared memory (if available) can be accessed by the DIP, the Gen2DSP and the CR16Cplus. This memory is used to allocate CR16Cplus variables, DECT control, transmit and receive data, Gen2DSP variables and the Gen2DSP SCP program.

32.4 DIP SEQUENCER RAM

The 512 words of internal DIP program RAM contains the DIP executable code. The executable code inside the RAM can be read and written by the CR16Cplus at any time. An internal bus arbiter takes care of the potential bus conflict if the DIP and CR16Cplus access the DIP sequencer at the same time.

32.5 PROGRAM FLASH

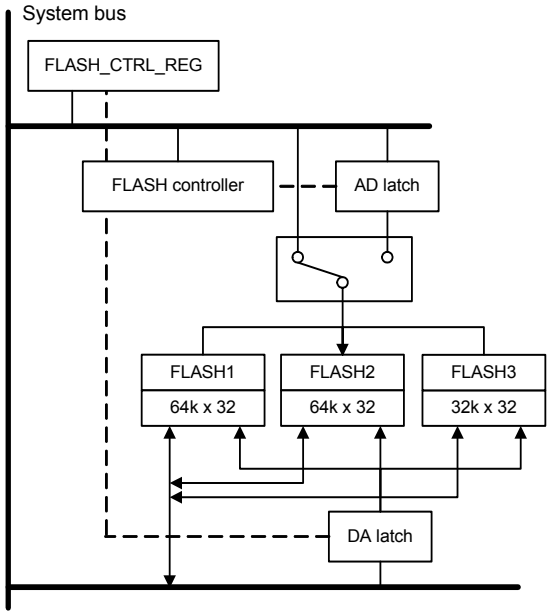

Figure 91 Program FLASH block diagram

The 5 Mbit of on-chip program FLASH memory is fully tested erasable and programmable FLASH and has the following **characteristics**:

- Maximum speed 20.736 MHz.
- Mass erase time: 20 ms (TYP)
- DWord (32bits) Program time: 20 us (TYP)
- Endurance of 500 worst case
- Page erase size of 256/512 Dwords

FLASH organisation

The FLASH memory is organized in three blocks:

- Address: 0xF0000 64k x 32 bits (2Mbit)
  page erase size 512 dWords = 2kbyte
- Address 0x130000 64k x 32 bits(2Mbit)
  page erase size 512 dWords = 2kbyte
- Address 0x170000 32k x 32 bits (1Mbit)
  page erase size 256 dWords = 1kbyte

Control registers

The FLASH block is controlled via the following registers:

- FLASH_CTRL_REG (0xFF7400)
- FLASH_PTNVH1_REG (0xFF7402)
- FLASH_PTPROG_REG (0xFF7404)
- FLASH_PTERASE_REG (0xFF7406)
- FLASH_PTME_REG (0xFF7408)
- MEM_CONFIG_REG (0xFF5006)

Read access

For read access FLASH_CTRL_REG (0xFF7400) must be 0. The other registers are don't care.

The FLASH can be accessed at 20.736 MHz maximum. With CR16Cplus maximum clock frequency of 41.472 MHz, one wait cycles must be inserted. The wait cycles can be set in the MEM_CONFIG_REG[T_RC]

Reprogramming and erasing of the program FLASH can be done at page boundaries of 2kbyte (FLASH 1 and FLASH 2) and 1kbyte (FLASH3). A page must be erased before it is reprogrammed. Hereafter the whole page can be rewritten.

The erase/reprogram flow diagram is shown in Figure 92 on page 129.

Erase operation

Erasing the program FLASH can be done either for each page separately (page erase) or for one of the FLASH block 1,2 or 3 completely (mass erase).

To erase the program FLASH, first a FLASH block must be selected for write/erase with FLASH_CTRL_REG (0xFF7400) bits **FLASH_SEL1** (2Mbit) and/or

FLASH_SEL2 (2+1Mbit). If FLASH_SEL1 is '1', Flash1 is selected for erase/write. If FLASH_SEL2 is '1', Flash2 and Flash3 are both selected for erase/write If FLASH_SEL1 and FLASH_SEL2 are both '1', then all FLASH blocks are selected for erase/write. (If both bits are '0', then the read only mode is selected and the FLASH is protected against erase and write operations.)

Next **PROG_MODE** must be set to 10 or 11 to select either page or bulk (mass) erase in the selected FLASH blocks. Hereafter, a sequence of write operations must be fulfilled. First data 0xAAAAAAAA (Dword) has to be written to the address 0x0F5554. (or 0x135554 or 0x175554) Secondly, data 0x55555555 (Dword) has to be written to the address 0x0FAAA8 (or 0x13AAA8 or 0x17AAA8)

To start the erase a dummy word must be written to anywhere in the selected flash block (bulk erase selected) or page (page erase) which should be erased. If the bulk-erase option is selected, the dummy word address selects one of the Flash blocks. If the page erasing is selected, the dummy word address selects the page address.

It takes 20 msec (minimum) to erase a page or a complete FLASH block. The page and mass erase duration and programming time are programmable in units of 0.86 us.

Device Programming

When the erase operation is completed the **PROG_ERS** bit becomes '0' and new data can be written to any location. **Data can only be written as aligned Dwords (32bits), however two write cycles of 16 bits to successive word addresses are also allowed.** The write mode must be enabled with bits **PROG_MODE** set to 01. While the write operation is in progress, bit **PROG_WRS** is 1. After the word is written, this bit becomes 0 (after 20 us), although the write mode stays enabled.

The FLASH automatically enables its fast page programming mode as long as the address stays in the same page range and a word is written.

If switching from erase or write mode to read mode the software must first check the FLASH_CTRL_REG[**PROG_RMIN**]. As long as this bit is '1', the previous operation is still in progress and the read mode may NOT be selected.

For optimal power saving, the software must switch to read mode for all Flash Blocks by writing '0' to FLASH_SEL1 and FLASH_SEL2

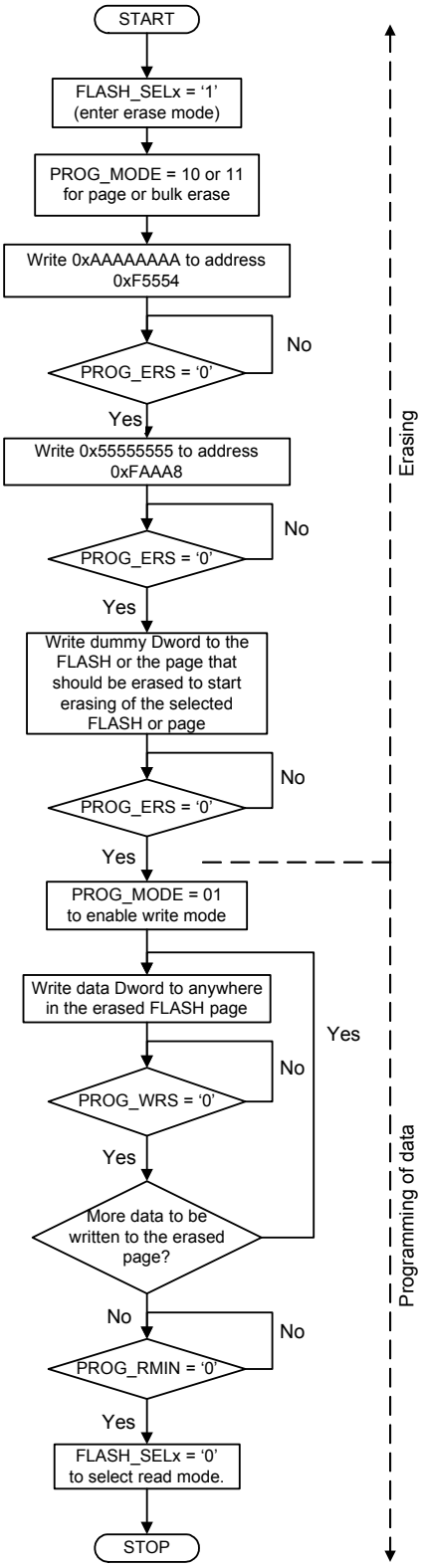

Figure 92 Program FLASH erasing/programming

32.5.1 Information blocks 1,2,3

Each program FLASH memory has an information block in addition to the main memory block. The info blocks are mirrored every 512 words.

PROG_INFO_SEL1=1 selects information block 1 (Start 0xF0000, size 512x32) of FLASH 1
PROG_INFO_SEL2=1 selects information block 2 (Start 0x130000, size 512x32) of FLASH 2 and information block 3 (Start 0x170000, size 256x32) of FLASH 3

A part of Information block 1 is used by the boot program as shown in Table 60. The remaining part of this block and information block 2 and 3 can be freely used for data storage.

Erasing/Programming of the information blocks is equal to the Erasing/programming procedure for the main blocks.

Parameter WPROT. If this value is “wW”, the boot program makes the complete program FLASH erase/write protected by setting the FLASH_CTRL_REG[FLASH_WPROT] = ‘1’. This bit can only be set and is only reset with RSTn.

Parameter FPROG. If this value is “pP”, this is an indication that the program FLASH contains a valid program. This value must be programmed by the user after the Flash is programmed. The boot program will jump to the on-chip program FLASH address $F0000_{16}$ if no boot option is selected.

If the information blocks are erased and contain $0xFFFFFFFF_{16}$, then the program FLASH is marked as ‘Not Programmed’ (FPROG is not equal to “pP”) and no read protection and no write protection in activated by the boot program.

Parameter START. If this value “sS” and FPROG is “pP”, the start address is read from parameter field PC_START. If START has another value, the start address is 0x0F0000. For migration to ROM later, it is not recommended to use the START and PC_START for start address redirection.

Table 60: Info block 1 information used by booter

Address (+N*0x0400)	Parameter	Value	Description
0x0F0000	WPROT	0x77 (‘w’)	Program FLASH 1,2,3 will be set to write protected if the indicated values are programmed
0x0F0001		0x57 (‘W’)	
0x0F0002		0	
0x0F0003		0	
0x0F0004	FPROG	0x70 (‘p’)	If indicated values are programmed, the FLASH is recognised as being available and programmed. The boot program can execute from on-chip FLASH
0x0F0005		0x50 (‘P’)	
0x0F0006		0	
0x0F0007		0	
0x0F0008	START	0x73 (‘s’)	If indicated values are programmed, the FLASH start address can be modified with parameter PC_START, otherwise start address 0x0F0000 is assumed
0x0F0009		0x53 (‘S’)	
0x0F000A		0	
0x0F000B		0	
0x0F000C 0x0F000F	PC_START	PC_START[7-0] PC_START[15-8] 0 0	Modified FLASH start address is written to the PC_START_REG[15:2] register if the START parameter indicates start address modification. Else this value is don’t care.
0x0F0010 0x0F00FF	-		Not used, free usage

32.6 PROGRAM ROM

The on-chip CR16plus program ROM, if available, is located at address 0xF0000.

The ROM can be accessed at 20.736 MHz maximum. With CR16Cplus maximum clock frequency of 41.472 MHz, one wait cycles must be set in the MEM_CONFIG_REG[T_RC].

32.7 MIGRATION FROM PROGRAM FLASH TO PROGRAM ROM

Refer to AN-D-153 “ SC14480 FLASH to ROM migration check list”

33.0 Memory map

33.1 MEMORY MAP OVERVIEW

Table 61: SC14480A5M, SC14480A2M6 CR16Cplus Memory Map

Address	Memory map
0x0000.0000 0x0000.7FFF	**Reserved** 32k reserved
0x0000.8000 0x0000.9FFF	**Non-shared RAM (A5M) (Not on A2M6)** 8 kbyte
0x0000.A000 0x0000.FFFF	**Reserved** 24k reserved
0x0001.0000 0x0001.FFFF	**Shared RAM for CR16Cplus, Gen2DSP and DIP** See Table 62 on page 132 for details
0x0002.0000 0x000E.FFFF	**Reserved** (832 kbyte)
0x000F.0000 0x002E.FFFF	**Program FLASH/ROM** 0x000F.0000-0x0012.FFFF for 2.0 Mbit ROM 0x000F.0000-0x0014.37FF for 2.6 Mbit ROM 0x000F.0000-0x0015.FFFF for 3.5 Mbit ROM 0x000F.0000-0x0018.FFFF for 5.0 Mbit ROM 0x000F.0000-0x0018.FFFF for 5.0 Mbit FLASH (FLASH including INFO block1, mirrored every 512 words)
0x002F.0000 0x00FE.EFFF	**Reserved**
0x00FE.F000 0x00FE.F7FF	**Boot ROM** (2 kbyte)
0x00FE.F800 0x00FE.FFFF	**Reserved** (2 kbyte)
0x00FF.0000 0x00FF.FBFF	On-chip Peripheral and Chip ID **Registers** (see page 135) (63 kbyte)
0x00FF.FC00 0x00FF.FFFF	Internally used for **ICU vectors** and traps (1 kbyte)
0x0100.0000 0x0100.01FF	DIP **Sequencer** RAM (512 bytes)
0x0100.0200 0x0100.03FF	DIP **Sequencer** RAM (512 bytes) addressed with <JMPF>,<BR_B1> commands
0x0100.0400 0x0101.FFFF	**Reserved** (127 kbyte)
0x0102.0000 0x0102.FFFF	**Shared ROM + Registers for the Gen2DSP and CR16plus** See Table 62 on page 132 for details
0x0103.0000 0x0104.FFFF	**Micro Program ROM and RAM for the Gen2DSP** See Table 63 on page 132 for details
0x0105.0000 0x01FF.FFFF	Reserved

Note 38: The Gen2DSP Micro program ROM is accessible by CR16Cplus only in testmode.

Note 39: 1 kbyte = 1024 bytes. 1Mbit = 1024*1024 bits 1Gbyte = 1024*1024*1024 bytes

Table 62: Detailed shared Data RAM Memory map for DIP, CR16Cplus and Gen2DSP

CR16Cplus Address	DIP Address	Gen2DSP Data Address	Description
0x001.0000 0x001.3FFF(16 kbyte)	0 0x3FFF (16k*8)	0 0x1FFF (8k*16)	Shared RAM
0x001.4000 0x001.FFFF (48 kbyte)	004000 0xFFFF (48k*8)	0x2000 0x7FFF (24k*16)	Shared RAM (Reserved)
0x102.0000 0x102.53FF (21kbyte)		0x8000 0xA9FF	Shared Data ROM(0k A2M6) **(Table 64 on page 133)**
0x102.5400 0x102.7F7F (11k-128)		0xAA00 0xBFBF	Shared ROM (reserved)
0x102.7F80 0x102.7FFF		0xBFC0 0xBFFF	Gen2DSP registers. **(Table 65 on page 133)**
0x102.8000 0x102.FFFF		0xC000 0xFFFF	Reserved

Note 40: Refer to "SC1448x_family_overview.xls" for the comparison of the memory sizes.
Refer to AN-D-153 "SC1448x ROm delivery Procedure and migration checklist" for differences between FLASH and ROM devices.

Table 63: Detailed micro code RAM and ROM Memory map for DIP, CR16Cplus and Gen2DSP

CR16Cplus Address	DIP Code Address	Gen2DSP Code Address	Micro Code Memory
0x100.0000 0x100.03FF (1 kbyte)	0 0x1FF (512*16)		DIP Micro code RAM
0x100.0400 0x100.0FFF (3 kbyte)	0x200 0x7FF (1536*16)		DIP Micro code RAM (reserved)
0x103.0000 0x103.07FF (2 kbyte)		0x0000 0x03FF	Gen2DSP Micro code RAM
0x103.0800 0x103.7FFF (30 kbyte)		0x0400 0x3FFF	Gen2DSP Micro code RAM (Reserved)
0x001.0000 0x001.3FFF(16 kbyte)		0x4000 0x5FFF	Gen2DSP Micro code RAM Mapped in Shared RAM
0x001.4000 0x001.7FFF (16 kbyte)		0x6000 0x7FFF	Gen2DSP Micro code RAM (Reserved)
0x104.0000 0x104.AFFF (44 kbyte)		0x8000 0xD7FF	Micro code ROM **(See also 10.13 on page 60)** (A2M6 22k)
0x104.B000 0x104.FFFF (20 kbyte)		0xD800 0xFFFF	Reserved

33.2 GEN2DSP /CR16CPLUS CROSS REFERENCE ROM TABLES

Table 64: Gen2DSP /CR16Cplus shared ROM tables

CR16Cplus address	Gen2DSP Data address	Port	Description	A5M
0x1020000	0x8000	CFFT_TWIDDLE_128	PAEC FFT Twiddle Factor	✓
0x1020200	0x8100	CFFT_WINDOW_SINE128	FFT Sine Window (obsolete)	✓
0x1020300	0x8180	CFFT_WINDOW_TRIANGLE128	FFT Triangle Window (obsolete)	✓
0x1020400	0x8200	DCT_QTABLE_ROM	JPEG DCT Quantization	✓
0x1020500	0x8280	DCT_ZIGZAG_ADDR_PTR	JPEG DCT ZigZag Table	✓
0x1020580	0x82C0	G726_xxx	G726 Data Tables	✓
0x10205E0	0x82F0	G722_xxx	G722 Constants Tables	✓
0x10207C2	0x83E1 0xA761	VAC_SCFTAB	SVC Constant Tables	✓

Note: A2M6 and A2L versions have no shared ROM constants, the tables for G722, G726, and optional PAEC must be placed in RAM.

33.3 GEN2DSP /CR16CPLUS CROSS REFERENCE REGISTER MAP

Table 65: Gen2DSP / CR16Cplus cross reference register map

CR16Cplus Address	Gen2DSP Data Address	Port	Description
0x102.7F80	0xBFC0	DSP_MAIN_SYNC0_REG	DSP main counter outputs selection register 0
0x102.7F82	0xBFC1	DSP_MAIN_SYNC1_REG	DSP main counter outputs selection register 1
0x102.7F84	0xBFC2	DSP_MAIN_CNT_REG	DSP main counter register
0x102.7F86	0xBFC3	DSP_ADC1S_REG	ADC1 Input 2's Complement register
0x102.7F88	0xBFC4	DSP_ADC0S_REG	ADC0 Input 2's Complement register
0x102.7F8A	0xBFC5	DSP_CLASSD_REG	CLASSD Output output data register
0x102.7F8C	0xBFC6	DSP_CODEC_MIC_GAIN_REG	CODEC MIC GAIN register
0x102.7F8E	0xBFC7	DSP_CODEC_OUT_REG	CODEC DATA register
0x102.7F90	0xBFC8	DSP_CODEC_IN_REG	CODEC DATA register
0x102.7F92	0xBFC9	DSP_RAM_OUT0_REG	Shared RAM output register 0
0x102.7F94	0xBFCA	DSP_RAM_OUT1_REG	Shared RAM output register 1
0x102.7F96	0xBFCB	DSP_RAM_OUT2_REG	Shared RAM output register 2
0x102.7F98	0xBFCC	DSP_RAM_OUT3_REG	Shared RAM output register 3
0x102.7F9A	0xBFCD	DSP_RAM_IN0_REG	Shared RAM input register 0
0x102.7F9C	0xBFCE	DSP_RAM_IN1_REG	Shared RAM input register 1
0x102.7F9E	0xBFCF	DSP_RAM_IN2_REG	Shared RAM input register 2
0x102.7FA0	0xBFD0	DSP_RAM_IN3_REG	Shared RAM input register 3
0x102.7FA2	0xBFD1	DSP_ZCROSS1_OUT_REG	ZERO CROSSING 1 output register
0x102.7FA4	0xBFD2	DSP_ZCROSS2_OUT_REG	ZERO CROSSING 2 output register
0x102.7FA6	0xBFD3	DSP_PCM_OUT0_REG	PCM channel 0 output register
0x102.7FA8	0xBFD4	DSP_PCM_OUT1_REG	PCM channel 1 output register
0x102.7FAA	0xBFD5	DSP_PCM_OUT2_REG	PCM channel 2 output register
0x102.7FAC	0xBFD6	DSP_PCM_OUT3_REG	PCM channel 3 output register

Table 65: Gen2DSP / CR16Cplus cross reference register map

CR16Cplus Address	Gen2DSP Data Address	Port	Description
0x102.7FAE	0xBFD7	DSP_PCM_IN0_REG	PCM channel 0 input register
0x102.7FB0	0xBFD8	DSP_PCM_IN1_REG	PCM channel 1 input register
0x102.7FB2	0xBFD9	DSP_PCM_IN2_REG	PCM channel 2 input register
0x102.7FB4	0xBFDA	DSP_PCM_IN3_REG	PCM channel 3 input
0x102.7FB6	0xBFDB	DSP_PCM_CTRL_REG	PCM Control register
0x102.7FB8	0xBFDC	DSP_PHASE_INFO_REG	Phase information between PCM FSC 8/16/32 and main counter 8/16/32 kHz
0x102.7FBA	0xBFDD		Reserved
0x102.7FBC	0xBFDE	DSP_MAIN_CTRL_REG	DSP Main counter control and preset value
0x102.7FBE	0xBFDF	DSP_CLASSD_BUZZOFF_REG	CLASSD buzzer on/off control
0x102.7FBF	0xBFE0	Reserved	
0x102.7FCE	0xBFE7	Reserved	
0x102.7FD0	0xBFE8	DSP_CTRL_REG	DSP control register
0x102.7FD2	0xBFE9	DSP_PC_REG	DSP Program counter
0x102.7FD4	0xBFEA	DSP_PC_START_REG	DSP Program counter start
0x102.7FD6	0xBFEB	DSP_IRQ_START_REG	DSP Interrupt vector start
0x102.7FD8	0xBFEC	DSP_INT_REG	DSP to CR16Cplus interrupt vector
0x102.7FDA	0xBFED	DSP_INT_MASK_REG	DSP to CR16Cplus interrupt vector maks
0x102.7FDC	0xBFEE	DSP_INT_PRIO1_REG	DSP interrupt mux 1
0x102.7FDE	0xBFEF	DSP_INT_PRIO2_REG	DSP interrupt mux 2
0x102.7FE0	0xBFF0	DSP_OVERFLOW_REG	DSP to CR16Cplus Interrupt overflow
0x102.7FE2 0x102.7FEE	0xBFF1 0xBFF7	Reserved	
0x102.7FF0	0xBFF8	DBG_IREG	DSP JTAG instruction register
0x102.7FF2	0xBFF9	Reserved	
0x102.7FF4 0x102.7FF6	0xBFFA	DBG_INOUT_REG (LSW) DBG_INOUT_REG (MSW)	DSP DEBUG data register (32 bits)
0x102.7FF8 0x102.7FFF	0xBFF4 0xBFFF	Reserved	

33.4 CR16CPLUS MEMORY MAP DETAILED

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0x000000		Reserved (32kbyte)
0x007FFF		
0x008000	RAM_START	Non-shared RAM up-to 8kbyte (See family overview for availability and size)
0x009FFF	RAM_END	
0x00A000		Reserved (24kbyte)
0x00FFFF		
0x010000	SHARED_RAM_START	Shared RAM up-to 16 kbytes (See family overview for availability and size)
0x013FFF	SHARED_RAM_END	
0x014000	-	Reserved
0x01FFFF	-	
0x020000	-	Free
0x07FFFF	-	
0x0F0000	PROGRAM_START	Program FLASH/ROM Up-to 5.0 Mbit (See family overview for availability and size)
0x2EFFFF	PROGRAM_END	
0xFEF000	BOOT_ROM_START	Boot ROM (2k)
0xFEF7FF	BOOT_ROM_END	
0xFEF800		Reserved for booter
0xFEFFFF		
0xFF0000		Reserved
0xFF07FF		
0xFF0800		Reserved for AHB peripherals
0xFF3FFF		
	-	
0xFF4000	CLK_AMBA_REG	HCLK, PCLK, divider and clock gates
0xFF4002	CLK_CODEC_DIV_REG	Codec divider register
0xFF4004	CLK_CODEC_REG	Codec clock selection register
0xFF4006	CLK_DSP_REG	DSP clock selection register
0xFF4008	Reserved	
0xFF400A	CLK_FREQ_TRIM_REG	Xtal frequency trimming register.
0xFF400C	CLK_PER_DIV_REG	Peripheral divider register for 2,1, 1/2, 1/4 MHz clocks
0xFF400E	CLK_PER10_DIV_REG	Peripheral divider register for 20, 10 MHz clocks
0xFF4010	CLK_PLL_CTRL_REG	PLL control register
0xFF4012	CLK_PLL_DIV_REG	PLL divider register
0xFF4014	Reserved	
0xFF4016	Reserved	
0xFF4018	CLK_XTAL_CTRL_REG	Crystal, PLL control register
0xFF401A	CLK_AUX_REG	Auxiliary clock control register

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF401C		Reserved
0xFF43FF		
0xFF4400	DMA0_A_STARTL_REG	Start address Low A of DMA channel 0
0xFF4402	DMA0_A_STARTH_REG	Start address Low A of DMA channel 0
0xFF4404	DMA0_B_STARTL_REG	Start address Low B of DMA channel 0
0xFF4406	DMA0_B_STARTH_REG	Start address High B of DMA channel 0
0xFF4408	DMA0_INT_REG	DMA receive interrupt register channel 0
0xFF440A	DMA0_LEN_REG	DMA receive length register channel 0
0xFF440C	DMA0_CTRL_REG	Control register for the DMA channel 0
0xFF440E	DMA0_IDX_REG	Internal Index register for the DMA channel 0
0xFF4410	DMA1_A_STARTL_REG	Start address Low A of DMA channel 1
0xFF4412	DMA1_A_STARTH_REG	Start address High A of DMA channel 1
0xFF4414	DMA1_B_STARTL_REG	Start address Low B of DMA channel 1
0xFF4416	DMA1_B_STARTH_REG	Start address High B of DMA channel 1
0xFF4418	DMA1_INT_REG	DMA receive interrupt register channel 1
0xFF441A	DMA1_LEN_REG	DMA receive length register channel 1
0xFF441C	DMA1_CTRL_REG	Control register for the DMA channel 1
0xFF441E	DMA1_IDX_REG	Internal Index register for the DMA channel 1
0xFF4420	DMA2_A_STARTL_REG	Start address Low A of DMA channel 2
0xFF4422	DMA2_A_STARTH_REG	Start address High A of DMA channel 2
0xFF4424	DMA2_B_STARTL_REG	Start address Low B of DMA channel 2
0xFF4426	DMA2_B_STARTH_REG	Start address High B of DMA channel 2
0xFF4428	DMA2_INT_REG	DMA receive interrupt register channel 2
0xFF442A	DMA2_LEN_REG	DMA receive length register channel 2
0xFF442C	DMA2_CTRL_REG	Control register for the DMA channel 2
0xFF442E	DMA2_IDX_REG	Internal Index register for the DMA channel 2
0xFF4430	DMA3_A_STARTL_REG	Start address Low A of DMA channel 3
0xFF4432	DMA3_A_STARTH_REG	Start address High A of DMA channel 3
0xFF4434	DMA3_B_STARTL_REG	Start address Low B of DMA channel 3
0xFF4436	DMA3_B_STARTH_REG	Start address High B of DMA channel 3
0xFF4438	DMA3_INT_REG	DMA receive interrupt register channel 3
0xFF443A	DMA3_LEN_REG	DMA receive length register channel 3
0xFF443C	DMA3_CTRL_REG	Control register for the DMA channel 3
0xFF443E	DMA3_IDX_REG	Internal Index register for the DMA channel 3
0xFF4440		Reserved
0xFF47FF		
0xFF4800	TEST_ENV_REG	CR16Cplus boot mode control register
0xFF4802	TEST_CTRL_REG	Test control register, shall not be modified
0xFF4804	TEST_CTRL2_REG	Test control register 2

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF4810	BANDGAP_REG	Bandgap register
0xFF4812	BAT_CTRL_REG	Power management control register
0xFF4814	BAT_CTRL2_REG	Power charge control register
0xFF4816	BAT_STATUS_REG	Power status register
0xFF4818	BAT_SOC_HIGH_REG	Power state of charge counter (high)
0xFF481A	BAT_SOC_LOW_REG	Power state of charge counter (low)
0xFF481C	CP_CTRL_REG	Charge pump tripler control register.
0xFF481E	PAD_CTRL_REG	PAD control register
0xFF4830	P0_DATA_REG	P0 Data register
0xFF4832	P0_SET_DATA_REG	P0 set port pins register
0xFF4834	P0_RESET_DATA_REG	P0 reset port pins register
0xFF4836	P0_DIR_REG	P0 direction register
0xFF4838	P0_MODE_REG	P0 Mode register
0xFF4840	P1_DATA_REG	P1 Data register
0xFF4842	P1_SET_DATA_REG	P1 set port pins register
0xFF4844	P1_RESET_DATA_REG	P1 reset port pins register
0xFF4846	P1_DIR_REG	P1 direction register
0xFF4848	P1_MODE_REG	P1 Mode register
0xFF4850	P2_DATA_REG	P2 Data register
0xFF4852	P2_SET_DATA_REG	P2 set port pins register
0xFF4854	P2_RESET_DATA_REG	P2 reset port pins register
0xFF4856	P2_DIR_REG	P2 direction register
0xFF4858	P2_MODE_REG	P2 Mode register
0xFF4860	P3_DATA_REG	P3 Data register
0xFF4862	P3_SET_DATA_REG	P3 set port pins register
0xFF4864	P3_RESET_DATA_REG	P3 reset port pins register
0xFF4866	P3_DIR_REG	P3 direction register
0xFF4868	P3_MODE_REG	P3 Mode register
Additional ports on KGD		
0xFF4870	P4_DATA_REG	P4 Data register
0xFF4872	P4_SET_DATA_REG	P4 set port pins register
0xFF4874	P4_RESET_DATA_REG	P4 reset port pins register
0xFF4876	P4_DIR_REG	P4 direction register
0xFF4878	P4_MODE_REG	P4 Mode register
0xFF4880	P5_DATA_REG	P5 Data register
0xFF4882	P5_SET_DATA_REG	P5 set port pins register
0xFF4884	P5_RESET_DATA_REG	P5 reset port pins register

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF4886	P5_DIR_REG	P5 direction register
0xFF4888	P5_MODE_REG	P5 Mode register
0xFF4900	UART_CTRL_REG	UART control register
0xFF4902	UART_RX_TX_REG	UART data transmit/receive register
0xFF4904	UART_CLEAR_TX_INT_REG	UART clear transmit interrupt
0xFF4906	UART_CLEAR_RX_INT_REG	UART clear receive interrupt
0xFF4908	UART_ERROR_REG	UART Parity error register
0xFF4920	ACCESS1_IN_OUT_REG	ACCESS bus 1 receive/transmit register
0xFF4922	ACCESS1_CTRL_REG	ACCESS bus 1 Control register
0xFF4924	ACCESS1_CLEAR_INT_REG	Clear ACCESS bus 1 interrupt
0xFF4930	ACCESS2_IN_OUT_REG	ACCESS bus 2 receive/transmit register
0xFF4932	ACCESS2_CTRL_REG	ACCESS bus 2 Control register
0xFF4934	ACCESS2_CLEAR_INT_REG	Clear ACCESS bus 2 interrupt
0xFF4940	SPI_CTRL_REG	SPI control register
0xFF4942	SPI_RX_TX_REG0	SPI RX/TX register0
0xFF4944	SPI_RX_TX_REG1	SPI RX/TX register1
0xFF4946	SPI_CLEAR_INT_REG	SPI clear interrupt register
Additional ports on KGD		
0xFF4950	SPI2_CTRL_REG	SPI2 control register
0xFF4952	SPI2_RX_TX_REG0	SPI2 RX/TX register0
0xFF4954	SPI2_RX_TX_REG1	SPI2 RX/TX register1
0xFF4956	SPI2_CLEAR_INT_REG	SPI2 clear interrupt register
0xFF4960	ADC_CTRL_REG	ADC control register
0xFF4962	ADC_CTRL1_REG	ADC control register 1
0xFF4964	ADC_CLEAR_INT_REG	Clears ADC interrupt if set in AD_CTRL_REG
0xFF4966	ADC0_REG	ADC0 result register
0xFF4968	ADC1_REG	ADC1 result registers
0xFF4970	TIMER_CTRL_REG	Timers control registers
0xFF4972	TIMER0_ON_REG	Timers 0 on control registers
0xFF4974	TIMER0_RELOAD_M_REG	2 x 16 bits reload value for Timer0
0xFF4976	TIMER0_RELOAD_N_REG	
0xFF4978	TIMER1_RELOAD_M_REG	2 x 16 bits reload value for Timer1
0xFF497A	TIMER1_RELOAD_N_REG	
0xFF497C	TIMER2_DUTY1_REG	Timer2 duty cycle for PWM1
0xFF497E	TIMER2_DUTY2_REG	Timer2 duty cycle for PWM 2
0xFF4980	TIMER2_FREQ_REG	Timer2 frequency prescaler

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF4990	TONE_CTRL1_REG	Capture timer control register 1
0xFF4992	TONE_COUNTER1_REG	Capture timer Counter 1
0xFF4994	TONE_LATCH1_REG	Capture timer Latch 1
0xFF4996	TONE_CLEAR_INT1_REG	Clears CT1 interrupt and TONE_LATCH1_REG
0xFF4998	TONE_CTRL2_REG	Capture timer control register 2
0xFF499A	TONE_COUNTER2_REG	Capture timer Counter 2
0xFF499C	TONE_LATCH2_REG	Capture timer Latch 2
0xFF499E	TONE_CLEAR_INT2_REG	Clears CT2 interrupt and TONE_LATCH2_REG
0xFF49B0	KEY_GP_INT_REG	General purpose interrupts for KEYB_INT
0xFF49B2	KEY_BOARD_INT_REG	Keyboard interrupt enable register
0xFF49B4	KEY_DEBOUNCE_REG	Keyboard debounce and auto key generation timer
0xFF49B6	KEY_STATUS_REG	Keyboard interrupt status.
0xFF49B8		Reserved
0xFF4BF		
0xFF49C0		Reserved
0xFF4BFF		
0xFF4C00	WATCHDOG_REG	Watchdog preset value.
0xFF4C02		Reserved
0xFF4FFF		
0xFF5000	SET_FREEZE_REG	Freeze watchdog, timer1 and DIP during debugging
0xFF5002	RESET_FREEZE_REG	Release watchdog, timer1 and DIP during debugging after setting in freeze mode
0xFF5004	DEBUG_REG	DEBUG_REG for boot program control and debug control
0xFF5006	MEM_CONFIG_REG	Memory configuration register
0xFF5010		Reserved
0xFF5012		Reserved
0xFF5014		Reserved
0xFF5016		Reserved
0xFF5018		Reserved
0xFF501A		Reserved
0xFF5020	TRACE_CTRL_REG	Trace control register
0xFF5022	TRACE_STATUS_REG	Trace status register
0xFF5024	TRACE_START0_REG	Trace start register 0
0xFF5026	TRACE_LEN0_REG	Trace length register 0
0xFF5028	TRACE_START1_REG	Trace start register 1
0xFF502A	TRACE_LEN1_REG	Trace length register 1
0xFF502C	TRACE_TIMERL_REG	Trace timer bits 15-0
0xFF502E	TRACE_TIMERH_REG	Trace timer bits 31-16

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF5030		Reserved
0xFF503F		
0xFF5040		Reserved
0xFF53FF		
0xFF5400	SET_INT_PENDING_REG	Set interrupt pending register
0xFF5402	RESET_INT_PENDING_REG	Reset interrupt pending register
0xFF5404	INT0_PRIORITY_REG	Interrupt priority register 0
0xFF5406	INT1_PRIORITY_REG	Interrupt priority register 1
0xFF5408	INT2_PRIORITY_REG	Interrupt priority register 2
0xFF540A	INT3_PRIORITY_REG	Interrupt priority register 2
0xFF540C	PC_START_REG	CR16Cplus startup address
0xFF540E		Reserved
0xFF57FF		
0xFF5800	CODEC_MIC_REG	Codec microphone control register
0xFF5802	CODEC_LSR_REG	Codec loudspeaker control register
0xFF5804	CODEC_VREF_REG	Codec vref control register
0xFF5806	CODEC_TONE_REG	Codec CID control register
0xFF5808	CODEC_ADDA_REG	Codec ad/da control register
0xFF580A	CODEC_OFFSET1_REG	Codec offset error and compensation register
0xFF580C	CODEC_TEST_CTRL_REG	Codec test control register codec
0xFF580E	CODEC_OFFSET2_REG	Codec offset compensation register
0xFF5810		Reserved
0xFF5BFF		
0xFF5C00	CLASSD_CTRL_REG	Class D control register
0xFF5C02	CLASSD_CLEAR_INT_REG	Class D Clear interrupt register
0xFF5C04	CLASSD_BUZZER_REG	Class D buzzer register
0xFF5C06	CLASSD_TEST_REG	Class D test register
0xFF5C08	CLASSD_NR_REG	Class D noise reduction register
0xFF5C0A		Reserved
0xFF5FFF		
0xFF6000	DIP_STACK_REG	DIP Stack pointer. (read only). The DIP stack is 4 deep
0xFF6002	DIP_PC_REG	DIP program counter
0xFF6004	DIP_STATUS_REG	DIP Status register,
0xFF6006	DIP_CTRL_REG	DIP Control register1
0xFF6008	DIP_STATUS1_REG	DIP Status register1,
0xFF600A	DIP_CTRL1_REG	DIP Control register, clears DIP_INT if read
0xFF600C	DIP_SLOT_NUMBER_REG	DIP slot number register, returns the current slot number
0xFF600E	DIP_CTRL2_REG	DIP Control register 2 (debug status information)
0xFF6010		Reserved
0xFF6012	DIP_MOD_SEL_REG	DIP Modulo counters selection

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF6014	DIP_MOD_VAL_REG	DIP Modulo values selection
0xFF6016		Reserved
0xFF63FF		
0xFF6400	BMC_CTRL_REG	BMC control register
0xFF6402	BMC_CTRL2_REG	BMC control register 2
0xFF6404	BMC_TX_SFIELDL_REG	BMC Tx S field register Low
0xFF6406	BMC_TX_SFIELDH_REG	BMC Tx S field register High
0xFF6408	BMC_RX_SFIELDL_REG	BMC Rx S field register Low
0xFF640A	BMC_RX_SFIELDH_REG	BMC Rx S field register High
0xFF640C		Reserved
0xFF67FF		
0xFF6800		Reserved
0xFF6FFF		
0xFF7000	RF_BURST_MODE_CTRL_REG	BMCW
0xFF7002		Reserved
0xFF7004		Reserved
0xFF7006		Reserved
0xFF7008	RF_ALW_EN_REG	always-enable bits for block activation
0xFF700A	RF_PORT_RSSI_SI_REG	SO_PORT/EO_RSSI switch instant settings
0xFF700C	RF_TX_SI_REG	TX switch instant settings
0xFF700E	RF_RX_SI_REG	RX switch instant settings
0xFF7010	RF_PORT1_DCF_REG	Port 1 dynamic control function settings
0xFF7012	RF_PORT2_DCF_REG	Port 2 dynamic control function settings
0xFF7014	RF_PORT3_DCF_REG	Port 3 dynamic control function settings
0xFF7016	RF_PORT4_DCF_REG	Port 4 dynamic control function settings
0xFF7018	RF_PLLCLOSED_DCF_REG	PLL closed loop dynamic control function
0xFF701A	RF_SYNTH_DCF_REG	voltage-controlled oscillator dynamic control function
0xFF701C	RF_BIAS_DCF_REG	bias circuit dynamic control function
0xFF701E	RF_RSSIPH_DCF_REG	RSSI peak-hold computation dynamic control function
0xFF7020	RF_DEM_DCF_REG	demodulator dynamic control function
0xFF7022	RF_ADC_DCF_REG	analog-to-digital converter dynamic control function
0xFF7024	RF_IF_DCF_REG	intermediate-frequency filter dynamic control function
0xFF7026	RF_LNAMIX_DCF_REG	low-noise amplifier and mixer dynamic control function
0xFF7028	RF_PADR_DCF_REG	PA driver dynamic control function
0xFF702A	RF_FAD_WINDOW_DCF_REG	FAD timing control function
0xFF7040	RF_RFCAL_CTRL_REG	RF calibration control settings
0xFF7042		reserved
0xFF7044	RF_DEM_CTRL_REG	demodulator control settings

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF7046	RF_PREAMBLE_REG	preamble-processing control settings
0xFF7048	RF_RSSI_REG	received-signal strength indication value, FAD choice and RF calibration result
0xFF704A	RF_PORT_CTRL_REG	port control settings
0xFF704C	RF_PAD_IO_REG	disable digital input/output on RFPORTs
0xFF704E	RF_TRIM_CTRL_REG	production trimming of PADR output power
0xFF7050	RF_PLL_CTRL1_REG	PLL control settings for frequency calculation
0xFF7052	RF_PLL_CTRL2_REG	PLL control settings for frequency calculation
0xFF7054	RF_PLL_CTRL3_REG	PLL control settings for frequency calculation
0xFF7056	RF_PLL_CTRL4_REG	PLL control settings for frequency calculation
0xFF7058	RF_SLICER_REG	RX active slicer settings
0xFF705A	RF_SLICER_RESULT_REG	Results computed by RX active slicer
0xFF705C	RF_GAUSS_GAIN_RESULT_REG	Result of modulation-gain calibration
0xFF7070	RF_BURST_MODE_SHADOW1_REG	BMCW shadow register
0xFF7072	RF_BURST_MODE_SHADOW2_REG	BMCW shadow register
0xFF7074	RF_DCF_MONITOR_REG	To monitor DCF strobes to GPIO pins
0xFF7080	RF_SYNTH_CTRL1_REG	These registers shall not be modified unless instructed by SiTel Semiconductor. Recommended settings are given in Table 68
0xFF7082	RF_SYNTH_CTRL2_REG	
0xFF7084	RF_AGC_REG	
0xFF7086	RF_AGC12_TH_REG	
0xFF7088	RF_AGC12_ALPHA_REG	
0xFF708C	RF_DC_OFFSET_REG	
0xFF708E	RF_DC_OFFSET34_REG	
0xFF7090	RF_IQ_DC_OFFSET_REG	
0xFF7092	RF_IF_CTRL_REG	
0xFF7094	RF_REF_OSC_REG	
0xFF7096	RF_ADC_CTRL_REG	
0xFF7098	RF_RFIO_CTRL_REG	
0xFF709A	RF_BIAS_CTRL_REG	
0xFF709C	RF_DRIFT_TEST_REG	
0xFF709E	RF_TEST_MODE_REG	
0xFF70A0	RF_LDO_TEST_REG	
0xFF70AC	RF_PLL_CTRL5_REG	
0xFF70AE	RF_PLL_CTRL6_REG	
0xFF70B0	RF_INTERNALPA_REG	
0xFF70B2	RF_PA_RESERVED1_REG	Reserved for compatibility with future devices
0xFF70B4	RF_PA_RESERVED2_REG	
0xFF70B6	RF_IFCAL_RESULT_REG	These registers shall not be modified unless instructed by SiTel Semiconductor. Recommended settings are given in Table 68
0xFF70B8	RF_DC_OFFSET12_REG	
0xFF70BA	RF_AGC_RESULT_REG	
0xFF70BC	RF_GAUSS_GAIN_MSB_REG	
0xFF70C0		Reserved for the radio transceiver

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0xFF7400	FLASH_CTRL_REG	Flash control register
0xFF7402	FLASH_PTNVH1_REG	Flash NVSTR hold time (mass erase)
0xFF7404	FLASH_PTPROG_REG	Flash program time
0xFF7406	FLASH_PTERASE_REG	Flash erase time (page)
0xFF7408	FLASH_PTME_REG	Flash erase time (mass)
0xFF740A		Reserved for FLASH control
0xFF77FF		
0xFF7800		Free
0xFFF7FF		
0xFFF800		Reserved for Chip id registers
0xFFFBF7		
0xFFFBF8	CHIP_ID1_REG	Chip identification register 1
0xFFFBF9	CHIP_ID2_REG	Chip identification register 2
0xFFFBFA	CHIP_ID3_REG	Chip identification register 3
0xFFFBFB	CHIP_MEM_SIZE_REG	Chip memory size register
0xFFFBFC	CHIP_REVISION_REG	Chip revision register (Correspond to Chip Marking)
0xFFFBFD	CHIP_TEST1_REG	Chip test register
0xFFFBFE	CHIP_TEST2_REG	Chip test register
0xFFFBFF		Reserved
0xFFFC00	INT_ACK_CR16_START	CR16Cplus interrupt acknowledge
0xFFFFFF	INT_ACK_CR16_END	
DIP RAM		
0x1000000	DIP_RAM_START	DIP Sequencer RAM (256 words)
0x10001FF	DIP_RAM_END	
0x1000200	DIP_RAM_2_START	Sequencer RAM (256 words) to be addressed with new <JMPF>,<BR_B1> DiP commands
0x10003FF	DIP_RAM_2_END	
0x1000400	-	Reserved 3k
0x1000FFF	-	
0x1002000	-	Free 120k
0x101FFFF	-	
Gen2DSP data ROM		
0x1020000	-	Shared Data ROM 21k (a5M only)
0x10253FF	-	
Gen2DSP registers		
0x1027F80	DSP_MAIN_SYNC0_REG	DSP main counter outputs selection register 0
0x1027F82	DSP_MAIN_SYNC1_REG	DSP main counter outputs selection register 1
0x1027F84	DSP_MAIN_CNT_REG	DSP main counter reload register
0x1027F86	DSP_ADC1S_REG	ADC1 Input 2's Complement register
0x1027F88	DSP_ADC0S_REG	ADC0 Input 2's Complement register
0x1027F8A	DSP_CLASSD_REG	CLASSD Output output data register

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0x1027F8C	DSP_CODEC_MIC_GAIN_REG	CODEC MIC GAIN register
0x1027F8E	DSP_CODEC_OUT_REG	CODEC DATA register
0x1027F90	DSP_CODEC_IN_REG	CODEC DATA register
0x1027F92	DSP_RAM_OUT0_REG	Shared RAM output register 0
0x1027F94	DSP_RAM_OUT1_REG	Shared RAM output register 1
0x1027F96	DSP_RAM_OUT2_REG	Shared RAM output register 2
0x1027F98	DSP_RAM_OUT3_REG	Shared RAM output register 3
0x1027F9A	DSP_RAM_IN0_REG	Shared RAM input register 0
0x1027F9C	DSP_RAM_IN1_REG	Shared RAM input register 1
0x1027F9E	DSP_RAM_IN2_REG	Shared RAM input register 2
0x1027FA0	DSP_RAM_IN3_REG	Shared RAM input register 3
0x1027FA2	DSP_ZCROSS1_OUT_REG	ZERO CROSSING 1 output register
0x1027FA4	DSP_ZCROSS2_OUT_REG	ZERO CROSSING 2 output register
0x1027FA6	DSP_PCM_OUT0_REG	PCM channel 0 output register
0x1027FA8	DSP_PCM_OUT1_REG	PCM channel 1 output register
0x1027FAA	DSP_PCM_OUT2_REG	PCM channel 2 output register
0x1027FAC	DSP_PCM_OUT3_REG	PCM channel 3 output register
0x1027FAE	DSP_PCM_IN0_REG	PCM channel 0 input register
0x1027FB0	DSP_PCM_IN1_REG	PCM channel 1 input register
0x1027FB2	DSP_PCM_IN2_REG	PCM channel 2 input register
0x1027FB4	DSP_PCM_IN3_REG	PCM channel 3 input register
0x1027FB6	DSP_PCM_CTRL_REG	PCM Control register
0x1027FB8	DSP_PHASE_INFO_REG	Phase information between PCM FSC 8/16/32 and main counter 8/16/32 kHz
0x1027FBA		Reserved
0x1027FBC	DSP_MAIN_CTRL_REG	DSP Main counter control and preset value
0x1027FBE	DSP_CLASSD_BUZZOFF_REG	CLASSD Buzzer on/off controller, bit 15
0x1027FC0		Reserved
0x1027FCE		
0x1027FD0	DSP_CTRL_REG	DSP control register
0x1027FD2	DSP_PC_REG	DSP Programma counter
0x1027FD4	DSP_PC_START_REG	DSP Programma counter start
0x1027FD6	DSP_IRQ_START_REG	DSP Interrupt vector start
0x1027FD8	DSP_INT_REG	DSP to CR16Cplus interrupt vector
0x1027FDA	DSP_INT_MASK_REG	DSP to CR16Cplus interrupt vector maks
0x1027FDC	DSP_INT_PRIO1_REG	DSP Interrupt source mux 1 register
0x1027FDE	DSP_INT_PRIO2_REG	DSP Interrupt source mux2 register
0x1027FE0	DSP_OVERFLOW_REG	DSP to CR16Cplus overflow register
0x1027FE2		Reserved
0x1027FEE		
0x1027FF0	DBG_IREG	DSP JTAG instruction register
0x1027FF2	Reserved	
0x1027FF4	DBG_INOUT_REG_LSW	DSP DEBUG data register (32 bits)
0x1027FF6	DBG_INOUT_REG_MSW	

Table 66: Register map

Note 41: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0x1027FF8	-	Reserved
0x102FFFF	-	
0x1030000	DSP_MC_RAM_START	Gen2DSP MicroCode RAM 2 kbyte (A5M FLASH only)
0x10307FF	DSP_MC_RAM_END	
0x1030800	-	Reserved
0x1037FFF	-	
0x010000	DSP_MC_SHARED_RAM_START	Gen2DSP MicroCode RAM mapped in Shared RAM (16 kbytes)
0x013FFF	DSP_MC_SHARED_RAM_END	
0x014000	-	Reserved 16 kbyte
0x017FFF	-	
0x1040000	DSP_MC_ROM_START	Gen2DSP MicroCode ROM 44 kbyte (A5M) 22kbyte (A2M6), 16byte (A2L)
0x104AFFF	DSP_MC_ROM_END	
0x104B000		Reserved
0x104FFFF		
0x1050000	-	Free
0x1FFFFF	-	

33.5 RECOMMENDED SETTINGS FOR RF APPLICATION REGISTERS

All RF application registers (address 0xFF7000 - 0xFF7074) can have arbitrary values, but the recommendations from Table 67 may serve as a starting point, compatible with an application of SiTel Semiconductor's LMX4180 and SC1443x.

These settings are used as a standard burst definition for the radio performance measurements as specified in sections 35.4, 35.5 and 35.6 starting on page 243.

They represent the setup for receiving or transmitting a P32 packet with a 16 bit preamble in the DECT application in blind slot operation. This means that the slot consists of 424 symbols in the physical packet (S-field 32 bits, D-field 388 bits and Z-field 4 bits) and the guard space is 56 symbols long.

The falling edge of LE when writing the BMCW is synchronized at 200 symbols before bit p0 of the physical packet. Note that the synchronization of the MICROWIRE™ interface takes only 3/9 to 4/9 symbol periods (= tLE_start).

Registers 0xFF7000 and 0xFF7008 change on a slot to slot basis, based on what type of function the SC14480A5M, SC14480A2M6 is supposed to perform (refer to Tables 233 and 235), so no recommendations are given.

Registers 0xFF7048, 0xFF705A and 0xFF705C are read only (R), so no recommendations are given. With varying slot length the registers 0xFF700A through 0xFF700E are the only ones that need to change.

Registers 0xFF7070 and 0x7072 are used with the alternative programming mode as described in section 9.6, so no recommendations are given.

Table 67: Recommended and reset values of application registers

Address	Port	Recommended value	Reset value
0xFF7000	RF_BURST_MODE_CTRL_REG	-	0x0000
0xFF7008	RF_ALW_EN_REG	-	0x0000
0xFF700A	RF_PORT_RSSI_SI_REG	0x1C07 (ES1 -ES3) 0x1C00 (ES4 and up)	0x3A08
0xFF700C	RF_TX_SI_REG	0x4E12	0x6C30
0xFF700E	RF_RX_SI_REG	0x4E13	0x6C31
0xFF7010	RF_PORT1_DCF_REG	0x6340 (ES1 -ES3) No Change(ES4 and up)	0x2346
0xFF7012	RF_PORT2_DCF_REG	No Change	0x145E

Table 67: Recommended and reset values of application registers

Address	Port	Recommended value	Reset value
0xFF7014	RF_PORT3_DCF_REG	0x9720	0x9714
0xFF7016	RF_PORT4_DCF_REG	No Change	0x102D
0xFF7018	RF_PLLCLOSED_DCF_REG	0x4720	0x4A14
0xFF701A	RF_SYNTH_DCF_REG	No Change	0x0754
0xFF701C	RF_BIAS_DCF_REG	No Change	0x0780
0xFF701E	RF_RSSIPH_DCF_REG	No Change	0x006A
0xFF7020	RF_DEM_DCF_REG	No Change	0x42CF
0xFF7022	RF_ADC_DCF_REG	0x04F2 (ES1 -ES3) 0x44C0 (ES4 and up)	0x44C0
0xFF7024	RF_IF_DCF_REG	0x0474 (ES1 -ES3) 0x4442 (ES4 and up)	0x4440
0xFF7026	RF_LNAMIX_DCF_REG	0x03F6 (ES1 -ES3) 0x43C4 (ES4 and up)	0x43C0
0xFF7028	RF_PADR_DCF_REG	0x8732 (ES1 -ES3) 0x0719 (ES4 and up)	0x872C
0xFF702A	RF_FAD_WINDOW_DCF_REG	No Change	0x0A23
0xFF7040	RF_RFCAL_CTRL_REG	No Change	0x0033
0xFF7044	RF_DEM_CTRL_REG	0x0A03	0x0A02
0xFF7046	RF_PREAMBLE_REG	No Change	0x052A
0xFF7048	RF_RSSI_REG	R	0x0030
0xFF704A	RF_PORT_CTRL_REG	No Change	0x0000
0xFF704C	RF_PAD_IO_REG	No Change	0x003F
0xFF704E	RF_TRIM_CTRL_REG	No Change	0x0020
0xFF7050	RF_PLL_CTRL1_REG	R	0x6894
0xFF7052	RF_PLL_CTRL2_REG	**(Note 42)** 0x2030 (ES1) 0x2036 (ES2 and up)	0x2090
0xFF7054	RF_PLL_CTRL3_REG	(ES4-ES5 and up) 0x0800	0x1800
0xFF7056	RF_PLL_CTRL4_REG	No Change	0xDAC0
0xFF7058	RF_SLICER_REG	0x00E0	0x00E1
0xFF705A	RF_SLICER_RESULT_REG	R	0x0000
0xFF705C	RF_GAUSS_GAIN_RESULT_REG	R	0x0000
0xFF7070	RF_BURST_MODE_SHADOW1_REG	-	0x0000
0xFF7072	RF_BURST_MODE_SHADOW2_REG	-	0x0000
0xFF7074	RF_DCF_MONITOR_REG	No Change	0x0000

Note 42: A recommended value for GAUSS_GAIN is given as starting point for RF evaluation. In the application this value should be (automatically) calibrated as described in SiTel Semiconductor Application Note AN-D-136.

33.6 RF TEST REGISTER VALUES

Test registers are used during production. They set several blocks in alternative operational modes. These modes are subject to change until this datasheet reaches V1.0

The recommended values are used for characterization and production tests and are the only settings that guarantee the performance specification as given in sections 35.4, 35.5 and 35.6 starting on page 243.

Registers of which the Recommended Value is indicated by R are read only registers and need never be written.

Table 68: RF Test register values ES1

Address	Port	Recommended Values	Reset Value
0xFF7080	RF_SYNTH_CTRL1_REG	0x048C (ES1-ES3) 0x028E (ES4 and up)	0x2404
0xFF7082	RF_SYNTH_CTRL2_REG	0x6781	0x8201
0xFF7084	RF_AGC_REG	0x0238	0x0148
0xFF7086	RF_AGC12_TH_REG	No Change	0x399A
0xFF7088	RF_AGC12_ALPHA_REG	No Change	0x0038
0xFF708C	RF_DC_OFFSET_REG	No Change	0x0000
0xFF708E	RF_DC_OFFSET34_REG	R	0x0000
0xFF7090	RF_IQ_DC_OFFSET_REG	No Change	0x4000
0xFF7092	RF_IF_CTRL_REG	No Change	0x059C
0xFF7094	RF_REF_OSC_REG	(ES4-ES5 and up) 0x2396	0x2256
0xFF7096	RF_ADC_CTRL_REG	0x000F	0x0007
0xFF7098	RF_RFIO_CTRL_REG	0x0810	0x1010
0xFF709A	RF_BIAS_CTRL_REG	0x0002(ES1) 0x0007(ES2 and up)	0x001E
0xFF709C	RF_DRIFT_TEST_REG	R	0x0000
0xFF709E	RF_TEST_MODE_REG	No Change	0x0001
0xFF70A0	RF_LDO_TEST_REG	No Change	0x0000
0xFF70AC	RF_PLL_CTRL5_REG	No Change	0x0000
0xFF70AE	RF_PLL_CTRL6_REG	0x0800	0x2800
0xFF70B0	RF_INTERNALPA_REG	No Change	0x0000
0xFF70B2	RF_PA_RESERVED1_REG	No Change	0x0000
0xFF70B4	RF_PA_RESERVED2_REG	No Change	0x0000
0xFF70B6	RF_IFCAL_RESULT_REG	R	0x0020
0xFF70B8	RF_DC_OFFSET12_REG	R	0x0000
0xFF70BA	RF_AGC_RESULT_REG	R	0x0110
0xFF70BC	RF_GAUSS_GAIN_MSB_REG	R	0x0000

34.0 Registers description

Table 69: ACCESS1_IN_OUT_REG, ACCESS2_IN_OUT_REG (0xFF4920, 0xFF4930)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-0	R/W	ACCESS_DATA	Read: ACCESS bus x input register Write: ACCESS bus x output register	0

Table 70: ACCESS1_CTRL_REG, ACCESS2_CTRL_REG (0xFF4922, 0xFF4932)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-11	-			0
10-9	R/W	SCK_SEL	00 = 100 kHz mode selected 01 = 400 kHz mode selected. 1x = 1.152 MHz mode selected.	0
8	R/W	SCK_NUM	0 = 8 bits without ACK bits are generated, SDAx push pull 1 = 8 bits with ACK bit are generated. SDAx open drain, Pull up required.	0
7	R/W	SDA_OD	0 = SDAx push pull 1 = SDAx open drain, Pull up required **(Note 43)**	1
6	R/W	SCL_OD	0 = SCLx push pull 1 = SCLx open drain, Pull up required, allows clock stretching **(Note 43)**	0
5	R/W	EN_ACCESS_INT	0 = Disable ACCESS x bus interrupt 1 = Enable ACCESS x bus interrupt	0
4	R	ACCESSx_INT	1 = ACCESS Bus x generated the interrupt. Must be reset by SW by writing to ACCESSx_CLEAR_INT_REG.	0
3	R/W	SDA_VAL	Output value of SDAx pin if EN_ACCESS_BUS= 0	1
2	R/W	SCL_VAL	Output value of SCLx pin if EN_ACCESS_BUS = 0	1
1	R/W	ACKn	In transmit mode: (Read only) 0 = ACK received 1 = No ACK received In receive mode: (Write only) 0 = transmit ACK on access bus 1 = transmit No ACK.	0
0	R/W	EN_ACCESS_BUS	0 = Disable ACCESS Bus x, power down mode 1 = Enable ACCESS Bus x	0

Note 43: See SC14480_buglist item 51. Open drain mode using these bits will reach the 'HIGH' pull-up output voltage in two steps. First step is 1.8V + 0.6V for the duration of about 10 to 20 usec. In the second step, the output stage is fully open drain and the output voltage reaches the pull-up voltage.
The problem does not occur if bits SDA_OD and SCL_OD are 0 and corresponding PAD_CTRL_REG[xx_OD] bits are set to 1.
In devices were this problem is solved, (see SC14480_buglist.xls),the alternative method by setting PAD_CTRL_REG[xx_OD] bits only, can also be used here.

Table 71: ACCESS1_CLEAR_INT_REG, ACCESS2_CLEAR_INT_REG (0xFF4924, 0xFF4934)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	ACCESS_CLEAR_INT	Writing any value to this register will clear the ACCESS bus x interrupt. Reading returns 0	0

Table 72: ADC_CTRL_REG (0xFF4960)

BIT	MODE	SYMBOL	DESCRIPTION	Reset
15	R/W	ADC2_PR_DIS	0 = ADC2 pad protection enabled 1 = ADC2 pad protection disabled.	0
14	R/W	ADC1_PR_DIS	0 = ADC1 pad protection enabled 1 = ADC1 pad protection disabled.	0
13	R/W	ADC0_PR_DIS	0 = ADC0 pad protection enabled 1 = ADC0 pad protection disabled.	0
12	R/W	ADC_MINT	0 = Disable (mask) ADC_INT. 1 = Enable ADC_INT to ICU	0
11	R	ADC_INT	1 = AD conversion ready and has generated an interrupt. Must be cleared by writing any value to ADC_CLEAR_INT_REG Will not be set in automatic mode.	0
10-7	R/W	ADC_TEST	Test bits Must be set to 0	0
6-3	R/W	ADC_IN_3_0	Primary ADC input selection (Manual and automatic mode) 0000 = ADC0 input 0001 = ADC1 input 0010 = ADC2 input 0011 = Caller ID output as input 0100 = Codec headset detection. 0101 = Ringing opamp 0110 = VBAT 0111 = Temperature sensor 1000 = Parallel set detection opamp otherwise = Reserved	0
2	R/W	ADC_ALT	0 = In automatic ADC mode ADC samples are always stored in ADC0_REG. 1 = In automatic ADC mode ADC samples are stored alternat-ingly in ADC0_REG and ADC1_REG.	0
1	R/W	ADC_AUTO	0 = Manual ADC mode, by setting ADC_CTRL_REG[ADC_START]. ADC result is stored in ADC0_REG 1 = Automatic ADC mode triggered by DSP_MAIN_SYNC1_REG[ADC_SYNC]. ADC_START read value must be 0 before auto mode is enabled. ADC_START write is ignored in auto mode ADC results is stored in ADC0_REG (ADC_ALT=0) or alternating ADC0_REG and ADC1_REG. **(Note 44)**	0
0	R/W	ADC_START	0: ADC conversion ready. **(Note 44)** 1: If a 1 is written, the ADC starts conversion. After conversion this bit will be set to 0 and the ADC_INT bit will be set.	0

Note 44: In both modes, the BAT_CTRL2_REG[CHARGE_LEVEL] bits are reset after each conversion depending on TWO_CELL value. This is used for non rechargable battery detection.

Table 73: ADC_CTRL1_REG (0xFF4962)

Bit	Mode	Symbol	Description	Reset
15-4	-	-		0
3-0	R/W	ADC_IN_3_0_1	Secondary ADC input selection in automatic ADC conversion Bit definitions are the same as ADC_IN_3_0	0

Table 74: ADC_CLEAR_INT_REG (0xFF4964)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	ADC_CLEAR_INT	Writing any value to this register will clear the ADC_INT interrupt. Reading returns 0.	0

Table 75: ADC0_REG (0xFF4966)

Bit	Mode	Symbol	Description	Reset
15-10	-			0
9-0	R/W	ADC0_VAL	Read: Returns the 10 bits linear value of the last ADC conversion. **(Note 45)**. In automatic ADC mode returns the first automatic ADC conversion Write: ADC_DAC value in test mode. Output of ADC_DAC can be read on ADC0 if selected.	0

Note 45: ADC input values may never be more than AVD, otherwise other ADC measurements will become inaccurate due to internal leakage.

Table 76: ADC1_REG (0xFF4968)

Bit	Mode	Symbol	Description	Reset
15-10	-			0
9-0	R	ADC1_VAL	Read: Returns the 10 bits linear value of the second automatic ADC conversion	0

Table 77: BANDGAP_REG (0xFF4810)

Bit	Mode	Symbol	Description	Reset (Note 46)
15-9	-			0
8-6	R/W	BANDGAP_I	Internal reference current adjust. Setting these bits will not affect the bandgap voltage. 100 = +40 % 101 = +30 % 110 = +20% 111 = +10% 000 = +0 % **<- default value may not be changed.** 001 = -10% 010 = -20% 011 = -30%	000
5-4	R/W	BANDGAP_VIT	00 = **<- default value may not be changed** 10 = Voltage and current -5.6 % <- for test purposes only ! 01 = Voltage and current +5.6 % <- for test purposes only.!	00
3-0	R/W	BANDGAP_VI	Bandgap reference voltage and current adjust to trim AVD. These bits must be set **before the current bits 8-6** because it affects the reference currents. 0000 = -5.6 % 0001 = -4.9 % 0010 = -4.2 % 0011 = -3.5 % 0100 = -2.8 % 0101 = -2.1 % 0110 = -1.4 % 0111 = -0.7 % 1000 = midlevel <- default value. 1001 = +0.7 % 1010 = +1.4 % 1011 = +2.1 % 1100 = +2.8 % 1101 = +3.5 % 1110 = +4.2 % 1111 = +4.9 % <- Reset Value	0xF

Note 46: The register is only reset with RSTn = 0, not on a SW_REST

Table 78: BAT_CTRL_REG (0xFF4812)

BIT	MODE	SYMBOL	DESCRIPTION	RESET (Note 47)
15-4	-		Reserved	0
3-2	R/W	LDORF_LEVEL	00 = 1.8V (This setting is for test purposes only) 01 = 2.0V 10 = 2.5V 11 = 3.0V	01
1	R/W	LDORF_ON	0 = off 1 = Optional RF supply LDO on in case of VBAT >3.45 for (e.g. Li-Ion battery). Controls LDORF_CTRL pin. **For power saving this bit must be switched off after start-up if external transistor is not used.**	1
0	R/W	REG_ON	0 = Off 1 = On chip BB LDOs on after power-on procedure (See Figure 13 and Figure 14) Not reset by SW reset	0

Note 47: The register is only reset with HW Reset, not on a SW_RESET

Table 79: BAT_CTRL2_REG (0xFF4814)

Bit	Mode	Symbol	Description	Reset
15	-	-	-	0
14	R/W	SOC_TEST2	0 = Normal operation. 1 = Test mode	0
13	R/W	SOC_TEST1	0 = Normal operation. 1 = Test mode	0
12	R/W	SOC_CAL	0 = Normal operation of the state-of-charge counter 1 = Internal 0.1V reference is used as input for the state -of charge counter for calibration purpose.	0
11	R/W	SOC_ON	0 = State Of Charge counter is disabled 1 = State Of Charge counter is enabled.	0
10-8	R/W	CHARGE_CUR	Charge current limit value: 000 = no current limit, Hysteresis mode enabled 001 = 65 mA 010 = 125 mA 011 = 190 mA 100 = 385 mA 101 = 450 mA 110 = 510 mA 111 = 575 mA	001
7	-	-	-	0
6	R/W	NTC_DISABLE	0 = Charger NTC protection enabled, 200 ms after power-up Charger will be disabled if NTC voltage is outside the window defined in Table 279 on page 223. 1 = Charger NTC protection disable. This bit must be set within 200 ms after start-up else Charger NTC protection will be enabled.	0
5	R/W	CHARGE_ON	0 = Charger in powerdown 1 = Charger enabled	1
4-0	R/W	CHARGE_LEVEL	Stop-charge levels // 2 Cell Ni-MH Levels 00000 = 3.0V (reset) 00010 = 3.4V 00011 = 3.74V (changes to 00010 after ADC conversion) // 3 Cell Ni-MH / Li-Ion Levels 00110= 4.9V 00111 = 5.43V (changed to 00110 after ADC conversion) 10000 = 3.86V 10010 = 3.9V 10100 = 3.95V 10110 = 4.0V 11000 = 4.05V 11010 = 4.1V 11100 = 4.15V 11110 = 4.2V 01010 = 4.25V 01100 = 4.3V 01110 = 5.02V	00000

Table 80: BAT_STATUS_REG (0xFF4816)

BIT	MODE	SYMBOL	DESCRIPTION	RESET (Note 48)
15-4	-			0
3	R	CHARGE_I_LIMIT	Returns current regulation loop status of the (Li-Ion) charger. 0 = Charger in Constant Voltage mode (or hysteresis mode) 1 = Charger in Constant Current mode	0
2	R/W	CHARGE_STS	Returns CHARGE pin status. Set if > 1.5V . Reset by software	0
1	R/W	PON_STS	Returns PON pin status. Set if > 1.5V . Reset by software	0
0	R/W	VBAT3_STS	New battery detection. Set at rising edge of VBAT. Reset by software.	0

Note 48: The reset values indicate whether CHARGE, PON or new battery started the chip
The actual value of PON and CHARGE can be read from P1_IN_OUT_DATA_REG.

Table 81: BAT_SOC_HIGH_REG (0xFF4818)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	SOC_HIGH	Most/least significant word of the state-of-charge counter Write: Preset counter (Most Significant Word). Read: Actual value of the counter. (Most Significant Word) **(Note 49)**	0

Table 82: BAT_SOC_LOW_REG (0xFF481A)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	SOC_LOW	Most/least significant word of the state-of-charge counter Write: Preset counter (Least Significant Word). Read: Actual value of the counter. (Least Significant Word) **(Note 49)**	0

Note 49: If either SOC_HIGH or SOC_LOW is written both register values are loaded into the SOC counter. So for a correct preset of the SOC counter, both values must be written. Reading the SOC counter must always be done twice, because the SOC_LOW can go from 0xFFFF to 0 while SOC_HIGH increments between reading the SOC_LOW and SOC_HIGH registers. This gives an incorrect value of the total SOC counter value. In order to avoid this problem the whole counter must be read again until the difference between two values is less then 10, indicating that no carry or borrow between LOW to HIGH had taken place

Table 83: BMC_CTRL_REG (0xFF6400)

Bit	Mode	Symbol	Description	Reset
15-14	-			0
13	R/W	BCNT_INH	0 = Normal operation B_BR2, B_BT2, B_BRFD and B_BTFM instructions 1 = Disable automatic bitcounter in B_BR2, B_BT2, B_BRFD and B_BTFM instructions. (X-CRC not transmitted)	0
12-9	-			0
8	R/W	SIO_PD	0 = SIO pull-down resistor is automatically enabled if SIO is input and automatically disabled if SIO output. 1 = SIO pull-down resistor disabled (also for test purposes)	0
7	-			0
6	-			0
5	-			0
4	-			0
3-0	-		Reserved	0

Table 84: BMC_CTRL2_REG (0xFF6402)

Bit	Mode	Symbol	Description	Reset
15-9	-		Reserved	0
8	R/W	RCK_SEL	0 = Use DPLL Recovered clock from BMC 1 = Use Recovered clock from RF receiver	0
7-3	R/W	RCV_CTL	For best clock recovery performance RCV_CTL bits shall be set to "11110" and B_RC[DPLL] shall be set to "000"	0
2-0	-		Reserved	0

Note 50: -

Table 85: BMC_TX_SFIELDL_REG (0xFF6404)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TX_SFIELDL	Transmitted S field register. If the <B_ST2> operand is unequal to 0 one or more bytes are transmitted from this register. For more information see AN-D-140	0xE98A

Table 86: BMC_TX_SFIELDH_REG (0xFF6406)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TX_SFIELDH	Bits 31-16 of BMC_TX_SFIELD_REG.	0xAAAA

Table 87: BMC_RX_SFIELDL_REG (0xFF6408)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	RX_SFIELDL	Received S field pattern bits 15-0.	0x9755

Table 88: BMC_RX_SFIELDH_REG (0xFF640A)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-0	R/W	RX_SFIELDH	Bits 23-16 of BMC_RX_SFIELD_REG If <B_SR> operand bit 6 is 1, register RX_SFIELD_REG[23-22] are overruled by <B_SR> operand[1-0].	0x51

Table 89: CHIP_ID1_REG (0xFFFBF8)

Bit	Mode	Symbol	Description	Reset
7-0	R	CHIP_ID1	First character of device type in ASCII. CHIP_ID1_REG, CHIP_ID2_REG, CHIP_ID3_REG form the three character device type “480”	0x34

Table 90: CHIP_ID2_REG (0xFFFBF9)

Bit	Mode	Symbol	Description	Reset
7-0	R	CHIP_ID2	Second character of device type in ASCII. CHIP_ID1_REG, CHIP_ID2_REG, CHIP_ID3_REG form the three character device type “480”	0x38

Table 91: CHIP_ID3_REG (0xFFFBFA)

Bit	Mode	Symbol	Description	Reset
7-0	R	CHIP_ID3	Third character of device type in ASCII. CHIP_ID1_REG, CHIP_ID2_REG, CHIP_ID3_REG form the three character device type “480”	0x30

Table 92: CHIP_MEM_SIZE_REG (0xFFFBFB)

Bit	Mode	Symbol	Description	Reset
7-0	R	MEM_SIZE_ID	Program FLASH/ROM size. 0x50 = 5 Mbit FLASH/No ROM 0x00 = No FLASH/19.5kbyte ROM 0x02 = No FLASH/2 or 2.6 Mbit ROM 0x03 = No FLASH/3.5 Mbit ROM 0x05 = No FLASH/5 Mbit ROM	0x50

Table 93: CHIP_REVISION_REG (0xFFFBFC)

Bit	Mode	Symbol	Description	Reset
7-0	R	REVISION_ID	Chip version, corresponds with type number 0x10 = ‘AxM’, 0x20 = ‘BxM’, etc 0x1C = “AxL”, 0x2C = “BxL”, etc	0x10

Table 94: CHIP_TEST1_REG (0xFFFBFD)

Bit	Mode	Symbol	Description	Reset
7-0	R	CHIP_TEST1	Die identification needed for FLASH to ROM migration (AN-D-153) to identify Gen2DSP FLASH version 0x11: ES6 FLASH 0x12: ES7 FLASH 0x13: ES8 FLASH	0

Table 95: CHIP_TEST2_REG (0xFFFBFE)

Bit	Mode	Symbol	Description	Reset
7-0	R	CHIP_TEST2	Reserved for test purposes	2

Table 96: CLASSD_BUZZER_REG (0xFF5C04)

Bit	Mode	Symbol	Description	Reset
15-5	-		not used	0
4	R/W	CLASSD_BUZ_MODE	0 = CLASSD normal audio path enable 1 = CLASSD Buzzer path enable. To enable the buzzer amplifier DSP_CLASSD_BUZZOFF_REG (0x1027FBE) bit 15 BUZZOFF must be set to '0'. To switch off the buzzer without audible side effects, bit 15 must be set to '1' at the end of a tone.	0
3-0	R/W	CLASSD_BUZ_GAIN	Amplitude control of the buzzer signal, relative to 1W into 4 Ohm: 1111 = +0dB 1110 = -2dB 1101 = -4dB 1100 = -6dB 1011 = -8dB 1010 = -10dB 1001 = -12dB 1000 = -18dB 0111 = -24dB 0110 = -30dB 0101 = -36dB 0100 = -42dB 0011 = -48dB 0010 = -54dB 0001 = -60dB 0000 = mute	0000

Table 97: CLASSD_CTRL_REG (0xFF5C00)

Bit	Mode	Symbol	Description	Reset
15	R/W	CLASSD_POPEN	0 = PAOUTp closed if CLASSD switched off (old situation) 1 = PAOUTp opens 1ms after CLASSD_PD is set to 1 if CLASSD mode selected (P3_1_MODE =01) This prevents noise pick-up if CLASSD is off. PAOUTp has an internal load of ~5k if CLASSD_VOUT =1, else ~6k.	0
14	R/W	CLASSD_MOPEN	0 = PAOUTn closed if CLASSD switched off (old situation) 1 = PAOUTn opens 1ms after CLASSD_PD is set to 1 if CLASSD mode selected (P3_0_MODE =01) This prevents noise pick-up if CLASSD is off. PAOUTn has an internal load of ~5k if CLASSD_VOUT =1, else ~6k.	0
13	R/W	CLASSD_MINT	0 = Disable (mask) CLASSD_INT_BIT to CT_CLASSD_INT 1 = Enable CLASSD_INT_BIT to CT_CLASSD_INT.	0
12	R/W	CLASSD_MODE	0 = Normal situation	0
11-10	R/W	CLASSD_DITH_A	Dithering in analog part 00 = Adaptive dithering 01 = Maximum dithering 10 = Small dithering 11 = No dithering	11
9-8	R/W	CLASSD_DITH_D	Dithering in digital part 00 = Adaptive dithering 01 = Maximum dithering 10 = Small dithering 11 = No dithering	00

Table 97: CLASSD_CTRL_REG (0xFF5C00)

Bit	Mode	Symbol	Description	Reset
7	R	CLASSD_INT_BIT	1 = the CLASSD amplifier has clipped (CLASSD_INT_BIT Must be reset by SW by writing to CLASSD_CLEAR_INT_REG.	0
6-4	R/W	CLASSD_CLIP	000 = no clipping detection 001 = CLASSD_INT after 32 clipping occurrences 010 = CLASSD_INT after 64 clipping occurrences 011 = CLASSD_INT after 128 clipping occurrences 100 = CLASSD_INT after 256 clipping occurrences 101 = CLASSD_INT after 512 clipping occurrences 110 = CLASSD_INT after 1024 clipping occurrences 111 = CLASSD_INT after 2048 clipping occurrences	0
3-2	R/W	CLASSD_VOUT	Maximum differential output voltage selection between PAOUTp and PAOUTm. x0 = 4 Vpp x1 = 6 Vpp	0
1	R	CLASSD_PROT	0 = Temperature and current are below safety limits 1 = Temperature and/or current exceeds the safety limits (automatic protection has been activated) ~~Must be reset by SW by writing to CLASSD_CLEAR_INT_REG.~~	0
0	R/W	CLASSD_PD	1 = CLASSD amplifier in powerdown, 0 = on	1

Table 98: CLASSD_CLEAR_INT_REG (0xFF5C02)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	CLASSD_CLEAR_INT	Writing any value to this register will clear the CLASSD_CTRL_REG[CLASSD_INT_BIT]. Reading returns 0.	0

Table 99: CLASSD_TEST_REG (0xFF5C06)

Bit	Mode	Symbol	Description	Reset
15-7	-	-	not used	0
6-4	-	CLASSD_ANA_TEST	0 = normal operation. 1 = map analog testpoints to the general purpose input of ADC	0
3	R/W	CLASSD_FORCE	0 = normal operation 1 = Force PAOUTp and PAOUTm to drive 1.	0
2	R/W	CLASSD_RST_A	0 = normal operation 1 = analog delta sigma modulator in reset	0
1	R/W	CLASSD_RST_D	0 = normal operation 1 = digital delta sigma modulator in reset	0
0	R/W	CLASSD_SWITCH	0 = normal operation 1 = alternative switching strategy (should result in less THD, but more risk of "plopping")	0

Note 51: The bits in CLASSD_TEST_REG must remain 0'

Table 100: CLASSD_NR_REG (0xFF5C08)

Bit	Mode	Symbol	Description	Reset
15-12	-		not used	0
11-10	R/W	CLASSD_NR_ZERO	Enable/disable noise reduction is delayed until 00 = no delay 01 = zero-crossing of input signal 10 = input level < -78dB 11 = input level < -60dB	10
9-8	R/W	CLASSD_NR_HYST	Noise reduction is disabled when level is ..dB higher than threshold: 00 = 0dB 01 = 6dB 10 = 12dB 11 = 18dB	00
7-4	R/W	CLASSD_NR_TON	Noise reduction is enabled when level is below threshold for: (based on 10.368/2 MHz) 0000 = direct 0001 = 0.8ms (2^12 periods) 0010 = 1.6ms (2^13 periods) 0011 = 3.2ms (2^14 periods) 0100 = 6.3ms (2^15 periods) 0101 = 12.6ms (2^16 periods) 0110 = 25ms (2^17 periods) 0111 = 50ms (2^18 periods) 1000 = 100ms (2^19 periods) 1001 = 200ms (2^20 periods) 1010 = 400ms (2^21 periods) 1011 = 800ms (2^22 periods)	0101
3-1	R/W	CLASSD_NR_LVL	Threshold for noise reduction, relative to full-scale: 111 = -30dB 110 = -36dB 101 = -42dB 100 = -48dB 011 = -54dB 010 = -60dB 001 = -66dB 000 = -72dB	100
0	R/W	CLASSD_NR_ACTIVE	0 = Noise reduction is disabled 1 = Noise reduction is enabled	1

Table 101: CLK_AMBA_REG (0xFF4000)

Bit	Mode	Symbol	Description	Reset
15-13	-			0
12-10	R/W	MEM_STROBE	CR16Cplus FLASH Memory Access strobe for power reduction. **The strobe must be minimum 48 ns. (Note 52)** 000 = Strobe always on. 001 = Strobe is 1x DIV2_CLK cycle 010 = Strobe is 2x DIV2_CLK cycles 011 = Strobe is 3x DIV2_CLK cycles .. 111 = Strobe is 7x DIV2_CLK cycles The MEM_STROBE value is don't care in the ROM versions.	0
9	R/W	HCLK_PRE	HCLK prescaler P3 0 = Divide by 1 or divide by 16 if PRESCALER =1 and <U_PSC> (DIP controlled, compatible mode with 42x, 43x) 1 = Divide by 16	0
8	-			0
7	R/W	MCRAM1_EN	0 = Micro Code RAM, ROM interface off, clock disabled Upon access, 0 is returned. The RAM contents will not be destroyed if this bit is 0. 1 = Micro Code RAM, ROM interface on	0
6				0
5	R/W	SRAM1_EN	0 = Shared RAM, ROM , Gen2DSP interface off, clocks disabled Upon access 0 is returned. The RAM contents will not be destroyed if this bit is 0 1 = Shared RAM, ROM, Gen2DSP interface on	1
4-3	R/W	PCLK_DIV	APB interface clock, **Maximum allowed clock frequency 41.472 MHz.** HCLK divided by PCLK_DIV[1] PCLK_DIV[0]: Divide by: 0 0 4 0 1 1 1 0 2 1 1 Reserved **(Note 52)**	0
2-0	R/W	HCLK_DIV	AHB interface and CR16Cplus clock **Maximum allowed clock frequency 41.472** MHz. DIV2_CLK divided by HCLK_DIV[2] HCLK_DIV[1] HCLK_DIV[0]: Divide by: 0 0 0 8 0 0 1 1 .. .. 1 1 1 7 **(Note 52)**	0

Note 52: PCLK_DIV and HCLK_DIV may not be changed at the same time. To avoid a CR16 crash due to missing readstrobe, always set MEM_STROBE to "000" when switching HDIV_CLK or when turning on the P3 and set MEM_STROBE is optimal value after switching. Switching prescaler P3 to normal mode gives no problems. Switching XDIV prescaler p1 on/off gives no problems.This problem only affects the FLASH versions, ROM versions have no mem_strobe.

Table 102: CLK_AUX_REG (0xFF401A)

Bit	Mode	Symbol	Description	Reset
15-119	-		Reserved	0
8	R/W	XDIV	0 = XDIV divider is not affected by <U_PSC> command and divides the Xtal/PLL frequency by 1 1 = The Xtal/PLL frequency will be divided by 16 started upon the execution of the <U_PSC> command in the DiP program and returned to divide by 1 until a DiP interrupt <U_INTx>, <U_VINT> or <U_VNMI> is executed. Note that all clocks are divided by 16 including timers/watchdog/ 10ms timer.	0
7	R/W	OWI_SEL	JTAG One Wire Interface (OWI) clock input selection. 0 = OWI clock is XTAL / JTAG_DIV[1-0] 1 = OWI clock is (PLL/2) / JTAG_DIV[1-0] Note that the OWI clock is enabled as soon as the JTAG pin is kept low for 20 us.	0
6-5	R/W	OWI_DIV	JTAG One wire interface clock divider factor. 0 = Divide by 8 1 = Divide by 1 2 = Divide by 2 3 = Divide by 4	1
4-3	R/W	BXTAL_EN	00 = BXTAL clock disabled 1x = BXTAL clock is enabled/disabled with <RF_EN>/<RF_DIS> (eg. RFCLK for external RF transceiver) x1 = BXTAL clock is always on (eg. BXTAL for external TAM chip SC14439)	0
2-0	-			0

Note 53: When using DiP prescalar make sure HCLK_DIV = 4,5,6,7 or 8. CLK_DIV must be set before PLL is enabled.

Table 103: CLK_CODEC_DIV_REG (0xFF4002)

Bit	Mode	Symbol	Description	Reset
15-9	-			0
8-7	R/W	CODEC_CLK_SEL	CODEC divider clock input selection. See "System Clock generation" on page 16 00 = DIVN_CLK. Use for 1.152MHz/8kHz Codec (**G.726**) 10.368 MHz in XTAL mode and PLL mode 01 = DIV2_CLK. Use for 2.304MHz/16 kHz (**G.722**) and 4.608MHz/32 kHz Codec **(Note 54)** PLL clock divided by 1 or 2 in PLL mode depending on DIV2_CLK_SEL 1x = DIV1_CLK. Optional clock selection	0
6-0	R/W	CODEC_DIV	Codec clock divider factor. This register must be set to obtain the 1.152 MHz base frequency, depending on the CODEC_CLK_SEL bits. **CODEC_DIV=1 is not possible.** Examples: - CODEC_CLK_SEL = 00 -> CODEC_CLK = 10.368 MHz (In XTAL and PLL mode) - > CODEC_DIV = 10.368/1.152 = 9 - CODEC_CLK_SEL = 01 -> CODEC_CLK = 82.944 MHz (PLL = 165.888 MHz) -> CODEC_DIV = 82.944/1.152 = 72 = 0x48 With this setting 2.304 and 4.608 MHz are automatically derived.	9

Note 54: WIth DIVN_CLK and 10.368 MHz input clock and CODEC_DIV=9 only 1.152 Mhz has a constant duty cycle, because of the integer divider factor 9. Clocks 2.304 and 4.608 MHz have a quasi jittering duty cycles due the divider factors 4.5 resp.2.25 which has effect on the output spectrum may have audible effects. To get constant duty cycle for 2.304 and 4.608 MHz clocks, the PLL must be switched, CODEC_CLK_SEL = 01, and CODEC_DIV must be selected to get 1.152 MHz.

Table 104: CLK_CODEC_REG (0xFF4004)

Bit	Mode	Symbol	Description	Reset
15	-			0
14	R/W	CLK_PCM_EN	0 = PCM_CLK off 1 = PCM_CLK on	0
13	R/W	CLK_DA_LSR_EN	0 = CLK_DA_LSR off 1 = CLK_DA_LSR on	0
12	R/W	CLK_DA_CLASSD_EN	0 = CLK_DA_CLASSD off 1 = CLK_DA_CLASSD on	0
11	R/W	CLK_AD_EN	0 = CLK_AD off 1 = CLK_AD on	0
10	R/W	CLK_MAIN_EN	0 = CLK_MAIN off 1 = CLK_MAIN on	0
9-8	R/W	CLK_PCM_SEL	PCM_CLK clock frequency selection 0x = 1.152 MHz 10 = 2 x 1.152 MHz 11 = 4 x 1.152 MHz	0
7-6	R/W	CLK_DA_LSR_SEL	Codec DA to loudspeaker clock frequency selection 0x = 1.152 MHz 10 = 2 x 1.152 MHz 11 = 4 x 1.152 MHz	0
5-4	R/W	CLK_DA_CLASSD_SEL	Codec DA to CLASSD amplifier clock frequency selection 0x = 1.152 MHz 10 = 2 x 1.152 MHz 11 = 4 x 1.152 MHz	0
3-2	R/W	CLK_AD_SEL	Codec AD from microphone clock frequency selection 0x = 1.152 MHz 10 = 2 x 1.152 MHz 11 = 4 x 1.152 MHz	0
1-0	R/W	CLK_MAIN_SEL	DSP main counter clock frequency selection 0x = 1.152 MHz **<- base frequency set by CODEC_DIV. With this setting 8, 16, 32 kHz are generated** 10 = 2 x 1.152 MHz (reserved) 11 = 4 x 1.152 MHz (reserved)=	0

Note 55: A change in frequency selection with CLK_XXX_SEL may only be done if the corresponding bit CLK_XXX_EN is 0.

Table 105: CLK_DSP_REG (0xFF4006)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7	-		Reserved	0
6-4	-		Reserved	0
3	R/W	CLK_DSP_EN	0 = Gen2DSP clock divider disabled 1 = Gen2DSP clock divider enabled, DSP_EN starts Gen2DSP, <WTF> disables local clocks	0
2-0	R/W	CLK_DSP_DIV	Gen2DSP clock divider factor. Divide XTAL or PLL/2 by 1,2,..6, 7. 0 = divide by 8.	0

Table 106: CLK_FREQ_TRIM_REG (0xFF400A)

Bit	Mode	Symbol	Description	Reset
15-11	-			0
10-8	R/W	COARSE_ADJ	Xtal frequency course trimming register. Increment or decrement the binary value with 1. Value 000 gives the same value as 001, this means that at least one capacitor always stays connected. This prevents that the oscillator stops due to lack of load capacitance,	7
7-0	R/W	FINE_ADJ	Xtal frequency fine trimming register. Increment or decrement the binary value with 1. Change 1 bit at a time to prevent phase jumps	0xFF

Table 107: CLK_PER_DIV_REG (0xFF400C)

Bit	Mode	Symbol	Description	Reset
15-9	-			0
8-7	R/W	PER_CLK_SEL	PERipheral divider clock input selection. See "System Clock generation" on page 16 00 = DIVN_CLK. 10.368 MHz in XTAL mode and PLL mode (Recommended default) 01 = DIV2_CLK. Optional clock selection. See examples. 1x = Reserved	0
6-0	R/W	PER_DIV	Peripheral clock divider factor. This register must be set to obtain the **1.152 MHz** base frequency for SOC, Timers, ADC, Capture timer and hot insertion detection. **PER_DIV=1 is not possible** Example. **Default** setting: - PER_CLK_SEL= 00 -> PER_CLK=10.368 MHz in XTAL mode and PLL mode -> PER_DIV= 10.368/1.152 = 9. - PER_CLK_SEL = 01 -> PLL 165.888 MHz -> PER_CLK = 82.944 if PLL on -> PER_DIV = 82.944/1.152 = 72.	9

Table 108: CLK_PER10_DIV_REG (0xFF400E)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-5	R/W	PER20_DIV	Peripheral clock divider factor for SPI. The SPI_CLK is equal to the PER20_DIV output divided by two. For **20.736 MHz** SPI clock the output of the PER20_DIV must be 41.472 MHz PER20_DIV[2] PER20_DIV[1] PER20_DIV[0]: Divide by: 0 0 0 8 0 0 1 1 .. .. 1 1 1 7	0
4-3	R/W	PER10_CLK_SEL	PERipheral divider clock input selection. See "System Clock generation" on page 16 00 = DIVN_CLK. 10.368 MHz in XTAL mode and PLL mode (Recommended default) 01 = DIV2_CLK. Optional clock selection. See examples. 1x = Reserved	0

Table 108: CLK_PER10_DIV_REG (0xFF400E)

Bit	Mode	Symbol	Description	Reset
2-0	R/W	PER10_DIV	Peripheral clock divider factor. This register must be set to obtain the **10.368 MHz** base frequency for UART, ACCESS, CLASSD and White LED charge pump. For best performance of CLASSD, PER10_DIV value must be 1,2,4,6 or 8. PER10_DIV[2] PER10_DIV[1] PER10_DIV[0]: Divide by: 0 0 0 8 0 0 1 1 .. .. 1 1 1 7	1

Table 109: CLK_PLL_CTRL_REG (0xFF4010)

Bit	Mode	Symbol	Description	Reset
15-13	-			0
12	R/W	DIV2_CLK_SEL	DIV2_CLK output clock selection DIV2_CLK_SEL XTAL Mode PLL Mode 0 Xtal clock PLL clock /2 (**recommended**) 1 Xtal clock PLL clock This bit may only be modified in XTAL mode with CLK_PLL_CTRL_REG[PLL_CLK_SEL]=0. With DIV2_CLK_SEL =0, the maximum allowed PLL frequency is 165.888MHz. For the Gen2DSP NO wait cycles are inserted if the CR16 or DIP access the shared RAM at the same time as the Gen2DSP. With DIV2_CLK_SEL =1, the maximum allowed PLL frequency is 82.944 MHz. In this mode a wait cycle is inserted for the Gen2DSP if the CR16 or DIP access the shared RAM. This mode has equal access timing than the XTAL and. **DIV2_CLK_SEL=1 must be avoided because the clocks are higher and therefore disipates more power and gives variable Gen2DSP load.**	0
11	R/W	DYN_SW	XTAL to PLL dynamic switching modes 0 = non dynamic switching, extra clock cycles introduced. Used if PLL frequency is not equal to Nx4 Xtal frequency 1 = dynamic switching, no extra cycles. (Recommended) Used if PLL frequency is equal to Nx4 Xtal frequency. For correct switching PLL_DIP_DIV must be a multiple of 4. (4, 8, 12, 0=16) and PLL also must be same multiple of 4 of the xtal frequency.	1
10-7	R/W	PLL_DIP_DIV	DIVN_CLK (DIP) clock divider. This divider must have value Fpll/10.368. Divide by 2..15, 0 = divide by 16. Value 1 not supported. E.g. With 165.888 Mhz PLL, this divider must be set to 0 first in XTAL mode Then with PLL on and selecting PLL mode, the DIVN_CLK (DIP) switches to the same 10.368 MHz without spikes.	0
6	R/W	HF_SEL	PLL High frequency mode selection. 0 = For PLL operation = 41.472 MHz 1 = For PLL operation > 41.472 MHz. This bit must be set at the same time as VCO_ON is set. Examples: Fxtal Fvco VD/XD Fupd HF_SEL ~~10.368~~ ~~41.472~~ ~~2x4/2~~ ~~5.184 MHz~~ ~~0~~ 41.472 MHz not allowed, use 82.944 MHz and set PLL_OUT_DIV=1 10.368 82.944 2x4/1 or 4x4/2 10.368 MHz 1 10.368 165.888 4x4/1 10.368 MHz 1	0

Table 109: CLK_PLL_CTRL_REG (0xFF4010)

Bit	Mode	Symbol	Description	Reset
5	-			0
4	R/W	VCO_ON	0 = PLL VCO off, can only be set to 0 if PLL_CLK_SEL=0 1 = PLL VCO on, settling time to be timed with software (See "PLL Clock switching" on page 20)	0
3	R/W	PLL_CLK_SEL	0 = Xtal clock is main system clock, (XTAL mode) 1 = PLL clock is main system clock (PLL mode)	0
2	R/W	PLL_OUT_DIV	0 = Divide PLL output by 1 1 = Divide PLL output by 2 (internal PLL frequency is not changed)	0
1	R/W	CP_ON	0 = PLL VCO Charge pump off, can only be set to 0 if PLL_CLK_SEL=0 1 = PLL VCO Charge pump on (Normal operation)	0
0	R/W	TESTMODE_SEL	If PLL test mode enabled: 0 = VCO test mode 1 = PLL divider test mode.	0

Table 110: CLK_PLL_DIV_REG (0xFF4012)

Bit	Mode	Symbol	Description	Reset
15-5	-			0
4-2	R/W	VD1	PLL VCO divider 000 = divide by 1x4 001 = divide by 2x4 010 = divide by 3x4 111 = divide by 4x4 100 = divide by 1x9 101 = divide by 2x9 110 = divide by 3x9	0
1-0	R/W	XD1	PLL xtal divider 00 = Divide by 1 01 = Divide by 2 1x = Reserved	0

Table 111: CLK_XTAL_CTRL_REG (0xFF4018)

Bit	Mode	Symbol	Description	Reset
15-2	-		Reserved	0
1	R/W	XTAL_DIV	XTAL divider for Baseband clock 0 = divide XTAL frequency by 1 (used with 10.368 MHz Xtal) 1 = divide XTAL frequency by 2 (used with 20.736 MHz Xtal) (TEST_CTRL2_REG[BXTAL_DIV] must be used to divide the BXTAL clock)	0
0	R	OSC300KHZ	Internal free running 600 kHz oscillator divided by 2 can be monitored via this bit. By counting the “high” and “low” period, the CR16Cplus can distinguish between 10.368 or 20.736 MHz xtal connection and set XTAL_DIV accordingly.	0/1

Table 112: CODEC_ADDA_REG (0xFF5808)

Bit	Mode	Symbol	Description	Reset
15	R/W	AUTO_SYNC	0 = Auto sync to Gen2DSP enabled. Codec resynchronises automatically after the main counter resynchronisation. (e.g after DIP <A_NORM>) (recommended) 1 = Codec auto sync to Gen2DSP disabled. Codec only automatically synchronises at initial main counter start-up.	0
14-13	R/W	ADC_VREF_LSR	Headset detection selection for ADC. 00 = VREF input selected for ADC input “0011” 01 = LSRp input selected for ADC input “0011” 10 = LSRn input selected for ADC input “0011” 11 = Reserved. (see Figure 44)	0
12-10	R/W	LPF_BW	Optional LPF filter after DAC Filter characteristics at CLK_DA_LSR = 1.152 Mhz. (8kHz) All frequencies scale with CLK_DA_LSR value. 000 = 5.5 kHz -1.85 dB@4kHz 001 = 10.9 kHz -0.56 dB@4kHz 010 = 16 kHz -0.28 dB@4kHz 011 = 21 kHz -0.16 dB@4kHz 100 = 16 kHz -0.28 dB@4kHz 101 = 21 kHz -0.16 dB@4kHz 110 = 26 kHz -0.10 dB@4kHz 111 = 30.7 kHz -0.07dB@4kHz This optional noise improvement can be set if Gen2DSP processes at 8kHz and interpolates to 16 kHz while CLK_DA_LSR is set to 2.304 MHz/16 kHz.	0
9	R/W	LPF_PD	Optional LPF filter after DAC 0 = Enabled. CODEC_LSR_REG[LSRP_MODE] and [LSRN_MODE] must also be set to 01 or 11 1 = Disabled.	1
8	R/W	DA_HBW	DAC Half bandwidth selection. Filter characteristics at CLK_DA_LSR_SEL = 1.152 Mhz. (8kHz) All frequencies scale with CLK_DA_LSR value 0 = Full bandwidth: -3dB@8kHz, -0.45dB@4kHz 1 = Half Bandwidth: -3dB@4kHz, -0.45dB@2kHz This optional noise improvement can be set if Gen2DSP processes at 8kHz and interpolates to 16 kHz while CLK_DA_LSR_SEL is set to 2.304 MHz/16 kHz.	0
7	R/W	AD_DITH_OFF	0 = Codec AD dithering on (normal), 1 = off	0
6	R/W	DA_DITH_OFF	0 = Code DA dithering on (normal) 1 = off	0
5-4	R/W	AD_CADJ	AD opamps bias current adjustment. Shall not be modified.	10
3-2	R/W	DA_CADJ	DA opamps bias current adjustment. Shall not be modified.	10
1	R/W	AD_PD	1 = Codec AD powerdown, 0 = on	1
0	R/W	DA_PD	1 = Codec DA powerdown, 0 = on	1

Table 113: CODEC_LSR_REG (0xFF5802)

Bit	Mode	Symbol	Description	Reset
15-10	-			0
9	R/W	LSREN_SE	1 = Differential to single ended conversion enabled. 0 = disabled	0
8-6	R/W	LSRATT	Loudspeaker amplifier analog gain in steps of 2 dB 000 = 2dB, 111 = -12 dB (See table 299 for voltage level at 0 dBm0)	0
5	R/W	LSRN_PD	1 = LSR- amplifier powerdown, 0 = on. This on function is overruled if CODEC_TEST_CTRL_REG [CODEC_PROT]=1 and CLASSD is still enabled.	1
4-3	R/W	LSRN_MODE	00 = LSR- output has AGND reference voltage (If LSRN_PD = 1 then LSR- has high impedance) 01 = DA- via extra LP-filter to LSR- amplifier 10 = Differential mode DA- to LSR- amplifier 11 = Single ended mode to LSR- amplifier (LSREN_SE must be set to 1)	00
2	R/W	LSRP_PD	1 = LSR+ amplifier powerdown, 0 = on. This on function is overruled if CODEC_TEST_CTRL_REG [CODEC_PROT]=1 and CLASSD is still enabled.	1
1-0	R/W	LSRP_MODE	00 = LSR+ output has AGND reference voltage (If LSRP_PD = 1 then LSR+ has high impedance) 01 = DA+ via extra LP-filter to LSR+ amplifier 10 = Differential mode DA+ to LSR+ amplifier 11 = Single ended mode to LSR+ amplifier (LSREN_SE must be set to 1)	00

Table 114: CODEC_MIC_REG (0xFF5800)

Bit	Mode	Symbol	Description	Reset
15-14	-			0
13-12	R/W	MIC_CADJ	Microphone amplifier current (bandwidth) adjustment 00 = 2 x currrent 01 = 1 x current (default fs = 8 kHz mode) 10 = 2/3 x current 11 = 1/2 x current	01
11	R/W	MICH_ON	0 = MICn input enabled. 1 = MICh input enabled.	0
10	R/W	DSP_CTRL	0 = Microphone gain controlled with MIC_GAIN 1 = Microphone gain controlled with GenDSP	0
9	R/W	MIC_OFFCOM_ON	Offset compensation control (**for test purpose only**) 0 = off (normal operation) 1 = on.	0
8	R/W	MIC_OFFCOM_SG	Offset compensation values (**for test purpose only**) 0 = added to MICp. 1 = added to MICn	0
7-4	R/W	MIC_GAIN	Microphone amplifier gain in steps of 2 dB 0000 = 0 dB, 1111 = +30 dB (See table 295 for voltage level at 0 dBm0)	0000
3	R/W	MIC_MUTE	0 = normal operation, 1 = mute MIC inputs for offset voltage measurement	0
2	R/W	MIC_PD	1 = Microphone amplifier powerdown, 0 = on.	1
1-0	R/W	MIC_MODE	Microphone input configuration M[1], M[0] 00 = Normal Differential or single ended AC coupled. 01 = MICp single ended. MICn disabled; High impedance 10 = MICn single ended. MICp disabled; High impedance 11 = MICp/n disabled; High impedance. And microphone amplifier is muted. Disabled pins are internally connected to analog ground.	00

Table 115: CODEC_OFFSET1_REG (0xFF580A)

Bit	Mode	Symbol	Description	Reset
15-0	R	COR1	Offset **error** value (2's complement) measured with MIC_MUTE=1. Each MIC_GAIN setting has a different offset error value.	0000

Table 116: CODEC_OFFSET2_REG (0xFF580E)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	COR2	Offset compensation value 2 (2's complement). For an applied MIC_GAIN setting, the offset error value must be copied to this register.	0000

Table 117: CODEC_TEST_CTRL_REG (0xFF580C)

Bit	Mode	Symbol	Description	Reset
15	-			0
14	R/W	CODEC_PROT	0 = Codec and CLASSD outputs can be enabled at the same time. 1 = LSRn_PD and LSRp_PD are automatically deactivated as long as CLASSD is active. (Also with delayed deactivation with CLASSD_MOPEN, CLASSD_POPEN). CODEC_PROT bit must be set if the CLASSD output is connected to the LSRp/n outputs for the CLASSD buzzer function on the the earpiece. Setting this bit prevents damaging the LSR output amplifier as long as CLASSD is still on and LSRp_PD/LSRn_PD is unintentionally set to 0. This bit can only be reset with a hardware reset (RSTn or watchdog time out).	0
13	R	COR_STAT	0 = CODEC_OFFSET2_REG may be loaded with a new value. 1 = The CODEC_OFFSET2_REG is being copied to the internal offset compensation register, caused by a write operation to the CODEC_MIC_REG. During this synchronisation process, the new MIC_GAIN and corresponding CODEC_OFFSET2_REG value become effective at the same time.	0
12	R/W	COR_ON	0 = Digital offset compensation disabled. 1 = Digital offset compensation enabled. Must be set to 1 **before** the CODEC_OFFSET2_REG and CODEC_MIC_REG[MIC_GAIN] are initially written.	0
11-0	R/W	TCR	Test control bit must be 0 for normal operation	0

Table 118: CODEC_TONE_REG (0xFF5806)

Bit	Mode	Symbol	Description	Reset
15-7	-			
6	R/W	RNG_CMP_PD	0 = Enable RINGING comparator. 1 = Disable RINGING comparator	1
5	R/W	PARA_PR_DIS	0 = Enable protection diodes on PARADET pin. 1 = Disable protection diodes on PARADET pin.	0
4	R/W	PARA_PD	0 = PARA opamp on 1 = PARA opamp powerdown.	1
3	R/W	RNG_PR_DIS	0 = Enable protection diodes on RINGp/RINGn pins 1 = Disable protection diodes on RINGp/ RINGn pins	0
2	R/W	RNG_PD	0 = RING opamp on 1 = RING opamp powerdown.	1
1	R/W	CID_PR_DIS	0 = Enable protection diodes on CIDINn/MICp, CIDINp/VREFp pins 1 = Disable protection diodes on CIDINn/MICp, CIDINp/VREFp pins.**(Note 56)**	0
0	R/W	CID_PD	0 = CID opamp on 1 = CID opamp powerdown	1

Note 56: CID opamp protection must be disabled (CODEC_TONE_REG[CID_PR_DIS]=1) if VREFp is enabled (CODEC_VREF_REG[VREF_PD]=0). With the protection and VREFp both enabled, the device will not be damaged but the extra current will increase the power dissipation.

Table 119: CODEC_VREF_REG (0xFF5804)

Bit	Mode	Symbol	Description	Reset
15-10	-			0
9	R/W	REFINT_PD	Internal reference opamps powerdown. Must be active if Codec AD or DA is used. 1 = powerdown 0 = on.	1
8	R/W	AGND_LSR_PD	1 = internal LSR analog ground buffer powerdown, 0 = on. Must be on if LSR is used.	1
7	R/W	BIAS_PD	1 = Bias current for all CODEC amplifiers powerdown. 0 = on.	1
6	R/W	VREF_BG_PD	1 = Bandgap current mirror powerdown. 0 = on. Must be active if VREFp is used.	1
5	R/W	AMP1V5_PD	1 = internal 0.9 V to 1.5 V convertor powerdown. 0 = on. Must be on if VREFp is used.	1
4	R/W	VREF_INIT	1 = bypass high-ohmic filter resistance with 200k ohm switch to precharge filter capacitor, 0 = high-ohmic resistance on **(must be set after 100 us)**	1
3-2	R/W	VREF_FILT_CADJ	Adjust noise filter bias current to adjust noise bandwidth. For Test purposes only. Recommended setting = 01.	01
1	R/W	VREF_FILT_PD	1 = bandgap noise filter powerdown. 0 = on	1
0	R/W	VREF_PD	1 = VREFp amplifier powerdown. 0 = on. Must be on to generate internal analog grounds.	1

Note 57: The CODEC AFE biasing (CODEC_VREF_REG) must be active before powering up the rest of the CODEC AFE blocks:
The following switch on order is recommended:
CODEC_VREF_REG -> bias on, all blocks on, VREF_INIT=1 to precharge filter capacitor,
wait at least 100 us
CODEC_VREF_REG[VREF_INIT] =0
CODEC_MIC_REG -> microphone amplifier on
CODEC_ADDA_REG -> AD and DA converters on
CODEC_LSR_REG -> loudspeaker amplifiers on.

Table 120: CP_CTRL_REG (0xFF481C)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-14	R/W	CP_FORCE_MODE	Output voltage limiter (used for test purpose only) 00 = CP_VOUTx up to 3 x VBAT (tripler, Normal operation) 01 = Reserved 10 = CP_VOUTx up to 2 x VBAT (doubler) 11 = CP_VOUTx up to 1x VBAT (single)	00
13	R/W	CP_TEST_ADC2	1 = CP_VOUT2 is mapped on internal ADC (test mode)	0
12	R/W	CP_TEST_ADC1	1 = CP_VOUT1 is mapped on internal ADC (test mode)	0
11	R/W	CP_MODE	0 = Normal mode. 1 = Disable low power mode (test mode)	0
10	R/W	CP_PARALLEL	0 = Independent outputs CP_VOUT1 is determined by CP_LEVEL1 and CP_VOUT by CP_LEVEL2. 1 = Single output mode for 10% lower output resistance. CP_VOUT1 and CP_VOUT2 must be connected to each other externally. The output voltage is determined by CP_LEVEL1. CP_LEVEL2 must be set 00.	0
9-8	R/W	CP_FREQ	Charge-pump frequency **ES1-ES3** 00 = PER10_DIV output / 2 (low ripple) 01 = PER10_DIV output / 4 10 = PER10_DIV output / 8 (high current) 11 = not used **From ES4** 00 = PER10_DIV output / 4 (low ripple) 01 = PER10_DIV output / 8 10 = PER10_DIV output / 16 (high current) 11 = not used	01
7	R/W	CP_PWM2	0 = No PWM control on CP_VOUT2/LED2, continuous output 1 = PWM control on CP_VOUT2/LED2 by timer 2	0
6	R/W	CP_PWM1	0 = No PWM control on CP_VOUT1/LED1, continuous output 1 = PWM control on CP_VOUT1/LED1 by timer 2	0
5-4	R/W	CP_LEVEL2	CP_VOUT2 output voltage (disabled if CP_PARALLEL=1) 00 = 2.5V 01 = 3.0V 10 = 4.0V 11 = 4.5V	00
3-2	R/W	CP_LEVEL1	CP_VOUT1 output voltage 00 = 2.5V 01 = 3.0V 10 = 4.0V 11 = 4.5V	00
1-0	R/W	CP_EN	00 = Charge-pump in powerdown 01 = Charge-pump on (CP_VOUT1 only) 10 = Charge-pump on (CP_VOUT2 only) 11 = Charge-pump on (CP_VOUT1 and CP_VOUT2)	00

Note 58: This mode can also be used as “Digital mode” with CP_VOUTx supplied via CP_C2y with Timer T2 as PWM control

Table 121: DEBUG_REG (0xFF5004)

Bit	Mode	Symbol	Description	Reset
15-12	-			0
11	R/W	CR16_DBGM	0 = Disable JTAG-SDI hot insertion/enable ROM patches 1 = Enable JTAG-SDI hot insertion/disable ROM patches Changing this bit has only effect after a SW_RESET. The application can copy this bit from EEPROM and issue a SW_RESET	1 NOTE
10	-		Reserved	0
9	-		Reserved	0
8	-			0
7	R/W	SW_RESET	Software reset. 1 = the SC14480 puts all its on chip peripherals and registers in the reset state and CR16Cplus starts executing at address indicated by PC_START_REG. Registers that are not reset upon a Sw reset can be found in **"Registers reset overview (table 7, page 31)"**	0
6-5	-		Reserved	00
4	R/W	ENV_B01	0 = Normal booter operation. 1 = Boot rom always jumps to on-chip RAM address 0x10080. Used to return to an on-chip program after a SW_RESET without booting.	0 NOTE
3	R/W	CLK100_SRC	0 = CLK100 frequency is derived form 10 msec DIP clock. Note that if the DIP is off (URST=1) no CLK100_INT is generated. 1 = CLK100 frequency is derived from a continuous 10.66 msec clock.	0
2	R/W	CLK100_POS	0 = No CLK100_INT generated on rising edge. 1 = Generate CLK100_INT on the rising edge of CLK100	0
1	R/W	CLK100_NEG	0 = No CLK100_INT generated on falling edge. 1 = Generate CLK100_INT on the falling edge of CLK100	0
0	R	CLK100_EDGE	0 = CLK100 has generated an interrupt on falling edge. 1 = CLK100 has generated an interrupt on rising edge.	0

NOTE: Not reset with SW_RESET, only with a HW reset.

Table 122: DIP_STACK_REG (0xFF6000)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-			0
7-0	R	STACK_REG	DIP Return address	0

Table 123: DIP_PC_REG (0xFF6002)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-9	-			0
8	R	DIP_BANK	Read only DiP sequencer RAM bank bit	0
7-0	R	DIP_PC	DiP program counter Valid upon break or freeze only	0

Table 124: DIP_STATUS_REG (0xFF6004)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-			0
7	R	URST	Read only value of DIP_CTRL_REG[URST]	1
6	R	PRESCALER	Read only value of DIP_CTRL_REG[PRESCALER]	0
5	R	DIP_BRK_INT	Read only value of DIP_CTRL_REG[DIP_BRK_INT]	0
4	R	PD1_INT	Read only value of DIP_CTRL_REG[PD1_INT]	0
3-0	R	DIP_INT_VEC	Read only value of DIP_CTRL_REG[DIP_INT_VEC]	0

Table 125: DIP_CTRL_REG (0xFF6006)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-			0
7	R/W	URST	If this bit is set to 0 the DIP starts executing the DIP sequencer program. The first DIP instruction executed is located at address DIP_RAM+1. Writing a 1 to this bit stops the DIP sequencer program execution.	1
6	R/W	PRESCALER	Global enable for P1 and P3 prescalers. If set to 1 and the DIP executes the <U_PSC> P3 divides by 16 and P1 divides by 16 if also XDIV =1. Both P1 and P3 are switched off/on if this bit is set to 0/1. The execution of <U_INTx>, <U_VINT> or <U_VNMI> DIP commands switches P1 and P3 always back to divide to 1. Note: If CLK_AMBA_REG[CLK_DIV_PRE] = 1, P3 always divides by 16, regardless of PRESCALER and <U_PSC>.	0
5	R/W	DIP_BRK_INT	If the DIP <BRK> command is executed the DIP stops executing the sequencer program and sets DIP_BRK_INT to 1. Also the DIP interrupt pending bit at the CR16Cplus is set to 1. The DIP_BRK_INT bit is cleared on reading. Writing a 1 to it starts DIP program execution at the location where the BRK command was located.	0
4	R/W	PD1_INT	Generates a DIP interrupt if S-field preamble detected. PD1 (SF) can be monitored on pin P2[5] /SF. See also chapter 7.3 This bit is ORed with DIP_CTRL2_REG[PD1_INT] Reading clears this bit and the DIP interrupt. Writing this bit: 0 = Disable PD1_INT interrupt 1 = Enabled PD1_INT interrupt is	0
3-0	R	DIP_INT_VEC	If the DIP <U_INTx> (x = 0..3) or <U_VINT> command is executed this bit is set to 1 and the DIP interrupt pending is set to 1. Reading this register sets these bits to 0.	0000

Note 59: The DIP_STATUS_REG is identical to DIP_CTRL_REG. If read, the DIP_INT the interrupt is not cleared

Note 60: In case a DIP_BRK_INT has occurred, the DIP can only be reset by writing 0xA0, instead of 0x80.

Table 126: DIP_STATUS1_REG (0xFF6008)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-4	-			0
3-0	R	DIP_VNMI_VEC	Read only value of DIP_CTRL1_REG[DIP_VNMI]	0

Table 127: DIP_CTRL1_REG (0xFF600A)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-4	-			0
3-0	R	DIP_VNMI_VEC	If the DIP <U_VNMI> command is executed the operand is ORed with these bits. Reading these bits sets the bits to 0.	0

Note 61: The DIP_STATUS_REG is identical to DIP_CTRL_REG. If read, the DIP_INT the interrupt is not cleared

Table 128: DIP_CTRL2_REG (0xFF600E)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-9	-			0
8	R/W	SLOTCNT_RES	Slot counter resume enable after <WSC> and rising edge PCM_CLK 0 = Resume on “OR” of RAMOUT[3-0]_SYNC and RAMIN[3-0]_SYNC] (compatible with SC1443x, Sc1442x) 1 = Resume if main counter resumes	0
7	R/W	EN_8DIV9	0 = <WNT> slot length 480 bits. (24slots/frame default for DECT) 1 = <WNT> slot length 512 bits. (20 slot/frame) See also DIP_SLOT_NUMBER_REG	0
6	-		Reserved, must be kept 0	0
5	R	DIP_BRK	DIP Break status 0 = No DIP <BRK> executed. 1 = The DIP has stopped due to the execution of a DIP <BRK>	0
4	R	PD1_INT	Read only value of DIP_CTRL_REG[PD1_INT]	0
3	-		Reserved, must be kept 0	0
2	R	BRK_PRE_OVR	0 = No DIP <BRK> issued while prescaler P3 was active. 1 = The DIP <BRK> is issued while prescaler P3 was active. This causes that prescaler P3 is automatically set to divide by 1. If DIP_CTRL_REG[DIP_BRK_INT] is set to 1, the prescaler is again set to divide by 16.	0
1	R	PRE_ACT	Prescaler status 0 = Prescaler P3 not active 1 = Prescaler P3 is active	0
0	R/W	DBUF	0 = Automatic double buffering of B-field data disabled 1 = Automatic double buffering of B-field data enabled. Refer to <A_TX>, <A_RX> for buffer selection. Modulo values of buffer pairs are the same and determined by the modulo value of the first pointer value: ARMOD0 for Rx buffer pair 0/2, ARMOD1 for Rx buffer pair 1/3 AWMOD0 for Tx buffer pair 0/2, AWMOD1 for Tx buffer pair 1/3	0

Table 129: DIP_MOD_SEL_REG (0xFF6012)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-			0
7	R/W	AWMOD3	**ADPCM Modulo register selection** 0 = DIP_MODVAL_REG[MODULO0] value selected 32kbit/s@10ms = 320bits@10ms = 40 bytes@10ms (G726) 1 = DIP_MODVAL_REG[MODULO1] value selected 64kbit/s@10ms = 640bits@10ms = 80 bytes@10ms (G722)	0
6	R/W	AWMOD2		0
5	R/W	AWMOD1		0
4	R/W	AWMOD0		0
3	R/W	ARMOD3		0
2	R/W	ARMOD2		0
1	R/W	ARMOD1		0
0	R/W	ARMOD0		0

Table 130: DIP_MOD_VAL_REG (0xFF6014)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	R/W	MODULO1	DIP Modulo counter maximum value. (Nr of bits/slot/8)-1. Eg. 640 bits@10ms, (640/8) -1 = 79 = 0x4F Eg. 320 bits@10ms, (320/8) -1 = 39 = 0x27	0x4F
7-0	R/W	MODULO0		0x27

Table 131: DIP_SLOT_NUMBER_REG (0xFF600C)

Bit	Mode	Symbol	Description	Reset
15-5	-			0
4-0	R	SLOT_CNTER	Read only actual value of DiP slot number counter. Value 0-23 if DIP_CTRL_REG[EN8DIV9] =0 (DECT) Value 0-19 if DIP_CTRL_REG[EN8DIV9] =1 This register is reset if the <SLOTZERO> instruction is executed.	00000

Table 132: DMA0_A_STARTL_REG, DMA1_A_STARTL_REG, DMA2_A_STARTL_REG, DMA3_A_STARTL_REG (0xFF4400, 0xFF4410, 0xFF4420, 0xFF4430)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DMAx_A_STARTL	Source Start address, bits 15-0	0

Table 133: DMA0_A_STARTH_REG, DMA1_A_STARTH_REG, DMA2_A_STARTH_REG, DMA3_A_STARTH_REG (0xFF4402, 0xFF4412, 0xFF4422, 0xFF4432)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-9	-			0
8-0	R/W	DMAx_A_STARTH	Source Start address, bits 24-16	0

Table 134: DMA0_B_STARTL_REG, DMA1_B_STARTL_REG, DMA2_B_STARTL_REG, DMA3_B_STARTL_REG (0xFF4404, 0xFF4414, 0xFF4424, 0xFF4434)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DMAx_B_STARTL	Destination start address, bits 15-0	0

Table 135: DMA0_B_STARTH_REG, DMA1_B_STARTH_REG, DMA2_B_STARTH_REG, DMA3_B_STARTH_REG (0xFF4406, 0xFF4416, 0xFF4426, 0xFF4436)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-9	-			0
8-0	R/W	DMAx_B_STARTH	Destination start address, bits 24-16.	0

Table 136: DMA0_IDX_REG, DMA1_IDX_REG, DMA2_IDX_REG, DMA3_IDX_REG (0xFF440E, 0xFF441E, 0xFF442E, 0xFF443E)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	DMAx_IDX	This internal register, added to DMA_A_STARTL/H_REG and DMA_B_STARTL/H_REG, determines the source/destination address of the next DMA cycle. The register value is multiplied. according to the AINC and BINC and BW values before it is added DMA_A_STARTL/H_REG and DMA_B_STARTL/H_REG	0

Table 137: DMA0_INT_REG, DMA1_INT_REG, DMA2_INT_REG, DMA3_INT_REG (0xFF4408, 0xFF4418, 0xFF4428, 0xFF4438)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DMAx_INT	Number of transfers until an interrupt is generated. The interrupt is generated after a transfer if DMAx_INT_REG is equal to DMAx_IDX_REG and before the DMAx_IDX_REG is incremented. DINT_MODE must be set to 1 to let the DMA controller generate the interrupt	0

Note 62: If an interrupt occurs this register can be used to distinguish between the DMA or basic interrupt source.

Table 138: DMA0_LEN_REG, DMA1_LEN_REG, DMA2_LEN_REG, DMA3_LEN_REG (0xFF440A, 0xFF441A, 0xFF442A, 0xFF443A)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DMA_LEN	DMA Transfer length. DMA_LEN 0,1,2, ...gives transfers length of 1,2,3,..	0

Table 139: DMA0_CTRL_REG, DMA1_CTRL_REG, DMA2_CTRL_REG, DMA3_CTRL_REG (0xFF440C, 0xFF441C, 0xFF442C, 0xFF443C)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-10	-			0
9-8	R/W	DMA_PRIO	Set priority level of DMA channel to determine which DMA channel will be activated in case more than one DMA channel requests DMA. 00 = lowest priority 01 = 10 = 11 = highest priority. If two or more priorities have the same level, an inherent priority is valid: Channel0 SPI Rx : 3 Channel1: SPI Tx: 1) Channel2: UART Rx: 2) Channel3: UARTTx 0 ~~DMA channels may **not** have the same priority, else a deadlock occurs.~~	0

Table 139: DMA0_CTRL_REG, DMA1_CTRL_REG, DMA2_CTRL_REG, DMA3_CTRL_REG (0xFF440C, 0xFF441C, 0xFF442C, 0xFF443C)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
7	R/W	CIRCULAR	0 = Normal mode. The DMA transfer stops the transfer after length DMAx_LEN_REG. 1 = Circular mode. The DMA channel repeats the transfer after length DMA_LEN_REGx with the initial register values DMAx_A_START_REG,DMAx_B_START_REG,DMAx_LEN_REG, DMAx_INT_REG. (Only works if DREQ_MODE=1)	0
6	R/W	AINC	Enable increment of source address. 0 = do not increment 1 = increment according value of BW	0
5	R/W	BINC	Enable increment destination address 0 = do not increment 1 = increment according value of BW	0
4	R/W	DREQ_MODE	0 = DMA channel starts immediately. 1 = DMA channel can be triggered by hardware interrupt source: Channel 0: SPI1_INT (BW may be set to 00 or 01) Rx Channel 1: SPI1_INT (BW must be set to 00 or 01) Tx Channel 2: UART RI (BW must be set to 00: 8 bits) Channel 3: UART TI (BW must be set to 00: 8 bits)	4
3	R/W	DINT_MODE	0 = ICU gets interrupt from Hardware interrupt source 1 = ICU gets interrupt from DMA channel (0-3) See Figure 81	3
2-1	R/W	BW	Bus transfer width: 00 = Byte (8 bits, used for UART and SPI 8 bits) 01 = Halfword (16 bits, used for SPI 16 bits) 10 = Word (32 bits, used e.g for SW transfer) 11 = reserved	2-1
0	R/W	DMA_ON	0 = DMA channel is off, clocks are disabled 1 = Enable DMA channel. This bit will be automatically cleared after a complete transfer. In circular mode this bit stays set.	0

Table 140: DSP_ADC1S_REG (0x1027F86)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	DSP_ADC1S	Gen2DSP Shared ADC1 register (2's complement value) ADC1_REG - 0x0200 = 7x(not)D9, D8-D0	0xFE00

Table 141: DSP_ADC0S_REG (0x1027F88)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	DSP_ADC0S	Gen2DSP Shared ADC0 register (2's complement value) ADC0_REG - 0x0200 = 7x(not)D9, D8-D0	0xFE00

Table 142: DSP_CLASSD_REG (0x1027F8A)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DSP_CLASSD	CLASSD Output data	0

Table 143: DSP_CLASSD_BUZZOFF_REG (0x1027FBE)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	R/W	BUZZOFF	0 = CLASSD buzzer gain amplifier on 1 = CLASSD buzzer gain amplifier off.	1
14-0	-			0

Table 144: DSP_CODEC_MIC_GAIN_REG (0x1027F8C)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-12	R/W	DSP_MIC_GAIN	Gen2DSP controlled Microphone amplifier gain in steps of 2 dB 0000 = 0 dB, 1111 = +30 dB To enable DSP controlled gain, set CODEC_MIC_REG [DSP_CTRL] =1	0
11-0	-			0

Note 63: DSP_CODEC_GAIN_REG can only be accessed WORD wise

Table 145: DSP_CODEC_OUT_REG (0x1027F8E)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DSP_CODEC_OUT	Codec output data	0

Table 146: DSP_CODEC_IN_REG (0x1027F90)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	DSP_CODEC_IN	Codec input data	0

Table 147: DSP_CTRL_REG (0x1027FD0)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-7	-			0
8	R/W	DBG_EN	0 = Disable Gen2DSP Debug module 1 = Enable Gen2DSP Debug module (done by SDI)	0
7-5	-			0
4	R/W	DSP_CR16_INT	CR16Cplus interrupt request/start-up request to Gen2DSP 0 = Idle 1 = Generate interrupt to the Gen2DSP. As soon as the Gen2DSP enters this interrupt routine, this bit is automatically cleared.	0
3	R/W	DSP_CLK_EN	Gen2DSP clock enabled 0 = Gen2DSP clock disabled if <WTF> executed (power saving) 1 = Gen2DSP Clock always on. (DSP_CLK_SEL Consumes more power, but giving a static supply load on VDD which might reduce TDD noise.	0
2	R/W	DSP_EN	0 = Gen2DSP in power down 1 = Gen2DSP out of reset.	0
1-0	-			

Table 148: DSP_INT_REG (0x1027FD8)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	VECTOR	The <int_vector> parameter of the Gen2DSP's <IRQ> instruction is "ored" with VECTOR bits. If one or more bits are set to 1 a DSP_INT to CR16Cplus is set. M_VECTOR bits only disables interrupts to ICU; they are always visible in the VECTOR bits if set. Register bits are cleared if a '1' is written to the corresponding bits. Writing a '1' to a bit that is already '1', clears the bit. Writing a '1' to a bit that changes from '0' to '1' does not clear the register bit.	0

Table 149: DSP_INT_MASK_REG (0x1027FDA)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	M_VECTOR	Mask DSP_INT_REG[VECTOR] bits 0 = Disable interrupt, 1 = Enable interrupt.	0

Table 150: DSP_INT_PRIO1_REG (0x1027FDC)

Bit	Mode	Symbol	Description	Reset
15-11	-		DSP Interrupt priority mux 1. 0 = DSP_SYNC0 1 = DSP_SYNC1 2 = DSP_SYNC2 3 = Reserved 4 = DIP trigger 5 = CR16Cplus trigger 6 = Reserved 7 = Output disabled Example: DSP_INT0_PRIO = 5: Give CR16Cplus the highest priority DSP_INT4_PRIO = 0: Give DSP_SYNC0 the lowest priority	0
10-8	R/W	DSP_INT0_PRIO		7
7	-			0
6-4	R/W	DSP_INT1_PRIO		7
3	-			0
2-0	R/W	DSP_INT2_PRIO		7

Table 151: DSP_INT_PRIO2_REG (0x1027FDE)

Bit	Mode	Symbol	Description	Reset
15-11	-		DSP Interrupt priority mux 2 0 = DSP_SYNC0 1 = DSP_SYNC1 2 = DSP_SYNC2 3 = Reserved 4 = DIP trigger 5 = CR16Cplus trigger 6 = Reserved 7 = Output disabled	0
10-8	R/W	DSP_INT3_PRIO		7
7	-			0
6-4	R/W	DSP_INT4_PRIO		7
3	-			0
2-0	R/W	CLK_DSP_DIVN	Optional DSP clock divider can be used for ramping up the DSP clock to maximum speed. This reduces VDD switching noise and RF performance. DSP_CLK = CLK_DSP_REG[CLK_DSP_REG(2,1,0] **OR** DSP_INT_PRIO2_REG[CLK_DSP_DIVN(2n,1n,0n] **(This means that if CLK_DSP_REG[CLK_DSP_REG(2,1,0]) must be 000 for the table below to be valid)** 000 = divide by 7 001 = divide by 6 010 = divide by 5 011 = divide by 4 100 = divide by 3 101 = divide by 2 110 = divide by 1 111 = divide by 8 -> CLK_DSP_REG[CLK_DSP_REG] table is valid. **Only available in ES4 and up.**	7

Table 152: DSP_IRQ_START_REG (0x1027FD6)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-4	R/W	DSP_IRQ_START	Bits 15-4 of DSP Interrupt Start address. Bits 3-0 are ORed with interrupt source: - Interrupt 0: jumps to DSP_IRQ_START - Interrupt 1: jumps to DSP_IRQ_START + 2 - Interrupt 2: jumps to DSP_IRQ_START + 4 - Interrupt 3: jumps to DSP_IRQ_START + 6 - Interrupt 4: jumps to DSP_IRQ_START + 8 - Interrupt 5: jumps to DSP_IRQ_START + 10	0
3-0	-			0

Table 153: DSP_MAIN_SYNC0_REG (0x1027F80)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	RAMOUT3_SYNC	**RAMIO and ADPCM Write/Read Tick Frequency.** RAMOUTx -> A_LDW -> B_TX -> TDOD RDI -> B_RX -> A_LDR-> RAMINx 00 = 4 kHz (E.g. G.726@8 kHz) 01 = 8 kHz (E.g. G.722@16kHz, G.726@16kHz) 10 = 16kHz 11 = RAMIO interface in Power-down	11
13-12	R/W	RAMOUT2_SYNC		11
11-10	R/W	RAMOUT1_SYNC		11
9-8	R/W	RAMOUT0_SYNC		11
7-6	R/W	RAMIN3_SYNC		11
5-4	R/W	RAMIN2_SYNC		11
3-2	R/W	RAMIN1_SYNC		11
1-0	R/W	RAMIN0_SYNC		11

Note 64: See SC14480_buglist item 58. Enabling/disabling RAMIO registers in DSP_MAIN_SYNC0_REG may cause RAMIO lock-up. To prevent this change DSP_MAIN_SYNC0_REG only during the following DSP_MAIN_CNT_REG counter states:
For 4kHz,8kHz ADPCM ticks(G.726, G722): between 0x18 ..0x78
For 16kHz ADPCM ticks: between 0x18 ..0x30 or 0x60.. 0x78

Table 154: DSP_MAIN_SYNC1_REG (0x1027F82)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	PCM_SYNC	PCM FSC output frequency. In PCM slave mode, this register must be set equal to the PCM_FSC input frequency. The phase difference between the internal and external PCM_FSC is calculated in the DSP_PHASE_INFO_REG. 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = PCM IO interface in Power-down	11
13-12	R/W	ADC_SYNC	ADC start frequency in automatic mode (May also be used the start a DMA transfer) 00 = 8 kHz 01 = 16kHz < - default for two conversions in 8 kHz frame 10 = 32kHz <- not allowed, test purpose only 11 = ADC IO interface in Power-down	11
11-10	R/W	DA_LSR_SYNC	Codec DA sample clock to loudspeaker 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = Codec DA lsr interface in Power-down	11
9-8	R/W	DA_CLASSD_SYNC	Codec DA sample clock to CLASSD amplifier 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = Codec DA CLASSD interface in Power-down	11

Table 154: DSP_MAIN_SYNC1_REG (0x1027F82)

Bit	Mode	Symbol	Description	Reset
7-6	R/W	AD_SYNC	Codec AD sample clock from microphone 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = Codec AD interface in Power-down	11
5-4	R/W	DSP_SYNC2	DSP start/interrupt 2 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = 8 kHz inverted	0
3-2	R/W	DSP_SYNC1	DSP start/interrupt 1 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = 8 kHz inverted	0
1-0	R/W	DSP_SYNC0	DSP start/interrupt 0 00 = 8 kHz 01 = 16kHz 10 = 32kHz 11 = 8 kHz inverted	0

Note 65: Above frequencies are generated if DSP_MAIN_CNT_REG[DSP_MAIN_REL] = 0x8F and clocked with 1.152 MHz. The main counter then outputs 8kHz, 16kHz and 32kHz automatically

Table 155: DSP_MAIN_CTRL_REG (0x1027FBC)

Bit	Mode	Symbol	Description	Reset
15-10	-			
9-8	R/W	DSP_MAIN_CTRL	Main counter on/off control. 00 = Main counter in reset. 01 = Main counter out of reset, free running. For DIP synchronisation later, toggle bits 01 -> 00 -> 10 and wait for new <A_NORM> instruction (Non DIP synchronised start-up for tone generation) 10 = Main counter starts on <A_NORM> instruction at value DSP_MAIN_PRESET. For a new DIP synchronisation toggle bits. 00 -> 10 and wait for new <A_NORM> **(Note 66)** (DIP synchronised start-up for voice connection) 11 = reserved	10
7-0	R/W	DSP_MAIN_PRESET	Main counter reset and preset value. Determines time between <A_NORM> instruction and first ADPCM tick. Value 0: Main counter counts: 0..DSP_MAIN_REL, 0..DSP_MAIN_REL (e.g 0..143, etc.) Values <> 0: Main counter counts: DSP_MAIN_PRESET..255, 0..DSP_MAIN_REL, 0..DSP_MAIN_REL, etc. During the time between DSP_MAIN_PRESET...255 no 8, 16 or 32 kHz syncs are generated. **Values for compatibility:** **15 for SC14430. 1 for SC14434 (See AN-D-140)**	175

Note 66: For proper synchronisation to the RAMINx_REG and RAMOUTx_REG, it is required that the Gen2DSP BUF_PACK/BUF_UNPACK buffers are also reset by software. For more information See AN-D-140 “chapter Synchronisation”

Table 156: DSP_MAIN_CNT_REG (0x1027F84)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	DSP_MAIN_REL	Main counter reload value. For all sample rates, the main counter must always be clocked with CLK_CODEC_REG[CLK_MAIN_SEL] = 1.152 MHz. With this frequency 4, 8, 16 and 32 kHz sync signals are always generated. DSP_MAIN_SYNC0_REG and DSP_MAIN_SYNC1_REG are used to select the appropriate sync signal. The reload values is calculated as follows: DSP_MAIN_REL = (Main counter clock/8000)-1 = (1.152 MHz /8000)-1 = 144-1 = **0x8F**	0x8F
7-0	R	DSP_MAIN_CNT	Read only value of DSP main counter	0

Table 157: DSP_OVERFLOW_REG (0x1027FE0)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	R/W	M_IRQ_OVERFLOW	Mask IRQ_OVERFLOW 0 = Disable 1 = Generate DSP_INT to CR16Cplus if IRQ_OVERFLOW bit is set	0
14	R/W	M_WTF_OVERFLOW	Mask WTF_OVERFLOW 0 = Disable 1 = Generate DSP_INT to CR16Cplus if WTF_OVERFLOW bit is set	0
13-8	R/W	M_INT_OVERFLOW	Mask INT_OVERFLOW[x] 0 = Disable 1 = Generate DSP_INT to CR16Cplus if INT_OVERFLOW[x] bit is set	0
7	R/W	IRQ_OVERFLOW	0 = No IRQ overflow 1 = Interrupt request overflow. New DSP_TRIG[5-0] occurred before corresponding internal DSP_INT[5-0] request was cleared. The DSP_INT[5-0] are cleared automatically as soon as the ISR is started. Register bit is cleared if a '1' is written. Writing a '1' to a bit that is already '1', clears the bit. Writing a '1' to a bit that changes from '0' to '1' does not clear the register bit.	0
6	R/W	WTF_OVERFLOW	0 = No WTF overflow 1 = WTF overflow. New DSP_TRIG[5-0] occurred before <WTF> was executed. This is the 43x compatible overflow condition without interrupts. Register bit is cleared if a '1' is written. Writing a '1' to a bit that is already '1', clears the bit. Writing a '1' to a bit that changes from '0' to '1' does not clear the register bit.	0
5-0	R/W	INT_OVERFLOW	0 = No Gen2DSP interrupt overflow 1 = Interrupt routine 5-0 overflow. New DSP_TRIG[5-0] occurred before <ISR_ACK[x]> executed. Register bits are cleared if a '1' is written to the corresponding bits. Writing a '1' to a bit that is already '1', clears the bit. Writing a '1' to a bit that changes from '0' to '1' does not clear the register bit. **(Note 68)**	0

Note 67: DSP_OVERFLOW_REG can only be accessed WORD wise

Note 68: If Gen2DSP interrupts are disabled with (IM[5-0] = 0), the INT_OVERFLOW[x] will also be set when the <ISR_ACK[x]> instruction is not executed before the new DSP_TRIG[x] occurs. To disable DSP_INT generation, M_INT_OVERFLOW[x] can be set to 0.

Table 158: DSP_PC_REG (0x1027FD2)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	DSP_PC	DSP Program counter relative to the Micro Code RAM Address. Read only for debug purposes only	0

Table 159: DSP_PC_START_REG (0x1027FD4)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DSP_PC_START	DSP Start address. Value 0 points to Micro Code RAM/ROM address 0. This register is loaded into the Gen2DSP Program counter from start-up.	0

Table 160: DSP_PCM_OUT0_REG, DSP_PCM_OUT1_REG, DSP_PCM_OUT2_REG, DSP_PCM_OUT3_REG (0x1027FA6, 0x1027FA8, 0x1027FBA, 0x1027FAC)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	DSP_PCM_OUTx	PCM output channel x 16 bits	0xFFFF

Table 161: DSP_PCM_IN0_REG, DSP_PCM_IN1_REG, DSP_PCM_IN2_REG, DSP_PCM_IN3_REG (0x1027FAE, 0x1027FB0, 0x1027FB2, 0x1027FB4)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	DSP_PCM_INx	PCM input channel x 16 bits	0x0000

Table 162: DSP_PCM_CTRL_REG (0x1027FB6)

Bit	Mode	Symbol	Description	Reset
15-8	-		-	0
7	R/W	PCM_CLKINV	0 = PCM_CLK Rising edge 1 = PCM_CLK Falling edge	0
6	R/W	PCM_PPOD	0 = PCM_DOUT is push-pull 1 = PCM_DOUT is open drain, requires external pull-up **(Note 69)**	0
5	R/W	PCM_FSC0DEL	0 = PCM_FSC starts 1 data bit before MSB bit 1 = PCM_FSC starts at the same time as MSB bit **(Note 70)**	0
4-3	R/W	PCM_FSC0LEN	If MASTER = 1 00 = length of PCM_FSC equal to 1 data bit 01 = length of PCM_FSC equal to 8 data bits 10 = length of PCM_FSC equal to 16 data bits 11 = length of PCM_FSC equal to 32 data bits	00
2	R/W	DSP_PCM_SYNC	Main counter PCM synchronization ~~if PCM slave~~ 0 = Count enable always true. 1 = Count enable upon PCM_FSC rising edge. DIP_CTRL2_REG[SLOTCNT_RES] determines if the main counter resumes directly or upon a RAMIOx_SYNC.	0
1	R/W	PCM_MASTER	PCM interface master/slave mode 0 = Slave mode 1 = Master mode	0
0	R/W	PCM_EN	0 = PCM interface down 1 = PCM interface enable.	0

Note 69: Open drain mode using this bit will reach the 'HIGH' pull-up output voltage in two steps. First step is 1.8V + 0.6V for the duration of about 10 to 20 usec. In the second step, the output stage is fully open drain and the output voltage reaches the pull-up voltage.

The problem does not occur if PCM_PPOD = 0 and corresponding PAD_CTRL_REG[P234_OD] = 1.
This problem is solved from SC14480A2M6, but the alternative method setting by PAD_CTRL_REG[P234_OD] only, can also be used here.

Note 70: In slave mode, Channel 0 bit 15 is always 0. (Only fixed in A5M FLASH, See buglist)

Table 163: DSP_PHASE_INFO_REG (0x1027FB8)

Bit	Mode	Symbol	Description	Reset
15-8	-		-	0
7-0	R	PHASE_INFO	Difference between rising edge of PCM_FSC and internal main-counter PCM_SYNC (in units of 1/(Main counter clock) determined by CLK_MAIN_SEL)	0

Table 164: DSP_RAM_OUT0_REG, DSP_RAM_OUT1_REG, DSP_RAM_OUT2_REG, DSP_RAM_OUT3_REG (0x1027F92, 0x1027F94, 0x1027F96, 0x1027F98)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-		-	0
7-0	R/W	DSP_RAM_OUTx	ADPCM output data to minimum delay buffers in shared RAM. The ADPCM pointers to shared RAM 1 or 2 are handled by the DIP instructions A_LDWx See AN-D-140 “DIP commands manual.”	0

Table 165: DSP_RAM_IN0_REG, DSP_RAM_IN1_REG, DSP_RAM_IN2_REG, DSP_RAM_IN3_REG (0x1027F9A, 0x1027F9C, 0x1027F9E, 0x1027FA0)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-		-	0
7-0	R	DSP_RAM_INx	ADPCM input data from minimum delay buffers in shared RAM. The ADPCM pointers to shared RAM 1 or 2 are handled by the DIP instructions A_LDRx. See AN-D-140 “DIP commands manual.”	0

Table 166: DSP_ZCROSS1_OUT_REG, DSP_ZCROSS2_OUT_REG (0x1027FA2, 0x1027FA4)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	R/W	DSP_ZCROSSx	Gen2DSP Output register ECZ1 and ECZ2 to Capture timer inputs. Signals ECZ1 and ECZ2 can also be used and general purpose GPIO port pins for diagnostics purpose.	0
14-0	-			

Table 167: FLASH_CTRL_REG (0xFF7400)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-11	-			0
10	R/W	FLASH_RPROT	If '1' the program FLASHes can not be read. This bit can only be set!! and is reset by HW reset This bit is no longer useful for copy protection, because the JTAG can alwasy read the program ROM.	NOTE
9	R/W	FLASH_WPROT	If '1' the program FLASHes cannot be erased. This bit can only be set!! and is reset by HW reset This bit can be set to protect unintentional erasing after a SW crash.	NOTE
8	R	PROG_RMIN	Program Flash Read mode inhibit. 1 = Read mode may not be selected after a write, page erase or mass erase of the selected FLASH as long as this bit is 1. 0 = Read mode may be selected.	0
7	R/W	PROG_INFO_SEL1	Program FLASH 1(2Mbit) Information block select. **(Note 71)** 0 = Main block selected 1 = Info block selected Info block 1 starts at 0xF0000	0
6	R/W	PROG_INFO_SEL2	Program FLASH 2+3 (2Mbit + 1 Mbit)Information block select. **(Note 71)** 0 = Main block(s) selected 1 = Info block(s) selected Info block 2 starts at 0x130000	0
5	R	PROG_ERS	Program flash erase status 1 = erase cycle in progress 0 = erase cycle ready.	0
4	R	PROG_WRS	Program flash write status 1 = write cycle in progress 0 = write cycle ready.	0
3	R/W	FLASH_SEL1	Select FLASH 1(2Mbit) read/write/erase mode: 0 = Read mode selected 1 = Erase/write mode selected Must be set back to 0 to reduce power consumption.	0
2	R/W	FLASH_SEL2	Select FLASH 2+3 (2Mbit + 1 Mbit) read/write/erase mode: 0 = Read mode selected 1 = Erase/write mode selected Must be set back to '0' to reduce power consumption.	0
1-0	R/W	PROG_MODE	Program FLASH mode 00 = No write or erase to FLASH(es) possible. 01 = **Write page** 10 = **Erase page**. Address first written to selects page. 11 = **Erase** one of Flash blocks **completely** (bulk erase) Address first written to selects block. FLash 1 and 2,3 are must be erased as group. If PROG_INFO_SEL1 or PROG_INFO_SEL2 =1, the info block and main block is mass erased. If PROG_INFO_SEL1 or PROG_INFO_SEL2 = 0, only the main block is erased. To only erase the info block, a page erase of the info block must be done.	00

NOTE: This bits are not reset on a SW reset

Note 71: After changing PROG_INFO_SEL1, PROG_INFO_SEL2 it takes two APB clock cycles until the new selection has effect. Therefor it is most safe to read back FLASH_CTRL_REG[PROG_INFO_SELx] before accessing the info/main blocks.

Table 168: FLASH_PTNVH1_REG (0xFF7402)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-			0
7-0	R/W	PTNVH1	Program flash NVSTR1 hold time in mass erase cycle. T = (PTNVH1 +1) x 0.86 us = 100 us (min). (Shall not be changed by customer)	0x74

Table 169: FLASH_PTPROG_REG (0xFF7404)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-8	-			0
7-0	R/W	PTPROG	Program flash programming time. T = (PTPROG +1) x 0.86 us = 20 us (min)	0x17

Table 170: FLASH_PTERASE_REG (0xFF7406)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	PTERASE	Program flash page Erase time T= (PTERASE+1) x 0.86 us = 20 msec (min)	0x5AD7

Table 171: FLASH_PTME_REG (0xFF7408)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R/W	PTME	Program flash bulk Erase time Low T= (PTME+1) x 0.86 us = 20 msec (min)	0x5AD7

Table 172: INT0_PRIORITY_REG (0xFF5404)

Bit	Mode	Symbol PR_LEVEL[2-0]	Description	Reset
15-11	-		The bits in INTx_PRIORITY_REG define the priority level of a maskable interrupt. The maskable interrupt with the interrupt pending bit set (1) and the highest priority, is serviced. After the interrupt is serviced the pending bit is NOT reset (0) by hardware. If the priority levels are equal, the inherent priority determines the priority (see Table 50)	0
10-8	-			0
7	-			0
6-4	R/W	DSP_INT_PRIO		0
3	-			0
2-0	R/W	SPI2_INT_PRIO		0

PR_LEVEL[2]	PR_LEVEL[1]	PR_LEVEL[0]:	Priority
0	0	0	0 Disabled
0	0	1	1 Lowest
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 Highest

Table 173: INT1_PRIORITY_REG (0xFF5406)

Bit	Mode	Symbol PR_LEVEL[2-0]	Description	Reset
15	-		The bits in INTx_PRIORITY_REG define the priority level of a maskable interrupt. The maskable interrupt with the interrupt pending bit set (1) and the highest priority, is serviced. After the interrupt is serviced the pending bit is NOT reset (0) by hardware. If the priority levels are equal, the inherent priority determines the priority (see Table 50) **PR_LEVEL[2] PR_LEVEL[1] PR_LEVEL[0]: Priority** **0 0 0 0 Disabled** **0 0 1 1 Lowest** **0 1 0 2** **0 1 1 3** **1 0 0 4** **1 0 1 5** **1 1 0 6** **1 1 1 7 Highest** **The CLK100 interrupt is also disabled if the DIP clock is selected and the DIP is stopped. See DEBUG_REG[3]**	0
14-12	R/W	AD_INT_PRIO		0
11	-			0
10-8	R/W	DIP_INT_PRIO		0
7	-			0
6-4	R/W	CLK100_INT_PRIO		0
3	-			0
2-0	R/W	TIM1_INT_PRIO		0

Table 174: INT2_PRIORITY_REG (0xFF5408)

Bit	Mode	Symbol PR_LEVEL[2-0]	Description	Reset
15	-		The bits in INTx_PRIORITY_REG define the priority level of a maskable interrupt. The maskable interrupt with the interrupt pending bit set (1) and the highest priority, is serviced. After the interrupt is serviced the pending bit is NOT reset (0) by hardware. If the priority levels are equal, the inherent priority determines the priority (see Table 50) **PR_LEVEL[2] PR_LEVEL[1] PR_LEVEL[0]: Priority** **0 0 0 0 Disabled** **0 0 1 1 Lowest** **0 1 0 2** **0 1 1 3** **1 0 0 4** **1 0 1 5** **1 1 0 6** **1 1 1 7 Highest**	0
14-12	R/W	TIM0_INT_PRIO		0
11	-			0
10-8	R/W	SPI_INT_PRIO		0
7	-			0
6-4	R/W	UART_TI_INT_PRIO		0
3	-			0
2-0	R/W	UART_RI_INT_PRIO		0

Table 175: INT3_PRIORITY_REG (0xFF540A)

Bit	Mode	Symbol PR_LEVEL[2-0]	Description	Reset
15	-		The bits in INTx_PRIORITY_REG define the priority level of a maskable interrupt. The maskable interrupt with the interrupt pending bit set (1) and the highest priority, is serviced. After the interrupt is serviced the pending bit is NOT reset (0) by hardware. If the priority levels are equal, the inherent priority determines the priority (see Table 50) **PR_LEVEL[2]PR_LEVEL[1]PR_LEVEL[0]:Priority** **0 0 0 0 Disabled** **0 0 1 1 Lowest** **0 1 0 2** **0 1 1 3** **1 0 0 4** **1 0 1 5** **1 1 0 6** **1 1 1 7 Highest**	0
14-12	R/W	CT_CLASSD_INT_PRIO		0
11	-			0
10-8	R/W	RESERVED_INT_PRIO		0
7	-			0
6-4	R/W	KEYB_INT_PRIO		0
3	-			0
2-0	R/W	ACCESS_INT_PRIO		0

Note 72: Reset value is device dependant according to CHIP_MEM_SIZE_REG (0xFFFBFB) (table 92, page 155).

Table 176: KEY_GP_INT_REG (0xFF49B0)

Bit	Mode	Symbol	Description	Reset
15-10	-			0
9	-			0
8-6	R/W	INT8_CTRL	0xx = Disable INT8 interrupt to KEYB_INT 100 = Pin INT8 generates a positive level interrupt on KEYB_INT 101 = Pin INT8 generates a negative level interrupt on KEYB_INT 110 = Pin INT8 generates a positive edge interrupt on KEYB_INT 111 = Pin INT8 generates a negative edge interrupt on KEYB_INT	0
5-3	R/W	INT7_CTRL	0xx = Disable INT7 interrupt to KEYB_INT 100 = Pin INT7 generates a positive level interrupt on KEYB_INT 101 = Pin INT7 generates a negative level interrupt on KEYB_INT 110 = Pin INT7 generates a positive edge interrupt on KEYB_INT 111 = Pin INT7 generates a negative edge interrupt on KEYB_INT	0
2-0	R/W	INT6_CTRL	0xx = Disable INT6 interrupt to KEYB_INT 100 = Pin INT6 generates a positive level interrupt on KEYB_INT 101 = Pin INT6 generates a negative level interrupt on KEYB_INT 110 = Pin INT6 generates a positive edge interrupt on KEYB_INT 111 = Pin INT6 generates a negative edge interrupt on KEYB_INT	0

Table 177: KEY_BOARD_INT_REG (0xFF49B2)

Bit	Mode	Symbol	Description	Reset
15-13	-			0
12	R/W	CHARGE_EDGE	0 = CHARGE pin generates KEYB_INT on rising edge 1 = CHARGE pin generates KEYB_INT on falling edge	1
11	R/W	KEY_REL	0 = No interrupt on key release 1 = Interrupt on key release after DEBOUNCE time.	0
10	R/W	KEY_LEVEL	0 = INT0 to INT5 generate KEYB_INT if one or more pins are low. 1 = INT0 to INT5 generate KEYB_INT if one or more pins are high	0
9	R/W	PON_CTRL	0 = PON will bypass debounce filter to generate KEYB_INT 1 = PON pin via debounce filter to generate KEYB_INT	0
8	R/W	CHARGE_CTRL	0 = CHARGE will bypass debounce filter to generate KEYB_INT 1 = CHARGE pin via debounce filter to generate KEYB_INT	0
7	R/W	INT_PON_EN	ES1: 0 = Disable PON pin , only if PON_CTRL = 1, else PON interrupt is enabled 1 = Enable PON pin to KEYB_INT ES2 and up: 0 = Disable PON pin to debounce timer and KEY_INT 1 = Enable PON pin to debounce timer if PON_CTRL=0 or to KEY_INT if PON_CTRL =1.	0
6	R/W	INT_CHARGE_EN	ES1: 0 = Disable CHARGE pin only if CHARGE_CTRL = 1, else CHARGE interrupt is enabled 1 = Enable CHARGE pin to KEYB_INT ES2 and up: 0 = Disable CHARGE pin to debounce timer and KEY_INT 1 = Enable CHARGE pin to debounce timer if CHARGE_CTRL=0 or to KEY_INT if CHARGE_CTRL =1.	0
5	R/W	INT5_EN	0 = Disable INT5 interrupt 1 = Enable INT5 interrupt to KEYB_INT via debounce timer	0
4	R/W	INT4_EN	0 = Disable INT4 interrupt 1 = Enable INT4 interrupt to KEYB_INT via debounce timer	0
3	R/W	INT3_EN	0 = Disable INT3 interrupt 1 = Enable INT3 interrupt to KEYB_INT via debounce timer	0
2	R/W	INT2_EN	0 = Disable INT2 interrupt 1 = Enable INT2 interrupt to KEYB_INT via debounce timer	0
1	R/W	INT1_EN	0 = Disable INT1 interrupt 1 = Enable INT1 interrupt to KEYB_INT via debounce timer	0
0	R/W	INT0_EN	0 = Disable INT0 interrupt 1 = Enable INT0 interrupt to KEYB_INT via debounce timer	0

Table 178: KEY_DEBOUNCE_REG (0xFF49B4)

Bit	Mode	Symbol	Description	Reset
15-12	-			0
11-6	R/W	KEY_REPEAT	While key is pressed, automatically generate repeating KEYB_INT after specified time unequal to 0. Repeat time: N*1 ms. N =1..63, N=0 disables timer. (Used clock is PER_CLK output /(8*144)) Refer to Figure 51 on page 82 for the keyboard interface statemachine.	0
5-0	R/W	DEBOUNCE	Keyboard debounce time. Generate KEYB_INT after specified time. Debounce time: N*1 ms. N =1..63 N=0 disables timer, gives immediate interrupt. (Used clock is PER_CLK output /(8*144)) Refer to Figure 51 on page 82 for the keyboard interface statemachine.	0

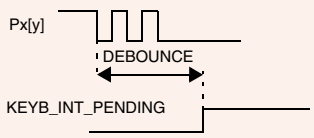

Figure 93 Keyboard Debounce Time

Table 179: KEY_STATUS_REG (0xFF49B6)

Bit	Mode	Symbol	Description	Reset
15-6	-			0
3-0	R/W	KEY_STATUS	Keyboard interrupt vector status. Register bits are cleared if a '1' is written to the corresponding bits. Writing a '1' to a bit that is '1', clears the bit. Writing a '1' to a bit that is '0' is not allowed. Writing a '0' is discarded. Bit 3= INT8 (connected to P1[3] Bit 2= INT7 (connected to P2[7] or P1[2] Bit 1= INT6 (connected to P2[6] or P1[1] Bit 0 = Debounce or key repeat timer.	0

Table 180: MEM_CONFIG_REG (0xFF5006)

Bit	Mode	Symbol	Description	Reset
15-3	-		-	0
2-0	R/W	T_RC	FLASH/ROM HCLK Wait states. Read cycle time: (1+T_RC) HCLK cycles E.g T_RC =7 -> Read cycle time = (1+7) HCLK clock cycles. **SC14480 FLASH/ROM speed is 20.736 MHz max.** **So before CR16Cplus HCLK is switched to 41.472 MHz, first T_RC must be set to 1.**	0

Table 181: PC_START_REG (0xFF540C)

Bit	Mode	Symbol	Description	Reset
15-2	R/W	PC_START	Bits 23-10 of the CR16Cplus start address in blocks of Nx1kbyte. Bits 24 and 9-0 of the CR16Cplus start address are always 0.. PC_START[15-2] = FFFF -> PC = 0xFFFC00 max start address Booter start: PC_START = FEF0 -> PC = 0xFEF000	FEF0
1-0	R	PC_START10	Always 0	0

Table 182: PAD_CTRL_REG (0xFF481E)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-12	-		Reserved	0
11	R/W	P5_OD	0 = P5[7-0] normal mode. 1 = P5[7-0] is forced to open drain if output and pull-up resistor is always disabled if input	0
10	R/W	P4_OD	0 = P4[7-0] normal mode. 1 = P4[7-0] is forced to open drain if output and pull-up resistor is always disabled if input	0
9	R/W	LED4_CUR	0 = 2.5 mA 1 = 5 mA	0
8	R/W	LED3_CUR	0 = 2.5 mA 1 = 5 mA	0
7	R/W	P20_OD	0 = P2[0] normal mode. 1 = P2[0] is forced to open drain if output and pull-up resistor is always disabled if input	1
6	R/W	P21_OD	0 = P2[1] normal mode. 1 = P2[1] is forced to open drain if output and pull-up resistor is always disabled if input	1
5	R/W	P234_OD	0 = P2[3-4] normal mode 1 = P2[3-4] is forced to open drain if output and pull-up resistor is always disabled if input	0
4	R/W	P225_OD	0 = P2[2,5] normal mode 1 = P2[2.5] is forced to open drain if output and pull-up resistor is always disabled if input	0
3	R/W	P27_OD	0 = P2[7] normal mode 1 = P2[7] is forced to open drain if output and pull-up resistor is always disabled if input	0
2	R/W	P001_OD	0 = P0[0-1] normal mode 1 = P0[0-1] is forced to open drain if output and pull-up resistor is always disabled if input	0
1	R/W	P023_OD	0 = P0[2-3] normal mode 1 = P0[2-3] is forced to open drain if output and pull-up resistor is always disabled if input	0
0	R/W	P04567_OD	0 = P0[4-7] normal mode 1 = P0[4-7] is forced to open drain if output and pull-up resistor is always disabled if input	0

Table 183: P0_DATA_REG, P1_DATA_REG, P2_DATA_REG, P3_DATA_REG, P4_DATA_REG, P5_DATA_REG (0xFF4830, 0xFF4840, 0xFF4850, 0xFF4860, 0xFF4870, 0xFF4880)

Bit	Mode	Symbol	Description	Reset P0-P3
15-8	-			0
7	R/W	Px_7_DATA	If output, set Px[7], else returns the value of Px[7]	0,0,0,0
6	R/W	Px_6_DATA	If output, set Px[6], else returns the value of Px[6]	0,0,0,0
5	R/W	Px_5_DATA	If output, set Px[5], else returns the value of Px[5]	0,1,0,0
4	R/W	Px_4_DATA	If output, set Px[4], else returns the value of Px[4]	0,0,0,0
3	R/W	Px_3_DATA	If output, set Px[3], else returns the value of Px[3]	0,0,0,0
2	R/W	Px_2_DATA	If output, set Px[2], else returns the value of Px[2]	0,0,0,0
1	R/W	Px_1_DATA	If output, set Px[1], else returns the value of Px[1]	0,0,0,0
0	R/W	Px_0_DATA	If output, set Px[0], else returns the value of Px[0]	0,0,0,0
NOTE: x = 0, 1, 2, 3. These registers are not reset with a SW reset				

Table 184: P0_SET_DATA_REG, P1_SET_DATA_REG, P2_SET_DATA_REG, P3_SET_DATA_REG ,P4_SET_DATA_REG, P5_SET_DATA_REG (0xFF4832, 0xFF4842, 0xFF4852 ,0xFF4862, 0xFF4862, 0xFF4872)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7	R/W	Px_7_SET	If Px[7] output, writing a 1 sets Px[7] to 1. Writing 0 is discarded, Reading returns 0	0
6	R/W	Px_6_SET	If Px[6] output, writing a 1 sets Px[6] to 1. Writing 0 is discarded. Reading returns 0	0
5	R/W	Px_5_SET	If Px[5] output, writing a 1 sets Px[5] to 1. Writing 0 is discarded. Reading returns 0	0
4	R/W	Px_4_SET	If Px[4] output, writing a 1 sets Px[4] to 1. Writing 0 is discarded. Reading returns 0	0
3	R/W	Px_3_SET	If Px[3] output, writing a 1 sets Px[3] to 1. Writing 0 is discarded. Reading returns 0	0
2	R/W	Px_2_SET	If Px[2] output, writing a 1 sets Px[2] to 1. Writing 0 is discarded. Reading returns 0	0
1	R/W	Px_1_SET	If Px[1] output, writing a 1 sets Px[1] to 1. Writing 0 is discarded. Reading returns 0	0
0	R/W	Px_0_SET	If Px[0] output, writing a 1 sets Px[0] to 1. Writing 0 is discarded. Reading returns 0	0
NOTE: x = 0, 1, 2, 3,4,5 These registers are not reset with a SW reset				

Table 185: P0_RESET_DATA_REG, P1_RESET_DATA_REG, P2_RESET_DATA_REG, P3_RESET_DATA_REG, P4_RESET_DATA_REG, P5_RESET_DATA_REG (0xFF4834, 0xFF4844, 0xFF4854, 0xFF4864 ,0xFF4864, 0xFF4874)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7	R/W	Px_7_RESET	If Px[7] output, writing a 1 resets Px[7] to 0. Writing 0 is discarded. Reading returns 0	0
6	R/W	Px_6_RESET	If Px[6] output, writing a 1 resets Px[6] to 0. Writing 0 is discarded. Reading returns 0	0
5	R/W	Px_5_RESET	If Px[5] output, writing a 1 resets Px[5] to 0. Writing 0 is discarded. Reading returns 0	0
4	R/W	Px_4_RESET	If Px[4] output, writing a 1 resets Px[4] to 0. Writing 0 is discarded. Reading returns 0	0
3	R/W	Px_3_RESET	If Px[3] output, writing a 1 resets Px[3] to 0. Writing 0 is discarded. Reading returns 0	0
2	R/W	Px_2_RESET	If Px[2] output, writing a 1 resets Px[2] to 0. Writing 0 is discarded. Reading returns 0	0
1	R/W	Px_1_RESET	If Px[1] output, writing a 1 resets Px[1] to 0. Writing 0 is discarded. Reading returns 0	0
0	R/W	Px_0_RESET	If Px[0] output, writing a 1 resets Px[0] to 0. Writing 0 is discarded. Reading returns 0	0
NOTE: x = 0, 1, 2, 3,4,5 These registers are not reset with a SW reset				

Table 186: P0_DIR_REG, P1_DIR_REG, P2_DIR_REG, P3_DIR_REG, P4_DIR_REG, P5_DIR_REG (0xFF4836, 0xFF4846, 0xFF4856, 0xFF4866,0xFF4866, 0xFF4876)

Bit	Mode	Symbol	Description	Reset P0-P3
15-14	R/W	Px_7_DIR	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, Pull-down selected 11 = Output, no resistors selected In analog mode, these bits mst be set to 0 to disable resistors and digital output mode.	1,-,1,0,1,1
13-12	R/W	Px_6_DIR		1,-,1,0,1,1
11-10	R/W	Px_5_DIR		1,3,1,0,1,1
9-8	R/W	Px_4_DIR		1,2,1,0,1,1
7-6	R/W	Px_3_DIR		1,2,1,0,1,1
5-4	R/W	Px_2_DIR		1,1,1,-,1,1
3-2	R/W	Px_1_DIR		1,1,1,-,1,1
1-0	R/W	Px_0_DIR		1,1,1,-,1,1
NOTE:x = 0,1,2,3,4,5 These registers are not reset with a SW reset				

Note 73: P1[5] is output from reset to supply an external EEPROM.
P1[6] and P1[]7 are pull-down only. , P3[0], P3[1] are output only
P2[0], P2[1] pull-up resistors are disabled in PAD_CTRL_REG[P20_OD, P21_OD] = 1.
If P3[3] and P1[0] are set to output, the ADC0 and ADC1 inputs are automatically disabled.

Table 187: P0_MODE_REG (0xFF4838)

Bit	Mode	Symbol	Description	Reset
15-14	-			0
13-12	R/W	P0_7_MODE	00 = P0_OUT_DATA_REG[7] on P0[7] 01 = SPI_DI on P0[7] 10 = Timer 0 PWM1 on P0[7] 11 = Reserved	0
11-10	R/W	P0_6_MODE	00 = P0_OUT_DATA_REG[6] on P0[6] 01 = SPI_DO on P0[6] 1x = Reserved	0
9-8	R/W	P0_5_MODE	00 = P0_OUT_DATA_REG[5] on P0[5] 01 = SPI_CLK on P0[5] 11 = Reserved	0
7-6	R/W	P0_4_MODE	00 = P0_OUT_DATA_REG[4] on P0[4] 01 = SPI_EN **input** on P0[4] 1x = Reserved	0
5-4	R/W	P0_3_MODE	00 = P0_OUT_DATA_REG[3] on P0[3] 01 = SCL2 on P0[3] **(Note 75)** 1x = Reserved	0
3-2	R/W	P0_2_MODE	00 = P0_OUT_DATA_REG[2] on P0[2] 01 = SDA2 on P0[2] **(Note 75)** 1x = Reserved	0
1	R/W	P0_1_MODE	0 = P0_OUT_DATA_REG[1] on P0[1] 1 = Timer 0 PWM0 on P0[1]	0
0	R/W	P0_0_MODE	0 = P0_OUT_DATA_REG[0] on P0[0] 1 = UART UTX on P0[0]	0
NOTE: This register is not reset with a SW reset				

Table 188: P1_MODE_REG (0xFF4848)

Bit	Mode	Symbol	Description	Reset
15-10	-			0
9-8	R/W	RF_BB_MODE	00 / 01 / 10 P1[5] See P1_5_MODE / RDI output / RDI input P1[4] See P1_4_MODE / TDOD output / TDOD output P1[3] See P1_3_MODE / SIO output / SIO input/output P1[2] See P1_2_MODE / SK output / SK output P1[1] See P1_1_MODE / LE output / LE output	0
7-5	R/W	P1_5_MODE	Reserved	0
4	R/W	P1_4_MODE	0 = P1_OUT_DATA_REG[4] on P1[4] (2mA drive) 1 = P1_OUT_DATA_REG[4] on P1[4] (1mA drive) for direct connection to base of external NPN transistor.	0
3	R/W	P1_3_MODE	0 = P1_OUT_DATA_REG[3] on P1[3] (2mA drive) 1 = P1_OUT_DATA_REG[3] on P1[3] (1mA drive) for direct connection to base of external NPN transistor.	0
2	R/W	P1_2_MODE	Reserved	0
1	R/W	P1_1_MODE	Reserved	0
0	R/W	P1_0_MODE	0 = P1_OUT_DATA_REG[0] on P1[0] ADC1 input disabled, input up-to VDD+0.3V 1 = Analog ADC1 mode, input upto 1.98V !! P1_DIR_REG[0] must be set to 0, to disable Pull-up, pull-down and digital output mode.	1
NOTE: This register is not reset with a SW reset				

Table 189: P2_MODE_REG (0xFF4858)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	R/W	P2_7_MODE	0 = P2_OUT_DATA_REG[7] on P2[7] 1 = BXTAL on P2[7] (Can be used as RFCLK for ext RF)	0
14	R/W	INT7_MODE	0 = P2[7] input to INT7 1 = P1[2] input to INT7	0
13	R/W	P2_6_MODE	0 = P2_OUT_DATA_REG[6] on P2[6] 1 = WTF_IN on P2[6] (monitor Gen2DSP load)	0
12	R/W	INT6_MODE	0 = P2[6] to INT6 1 = P1[1] to INT6	0
11-10	R/W	P2_5_MODE	00 = P2_OUT_DATA_REG[5] on P2[5] 01 = PCM_FSC on P2[5] 10 = SF on P2[5] 11 = Reserved	0
9-8	R/W	P2_4_MODE	00 = P2_OUT_DATA_REG[4] on P2[4] 01 = PCM_DO on on P2[4] **(Note 74)** 10 = SCL1 on P2[4] **(Note 75)** 11 = DP3 on on P2[4]	0
7-6	R/W	P2_3_MODE	00 = P2_OUT_DATA_REG[3] on P2[3] 01 = PCM_DI input on P2[3] 10 = SDA1 on P2[3] **(Note 75)** 11 = DP2 on on P2[3]	0
5-4	R/W	P2_2_MODE	00 = P2_OUT_DATA_REG[2] on P2[2]. 01 = PCM_CLK on P2[2] 10 = CLK100 on P2[2] 11 = Reserved	0
3-2	R/W	P2_1_MODE	00 = P2_OUT_DATA_REG[1] on P2[1] 01 = ECZ2 (from DSP) on P2[1] 10 = Timer 0 PWM1 on P2[1] 11 = LED4 mode on P2[1]. PAD_CTRL_REG[P21_OD] must kept '1' if LED is connected to VBAT	0
1-0	R/W	P2_0_MODE	00 = P2_OUT_DATA_REG[0] on P2[0] 01 = ECZ1 (from DSP) on P2[0] 10 = Timer0 PWM0 on P2[0] 11 = LED3 mode on P2[0]. PAD_CTRL_REG[P20_OD] must kept '1' if LED is connected to VBAT	0
NOTE: This register is not reset with a SW reset				

Note 74: Push/pull or opendrain function is controlled from the subblock's DSP_PCM_CTRL_REG, resp ACCESSx_CTRL_REG

Note 75: To enable outputs, the corresponding P2_DIR_REG[y] bit(s) do **not** have to be controlled, this is done by the sub block.

Table 190: P3_MODE_REG (0xFF4868)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	P3_7_MODE	00 = P3_OUT_DATA_REG[7] on P3[7] 01 = Analog mode RINGp on P3[7] **(Note 76)** 1x = Reserved	1
13-12	R/W	P3_6_MODE	00 = P3_OUT_DATA_REG[6] on P3[6] 01 = Analog mode RINGn on P3[6] **(Note 76)** 1x = Reserved	1
11-10	R/W	P3_5_MODE	00 = P3_OUT_DATA_REG[5] on P3[5] 01= Analog mode RINGING/RINGout on P3[5] **(Note 76)** 1x = Reserved	1
9-8	R/W	P3_4_MODE	00 = P3_OUT_DATA_REG[4] on P3[4]. 01 = Analog mode PARAdet on P3[4] 1x = Reserved	1
7-6	R/W	P3_3_MODE	00 = P3_OUT_DATA_REG[2] on P3[3] ADC0 input disabled, input upto VDD+0.3V 01 = Analog ADC0 mode, input upto 1.98V !! 1x = Reserved	1
5-4	R/W	P3_2_MODE	Reserved	0
3-2	R/W	P3_1_MODE	00 = P3_OUT_DATA_REG[1] on P3[1]. 01 = PAOUTp on P3[1] 10 = DP1 on P3[1] 11 = Reserved	1
1-0	R/W	P3_0_MODE	00 = P3_OUT_DATA_REG[0] on P3[0]. 01 = PAOUTn on P3[0] 10 = DP0 on P3[0] 11 = Reserved	1
NOTE: This register is not reset with a SW reset				

Note 76: Ringing opamp must be enabled CODEC_TONE_REG[RNG_PD] if for RINGp, RINGn, RINGout to function. For the RINGING input, the RINGING comparator must be enabled CODEC_TONE_REG[RNG_CMP_PD]

Note 77: In analog mode make sure P3_DIR_REG[7-3] is set to 0 to disable Pull-up, pull-down and digital output mode.

Table 191: P4_MODE_REG (0xFF4858)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-2	R/W	P4_MODE	Don't care. Always P4_OUT_DATA_REG[7-3,0] on P4[7-3,0] SPI2_DI always on P4[3], SPI2_EN (input) always on P4[0]	0
1	R/W	P4_1_MODE	0 = P4_OUT_DATA_REG[1] on P4[1] 1 = SPI2_CLK on P4[1]	0
0	R/W	P4_2_MODE	0 = P4_OUT_DATA_REG[2] on P4[2] 1 = SPI2_DO on P4[2]	0
NOTE: This register is not reset with a SW reset				

Table 192: P5_MODE_REG (0xFF4868)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-0	R/W	P5_MODE	Don't care. Always P5_OUT_DATA_REG[7-0] on P5[7-0]	0
NOTE: This register is not reset with a SW reset				

Table 193: RESET_FREEZE_REG (0xFF5002)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7	R/W	FRZ_DMA3	If 1 DMA channel 3 continues. 0 is discarded	0
6	R/W	FRZ_DMA2	If 1 DMA channel 2 continues. 0 is discarded	0
5	R/W	FRZ_DMA1	If 1 DMA channel 1 continues. 0 is discarded	0
4	R/W	FRZ_DMA0	If 1 DMA channel 0 continues. 0 is discarded	0
3	R/W	FRZ_WDOG	If 1 the watchdog timer continues. 0 is discarded	0
2	R/W	FRZ_TIM1	If 1 timer 1 continues. 0 is discarded	0
1	R/W	FRZ_TIM0	If 1 timer 0 continues. 0 is discarded	0
0	R/W	FRZ_DIP	If 1 the DIP continues. 0 is discarded	0

Note 78: Reading the RESET_FREEZE_REG register returns the actual freeze status

Table 194: RESET_INT_PENDING_REG (0xFF5402)

Bit	Mode	Symbol	Description	Reset
15	-			0
14	-			0
13	R/W	DSP_INT_PEND	Writing a 1 clears the pending DSP interrupt. On reading the DSP interrupt status (pending/not pending) is returned.	0
12	-			0
11	R/W	AD_INT_PEND	Writing a 1 clears the pending AD interrupt. On reading the interrupt status (pending/not pending) is returned.	0
10	R/W	DIP_INT_PEND	Writing a 1 clears the pending DIP interrupt. On reading the DIP interrupt status (pending/not pending) is returned.	0
9	R/W	CLK100_INT_PEND	Writing a 1 clears the pending Clock 100/SPI interrupt. On reading the Clock 100 interrupt status (pending/not pending) is returned. See also DEBUG_REG[3-0]	0
8	R/W	TIM1_INT_PEND	Writing a 1 clears the pending Timer1 interrupt. On reading the Timer1 interrupt status (pending/not pending) is returned.	0
7	R/W	TIM0_INT_PEND	Writing a 1 clears the pending Timer0 interrupt. On reading the Timer0 interrupt status (pending/not pending) is returned.	0
6	R/W	SPI_INT_PEND	Writing a 1 clears the pending SPI interrupt. On reading the SPI interrupt status (pending/not pending) is returned.	0
5	R/W	UART_TI_INT_PEND	Writing a 1 clears the pending UART TI interrupt. On reading the UART TI interrupt status (pending/not pending) is returned.	0
4	R/W	UART_RI_INT_PEND	Writing a 1 clears the pending UART RI interrupt. On reading the UART TI interrupt status (pending/not pending) is returned.	0
3	R/W	CT_CLASSD_INT_PEND	Writing a 1 clears the pending CT interrupt. On reading the CT interrupt status (pending/not pending) is returned. The CT interrupt is shared with the CLASSD interrupt.	0
2	R/W	RESERVED_INT_PEND	Writing a 1 clears the pending RESERVED interrupt. On reading the RESERVED interrupt status (pending/not pending) is returned.	0
1	R/W	KEYB_INT_PEND	Writing a 1 clears the pending keyboard interrupt. On reading the keyboard interrupt status (pending/not pending) is returned.	0

Table 194: RESET_INT_PENDING_REG (0xFF5402)

Bit	Mode	Symbol	Description	Reset
0	R/W	ACCESS_INT_PEND	Writing a 1 clears the pending Access bus interrupt. On reading the Access bus interrupt status (pending/not pending) is returned.	0

Note 79: Do not use CR16Cplus bit instruction on this register (read-modify-write will clear ALL pending bits

Table 195: SET_FREEZE_REG (0xFF5000)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7	R/W	FRZ_DMA3	If 1 the DMA channel 3 is frozen. 0 is discarded	0
6	R/W	FRZ_DMA2	If 1 the DMA channel 2 is frozen. 0 is discarded	0
5	R/W	FRZ_DMA1	If 1 the DMA channel 1 is frozen. 0 is discarded	0
4	R/W	FRZ_DMA0	If 1 the DMA channel 0 is frozen. 0 is discarded	0
3	R/W	FRZ_WDOG	If 1 the watchdog timer is frozen. 0 is discarded	0
2	R/W	FRZ_TIM1	If 1 timer 1 is frozen. 0 is discarded	0
1	R/W	FRZ_TIM0	If 1 timer 0 is frozen. 0 is discarded	0
0	R/W	FRZ_DIP	If 1 the DIP is frozen. 0 is discarded	0

Note 80: Reading the SET_FREEZE_REG register returns the actual freeze status

Table 196: SET_INT_PENDING_REG (0xFF5400)

Bit	Mode	Symbol	Description	Reset
15	-			0
14	-			0
13	R/W	DSP_INT_PEND	If a GenDSP interrupt is generated this bit is set to 1. Writing a 1 will also generate a DSP interrupt. A 0 insertion is discarded. On reading the DSP interrupt status (pending/not pending) is returned.	0
12	-			0
11	R/W	AD_INT_PEND	If a AD interrupt is generated this bit is set to 1. Writing a 1 will also generate a AD interrupt. A 0 insertion is discarded. On reading the AD interrupt status (pending/not pending) is returned.	0
10	R/W	DIP_INT_PEND	If a DIP interrupt is generated this bit is set to 1. Writing a 1 will also generate a DIP interrupt. A 0 insertion is discarded. On reading the DIP interrupt status (pending/not pending) is returned.	0
9	R/W	CLK100_INT_PEND	If a Clock 100 interrupt is generated this bit is set to 1. Writing a 1 will also generate a Clock 100 interrupt. A 0 insertion is discarded. On reading the Clock 100 interrupt status (pending/not pending) is returned. See also DEBUG_REG[3-0]	0
8	R/W	TIM1_INT_PEND	If a Timer1interrupt is generated this bit is set to 1. Writing a 1 will also generate a Timer1interrupt. A 0 insertion is discarded. On reading the Timer1interrupt status (pending/not pending) is returned.	0
7	R/W	TIM0_INT_PEND	If a Timer0 interrupt is generated this bit is set to 1. Writing a 1 will also generate a Timer0interrupt. A 0 insertion is discarded. On reading the Timer0interrupt status (pending/not pending) is returned.	0

Table 196: SET_INT_PENDING_REG (0xFF5400)

Bit	Mode	Symbol	Description	Reset
6	R/W	SPI_INT_PEND	Writing a 1 sets the pending SPI interrupt. On reading the SPI interrupt status (pending/not pending) is returned.	0
5	R/W	UART_TI_INT_PEND	If a UART TI interrupt is generated this bit is set to 1. Writing a 1 will also generate a UART TI interrupt. A 0 insertion is discarded. On reading the UART TI interrupt status (pending/not pending) is returned.	0
4	R/W	UART_RI_INT_PEND	If a UART RI interrupt is generated this bit is set to 1. Writing a 1 will also generate a UART RI interrupt. A 0 insertion is discarded. On reading the UART RI interrupt status (pending/not pending) is returned.	0
3	R/W	CT_CLASSD_INT_PEND	If a CT interrupt is generated this bit is set to 1. Writing a 1 will also generate a CT interrupt. A 0 insertion is discarded. On reading the CT interrupt status (pending/not pending) is returned. The CT interrupt is shared with the CLASSD interrupt.	0
2	R/W	RESERVED_INT_PEND	Writing a 1 will set the RESERVED interrupt. On reading the RESERVED interrupt status (pending/not pending) is returned.	0
1	R/W	KEYB_INT_PEND	If a keyboard interrupt is generated this bit is set to 1. Writing a 1 will also generate a keyboard interrupt. A 0 insertion is discarded. On reading the keyboard interrupt status (pending/not pending) is returned.	0
0	R/W	ACCESS_INT_PEND	Writing a 1 will generate a Access Bus interrupt. A 0 insertion is discarded. On reading the Access Bus interrupt status (pending/not pending) is returned.	0

Table 197: SPI_CTRL_REG, SPI2_CTRL_REG (0xFF4940, 0xFF4950)

Bit	Mode	Symbol	Description	Reset
15	R/W	SPI_EN_CTRL	0 = SPI_EN pin disabled. In slave mode pin SPI_CLK is not gated. 1 = SPI_EN pin enabled. In slave mode SPI_CLK is active if SPI_EN=0 and inactive if SPI_EN=1.	0
14	R/W	SPI_MINT	0 = Disable SPI_INT_BIT to ICU 1 = Enable SPI_INT_BIT to ICU.	0
13	R	SPI_INT_BIT	1 = the SPI interrupt has transmitted, receive data Must be reset by SW by writing to SPI_CLEAR_INT_REG.	0
12	R	SPI_DI	Returns the sampled value of pin SPIDI.	0
11	R	SPI_TXH	0 = Transmitter holding register SPI_TX0/1_REG is empty, copied to IO buffer 1 = Transmitter holding register SPI_TX0/1_REG not empty, not yet copied to IO buffer	0
10	R/W	SPI_FORCE_DO	0 = normal operation 1 = Force SPIDO output level to value of SPI_DO. Must be used in slave modes 1 and 3 to set SPIDO manually.	0
9	R/W	SPI_RST	0 = normal operation 1 = Reset SPI IO buffer. Can be used in slave modes 1 and 3 to set SPIDO to final (lsb) level 0.	0
8-7	R/W	SPI_WORD	00 = 8 bits mode, only SPI_RX_TX_REG0 used 01 = 16 bit mode, only SPI_RX_TX_REG0 used 10 = 32 bits mode, SPI_RX_TX_REG0 and SPI_RX_TX_REG1 used 11 = reserved	0
6	R/W	SPI_SMN	Master/slave mode 0 = Master, 1 = Slave	0
5	R/W	SPI_DO	Pin SPIDO output level when SPI is idle. Automatically set in all master modes and slave modes 0 and 2 before and after the burst. In slave mode 1 and 3 SPIDO output level is the value of the lsb of the IO buffer, but if desired the SPI_DO bit can be switched to SPIDO by setting SPI_FORCE_DO to1.	0
4-3	R/W	SPI_CLK	Select SPI_CLK clock frequency in master mode: 00 = (XTAL or PLL/2) / (PER_DIV20 *8) 01 = (XTAL or PLL/2) / (PER_DIV20 *4) 10 = (XTAL or PLL/2) / (PER_DIV20 *2) 11 = (XTAL or PLL/2) / (PER_DIV20 *14) *(Max frequency 41.472 MHz@PLL=165888 MHz)	0
2	R/W	SPI_POL	Select SPICLK polarity. See paragraph 18.0 0 = SPIx_CLK is initially low. 1 = SPIx_CLK is initially high.	0
1	R/W	SPI_PHA	Select SPICLK phase.See paragraph 18.0	0
0	R/W	SPI_ON	0 = SPI Module switched off (power saving) When this bit is cleared the SPI will remain active in master mode until the shift register and holding register are both empty. 1 = SPI Module switched on. **Should only be set after all control bits 1-8 have their desired values**.	0

Note 81: SPi block input clock is selected with CLK_PER10_DIV_REG[PER20_DIV]

Note 82: In slave mode P4[2] /SPI2_DO is not tri-state if SPI2_EN = 1, unless SPI2_DO is set to '1' and set to PAD_CTRL_REG[P4_OD] is set.

Table 198: SPI_RX_TX_REG0, SPI2_RX_TX_REG0 (0xFF4942, 0xFF4952)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	SPI_DATA0	Write: SPI_TX_REG0 output register 0 Read: SPI_RX_REG0 input register 0 In 8 bits mode bits 15 to 8 are not used	0

Table 199: SPI_RX_TX_REG1, SPI2_RX_TX_REG1 (0xFF4944, 0xFF4954)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	SPI_DATA1	Write: SPI_TX_REG1 output register 1 Read: SPI_RX_REG1 input register 1 In 8 or 16 bits mode bits this register is not used.	0

Table 200: SPI_CLEAR_INT_REG, SPI2_CLEAR_INT_REG (0xFF4946, 0xFF4956)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	SPI_CLEAR_INT	Writing any value to this register will clear the SPI_CTRL_REG[SPI_INT_BIT] Reading returns 0.	0

Table 201: TEST_ENV_REG (0xFF4800)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-5	R	ENV_REG7_5	Value of port P0[7-5] on rising edge of RSTn pin. Free environment bits for application. Internally used in test mode.	**(Note 83)**
4	R	ENV_SDI	0 = JTAG SDI+ enabled. (See chapter "JTAG-SDI"). This bit is set to '0' if the JTAG pin is set to '0' for more than 20 us if the RSTn pin = '1'. Writing a '0' is discarded. 1 = Writing a '1' to this register disables the JTAG SDI interface; JTAG pin must stay '1' else JTAG SDI+ is enabled again after 20 us. If this register is written as last command from the NTA, the JTAG pin stays high. Any new command enables the JTAG SDI again. **Writing this bit is done with Bit 2 ENV_SDI_W**	1
3	-		Reserved	
2	W	ENV_SDI_W	**ENV_SDI Write bit. Reading this bit is done at bit 4 ENV_SDI**	0
1	-		Reserved	
0	R	BOOT	Value of port P0[0] on rising edge of RSTn pin. Controls the on-chip boot program execution (See "Reset circuit" on page 30) 0 = The boot program loads a program from the UART and executes it from 0x10080. If DEBUG_REG[ENV_B01] = 1 no program is loaded but execution is started from 0x10080 immediately. 1 = The boot program jump to on-chip program at 0xF0000	**(Note 83)**

Note 83: Value on rising edge of RSTn

Table 202: TEST_CTRL2_REG (0xFF4804)

Bit	Mode	Symbol	Description	Reset
15-3	-		Reserved. Keep 0	0
2	R/W	BXTAL_DIV	XTAL divider for BXTAL pin 0 = BXTAL frequency is XTAL frequency 1 = BXTAL frequency is XTAL frequency divided by 2. (CLK_XTAL_CTRL_REG[XTAL_DIV] must be used to divide the baseband clock) **Only available in ES5 and up.**	0
1	R/w	T2_FRZ_DIS	**For FLASH ES3 and higher and ROM versions** 0 = Timer 2 / charge pump trippler clock froozen if BIAS_DCF =1 1 = Timer 2 / charge pump trippler clock continuous.	0
0	-		Reserved. Keep 0	0

Table 203: TIMER_CTRL_REG (0xFF4970)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7	R/W	TIM2_CTRL	0 = Timer2 is off and in reset state. 1 = Timer2 is running.	0
6	R/W	CLK_DIV8	0 = TImer1 uses clock as selected by bit 3 CLK_CTRL1 1 = Timer1 uses clock as selected by bit 3 CLK_CTRL1 divided by 8	0
5	R/W	TIM1_MODE	0 = Timer1 mode1 selected 1 = Timer1 mode2 selected.	0
4	R/W	WDOG_CTRL	0 = Watchdog Timer generates NMI. 1 = Watchdog Timer generates hardware Reset signal and watchdog cannot be frozen. Note that this bit can only be set to 1 by SW and only be reset with a HW reset or SW reset	0
3	R/W	CLK_CTRL1	0 = Timer1 uses 1.152 MHz clock frequency 1 = Timer1 uses 115.2 kHz clock frequency	0
2	R/W	CLK_CTRL0	0 = Timer0 uses 1.152 MHz clock frequency 1 = Timer0 uses 115.2 kHz clock frequency	0
1	R/W	TIM1_CTRL	0 = Timer1 is off and in reset state. 1 = Timer1 is running.	0
0	R/W	TIM0_CTRL	0 = Timer0 is off and in reset state. 1 = Timer0 is running.	0

Table 204: TIMER0_ON_REG (0xFF4972)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TIM0_ON	Timer0 On reload value: If read the actual counter value ON_CNTer is returned	0

Table 205: TIMER0_RELOAD_M_REG (0xFF4974)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TIM0_M	Timer0 'high' reload value If read the actual counter value T0_CNTer is returned	0

Table 206: TIMER0_RELOAD_N_REG (0xFF4976)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TIM0_N	Timer0 'low' reload value: If read the actual counter value T0_CNTer is returned	0

Table 207: TIMER1_RELOAD_M_REG (0xFF4978)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TIM1_M	Timer1 'high' reload value: If read TIM1_M value is returned	0

Table 208: TIMER1_RELOAD_N_REG (0xFF497A)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TIM1_N	Timer1 'low' reload value: If read the actual counter value T1_CNTer is returned	0

Table 209: TIMER2_DUTY1_REG (0xFF497C)

Bit	Mode	Symbol	Description	Reset
15-14	-			0
13-0	R/W	TIM2_DUTY1	Timer2 duty cycle for T2_PWM1 signal (White LED1)	0

Table 210: TIMER2_DUTY2_REG (0xFF497E)

Bit	Mode	Symbol	Description	Reset
15-14	-			0
13-0	R/W	TIM2_DUTY2	Timer2 duty cycle for T2_PWM2 signal (White LED2)	0

Table 211: TIMER2_FREQ_REG (0xFF4980)

Bit	Mode	Symbol	Description	Reset
15-14	-	-	-	0
13-0	R/W	TIM2_FREQ	Timer2 frequency divider	0

Table 212: TONE_CTRL1_REG(0xFF4990)

Bit	Mode	Symbol	Description	Reset
15-11	-			0
10	R/W	GATE_EDGE1	0 = Rising edge of GATE_CLK used to clock TONE_TIMER 1 = Rising and falling edge of GATE_CLK used	0
9	R/W	MCT1_INT	0 = Disable CT1_INT to CT_CLASSD_INT 1 = Enable CT1_INT to CT_CLASSD_INT, **(Note 84)**	0
8	R	CT1_INT	1 = Tone latch 1 interrupt. Must be cleared by writing to TONE_CLEAR_INT1_REG	0
7-4	R/W	TIMER_RELOAD1	Select clock divider reload value for clock to latch timer periodically 0 = divide by 1, 15 = divide by 16	0
3-2	R/W	CLKSRC1	00 = 144 kHz 01 = reserved 10 = ECZ1 from GenDSP 11 = ECZ2 from GenDSP	0
1-0	R/W	GATESRC1	00 = 93.8 Hz 01 = RINGING comparator 10 = ECZ1 from Gen2DSP 11 = ECZ2 from Gen2DSP	0

Note 84: CT1_INT and CT2_INT are ored to CT_CLASSD_INT

Table 213: TONE_COUNTER1_REG (0xFF4992)

Bit	Mode	Symbol	Description	Reset
15-0	R	TONE_COUNTER	The TONE_COUNTER counts continuously with a selectable clock source. Sources are selected with CLKSRC values in the TONE_CTRL1_REG. Periodically the counter is latched in TONE_LATCH1_REG	0

Table 214: TONE_LATCH1_REG (0xFF4994)

Bit	Mode	Symbol	Description	Reset
15-0	R	TONE_LATCH1	Contains the latched TONE_COUNTER1_REG value. Will be cleared when writing to TONE_CLEAR_INT1_REG	0

Table 215: TONE_CLEAR_INT1_REG (0xFF4996)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TONE_CLEAR_INT1	Writing clears TONE_LATCH1_REG and bit CT1_INT. (Note: it takes maximum 7 us before register TONE_LATCH1_REG is cleared) Reading returns 0.	0

Table 216: TONE_CTRL2_REG (0xFF4998)

Bit	Mode	Symbol	Description	Reset
15-11	-			0
10	R/W	GATE_EDGE2	0 = Rising edge of GATE_CLK used to clock TONE_TIMER 1 = Rising and falling edge of GATE_CLK used	0
9	R/W	MCT2_INT	0 = Disable CT2_INT to CT_CLASSD_INT 1 = Enable CT2_INT to CT_CLASSD_INT, **(Note 84)**	0
8	R	CT2_INT	1 = Tone latch 2 interrupt. Must be cleared by writing to TONE_CLEAR_INT2_REG	0
7-4	R/W	TIMER_RELOAD2	Select clock divider reload value for clock to latch timer periodically 0 = divide by 1, 15 = divide by 16	0
3-2	R/W	CLKSRC2	00 = 144 kHz 01 = reserved 10 = ECZ1 from Gen2DSP 11 = ECZ2 from Gen2DSP	0
1-0	R/W	GATESRC2	00 = 93.8 Hz 01 = RINGING comparator 10 = ECZ1 from Gen2DSP 11 = ECZ2 from Gen2DSP	0

Table 217: TONE_COUNTER2_REG (0xFF499A)

Bit	Mode	Symbol	Description	Reset
15-0	R	TONE_COUNTER2	The TONE_COUNTER2 counts continuously with a selectable clock source. Sources are selected with CLKSRC2 values in the TONE_CTRL2_REG. Periodically the counter is latched in TONE_LATCH2_REG	0

Table 218: TONE_LATCH2_REG (0xFF499C)

Bit	Mode	Symbol	Description	Reset
15-0	R	TONE_LATCH2	Contains the latched TONE_COUNTER2_REG value. Will be when writing to TONE_LATCH2_REG.	0

Table 219: TONE_CLEAR_INT2_REG (0xFF499E)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	TONE_CLEAR_INT2	Writing clears TONE_LATCH2_REG and bit CT2_INT. (Note: it takes maximum 7 us before register TONE_LATCH2_REG is cleared) Reading returns 0.	0

Table 220: TRACE_CTRL_REG (0xFF5020)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	R/W	TRACE_MODE	0 = Cyclic mode 1 = One shot	0
14-12	R/W	TRACE_COND_EXT	Trace conditions using external pins P2[2], P2[5] 0 = P2[2], P2[5] are don't care 1 = reserved 2 = Trace if or(P2[2], P2[5]) = 1 3 = Trace if nor(P2[2], P2[5]) = 1 4 = Trace if and(P2[2], P2[5]) = 1 5 = Trace if nand(P2[2], P2[5]) = 1 6 = Trace if xor(P2[2], P2[5]) = 1 7 = Trace if nxor(P2[2], P2[5]) = 1	0
11	R/W	I_TRACE_ON	1 = Instruction trace enabled	0
10	R/W	D_TRACE_ON	1 = Data trace enabled	0
9	R/W	I_TRACE_EV_ON	1 = Generate Event after an Instruction trace record is written	0
8	R/W	D_TRACE_EV_ON	1 = Generate Event after a Data trace record is written	0
7	R/W	BUS_EVENTS_ON	1 = Generate Event at internal Bus grant change	0
6	R/W	DSP_EVENTS_ON	1 = Generate Event at internal DSP WTF_IN or ECZ2 output change	0
5	R/W	DIP_EVENTS_ON	1 = Generate Event at internal DIP DP0_OUT or DP1_OUT output changes.	0
4	R/W	EXT_EVENTS_ON	1 = Generate Event at port P2[2] or P2[5] input changes	0
3	R/W	TRACE_COND	Trace conditions global setting. 0 = Trace if and (TRACE_COND_EXT, address range 0 or 1) 1 = Trace if or(TRACE_COND_EXT, address range 0 or 1)	0
2-0	R/W	TRACE_SIZE	0 = No trace 4 = 1kByte 5 = 2kByte 6 = 4kByte 7 = 8kByte	0

Table 221: TRACE_STATUS_REG (0xFF5022)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	R	TRACE_BUSY	Busy with tracing	0
14	R	TRACE_EOB	End of trace buffer reached	0
13	R	TRACE_TOUCH_TOGGLE	This bit will change value each time the cache buffer is written by a source other then cache control.	0
12	-		reserved	0
11	-		reserved	0
10-0	R	TRACE_IDX	Trace buffer index. Reset if TRACE_CTRL_REG[11-4] =0	0

Table 222: TRACE_START0_REG (0xFF5024)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	-		Reserved	0
14-0	R/W	TRACE_START0	Start address of Trace region, N*1kbyte, N= 0 to 0x7fff (Max 32Mbyte)	0

Table 223: TRACE_LEN0_REG (0xFF5026)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	-		Reserved	0
14-0	R/W	TRACE_LEN0	Length of Trace region, N*1kbyte, N= 0 to 0x7fff (Max range of 32Mbyte)	0

Table 224: TRACE_START1_REG (0xFF5028)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	-		Reserved	0
14-0	R/W	TRACE_START1	Sttart address of Trace region, N*1kbyte, N= 0 to 0x7fff (Max 32Mbyte)	0

Table 225: TRACE_LEN1_REG (0xFF502A)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15	-		Reserved	0
14-0	R/W	TRACE_LEN1	Length of Trace region, N*1kbyte, N= 0 to 0x7fff (Max range of 32Mbyte)	0

Table 226: TRACE_TIMERL_REG (0xFF502C)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	TRACE_TIMERL	Trace timer Bits 15-0. Reset if TRACE_CTRL_REG[9-4] =0	0

Table 227: TRACE_TIMERH_REG (0xFF502E)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
15-0	R	TRACE_TIMERH	Trace timer Bits 23-16. Reset if TRACE_CTRL_REG[9-4] =0	0

Table 228: UART_CTRL_REG (0xFF4900)

Bit	Mode	Symbol	Description	Reset
15-11	-			0
10	R/W	INV_UTX	0 = UTX is not inverted 1 = UTX is inverted	0
9	R/W	INV_URX	0 = URX is not inverted 1 = URX is inverted	0
8	R/W	IRDA_EN	0 = NRZ mode, normal UART mode 1 = RZI mode enabled for IrDA.	0
7	R/W	UART_MODE	0 = Baudrates according to bits 4,3,2 format: 8 bits no parity 1 = 10.125kbaud is selected. 8 bits even parity. **(Note 86)**	0
6	R	RI	If 1 UART receive interrupt. Must be cleared by SW by writing to UART_CLEAR_RX_INT_REG	0
5	R	TI	If 1 UART transmit interrupt. Must be cleared by SW by writing to UART_CLEAR_TX_INT_REG **(Note 85)**	0
4-2	R/W	BAUDRATE	UART baud rate selection: **(Note 86)** 000 = 9600 Baud 001 = 19200 Baud 010 = 57.6 kBaud 011 = 115.2 kBaud 100 = Fsys/(X*45) (230.4 kBaud @10.368 MHz0 **(Note 87)** 101 = reserved 11x = reserved.	000
1	R/W	UART_TEN	If 1 the UART transmitter is enabled.	0
0	R/W	UART_REN	If 1 the UART receiver is enabled.	0

Note 85: TI reset value is 0 and will be 1 as soon as UART_TEN is enabled.
Note 86: The indicated baudrates are valid with Fsys/CLK_PER_DIV_REG[PER_DIV]=1.152 MHz.
Note 87: f the DMA unit is used make sure that the HCLK_DIV is set such that the system clock Fsys is higher than the baudrate.

Table 229: UART_CLEAR_TX_INT_REG (0xFF4904)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	CLEAR_TX	Writing any value to this register will clear the UART TI interrupt Reading returns 0.	0

Table 230: UART_CLEAR_RX_INT_REG (0xFF4906)

Bit	Mode	Symbol	Description	Reset
15-0	R/W	CLEAR_RX	Writing any value to this register will clear the UART RI interrupt Reading returns 0.	0

Table 231: UART_ERROR_REG (0xFF4908)

Bit	Mode	Symbol	Description	Reset
15-2	-		-	0
1	R/W	DMA_PARITY_ERROR	Is set by PAR_STATUS and will be reset by writing any value to UART_ERROR_REG	0
0	R	PAR_STATUS	0: no parity error, 1: parity error. Updated every new byte.	0

Table 232: UART_RX_TX_REG (0xFF4902)

Bit	Mode	Symbol	Description	Reset
15-8	-			0
7-0	R/W	UART_DATA	UART x input/output register	0

Note 88: Same address for two registers one being for data input and the other for data output.

Table 233: RF_BURST_MODE_CTRL_REG (0xFF7000) (Note 89)

Note 89: This register takes the address bits A[1:0] as extra data.

Bit	Mode	Symbol	Description	Reset
17-16	W	RX_TX	0 = Stop any running DCFs. If no DCFs are active, bits 15-0 can be programmed without starting DCFs. 1 = Initiate a new transmit slot 2 = Initiate a new receive slot 3 = Initiate a general calibration slot (ref. Section 9.8)	0
15-14	R/W	FAD	0 = use antenna1 (connected to RFP0) 1 = use antenna 2 (connected to RFP0n) 2 = Do not use antenna switching (RFP0, RFP0n inactive) 3 = Use the best antenna (in RX mode), use the best antenna from the previous RX-slot (in TX mode)	0
13	R/W	RSSI_PA_MODE	In RX Mode: Set the behavior of the RSSI measurement 0 = use EO_RSSI as the Stop SI for RSSIPH 1 = use EO_RX as the Stop SI for RSSIPH In TX Mode: Set the behavior of the PA Power Setting Port 0 = Mask the DCF of the port(s) which PA_PS = '1' 1 = Enable the DCF of the port(s) which PA_PS = '1'	0
12-7	R/W	RFCAL	RF calibration setting (ref. RF_RFCAL_CTRL_REG)	0
6-0	R/W	CN	RF channel number (ref. RF_PLL_CTRL_REG)	0

Table 234: RF_BURST_MODE_SHADOW1_REG (0xFF7070)

Bit	Mode	Symbol	Description	Reset
15	-		-	
14	R/W	RSSI_PA_MODE_SHW	In RX Mode: Set the behavior of the RSSI measurement 0 = use EO_RSSI as the Stop SI for RSSIPH 1 = use EO_RX as the Stop SI for RSSIPH In TX Mode: Set the behavior of the PA Power Setting Port 0 = Mask the DCF of the port(s) which PA_PS = '1' 1 = Enable the DCF of the port(s) which PA_PS = '1'	0
13-8	R/W	RFCAL_SHW	RF calibration setting (ref. RF_RFCAL_CTRL_REG)	0
7-0	R/W	CN_SHW	RF channel number (ref. RF_PLL_CTRL_REG)	0

Table 235: RF_BURST_MODE_SHADOW2_REG (0xFF7072)

Bit	Mode	Symbol	Description	Reset
15-5	-		-	
4	R/W	SHADOW_EN	0 = The shadowing of the BURST_MODE_CTRL_REG disabled. 1 = The shadowing of the BURST_MODE_CTRL_REG enabled.	0
3	R/W	RX_ASSERT	0 = no assertion; 1 = assert an RX slot when SO_SLOT (R_LD0 DIP command) is active.	0
2	R/W	TX_ASSERT	0 = no assertion; 1 = assert a TX slot when SO_SLOT (R_LD0 DIP command) is active.	0
1-0	R/W	FAD_SHW	0 = use antenna1 (connected to RFP0) 1 = use antenna 2 (connected to RFP0n) 2 = Do not use antenna switching (RFP0, RFP0n inactive) 3 = Use the best antenna (in RX mode), use the best antenna from the previous RX-slot (in TX mode)	0

Table 236: RF_ALW_EN_REG (0xFF7008)

Bit	Mode	Symbol	Description	Reset
12	R/W	PADR_ALW_EN	power-amplifier driver always enable	0
11	R/W	LNAMIX_ALW_EN	low-noise amplifier and mixer always enable	0
10	R/W	IF_ALW_EN	intermediate-frequency filter always enable	0
9	R/W	ADC_ALW_EN	analog-to-digital converter always enable	0
8	R/W	DEM_ALW_EN	demodulator always enable	0
7	R/W	RSSIPH_ALW_EN	RSSI peak-hold computation always enable	0
6	R/W	BIAS_ALW_EN	bias circuit always enable	0
5	R/W	SYNTH_ALW_EN	voltage-controlled oscillator always enable	0
4	R/W	PLLCLOSED_ALW_EN	PLL closed loop always enable	0
3	R/W	PORT1_ALW_EN	PORT1 always enable	0
2	R/W	PORT2_ALW_EN	PORT2 always enable	0
1	R/W	PORT3_ALW_EN	PORT3 always enable	0
0	R/W	PORT4_ALW_EN	PORT4 always enable	0

Table 237: RF_PORT_RSSI_SI_REG (0xFF700A)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	EO_RSSI_VAL	End-of-RSSI switch instant activation value	0x3A
7-0	R/W	SO_PORT_VAL	Start-of-PORT switch instant activation value	0x08

Table 238: RF_TX_SI_REG (0xFF700C)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	EO_TX_VAL	End-of-TX switch instant activation value	0x6C
7-0	R/W	SO_TX_VAL	Start-of-TX switch instant activation value	0x30

Table 239: RF_RX_SI_REG (0xFF700E)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	EO_RX_VAL	End-of-RX switch instant activation value	0x6C
7-0	R/W	SO_RX_VAL	Start-of-RX switch instant activation value	0x31

Table 240: RF_PORT1_DCF_REG (0xFF7010)

Bit	Mode	Symbol	Description	Reset
15	R/W	PA_PS	Set the behavior of the DCF in a TX slot 0 = use Start SI as programmed by SSI; 1 = use the port for PA power setting, i.e. use SO_SLOT as the Start SI and enable the DCF only when BURST_MODE_CTRL_REG[RSSI_PA_MODE] = '1'.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot	1
12	R/W	EN_BY_TX	enable DCF in TX slot	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x0D
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX, SO_PORT or SO_SLOT)	0x06

Table 241: RF_PORT2_DCF_REG (0xFF7012)

Bit	Mode	Symbol	Description	Reset
15	R/W	PA_PS	Set the behavior of the DCF in a TX slot 0 = use Start SI as programmed by SSI; 1 = use the port for PA power setting, i.e. use SO_SLOT as the Start SI and enable the DCF only when BURST_MODE_CTRL_REG[RSSI_PA_MODE] = '1'.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x11
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX, SO_PORT or SO_SLOT)	0x1E

Table 242: RF_PORT3_DCF_REG (0xFF7014)

Bit	Mode	Symbol	Description	Reset
15	R/W	PA_PS	Set the behavior of the DCF in a TX slot 0 = use Start SI as programmed by SSI; 1 = use the port for PA power setting, i.e. use SO_SLOT as the Start SI and enable the DCF only when BURST_MODE_CTRL_REG[RSSI_PA_MODE] = '1'.	1
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x1C
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX, SO_PORT or SO_SLOT)	0x14

Table 243: RF_PORT4_DCF_REG (0xFF7016)

Bit	Mode	Symbol	Description	Reset
15	R/W	PA_PS	Set the behavior of the DCF in a TX slot 0 = use Start SI as programmed by SSI; 1 = use the port for PA power setting, i.e. use SO_SLOT as the Start SI and enable the DCF only when BURST_MODE_CTRL_REG[RSSI_PA_MODE] = '1'.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x00
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX, SO_PORT or SO_SLOT)	0x2D

Table 244: RF_PLLCLOSED_DCF_REG (0xFF7018)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_TRX as the Stop SI; 1 = use EO_TRX as the Stop SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop switch instant (SO_TRX or SO_TX/EO_RX)	0x28
5-0	R/W	SET_OFFSET	offset w.r.t. SO_SLOT	0x14

Table 245: RF_SYNTH_DCF_REG (0xFF701A)

Bit	Mode	Symbol	Description	Reset
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop EO_TRX	0x1D
5-0	R/W	SET_OFFSET	offset w.r.t. SO_SLOT	0x14

Table 246: RF_BIAS_DCF_REG (0xFF701C)

Bit	Mode	Symbol	Description	Reset
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x1E
5-0	R/W	SET_OFFSET	offset w.r.t. SO_SLOT	0x00

Table 247: RF_RSSIPH_DCF_REG (0xFF701E)

Bit	Mode	Symbol	Description	Reset
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop switch instant (EO_RSSI or EO_RX)	0x01
5-0	R/W	SET_OFFSET	offset w.r.t. start instant of the demodulator	0x2A

Table 248: RF_DEM_DCF_REG (0xFF7020)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x0B
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x0F

Table 249: RF_ADC_DCF_REG (0xFF7022)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x13
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x00

Table 250: RF_IF_DCF_REG (0xFF7024)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x11
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x00

Table 251: RF_LNAMIX_DCF_REG (0xFF7026)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x0F
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x00

Table 252: RF_PADR_DCF_REG (0xFF7028)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	PADR_SSI	Select the PA driver start switch instance: 0x0 = SO_TRX 0x1 = SO_PORT 0x2, 0x3 = SO_SLOT	0x2
13	R/W	RX_SENSITIVE	enable PA driver also in RX mode	0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop switch instant (EO_TX or EO_TRX)	0x1C
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (depending on PADR_SSI)	0x2C

Table 253: RF_FAD_WINDOW_DCF_REG (0xFF702A)

Bit	Mode	Symbol	Description	Reset
11-6	R/W	FAD_DECIDE	moment when FAD algorithm makes a choice between either of the two antennas. (offset w.r.t. start instant of the demodulator)	0x28
5-0	R/W	FAD_SWAP	moment when the FAD algorithm starts measuring from the second antenna. (offset w.r.t. start instant of the demodulator)	0x23

Table 254: RF_RFCAL_CTRL_REG (0xFF7040)

Bit	Mode	Symbol	Description	Reset
6-5	R/W	RFCAL_PERIOD	Length of a (single) RF calibration step 0 = 1.36µs 1 = 2.51µs 2 = 3.67µs 3 = 4.83µs	0x1
4-3	R/W	RFCAL_MODE	0 = No RF calibration, use the value in RFCAL field 1 = RF calibration using BMCW[RFCAL] as CC_{start} 2, 3 = RF calibration using RF_RSSI_REG[RFCAL_CAP] as CC_{start}	0x2
2-0	R/W	RFCAL_STEPS	Number of measurement steps used for RF calibration (0-6) 0 = No updates, use CC_{start} as defined by RFCAL_MODE 1 = Perform 1 update, ... 6 = Perform 6 updates, 7 = Perform 7 updates in a special sequence such that the VCO frequency is minimized during calibration. (This is the setting, used during general calibration)	0x3

Table 255: RF_DEM_CTRL_REG (0xFF7044)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	SLICE_VAL	Slice or threshold value in 2's complement (-1 to 127/128) write: fixed-slice value when SLICE_EN = 0; threshold value for enabling positive frequency offset compensation when SLICE_EN = 1 & AFC_EN = 1. (recommended 0x0A in FBR, 0x14 in HBR);	0x0A
7	R/W	SLICE_EARLY	compute slice level by averaging 0 = the post-demodulation filter output 1 = the post-demodulation filter input	0
6-2	-			0
1	R/W	SLICE_EN	0 = use slice value given by SLICE_VAL **(value 0 must be used in search mode)** 1 = use measured slice value	1
0	R/W	DEM_INVERT	0 = normal demodulator output 1 = inverted demodulator output	0

Table 256: RF_PREAMBLE_REG (0xFF7046)

Bit	Mode	Symbol	Description	Reset
15	R/W	SYNC_RX_DATA	0 = output raw slicer output on RX_DATA 1 = output synchronized slicer output on RX_DATA	0
14	R/W	HALF_BIT_RATE	0 = normal operation 1 = set the DEM clock frequency to REFCLK/2, operate at half bit rate.	0
13	R/W	GATE_DATA	0 = output demodulator permanently active 1 = output demodulator equal to 0 until 4 symbols after PREAMBLE_DEL	0
12-11	R/W	PREAMBLE_SYM	Compute final slice level by 0 = averaging 4 symbols 1 = averaging 8 symbols 2 = averaging 12 symbols 3 = averaging 14 symbols	0x0
10-9	R/W	AFC_SETTLE_DEL	Delay in symbols (0, 1, 2, or 3) between switching LO and start of final slice-level computation	0x2
8	R/W	AFC_EN	0 = use digital LO as given by AFC_VAL (see above) **(value 0 must be used in search mode)** 1 = enable automatic frequency compensation	1
7-6	R/W	AFC_VAL	Value supplied (write) or computed (read) for LO: 0 = 864 kHz 1 = 943 kHz 2, 3 = 798 kHz	0x0
5-0	R/W	PREAMBLE_DEL	Delay in symbols of start moment for frequency compensation, measured from enabling time of demodulator	0x2A

Table 257: RF_SLICER_RESULT_REG (0xFF705A)

Bit	Mode	Symbol	Description	Reset
15-8	R	SLICE_VAL	Slice value computed by active slicer (not the written value)	0x00
7-6	R	AFC_VAL	Computed result for LO after AFC: 0 = 864 kHz 1 = 943 kHz 2, 3 = 798 kHz	0x0

Table 258: RF_RSSI_REG (0xFF7048)

Bit	Mode	Symbol	Description	Reset
14	R	FAD_CHOICE	The antenna chosen by the FAD algorithm 0 = Antenna 1 (connected to RFP0) 1 = Antenna 2 (connected to RFP0n)	0
13-8	R	RSSI_VAL	Received Signal Strength Indication. Reading this register resets the RSSI peak-hold circuit, allowing a very simple search mode. (Reset via MWR programming only)	0x00
7-6	-			
5-0	R	RFCAL_CAP	Return value of the RF calibration algorithm	0x30

Table 259: RF_PORT_CTRL_REG (0xFF704A)

Bit	Mode	Symbol	Description	Reset
4	R/W	ANT_INACTIVE_VAL	output value when RFP0/RFP0n inactive.	0
3	R/W	PORT4_INV	0 = PORT4 DCF on RFP4 pin; 1 = inverted PORT4 DCF on RFP4 pin.	0
2	R/W	PORT3_INV	0 = PORT3 DCF on RFP3 pin; 1 = inverted PORT3 DCF on RFP3 pin.	0
1	R/W	PORT2_INV	0 = PORT2 DCF on RFP2 pin; 1 = inverted PORT2 DCF on RFP2 pin.	0
0	R/W	PORT1_INV	0 = PORT1 DCF on RFP1 pin; 1 = inverted PORT1 DCF on RFP1 pin.	0

Table 260: RF_PAD_IO_REG (0xFF704C) (Note 90)

Note 90: All ports and test pads are supplied by an internal LDO. Their inputs and outputs can only be enabled when BIAS_DCF is active. When BIAS_DCF is inactive, the ports and test pads are in tri-state.

Bit	Mode	Symbol	Description	Reset
5-0	R/W	PAD_OE	enable digital output on pads (MSB-LSB order is: RFP4, RFP3, RFP2, RFP1, RFP0n, RFP0).	0x3F
6	R/W	P0_IE	enable digital input on pad RFP0	0
5	R/W	P4_OE	enable digital output on pad RFP4	1
4	R/W	P3_OE	enable digital output on pad RFP3	1
3	R/W	P2_OE	enable digital output on pad RFP2	1
2	R/W	P1_OE	enable digital output on pad RFP1	1
1	R/W	P0N_OE	enable digital output on pad RFP0n	1
0	R/W	P0_OE	enable digital output on pad RFP0	1

Table 261: RF_TRIM_CTRL_REG (0xFF704E)

Bit	Mode	Symbol	Description	Reset
5-4	R/W	PADR_ITRIM	PADR fine supply current setting in % of nominal current in stage 1. 0 = 50% 1 = 75% 2 = 100% 3 = 125%	0x2
3-0	-	-	-	-

Table 262: RF_PLL_CTRL1_REG (0xFF7050)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	CS_MO	Channel spacing in multiples of f_{IF} 0 = CS = 1 1 = CS = 2 2 = CS = 3 3 = CS = 4.	0x1
13	R/W	SGN_NEG	0 = SGN = +1, Channels numbers count up 1 = SGN = -1, Channel numbers count down	1
12-0	R/W	CH_ZERO	Base channel number (CH0) in multiples of f_{IF}	0x894

Table 263: RF_PLL_CTRL2_REG (0xFF7052)

Bit	Mode	Symbol	Description	Reset
15	-		Reserved, must be kept 0	0
14	R/W	MODE20M	0 = 10.368 MHz XTAL 1 = 20.736 MHz XTAL	0
13-8	R/W	MODINDEX	Modulation index *h* = MODINDEX/64	0x20
7-0	R/W	GAUSS_GAIN	Externally supplied Gaussian DAC volume,	0x90

Table 264: RF_GAUSS_GAIN_RESULT_REG (0xFF705C)

Bit	Mode	Symbol	Description	Reset
7-0	R	GAUSS_GAIN	Corrected Gaussian DAC volume after modulation gain calibration.	0

Table 265: RF_PLL_CTRL3_REG (0xFF7054)

Bit	Mode	Symbol	Description	Reset
12-11	R/W	LOCK_TIME	Lock time of the PLL 0 = 55µs 1 = 70µs (recommended with best residual FM) 2, 3 = not allowed, can give synchronisation errors in extreme cases.	0x3
10	R/W	FASTLOCK	Set the lock time of the PLL during frequency acquisition 0: Lock time defined by LOCK_TIME 1: Lock time is approximately t(LOCK_TIME)/2	0
9-0	R/W	FASTLOCK_PERIOD	First period of frequency acquisition when SD1_ORDER is set and, if FASTLOCK='1', the PLL bandwidth is doubled	0x000

Table 266: RF_PLL_CTRL4_REG (0xFF7056)

Bit	Mode	Symbol	Description	Reset
15-13	R/W	KMOD_ALPHA	Kmod channel dependent trimming constant. The modulation gain in the direct path is modified with a factor: 1-SGN×KMOD_ALPHA×CN/2048 0 = no scaling 1 = Preferred for ISM5G8, half rate 2 = Preferred for ISM5G8, full rate 5 = Preferred for US-DECT 6 = Preferred for EU-DECT	0x6
12-11	R/W	SD2_ORDER	Sigma-Delta order after FASTLOCK_PERIOD	3
10-9	R/W	SD1_ORDER	Sigma-Delta order during FASTLOCK_PERIOD 0 = use nearest integer 1 = first order ΣΔ modulator 2 = second order ΣΔ modulator 3 = third order ΣΔ modulator	1
8	R/W	MODCAL_TRIG	Trigger modulation gain calibration by a single rising edge.	0
7-0	R/W	MODCAL_PERIOD	Length of the modulation gain calibration step time = MODCAL_PERIOD/288kHz	0xC0

Table 267: RF_SLICER_REG (0xFF7058)

Bit	Mode	Symbol	Description	Reset
7-2	R/W	SLICE_LOW	threshold slicer value in 2s complement (-32/128 to 31/128) for enabling negative frequency-offset compensation (recommended 0x38 in FBR, 0x30 in HBR)	0x38
1	R/W	DECIDE_ON_AVG	when SYNC_RX_DATA enabled: 0 = decide on central sample of symbol 1 = decide on sample average	0
0	R/W	TRACK_SLICE	0 = slice-level computation enabled during preamble only 1 = slice-level computation enabled in entire slot	1

Table 268: RF_DCF_MONITOR_REG (0xFF7074)

Bit	Mode	Symbol	Description	Reset
15-12	R/W	DP3_SEL	DP3_OUT output multiplexer selector 0x0 = DP3, as programmed with R_LD commands 0x1 = DP1, as programmed with R_LD commands Rest as for field DPO_SEL	0x0
11-8	R/W	DP2_SEL	DP2_OUT output multiplexer selector 0x0 = DP2, as programmed with R_LD commands 0x1 = DP0, as programmed with R_LD commands Rest as for field DPO_SEL	0x0
7-4	R/W	DP1_SEL	DP1_OUT output multiplexer selector 0x0 = DP1, as programmed with R_LD commands 0x1 = DP3, as programmed with R_LD commands Rest as for field DPO_SEL	0x0
3-0	R/W	DP0_SEL	DP0_OUT output multiplexer selector 0x0 = DP0, as programmed with R_LD commands 0x1 = DP2, as programmed with R_LD commands 0x2 = SO_SLOT (R_LD command) 0x3 = BIAS_DCF (R_LD *OR* MWR DCF) 0x4 = SYNTH_DCF (R_LD *OR* MWR DCF) 0x5 = PLLCLOSED_DCF (R_LD *OR* MWR DCF) 0x6 = PADR_DCF (R_LD *OR* MWR DCF) 0x7 = LNAMIX_DCF (R_LD *OR* MWR DCF) 0x8 = IF_DCF (R_LD *OR* MWR DCF) 0x9 = ADC_DCF (R_LD *OR* MWR DCF) 0xA = DEM_DCF (R_LD *OR* MWR DCF) 0xB = FAD_WINDOW_DCF (R_LD *OR* MWR DCF) 0xC = RSSIPH_DCF (R_LD *OR* MWR DCF) 0xD = MODCAL (R_LD DCF) 0xE, 0xF unused, constant output 0	0x0

Table 269: WATCHDOG_REG (0xFF4C00)

Bit	Mode	Symbol	Description	Reset
15-8	-		-	0
7-0	R/W	WDOG_VAL	Watchdog preset value. Decremented by 1 every 10.66 msec. If 0 a NMI interrupt or internal reset is generated, depending on the TIMER_CTRL_REG[WDOG_CTRL] and value 0xFF is automatically reloaded into the watchdog timer. See also Figure 16	0xFF

35.0 Specifications

All MIN/MAX specification limits are guaranteed by design, or production test, or statistical methods unless note 91 is added to the parameter description. Typical values are informative.

Note 91: This parameter will not be tested in production. The MIN/MAX values are guaranteed by design and verified by characterization.

Table 270: ABSOLUTE MAXIMUM RATINGS (Note 92)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
VBAT_max	Max voltage on VBAT, PON, CHARGE, LDO_CTRL, LDORF_CTRL			**5.5**	**V**
Vdd_max	Max Core supply voltage (VDD-VSS / AVD-AVS / CP_VDD-CP_VSS)			**2.0**	**V**
Vesd_mm	ESD voltage according to machine model			**150**	**V**
Vesd_hbm	ESD voltage according to human body model			**2000**	**V**

Note 92: Absolute maximum ratings are those values that may be applied for maximum 50 hours. Beyond these values, damage to the device may occur.

Table 271: OPERATING CONDITIONS (Note 93)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vbat	Supply voltages VBAT, PON, CHARGE, LDO_CTRL, LDORF_CTRL				**5.5**	**V**
RF_SUPPLY	Supply voltages RF_SUPPLY-VSS_PADR		**1.9**		**3.45**	**V**
Vpa	CLASSD Supply voltage VDDPA-VSSPA	**(Note 98)**			**3.45**	**V**
AVD	Supply voltage AVD-VSS.	**(Note 96)**	**1.75**	**1.8**	**1.98**	**V**
VDD	Supply voltages VDD-VSS	**(Note 96)**	**1.75**	**1.8**	**1.98**	**V**
Vdig	Voltage on all digital pin without backdrive protection				**VDD+ 0.3**	**V**
Vana	Voltage on analog pins **and RSTn pin**				**AVD+ 0.3**	**V**
Vdig_bp	Voltage on digital pins with backdrive protection (pad type DIO-BP), regardless of the state of PAD_CTRL_REG[xxx_OD]				**3.45**	**V**
Vntc_adc2	Voltage on NTC/ADC2 with BAT_CTRL2_REG[NTC_DISABLE] = 0 and AD_CTRL_REG[ADC2_PR_DIS] = 1				**3.45**	**V**
Vpin_neg	Minimum voltage on any pin		**VSS-0.3 AVS-0.3**			**V**
Iprot_mic	Current through protection diode MICh to internal AGND	**(Note 97)**			**2.4**	**mA**
Iprot_cid	Current through protection diode PARADET, RINGp, RINGn, CIDINp, MICp/CIDINn to internal AGND	**(Note 97)**			**1**	**mA**
Iprot_adc	Current through protection diode of ADC0, ADC1, ADC2 inputs to internal AGND.	**(Note 97)**			**1**	**mA**
Ipa	Current through VDDPA, PAOUTx, VSS	**(Note 94)**			**500**	**mA**
Ivddio_tot	Total sink current of IOs (including BP pads)				**120**	**mA**
Ppackage	Package power dissipation @ 25 °C				**1**	**W**
V_RF_TXout	PA driver output biasing voltage on pins RF_TXp, RF+TXn		-	**1.2**	-	**V**

Table 271: OPERATING CONDITIONS (Note 93)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
R_ref	Reference resistor (2% accuracy)		**54.9**	**56**	**57.1**	**kΩ**
Tstorage	Refer to SiTel Portal “Floor- and shelf life advisory”					
TA	Ambient temperature with all specifications guaranteed	**(Note 95)**	**-20**		**+60**	**°C**

Note 93: Within the specified limits, a life time of 10 years is guaranteed.

Note 94: A life time of 10 years of the CLASSD amplifier is guaranteed if switched on for 10% of the time.

Note 95: Within this temperature range full operation is guaranteed

Note 96: Full operating mode; the differences between AVD, VDD may never be more than 300mV; during a short period of time e.g. during power up more than 300mV difference is allowed. Analog performance is only guaranteed from 1.75-1.98V

Note 97: For pads with the protection circuit enabled, the protection current **must** be limited with external source resistor Rext.
Without series resistor on ADC0, ADC1, ADC2, the voltage must stay below 1.4V
Without series resistor on MICp, MICn, MICh, CIDINn, CIDINp and PARADET the voltage must stay between 0.4V and 1.4V.
The series resistor Rext can be calculated as follows: Rext >(Vext-1.4)/Iprot_xxx).

Note 98: PAOUTp and PAOUTn are forced to VSSPA if
VDDPA > 3.3V ... 3.45V (trimmed BANDGAP_REG: AVD = 1.8V)
VDDPA > 3.15V ... 3.6V (BANDGAP_REG = 0x8).
This mechanism protects VDDPA when the loudspeaker coils returns its energy when the battery is disconnected. Protection status is shown in CLASSD_CTRL_REG[1].

35.1 ELECTRICAL CHARACTERISTICS

VDD, AVD = 1.8 Volt all signals are related to VSS. Typical values are at +25 °C. MAX and MIN values are over the full temperature range TA. Crystal frequency = 10.368 MHz unless specified otherwise.

Table 272: Battery Supply currents

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Ivbat_off	VBAT input current in off state **(Note 91)**	0V < VBAT <2.4V PON, CHARGE = 0V.		**25**	**50**	**µA**

Table 273: Supply currents (values derived from characterization, 4 sigma extrapolated values)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Ivdd_static	Static VDD current	XTAL = VSS, T=25 deg C		**40**	**75**	**µA**
Ivdd_static_t		XTAL = VSS, T=TA		**40**	**220**	**µA**
Ivdd_rcur_ram108p	VDD supply current when CR16 is executing “while (1)” from **shared RAM**, Not including Ivdd_static (FLASH device)	CR16@10.368/(8*16) MHz, PLL off. DIP executing U_PSC, PAGON, WT FF,		**1.1**	**1.3**	**mA**
Ivdd_rcur_ram108		CR16@10.368/8 MHz, PLL off		**1.2**	**1.5**	**mA**
Ivdd_rcur_ram101		CR16@10.368 MHz, PLL off		**2.7**	**2.9**	**mA**
Ivdd_rcur_ram_40_1p25		CR16@10.368/8 MHz, PLL@41.472 MHz		**2.5**	**3.0**	**mA**
Ivdd_rcur_ram_40_20		CR16@20.736 MHz, PLL@41.472 MHz		**5.5**	**5.9**	**mA**
Ivdd_rcur_ram_80_1p25		CR16@10.368/8 MHz, PLL@82.944 MHz		**3.7**	**4.5**	**mA**
Ivdd_rcur_ram_80_20		CR16@20.736 MHz, PLL@82.944 MHz		**6.8**	**7.2**	**mA**
Ivdd_rcur_ram_165_1p25		CR16@10.368/8 MHz, PLL@165.888 MHz		**6.2**	**7.5**	**mA**
Ivdd_rcur_ram_165_10		CR16@10.368 MHz, PLL@165.888 MHz		**7.7**	**9.3**	**mA**
Ivdd_rcur_ram_165_20		CR16@20.736 MHz, PLL@165.888 MHz		**9.4**	**10.3**	**mA**
Ivdd_rcur_ram_165_40		CR16@41.472 MHz, PLL@165.888 MHz		**12.6**	**13.3**	**mA**

Table 273: Supply currents (values derived from characterization, 4 sigma extrapolated values)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
lvdd_rcur_flash108p	VDD supply current when CR16 is executing “while (1)”, Not including lvdd_static	CR16@10.368/(8*16) MHz, PLL off. DIP executing U_PSC, PAGON, WT FF,		1.5	1.8	mA
lvdd_rcur_flash108		CR16@10.368/8 MHz, PLL off		1.8	2.2	mA
lvdd_rcur_flash101		CR16@10.368 MHz, PLL off		4.7	5.6	mA
lvdd_rcur_flash_40_1p25		CR16@10.368/8 MHz, PLL@41.472 MHz		3.3	4	mA
lvdd_rcur_flash_40_20		CR16@20.736 MHz, PLL@41.472 MHz		8.2	10	mA
lvdd_rcur_flash_80_1p25		CR16@10.368/8 MHz, PLL@82.944 MHz		4.9	6	mA
lvdd_rcur_flash_80_20		CR16@20.736 MHz, PLL@82.944 MHz		10	12	mA
lvdd_rcur_flash_165_1p25		CR16@10.368/8 MHz, PLL@165.888 MHz		8	10	mA
lvdd_rcur_flash_165_10		CR16@10.368 MHz, PLL@165.888 MHz		10.6	13	mA
lvdd_rcur_flash_165_20		CR16@20.736 MHz, PLL@165.888 MHz		13	16	mA
lvdd_rcur_flash_165_40		CR16@41.472 MHz, PLL@165.888 MHz		17	20	mA
lvdd_rcur_rom108p	VDD supply current when CR16 is executing “while (1)”, Not including lvdd_static	CR16@10.368/(8*16) MHz, PLL off. DIP executing U_PSC, PAGON, WT FF,		0.9	1.1	mA
lvdd_rcur_rom108		CR16@10.368/8 MHz, PLL off		1.0	1.2	mA
lvdd_rcur_rom101		CR16@10.368 MHz, PLL off		2.4	2.7	mA
lvdd_rcur_rom_40_1p25		CR16@10.368/8 MHz, PLL@41.472 MHz		2.3	2.6	mA
lvdd_rcur_rom_40_20		CR16@20.736 MHz, PLL@41.472 MHz		5.3	5.5	mA
lvdd_rcur_rom_80_1p25		CR16@10.368/8 MHz, PLL@82.944 MHz		2.7	3	mA
lvdd_rcur_rom_80_20		CR16@20.736 MHz, PLL@82.944 MHz		5.7	6	mA
lvdd_rcur_rom_165_1p25		CR16@10.368/8 MHz, PLL@165.888 MHz		5	5.3	mA
lvdd_rcur_rom_165_10		CR16@10.368 MHz, PLL@165.888 MHz		6.4	6.7	mA
lvdd_rcur_rom_165_20		CR16@20.736 MHz, PLL@165.888 MHz		8	8.3	mA
lvdd_rcur_rom_165_40		CR16@41.472 MHz, PLL@165.888 MHz		10.8	11.3	mA
lvdd_bmcrx	**Delta** VDD supply current of BMC Rx	BMC all slots, encryption on, 1.152 Mbit/s (B_DIV1), RFCLK disabled.		320	370	uA
lvdd_bmctx	**Delta** VDD supply current of BMC Tx	BMC all slots encryption on, 1.152 Mbit/s (B_DIV1), RFCLK disabled.		235	290	uA
lvdd_dspmin10	**Delta** VDD DSP supply current (PLL currents are included in lvdd_rcur_xx)	Gen2DSP@10.368 MHz. DSP_EN=1 waiting for trigger.		0.1	0.12	mA
lvdd_dspmax10		Gen2DSP@10.368 MHz. 1296 cycles 10/90% SCP RAM/ROM load		2.8	3.8	mA
lvdd_dspmin80		GenDSP@81.944 MHz. PLL@165.888 MHz. DSP_EN=1 waiting for trigger.		0.78	0.85	mA
lvdd_dspmax80		GenDSP@82.944MHz.. PLL@165.888 MHz 10368 cycles 10/90% SCP RAM/ ROM load		24.5	32	mA
lvdd_codec	**Delta** VDD Codec supply current	MIC_PD=0.		0.2	0.4	mA

Table 273: Supply currents (values derived from characterization, 4 sigma extrapolated values)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Iavd_codec	**Delta** AVD Codec supply current	Reference amplifiers on, microphone amp on, LSRp/n on, Codec on.		**4.2**	**5**	**mA**
Iavd_power	AVD Power circuit current	Includes AVD static current in LDO baseband.		**0.18**	**0.25**	**mA**
Iavd_cid	**Delta** AVD opamps current	One of Caller-id, paradet, ringing opamps is on		**0.35**	**0.5**	**mA**
Ivbat_cp	**Delta** VBAT + AVD Charge pump current	VBAT = 2.4V, No load at CP_VOUT1, CP_VOUT2, CP_CTRL_REG=0x103		**150**		**µA**
Irf_supply	RF_SUPPLY (pin 71+12) currents	LDO XTAL + XTAL oscilator + static bias currents. Trimmed bandgap and 10.368MHz Crystal. type CMT1036_KJAK. LDORF_ON=0		**0.8**	**1.1**	**mA**

Table 274: RF Supply currents

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Irf_supply_RX	Total supply current in receive mode	RF_ALW_EN_REG = 0x0FE0		**68**	**81**	**mA**
Irf_supply_TX	Total supply current in transmit mode	RF_ALW_EN_REG = 0x1060		**38**	**46**	**mA**
Irf_supply_TUNE	Total supply current in tuning mode	RF_ALW_EN_REG = 0x0070		**27**	**33**	**mA**
Irf_supply_CAL	Average supply current during General Calibration	RF_BURSTMODE_CTRL_REG[RX_TX] = 0x3		**10**		**mA**

Table 275: Supply currents (Indicative value)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Iavd_pa	CLASSD normal mode supply current at AVD	CLASSD_PD=0		**3.5**		**mA**
Iavd_paport	CLASSD digital port mode supply current at AVD	(P3_0_MODE = 00 or P3_1_MODE = 00) and CLASSD_PD=1.**(Note 99)**		**5**		**uA**

Note 99: PAOUTp and PAOUTn have internally fixed resistors connected to VSSPA. The values are 5k if CLASSD[CLASSD_VOUT] = 01, else 6k.So in digital mode with a '1' on output a small static current will flow.

Table 276: Baseband Charge pump tripler (Note 100)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vcp_vout_0	CP_VOUTx Output voltage.	CP_CTRL_REG[CP_LEVELx] = 00, trimmed bandgap, 1uF load 1k	**2.4**	**2.5**	**2.7**	**V**
Vcp_vout_1	CP_VOUTx Output voltage.	CP_CTRL_REG[CP_LEVELx] = 01, trimmed bandgap	**2.9**	**3.0**	**3.2**	**V**
Vcp_vout_2	CP_VOUTx Output voltage.	CP_CTRL_REG[CP_LEVELx] = 10, trimmed bandgap	**3.9**	**4.0**	**4.2**	**V**
Vcp_vout_3	CP_VOUTx Output voltage.	CP_CTRL_REG[CP_LEVELx] = 11, trimmed bandgap	**4.3**	**4.5**	**4.7**	**V**

Table 276: Baseband Charge pump tripler (Note 100)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vcp_vout1_load	CP_VOUT1 Output voltage with full load condition at low VBAT voltage	CP_VOUT1 loaded with 50mA, CP_VOUT2 loaded with 10mA VBAT = 2.1V. CP_LEVEL1 = 11 (4.5V) CP_FREQ = 10 (CLK/16) trimmed bandgap (See AN-D-159)	**3.6**	**4**		**V**
Vcp_vout2_load	CP_VOUT2 Output voltage with full load condition at low VBAT voltage	CP_VOUT1 loaded with 50mA, CP_VOUT2 loaded with 10mA VBAT = 2.1V. CP_LEVEL1 = 11 (4.5V) CP_FREQ = 10 (CLK/16) trimmed bandgap (See AN-D-159)	**4.2**	**4.5**		**V**

Note 100: The tripler requires as least 1.98V

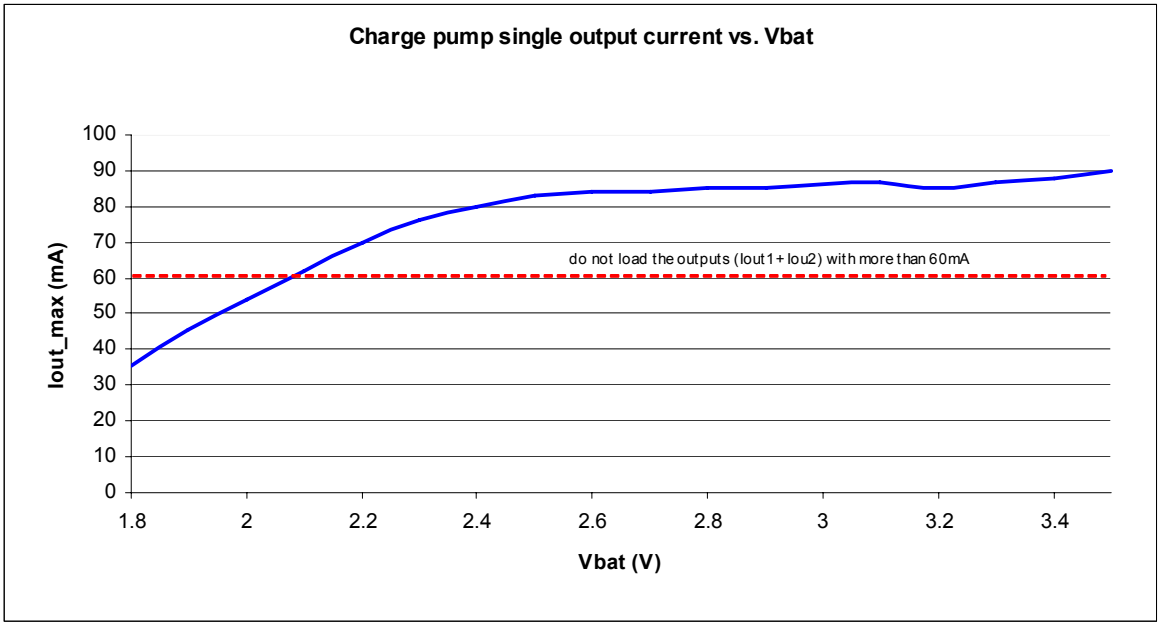

Figure 94 Typical Charge Pump maximum currents as function of VBAT

Table 277: Reset circuit

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vrst_on	Out of reset on-level	BANDGAP_REG = 0xF **(Note 101)**	**1.8**		**2.0**	**V**
Vrst_hyst	Vrst_on-Vrst_off			**150**		**mV**

Note 101: The device leaves the reset state if either the AVD > Vrst_on or the LDO2 voltage regulator has stabilized. This guarantees that the device always goes out of reset even with the smallest offset in the reset comparator. As soon as the reset circuit is in the out of reset on- state, the reset level is automatically switched to the off value Vrst_off.

Table 278: VBAT ON level

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vbat_on	VBAT Switch on level	BANDGAP_REG = 0xF	**1.8**		**2.0**	**V**
Vbat_hyst	VBATon-VBAToff			**375**		**mV**

Table 279: NTC input shuff-off level

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
NTC_hot	(NTC voltage/CHARGE voltage) below which charger shuff-off is performed	ADC2_PRDIS=1, NTC_DISABLE=0	**45**	**50**	**55**	**%**
NTC_disable	(NTC voltage/CHARGE voltage) below which charger shuff-off is disabled		**5**	**6**	**7**	**%**

Table 280: Digital and analog switching inputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vil_dig	Logic 0 input level all digital pads	VDD = 1.75-1.98V			**0.3*VDD**	**V**
Vil_pon	Logic 0 input level PON pad				**0.9**	**V**
Vil_charge	Logic 0 input level CHARGE pad				**0.9**	**V**
Vil_rst	Logic 0 input level RSTn pad	VDD = 1.75-1.98V			**0.2*VDD**	**V**
Vih_dig	Logic 1 input level all digital pads	VDD = 1.75-1.98V	**0.7*VDD**			**V**
Vih_pon	Logic 1 input level PON pad		**1.5**			**V**
Vih_charge	Logic 1 input level CHARGE pad		**1.5**			**V**
Vih_rst	Logic 1 input level RSTn pad	VDD = 1.75-1.98V	**0.8*VDD**			**V**
Ileak_hi	Input current of all inputs with (programmable) pull-down resistors disabled, except ADC inputs (see ADC) and CHARGE/P1[6]	VDD = 1.8V			**10**	**uA**
Ileak_lo	Input current of all inputs with (programmable) pull-up resistors disabled, except ADC inputs (see ADC)	Vin = VSS			**10**	**uA**
Ipull_up_lo_10k	Input current with internal **pull up** enabled.	Vin = VSS (Pad P0[1] only)	**-240**		**-120**	**uA**
Ipull_up_lo	Input current with internal **pull up** enabled.	Vin = VSS	**-100**		**-40**	**uA**
Ipull_down_hi	Input current with internal **pull down** enabled	Vin =VDD	**40**		**100**	**uA**
Ileak_pon_hi	PON Input current through pulldown resistor	Vin = 1.8V			**20**	**uA**
Ipu_rst_lo	Input current of RSTn from internal VDD through pull-up resistor.	Vin = AVS, VDD=1.8V	**-20**		**-5**	**uA**

Table 281: Digital outputs (except CLASSDp, CLASSDm digital mode)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vol_100u	Logic 0 output level	Iout = 100 uA. VDD = 1.75-1.98V			**0.1**	**V**
Vol_1ma	Logic 0 output level	Iout = 1mA PAD type VDD = 1.75-1.98V **(Note 102)**			**0.2*VDD**	**V**
Vol_2ma	Logic 0 output level	Iout = 2 mA PAD type VDD = 1.75-1.98V **(Note 102)**			**0.2*VDD**	**V**
Vol_4ma	Logic 0 output level	Iout = 4 mA PAD type VDD = 1.75-1.98V **(Note 102)**			**0.2*VDD**	**V**
Vol_8ma	Logic 0 output level (Backdrive prot. pads)	Iout = 6mA PAD type VDD = 1.75-1.98V **(Note 102)**			**0.2*VDD**	**V**
Voh_100u	Logic 1 output level	Iout = 100 uA	**VDD - 0.1**			**V**
Voh_1ma	Logic 1 output level	Iout = 1 mA PAD type VDD = 1.75-1.98V **(Note 102)**	**0.8*VDD**			**V**
Voh_2ma	Logic 1 output level	Iout = 2 mA PAD type VDD = 1.75-1.98V **(Note 102)**	**0.8*VDD**			**V**
Voh_4ma	Logic 1 output level	Iout = 4 mA PAD type VDD = 1.75-1.98V **(Note 102)**	**0.8*VDD**			**V**
Voh_8ma	Logic 1 output level (Backdrive prot. pads)	Iout = 8 mA PAD type VDD = 1.75-1.98V **(Note 102)**	**0.8*VDD**			**V**

Note 102: For open drain configurations, only V_{OL} is applicable.

Note 103: Output must stay below Vil or above Vih to avoid switching cross currents in the input stage.

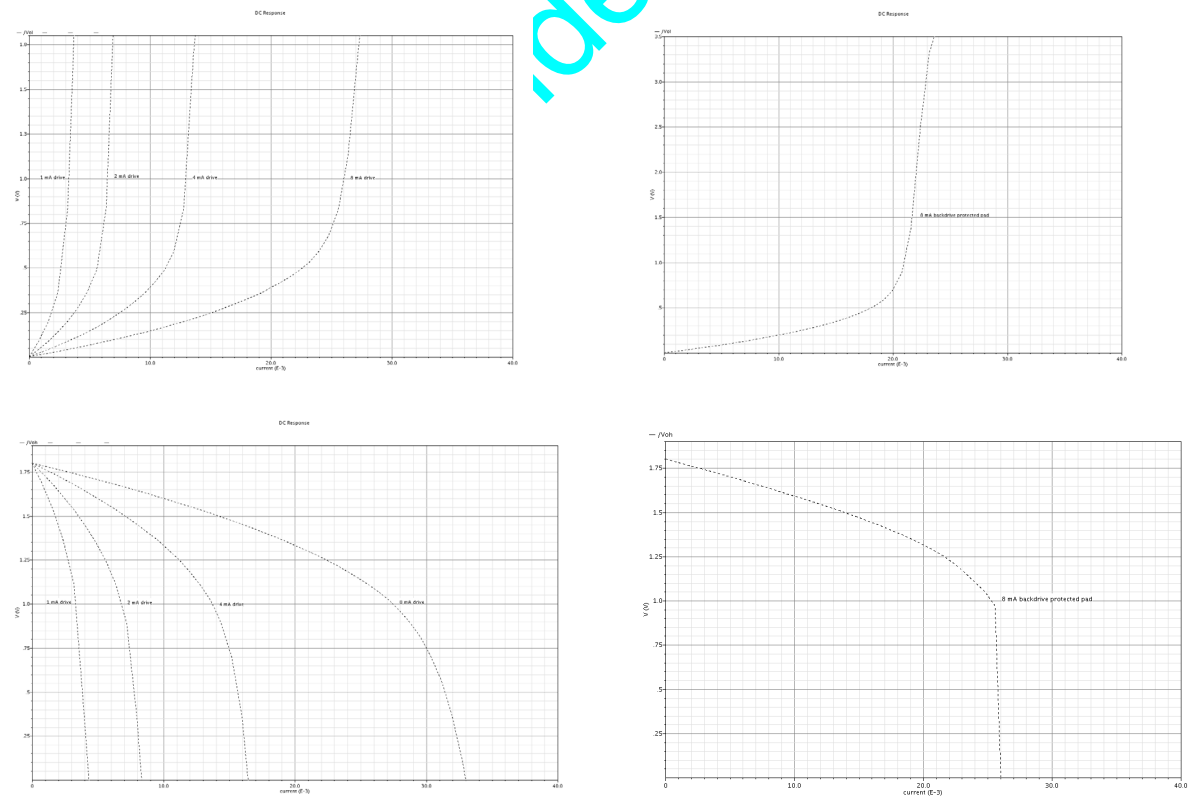

Figure 95 Digital pads output characteristics, Normal 1,2,4,8 mA (Left), Backdrive prot 8 mA (Right)

Table 282: Regulated digital RF outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Voh_e	High level output voltage for RF 'enable' ports, as used for external PA's. (measured on RFP3 and RFP4 simulta-neously)	I_out = -2 mA Internal core supply = 1.7V **(Note 104)**	**1.7-0.1**			**V**
Voh_s	High level output voltage for RF 'switch' ports, as used for e.g. PIN diode switches. (measured on RFP0, RFP0n, RFP1 and RFP2 simultaneously)	I_out = -5 mA Internal core supply = 1.7V **(Note 104)**	**1.7-0.25**			**V**

Note 104: The RF ports can provide 8 mA@0.2x1.7V, but they are tested with 2 resp 5 mA

Table 283: LED Current sources

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Iled_25	Trimmed and untrimmed LED3, LED4 output sink current	Vled_sat = 0.2V See Figure 96 curve	**1.75**	**2.5**	**3.25**	**mA**
Iled_5	Trimmed and untrimmed LED3, LED4 output sink current	Vled_sat = 0.2V See Figure 96 curve	**3.5**	**5**	**6.5**	**mA**
Iled_off	LEDs output off current	P20_OD = 1, P21_OD = 1			**10**	**uA**

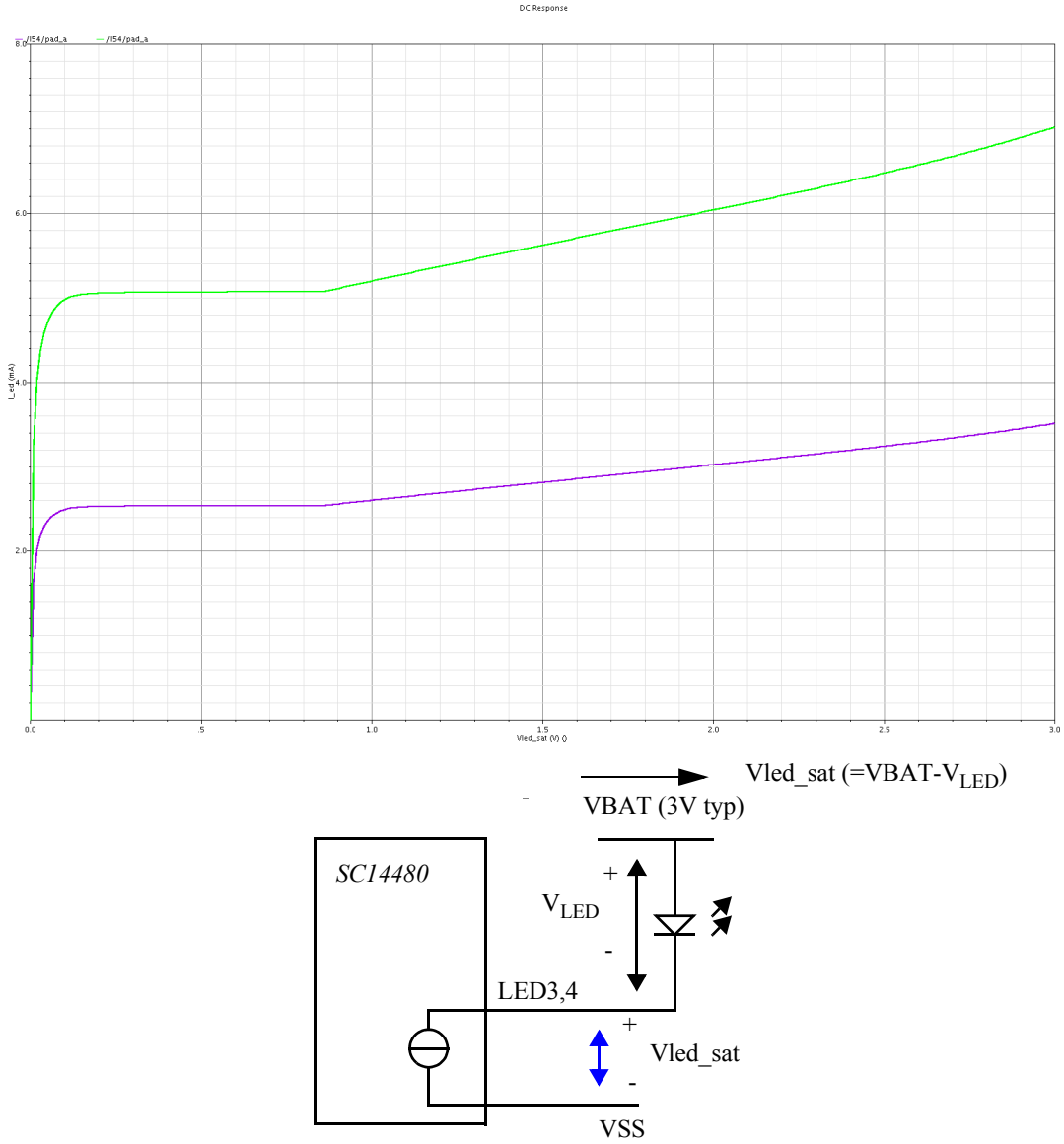

Figure 96 SC14480 LED3, 4 Typical Voltage/current saturation characteristics

Table 284: Temperature sensor

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Ttemp_sense	Temperature range inside the IC		**5**		**55**	**deg. C**
Rtemp_sense	Sensor resolution within temperature range including ADC tolerances		**-**	**0.125**	**-**	**deg / bit**
ADCtemp_sense	Decimal value of ADCout. K is temperature in Kelvin (0K = -273 deg C).		**2960-9.02*K**	**2960-8*K**	**2960-6.97*K**	

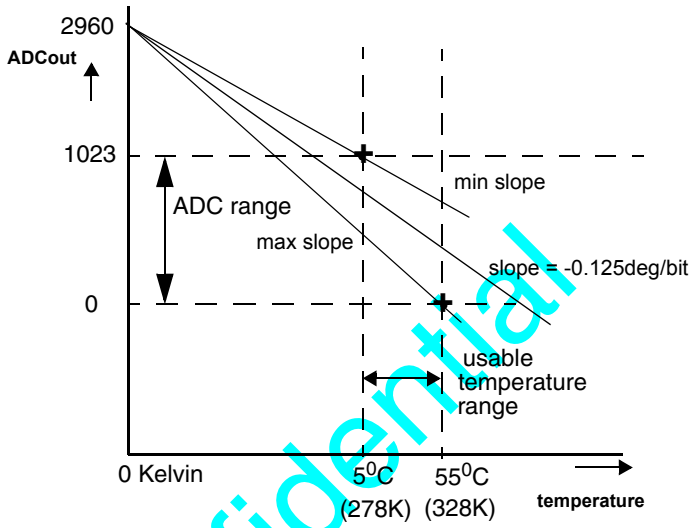

Figure 97 Temperature sensor accuracy and calibration references

Table 285: General purpose ADC. Inputs ADC0,1, 2, VBAT (Operating conditions)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Nadc_bits	ADC Resolution			**10**		**bits**
Tadc_conv	ADC Conversion time			**55**		**us**
Vadc_range	ADC0,1 linear input range with protection disabled.	ADCx_PR_DIS=1 **(Note 107)**	**0**		**1.8**	**V**
Vadc_range_adc2	ADC2 linear input range with protection disabled and NTC protected disabled	ADC2_PR_DIS=1 NTC_DISABLE=1 **(Note 107)**	**0**		**1.5**	**V**

Table 285: General purpose ADC. Inputs ADC0,1, 2, VBAT (Operating conditions)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vadc_range_p	ADC0,1,2 linear input range with protection enabled.	ADCx_PR_DIS=0 **(Note 108)(Note 97)**	**0**		**0.9**	**V**
Vadc_data0_r	Internal ADC DAC accuracy	ADC_DAC = 0 ADC_VREF = 0		**0**		**V**
Vadc_data1023_r		ADC_DAC = 0x3FF ADC_VREF = 0		**AVD**		**V**
Rsrc_adc	Output resistance of external circuit connected to ADC input				**25**	**kΩ**

Table 286: ADC0, ADC1, ADC2, CID inputs (Note 105)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Ladc_lsb_dnl	Differential non linearity **(Note 106)** **(Note 91)**		**-0.5**		**+0.5**	**LSB**
Ladc_lsb_inl	Integral non linearity **(Note 106)** **(Note 91)**		**-8**		**+8**	**LSB**
Ileak_adc0_lo	ADC0 Input leakage with pad protection disabled **(Note 91)**	ADC0 selected ADC0_PR_DIS=1 Vin = AVS	**-0.90**		**0.90**	**uA**
Ileak_adc0_hi	ADC0 Input leakage with pad protection disabled **(Note 91)**	ADC0 selected ADC0_PR_DIS=1 Vin = AVD	**-0.90**		**0.90**	**uA**
Ileak_adc0_pn	ADC0 Input leakage with pad protection enabled **(Note 91)**	ADC0 selected ADC0_PR_DIS=0 Vin = AVD/2	**-0.90**		**0.90**	**uA**
Ileak_adc1_lo	ADC1 Input leakage with pad protection disabled **(Note 91)**	ADC1 selected ADC1_PR_DIS=1 Vin = AVS	**-0.90**		**0.90**	**uA**
Ileak_adc1_hi	ADC1 Input leakage with pad protection disabled **(Note 91)**	ADC1 selected ADC1_PR_DIS=1 Vin = AVD	**-0.90**		**0.90**	**uA**
Ileak_adc1_pn	ADC1 Input leakage with pad protection enabled **(Note 91)**	ADC1 selected ADC1_PR_DIS=0 Vin = AVD/2	**-0.90**		**0.90**	**uA**
Ileak_adc2_lo	ADC2 Input leakage with pad protection disabled **(Note 91)**	ADC2 selected ADC2_PR_DIS=1 Vin = AVS	**-0.90**		**0.90**	**uA**
Ileak_adc2_hi	ADC2 Input leakage with pad protection disabled **(Note 91)**	ADC2 selected ADC2_PR_DIS=1 Vin = AVD	**-0.90**		**0.90**	**uA**
Ileak_adc2_pn	ADC2 Input leakage with pad protection enabled **(Note 91)**	ADC2 selected ADC2_PR_DIS=0 Vin = AVD/2	**-0.90**		**0.90**	**uA**

Note 105: ADC specifications are valid for BANDGAP_REG trimmed such that AVD=1.800V.

Note 106: 1 LSB equals to AVD/1024.

Differential non-linearity (DNL) error is defined as the difference between an actual step width and the ideal value of 1 LSB

Integral non-linearity (INL) is defined as being the maximum deviation from the ideal curve.

Note 107: ADC input may never be above the AVD+0.3V supply voltage, since it will influence the ADC convertor value on the other inputs.

Note 108: If the input protections are enabled the ADCs inputs have 9 bits linear range for Vin < internal AGND (0.9V)

Table 287: VBAT Scaler circuit (Note 105)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vbat_scaler	Scaler output voltage to ADC	0 <VBAT<5.5V		**1.8/5.12*VBAT**		**V**

Table 288: VBAT Scaler circuit accuracy

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vbat_scaler_1	Scaler accuracy at high input voltage including ADC INL	VBAT=3.6V	**-50**		**+50**	**mV**
Vbat_scaler_2	Scaler accuracy at low input voltage including ADC INL	VBAT=1V	**-50**		**+50**	**mV**

Table 289: CHARGER circuit (with external components)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vcharge_0	Charger output voltage	AVD trimmed to 1.8V Voltages set by VBAT_CTRL2_REG[CHARGE_LEVEL] **NOTE: For Li-Ion applications it is recommended to use the charger output as trimming reference (in stead of AVD). This way an accuracy better than 1% can be obtained.**	**2.91**	**3.0**	**3.09**	**V**
Vcharge_1			**3.3**	**3.4**	**3.5**	**V**
Vcharge_2			**3.63**	**3.74**	**3.85**	**V**
Vcharge_3			**4.75**	**4.9**	**5.05**	**V**
Vcharge_4			**5.27**	**5.43**	**5.59**	**V**
Vcharge_5			**3.74**	**3.86**	**3.98**	**V**
Vcharge_6			**3.78**	**3.9**	**4.02**	**V**
Vcharge_7			**3.83**	**3.95**	**4.07**	**V**
Vcharge_8			**3.88**	**4.0**	**4.12**	**V**
Vcharge_9			**3.93**	**4.05**	**4.17**	**V**
Vcharge_10			**3.98**	**4.1**	**4.22**	**V**
Vcharge_11			**4.03**	**4.15**	**4.27**	**V**
Vcharge_12			**4.07**	**4.2**	**4.33**	**V**
Vcharge_13			**4.12**	**4.25**	**4.38**	**V**
Vcharge_14			**4.17**	**4.3**	**4.43**	**V**
Vcharge_15			**4.87**	**5.02**	**5.17**	**V**
Icharge_001	Battery charge current	Rsense = 0.1Ω Currents set by VBAT_CTRL_REG[CHARGE_CUR]	**20**	**60**	**90**	**mA**
Icharge_010			**70**	**120**	**160**	**mA**
Icharge_011			**110**	**180**	**230**	**mA**
Icharge_100			**250**	**360**	**465**	**mA**
Icharge_101			**300**	**420**	**550**	**mA**
Icharge_110			**350**	**480**	**620**	**mA**
Icharge_111			**400**	**540**	**690**	**mA**
Voh_charge_ctrl	Drive capability of the CHARGE_CTRL pin	sourcing 500uA	**1.6**			**V**
Vol_charge_ctrl		sinking 100uA			**0.2**	**V**
Cout_ldorf	Output capacitor value (Electrolitic capacitor type)	Make sure the output capacitor is connected to ground via the 0.1Ω SoC sense resistor (see application diagrams)	**68**	**100**		**µF**

Table 290: State of charge circuit (SoC) (Operating condition)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vsocp_socn	Input voltage between SOCp and SOCn	With the prescribed 0.1 Ohm sense-resistor this results in the usable current range	**-100**		**+100**	**mV**

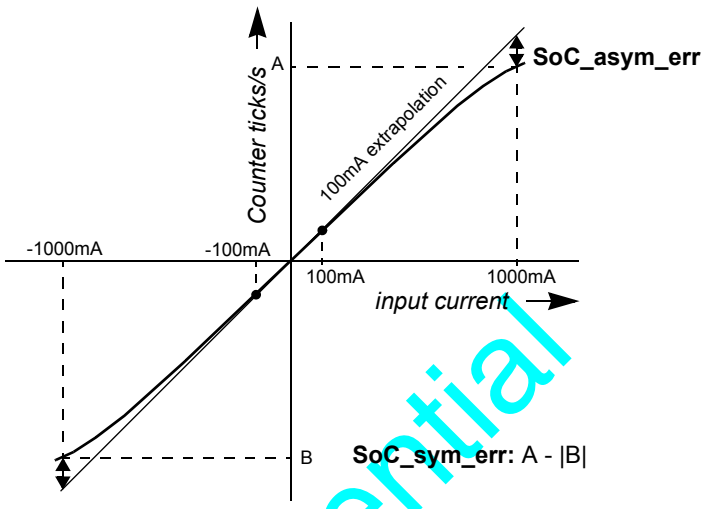

Figure 98 State of charge (SOC) counter accuracy

Table 291: State of charge circuit (SoC)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
SoC_sym_err	Relative SoC error between actual charge and discharge value at 1000 mA (see Figure 98).	Rsense = 0.1 ohm	**-3**		**+3**	**%**
SoC_asym_err	Relative SoC error between 1000 mA extrapolated (from 100 mA) and actual value. (see Figure 98).	Rsense = 0.1 ohm	**-8**		**0**	**%**
SoC_cal_err	Relative SoC error between calibration and normal mode.	100mV between SOCp, SOCn	**-2**		**+6**	**%**

Table 292: LDO_BB (with external transistor BC807-40 or equivalent) on pin VDD

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vldo	Trimmed output voltage **(Note 91)**	AVD trimmed to 1.8V	**1.76**	**1.8**	**1.84**	**V**
Vldo_8	Untrimmed output voltage **(Note 91)**	BANDGAP_REG= xx8	**1.67**	**1.8**	**1.93**	**V**
psrr_ldo	Line regulation	Dropout voltage > 200mV, 1mA < Iload < 50mA		**0.05**		**%/V**
LR_ldo	load regulation	Dropout voltage > 200mV, 1mA < Iload < 50mA		**0.0005**		**%/mA**

Table 292: LDO_BB (with external transistor BC807-40 or equivalent) on pin VDD

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Imax_ldo_ctrl	Maximum sink current in LDO_CTRL pin (for maximum LDO output current multiply this value by current gain of external transistor)	**V(LDO_CTRL) > 1V**	**6**	**11**		**mA**
Cout_ldo	Output capacitor (ceramic)		**1.0**			**µF**

Table 293: LDO_RF (with external transistor BC807-40 or equivalent) on pin RF_SUPPLY

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vldorf_20	Trimmed output voltage **(Note 91)**	AVD trimmed to 1.8V	**1.96**	**2.0**	**2.04**	**V**
Vldorf_25	Trimmed output voltage **(Note 91)**	AVD trimmed to 1.8V	**2.45**	**2.5**	**2.55**	**V**
Vldorf_30	Trimmed output voltage **(Note 91)**	AVD trimmed to 1.8V	**2.94**	**3.0**	**3.06**	**V**
Vldorf_20_8	Untrimmed output voltage **(Note 91)**	BANDGAP_REG= xx8	**1.9**	**2.0**	**2.1**	**V**
psrr_ldorf	Line regulation	Dropout voltage > 200mV, 1mA < Iload < 50mA		**0.05**		**%/V**
LR_ldorf	load regulation	Dropout voltage > 200mV, 1mA < Iload < 50mA		**0.0005**		**%/mA**
Imax_ldorf_ctrl	Maximum sink current in LDO_CTRL pin (for maximum LDO output current multiply this value by current gain of external transistor)	V(LDORF_CTRL) > 1V	**6**	**11**		**mA**
Cout_ldorf	Output capacitor (ceramic)		**1.0**			**µF**

Table 294: LDO_XTAL on pin AVD_XTAL

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vldoxtal_out	Trimmed output voltage **(Note 91)**	unloaded,AVD trimmed to 1.8V	**1.66**	**1.7**	**1.74**	**V**
Vldoxtal_out_8	Untrimmed Output voltage	unloaded, BANDGAP_REG= xx8	**1.6**	**1.7**	**1.8**	**V**
Vldoxtal_do	Dropout voltage	Iload = 5mA			**200**	**mV**
psrr_ldoxtal	Line regulation			**0.12**		**%/V**
LR_ldoxtal	load regulation	1mA < Iload < 10mA		**0.07**		**%/mA**
Imax_ldoxtal	Maximum output current		**5**			**mA**
Cout_ldoxtal	Output capacitor (ceramic)		**1.0**			**µF**

35.2 ANALOG FRONTEND SPECIFICATIONS

Table 295: Microphone amplifier

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vmic_0dB_unt	Untrimmed differential RMS input voltage between MICp and MICn (0dBm0 reference level) **(Note 91)**	0dBm0 on COUT **(Note 109)** MIC_GAIN[3:0] = 0, @ 1020 Hz; Tolerance: • 13% when untrimmed (BANDGAP_REG=8) • 6% when trimmed **(Note 110)**	**114**	**131**	**149**	**mV**
Amic_gain_0	Reference level at Vmic_0dB_unt	MIC_GAIN[3:0] = 0000		**0**		**dB**
Amic_gain_1	Microphone gain relative to Amic_gain_0	MIC_GAIN[3:0] = 0001		**1.8**		**dB**
Amic_gain_2		MIC_GAIN[3:0] = 0010		**4.1**		**dB**
Amic_gain_3		MIC_GAIN[3:0] = 0011		**6.0**		**dB**
Amic_gain_4		MIC_GAIN[3:0] = 0100		**7.8**		**dB**
Amic_gain_5		MIC_GAIN[3:0] = 0101		**10.1**		**dB**
Amic_gain_6		MIC_GAIN[3:0] = 0110		**12.0**		**dB**
Amic_gain_7		MIC_GAIN[3:0] = 0111		**14.5**		**dB**
Amic_gain_8		MIC_GAIN[3:0] = 1000		**16.1**		**dB**
Amic_gain_9		MIC_GAIN[3:0] = 1001		**18.1**		**dB**
Amic_gain_A		MIC_GAIN[3:0] = 1010		**20.6**		**dB**
Amic_gain_B		MIC_GAIN[3:0] = 1011		**22.0**		**dB**
Amic_gain_C		MIC_GAIN[3:0] = 1100		**24.0**		**dB**
Amic_gain_D		MIC_GAIN[3:0] = 1101		**26.4**		**dB**
Amic_gain_E		MIC_GAIN[3:0] = 1110		**27.9**		**dB**
Amic_gain_F		MIC_GAIN[3:0] = 1111		**29.8**		**dB**
Rin_mic	Resistance of activated microphone amplifier inputs (MICp, MICn and MICh) to internal GND **(Note 91)**		**75**	**150**		**kΩ**
Vmic_offset	Input referred DC-offset **(Note 91)**	MIC_GAIN[3..0] = 1111 3 sigma deviation limits	**-2.6**		**+2.6**	**mV**

Note 109: 0 dBm0 on COUT = -3.14 dB of max PCM value. COUT is CODEC output in test mode

Note 110: Trimming possibility is foreseen. At system production the bandgap reference voltage can be controlled within 2% accuracy and data can be stored in Flash. Either AVD or VREF can be trimmed within 2% accuracy. If AVD is trimmed VREF will be within 2% accuracy related to either AVD. Or vice versa VREF can be trimmed. For Vref trimming measure Δ (VREFp VREFm) and update BANDGAP_REG[3..0]

Table 296: Microphone amplifier (Operating Condition)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vmic_cm_level	MICp and MICn common mode voltage	MICp and MICn are set to GND with internal resistors (Rin_mic). If DC coupled the input voltage must be equal to this voltage.		**(0.9V/1.5)* VREFp**		**V**

Table 297: Microphone supply voltages

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vref_unt	VREFp-VREFm untrimmed	I_{LOAD} = 0 mA BANDGAP_REG = 8 **(Note 110)**	**1.41**	**1.5**	**1.59**	**V**
Rout_vrefp_fp	VREFp output resistance FLASH PP and FP versions	Figure 99		**25**		**Ohm**
Rout_vrefp_pp	VREFp output resistance ROM PP versions	Figure 99		**1**		**Ohm**
Nvrefp_idle	Peak noise on VREFp- VREFm **(Note 91)**	CCITT weighted			**-115**	**dBV**
PSRRvrefp	Power supply rejection Vref output **(Note 91)**	See Figure 99, AVD to VREFp/m, f = 100 Hz to 4 kHz BANDGAP_REG[5:4] = 3	**40**			**dB**

Note 111: Vrefm is a clean ground input and is the 0V reference.

Table 298: VREFp load circuits

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Cload_vrefp	VREFp (parasitic) load capacitance				**20**	**pF**
Iout_vrefp	VREFp output current				**1**	**mA**

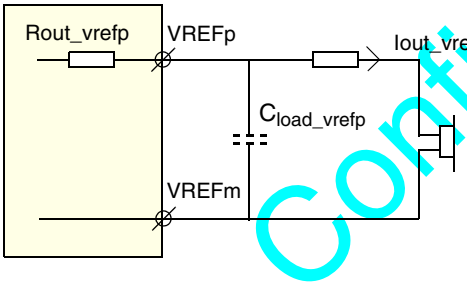

Figure 99 VREFp load circuit

Table 299: LSRp/LSRn outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vlsr_0dB_unt	Untrimmed differential RMS output voltage between LSRp and LSRn in audio mode (0dBm0 reference level)	0dBm0 on CIN **(Note 112)**, LSRATT[2:0] = 001, @ 1020 Hz Load circuit A (see Figure 100, Table 300) with RL1= inf ohm, Cp1 or load circuit B (see Figure 101) with RL2, Cp2 and Cs2 Tolerance: • 13% when untrimmed (BANDGAP_REG=8) • 6% when trimmed **(Note 110)**	**621**	**714**	**807**	**mV**

Table 299: LSRp/LSRn outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Rout_lsr	Resistance of activated loudspeaker amplifier outputs LSRp and LSRn			**1**		Ω
Alsr_gain_0	Loudspeaker gain relative to Vlsr_0dB_unt	LSRATT[2:0] =000		**2.3**		**dB**
Alsr_gain_1		LSRATT[2:0] =001		**0**		**dB**
Alsr_gain_2		LSRATT[2:0] =010		**-2.2**		**dB**
Alsr_gain_3		LSRATT[2:0] =011		**-4.0**		**dB**
Alsr_gain_4		LSRATT[2:0] =100		**-5.7**		**dB**
Alsr_gain_5		LSRATT[2:0] =101		**-8.0**		**dB**
Alsr_gain_6		LSRATT[2:0] =110		**-9.9**		**dB**
Alsr_gain_7		LSRATT[2:0] =111		**-12.1**		**dB**
Vlsr_dc	DC offset between LSRp and LSRn **(Note 91)**	LSRATT[2:0] = 3 R_{L1} = 28 Ω 3 sigma deviation limits	**-20**		**20**	**mV**

Note 112:0 dBm0 on CIN = -3.14 dB of max PCM value

Table 300: LSRp/LSRn load circuits

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Cp1_Rl1_inf	Load capacitance	see Figure 100, $R_{L1} = \infty$			**30**	**pF**
Cp1_Rl1_1k	Load capacitance	see Figure 100, $R_{L1} \leq 1$ kΩ			**100**	**pF**
Rl1	Load resistance		**28**			Ω
Cp2	Parallel load capacitance	see Figure 101			**30**	**pF**
Cs2	Serial load capacitance				**30**	**µF**
Rl2	Load resistance		**600**			Ω

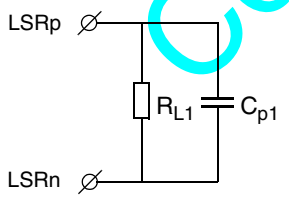

Figure 100 Load circuit A Dynamic loudspeaker

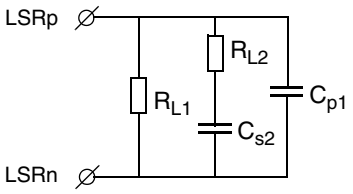

Figure 101 Load circuit B Piezo loudspeaker

Table 301: PAOUTp, PAOUTm outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vpa_4v	Differential rms output voltage between PAOUTp and PAOUTm	Trimmed bandgap input = 0dBm0, 1kHz **(Note 109)** Output low-pass filtered CLASSD_VOUT = 0		**0.985**		**Vrms**
Vpa_6v		As above CLASSD_VOUT = 1		**1.478**		**Vrms**
Zload_pa_4v	Speaker impedance, connected between PAOUTp and PAOUTm	With these values, the peak currents stays within the operating range.	**4**			Ω
Zload_pa_6v			**6**			Ω

Table 302: PAOUTp, PAOUTm outputs (Note 113)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Rout_pa	Differential output resistance between PAOUTp and PAOUTm	See remark in **(Note 113)**		**1**		Ω

Note 113: Clipping of the outputs occurs when the VDDPA drops and the following conditions becomes true. If CLASSD_CTRL_REG[CLASSD_CLIP] is unequal to zero then upon a programmable number of clipping occurences a CLASSD_INT is generated:
The software can stop clipping by reducing the gain by the GENDSP:

$$\text{Clipping occurs if } \frac{peak(LowPassFiltered(PAOUTp-PAOUTm))}{VDDPA-VSSPA} > \frac{Zload}{Zload+Rout\_pa}$$

Table 303: CLASSD THD noise

PARAMETER	DESCRIPTION	CONDITIONS	VALUES
classd_THDN	Typical THD + noise versus output power **(Note 91)**	VDDPA-VSSPA = 2.5V CLASSD_CTRL_REG = 0C.00 Frequency = 1kHz, Output signal 22kHz filtered See **Figure 103** for measurement setup	**(see Figure 102)**

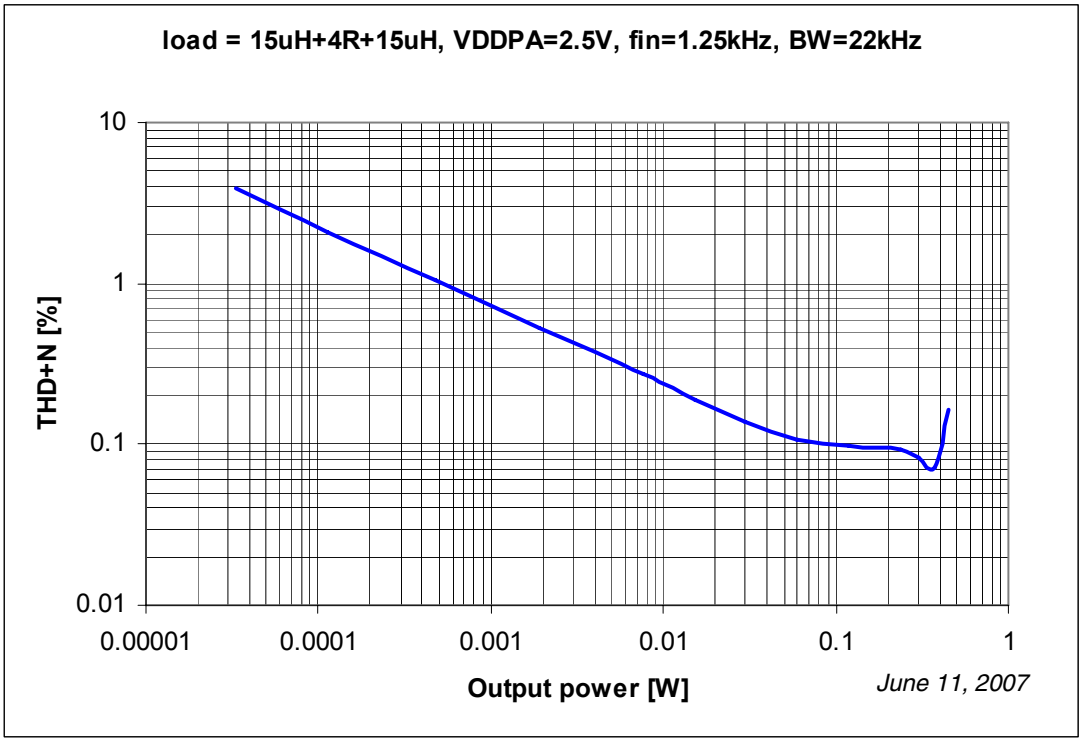

Figure 102 Class-D THD+N (total harmonic distortion + noise) versus output power

Table 304: CLASS-D output noise

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
N_classd_idle	CLASS-D amplifier Output noise. **(Note 91)**	CLASSD_CTRL_REG = 0x0308 CLASSD_BUZZER_REG = 0x0010 CODEC_ADDA_REG = 0x0002 DSP_CTRL_REG = 0xCF0E See **Figure 103** for measurement setup		**0.13**	**1.0**	**mV**

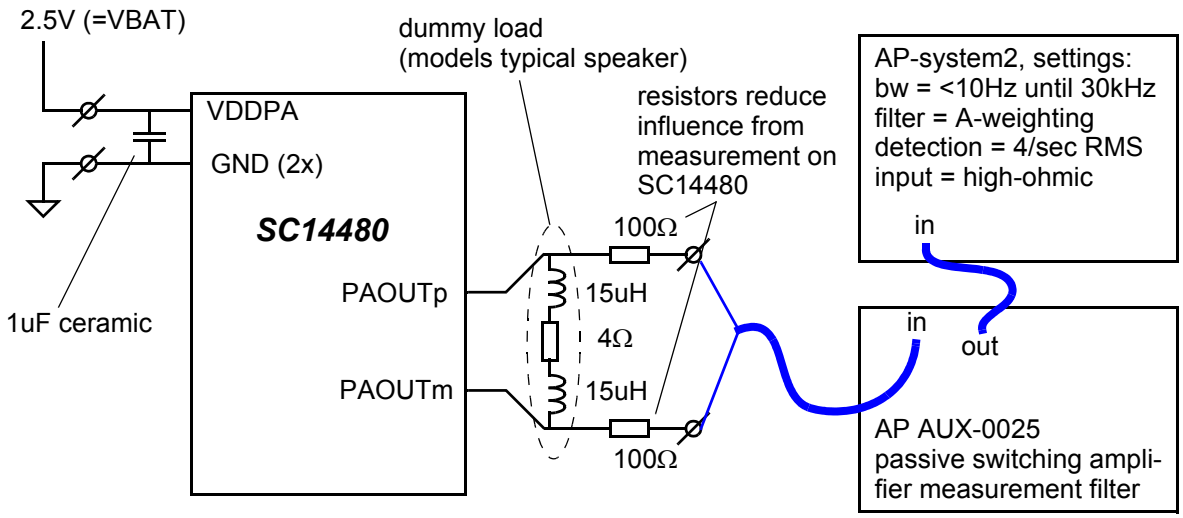

Figure 103 CLASSD amplifier measurement setup

Note 114:

Table 305: Caller ID / RING / PARA opamps

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vcid_offset	Offset voltage CID opamp **(Note 91)**	3 Sigma deviation limits	**-10**		**10**	**mV**
Vring_offset	Offset voltage RING opamp **(Note 91)**	3 Sigma deviation limits	**-10**		**10**	**mV**
Vpara_offset	Offset voltage PARA opamp **(Note 91)**	3 Sigma deviation limits	**-10**		**10**	**mV**
Vcidout	CIDOUT output range	AVD=1.8V, Rl1 = 5k	**1.6**			**V**
Vringout	RINGOUT output range	AVD=1.8V, Rl1 = 5k	**1.6**			**V**
Fcid	CID opamp bandwidth **(Note 91)**			**40**		**kHz**
Fring	RING opamp bandwidth **(Note 91)**			**40**		**kHz**
Fpara	PARA opamp bandwidth **(Note 91)**	This opamp is tested for DC only and is not tested for AC.		**0**		**kHz**

Table 306: Caller ID / RING / PARA opamps (Operation Condition)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vcid_cm_level	CIDINp and CIDINn common mode range	Trimmed AVD=1.8V VREF_PD=1, CID_PR_DIS=0 **(Note 115)**		**AVD/2 +/- 0.5**		**V**
Vring_cm_level	RINGp and RINGn common mode range	Trimmed AVD=1.8V VREF_PD=1, RNG_PR_EN=1 **(Note 115)**		**AVD/2 +/- 0.5**		**V**
Vparadet_level	PARADET Linear input range	Trimmed AVD=1.8V VREF_PD=1, PARA_PR_EN=1 **(Note 115)**		**AVD/2 +/- 0.5**		**V**

Note 115: The extra pad protection to internal AGND for the three opamps can be disabled with CID_PR_DIS =1, RING_PR_EN=0, PARA_PR_EN=0. If the extra protection is switched off, the pad protection to AVS and AVD remains.
If the extra protection circuit is enabled the total current through the protection is <100uA (worst case) for the maximum values of the specified input range. For an input range of 0.5 -> 1.3V the protection current is <12uA (worst case)

Table 307: CIDOUT, PARAOUT, RINGOUT load circuit

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Cp1	Equivalent load capacitance	(see Figure 104)			**50**	**pF**
Rl1	Equivalent load resistance	(see Figure 104)	**5**			**kohm**

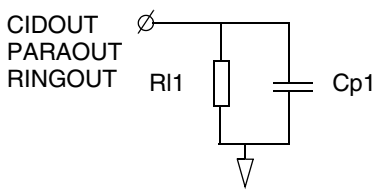

Figure 104 Load circuit CIDOUT

35.3 CODEC SPECIFICATIONS

Table 308: CODEC characteristics

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
SDad_0dB	Signal to total distortion ratio Analog/Digital	differential input signal between MICp and MICn with f=(1020/8000)* Fs Hz ADPCM transcoder active MIC_GAIN[3:0] = 0. 0 dBm0 on COUT	**40**	**60**		**dB**
SDad_40dB		-40 dBm0 on COUT	**35**			**dB**
SDad_45dB		-45 dBm0 on COUT	**30**			**dB**
SDda_0dB	Signal to total distortion ratio Digital/Analog	Differential input signal between MICp and MICn with f= (1020/8000)* Fs Hz. ADPCM transcoder active LSRATT[2:0] = 3. 0 dBm0 on CIN	**40**	**65**		**dB**
SDda_40dB		-40 dBm0 on CIN	**35**			**dB**
SDda_45dB		-40 dBm0 on CIN	**30**			**dB**
Nad_idle	Idle channel noise Analog/ Digital	MICp short circuit to MICn Relative to 0 dBm0, CCITT weighted (Fs = 8kHz) MIC_GAIN[3:0] = 0x0B		**-80**		**dBm0**
Nda_idle	Idle channel noise Digital/ Analog	Relative to 0 dBm0, CCITT weighted (Fs = 8kHz) LSRATT[2:0] = 3		**-83**	**-77**	**dBm0**
PSRRad_0	Power supply rejection ratio Analog/Digital	AVD to COUT, f = 100 Hz to (Fs/2) kHz MIC_GAIN[3:0] = 0	**40**			**dB**
PSRRad_F		MIC_GAIN[3:0] = 0x0F	**30**			**dB**
PSRRda	Power supply rejection ratio Digital/Analog	AVD to LSRp/n, f = 100 Hz to (Fs/2) kHz LSRATT[2:0] = 3	**40**			**dB**

Table 309: CODEC frequency responses

PARAMETER	DESCRIPTION	CONDITIONS	RESULT
Fad_freq	Frequency response Analog/ Digital	Relative to (1020/8000)*Fs Hz	**see frequency response diagrams Figure 105 on page 240, Figure 106 on page 240, Figure 107 on page 241**
Fda_freq	Frequency response Digital/Analog	Relative to (1020/8000)*Fs Hz	**see frequency response diagrams Figure 108 on page 241, Figure 109 on page 242, Figure 110 on page 242**

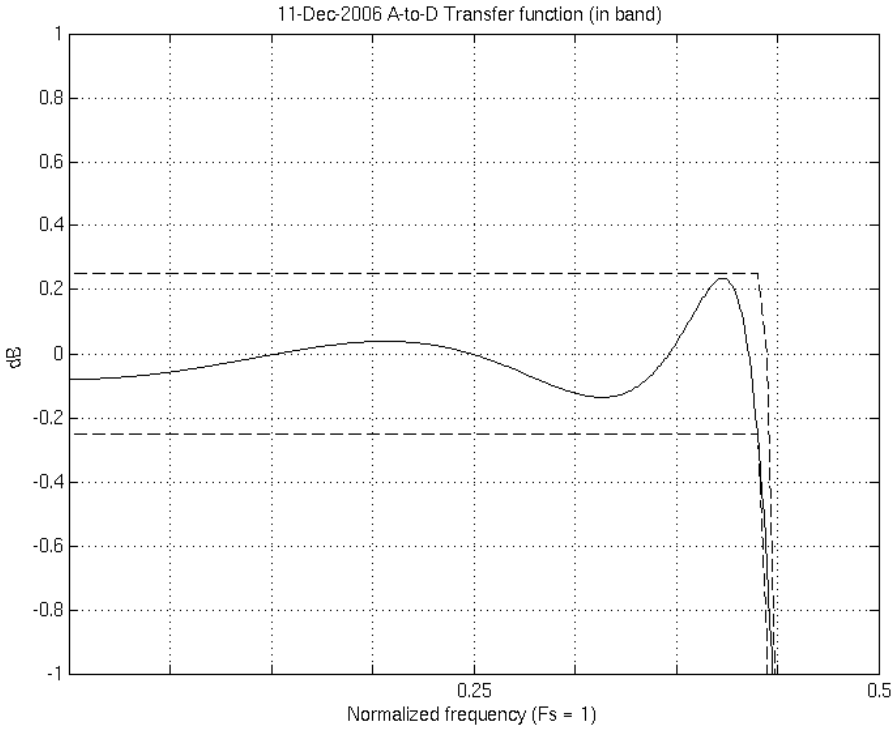

Figure 105 Codec Frequency Response, analog to digital, pass band.

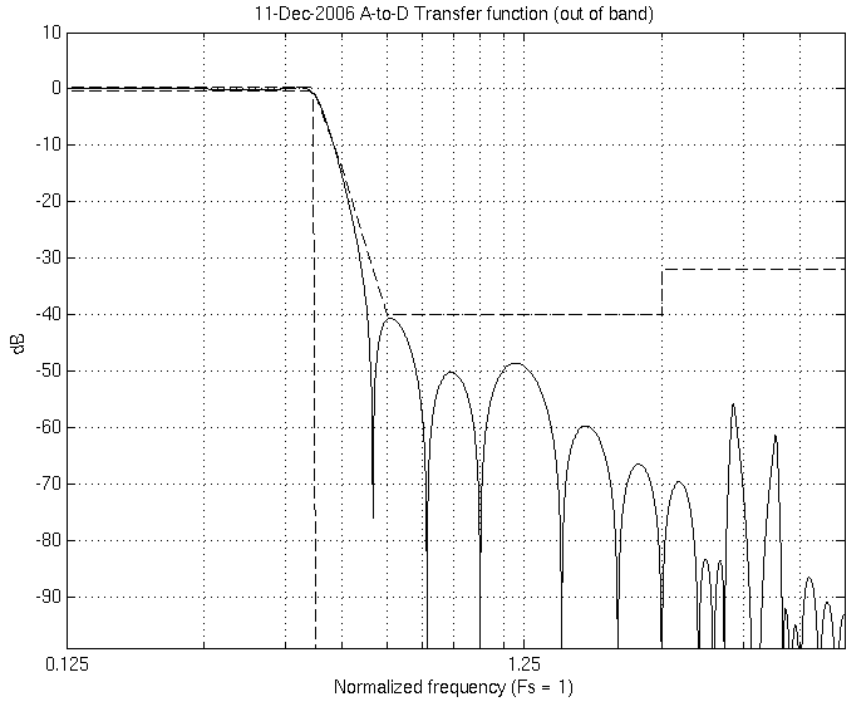

Figure 106 Codec Frequency Response analog to digital, Stop band

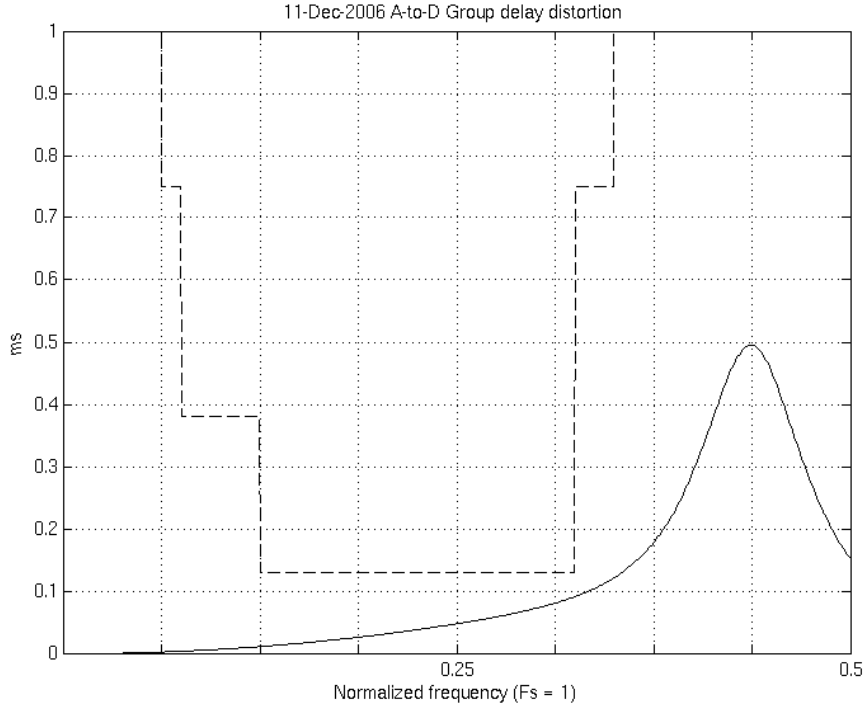

Figure 107 Codec analog to digital, group delay

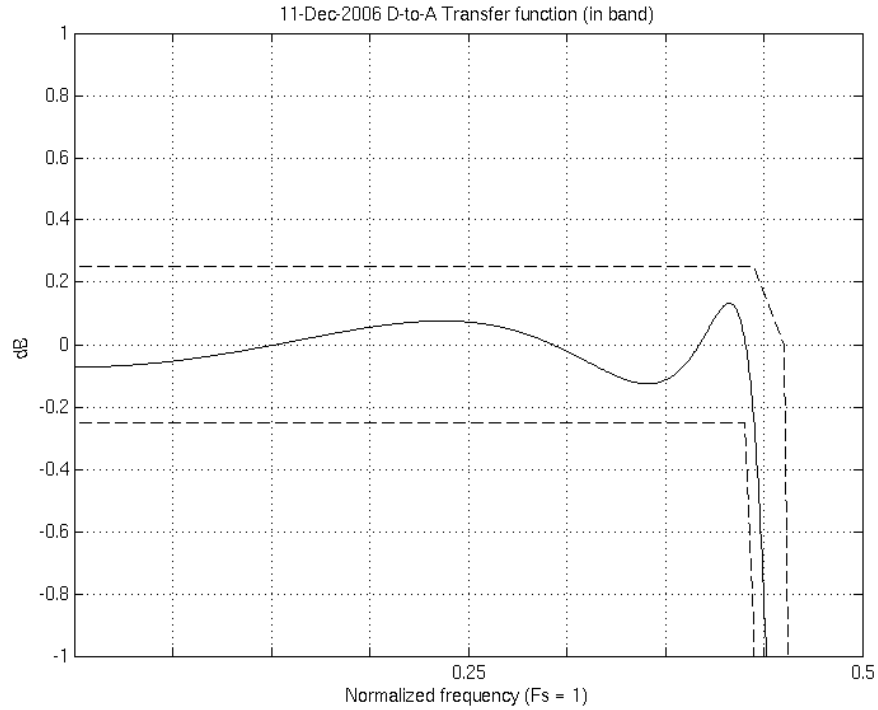

Figure 108 Frequency Response, digital to analog, pass band

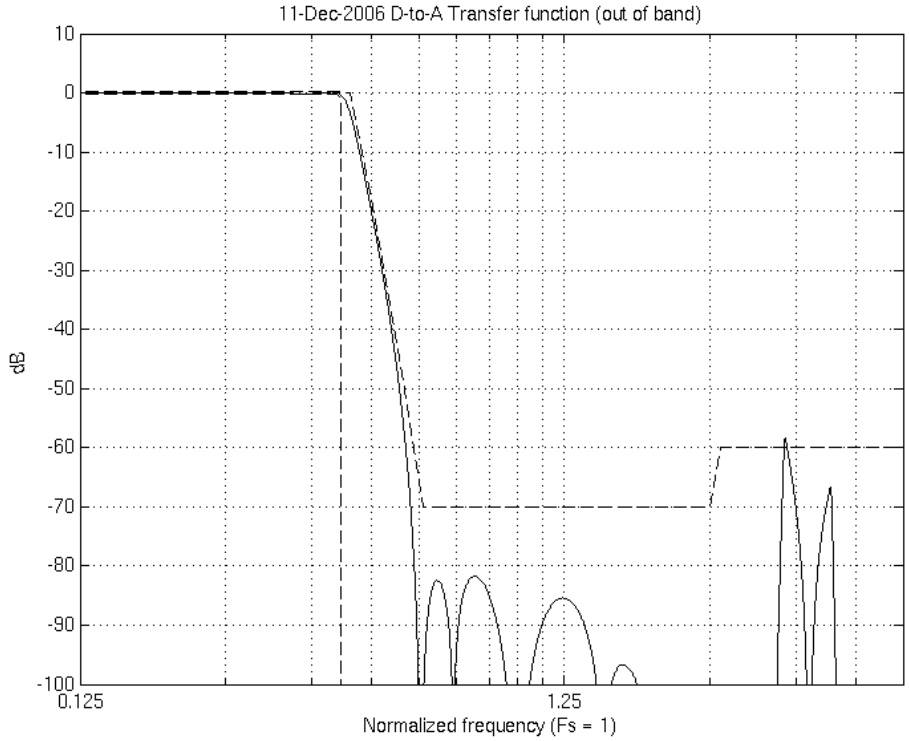

Figure 109 Codec Frequency Response, digital to analog, Stop band .

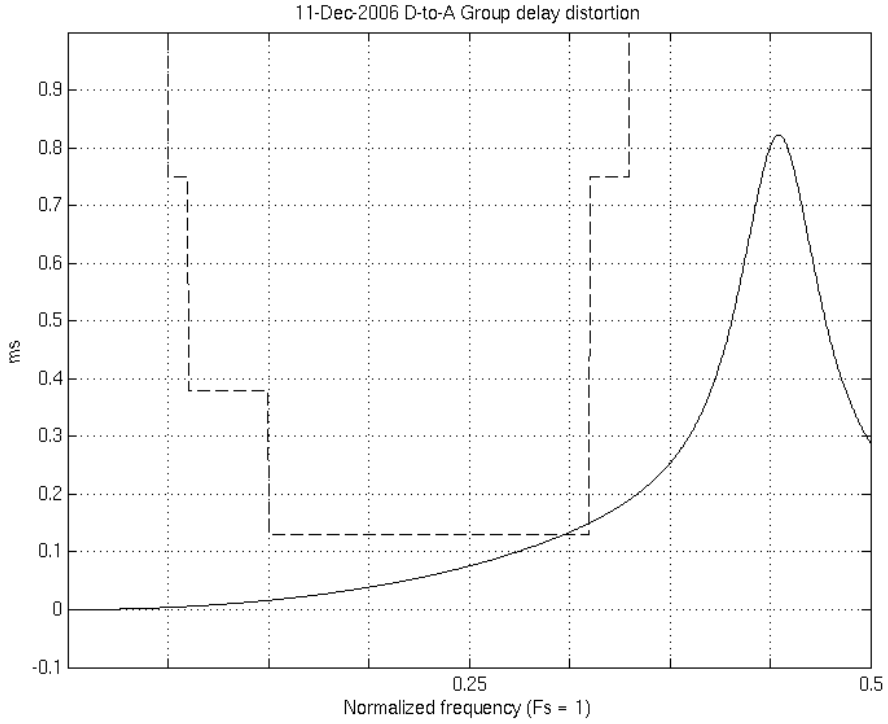

Figure 110 Codec digital to analog, Group delay distortion

35.4 RADIO RECEIVER SPECIFICATION

For s-parameters of the input RF_RXp, RF_RXn and design guidelines for an RX matching network, please refer to SiTel Semiconductor Application Note AN-D-137. All measurements are done in burst mode, using the preferred settings given in sections 33.5 and 33.6, starting on page 146.

Table 310: Receiver (Note 116), (Note 117)

Note 116: R_ref = 56kΩ.

Note 117: All Rx powers specified at input of SiTel proposed matching network.

Note 118: Tests performed on DECT channel 0, 5 , 9 (EU-DECT), 23 and 27 (US-DECT).

Note 119: Guaranteed by design.

Parameter	Description	Condition	Min	Typ	Max	Units
f_in	Receiver input frequency range		**1880**	**-**	**1950**	**MHz**
P_Rx	Receiver sensitivity at room temperature **(Note 118)**	TA = 25°C	**-**	**-96**	**-93**	**dBm**
P_Rx_T	Receiver sensitivity, full temperature range **(Note 118)**	0°C ≤ TA ≤ +55°C	**-**	**-**	**-92**	**dBm**
P_Rx_f	Receiver sensitivity, degraded by frequency offset F_os **(Note 118)**	−100 kHz ≤ F_os ≤ +100 kHz; TA = 25°C	**-**	**-**	**-90**	**dBm**
P_in	Receiver input power range	TA = 25°C BER ≤ 1E-5	**-**	**-**	**+13**	**dBm**
IPL	Intermodulation performance level (TBR06-TC19) **(Note 118)**	TA = 25°C	**-47**	**-45**	**-**	**dBm**
CI_0	Interferer performance (TBR06-TC16) **(Note 118)**	Y = M; TA=25°C	**-**	**9**	**10**	**dB**
CI_1		Y = M±1; TA = 25°C	**-**	**-17**	**-13**	**dB**
CI_2		Y = M±2; TA = 25°C	**-**	**-40**	**-34**	**dB**
CI_3		Y = any other DECT channel in range [0, 9]∪[23, 27]; TA=25°C	**-**	**-46**	**-40**	**dB**
P_Rx_RSSI_min	lower limit of RSSI monotonous range	TA = 25°C	**-**	**-108**	**-95**	**dBm**
P_Rx_RSSI_max	upper limit of RSSI monotonous range	TA = 25°C	**-31**	**-28**	**-**	**dBm**
RSSI_acc	RSSI accuracy. Tolerance of P_Rx when RSSI_VAL = *X* on a slot to slot basis.	Measured in burst mode; RSSI_VAL is a 4 sample average; 25 < *X* < 45, TA = 25°C	**-3**	**-**	**3**	**dB**
RSSI_res	RSSI resolution **(Note 119)**	Guaranteed by design	**-**	**2**	**-**	**dB/step**

35.5 RADIO TRANSMITTER SPECIFICATION

For s-parameters of the input RF_TXp, RF_TXn and design guidelines for an TX matching network, please refer to SiTel Semiconductor Application Note AN-D-137. All measurements are done in burst mode, using the preferred settings given in sections 33.5 and 33.6, starting on page 146.

Table 311: Transmitter (Note 120), (Note 121)

Note 120: R_ref = 56 kΩ;

Note 121: All Tx powers specified at output of SiTel proposed matching network.

Note 122: Tests performed on DECT channel 0, 5 , 9 (EU-DECT), 23 and 27 (US-DECT).

Parameter	Description	Condition	Min	Typ	Max	Units
f_out	Transmitter output frequency range		**1880**	**-**	**1950**	**MHz**
P_Tx	Transmitter output power, **(Note 122)**		**-1**	**-**	**3**	**dBm**
P_LO2	Suppression of the 2nd harmonic of the LO, (VCO fundamental) **(Note 122)**	TA = 25°C	**-**	**-35**	**-29**	**dBc**
P_LO3	Suppression of the 3rd harmonic of the LO **(Note 122)**	TA = 25°C	**-**	**-42**	**-35**	**dBc**
I_PADR	PA driver bias current. Refer to the equivalent circuit in Table 2.	TA = 25°C		**7**	**9**	**mA**

35.6 RADIO SYNTHESIZER SPECIFICATION

All measurements are done in burst mode, using the preferred settings given in sections 33.5 and 33.6, starting on page 146.

Table 312: Synthesizer (Note 123)

Note 123: R_ref = 56kΩ, Fxtal = 10.368MHz;

Note 124: Guaranteed by design.

Note 125: ests performed on DECT channel 0, 5 , 9 (EU-DECT), 23 and 27 (US-DECT), after modulation gain calibration is performed and with setting RF_PPL_CTRL2_REG[MODINDEX] = 0x20 (*h* = 0.5).

Note 126: Residual FM depends on the measurement bandwidth (in an almost proportinal fashion). The most appropriate bandwidth is the IF bandwidth of the receiver (1.2MHz). Due to equipment constraints the measurement bandwidth is set to 1.6MHz. The crest factor is about 3.4.

Parameter	Description	Condition	Min	Typ	Max	Units
t_settle	Settling time of synthesizer blocks before coarse calibration may be started		**10**			µs
t_cc_0	Time needed for coarse calibration (fastest), **(Note 124)**	RFCAL_PERIOD = 0	-	**1.36**	-	µs/step
t_cc_1	Time needed for coarse calibration, **(Note 124)**	RFCAL_PERIOD = 1	-	**2.51**	-	µs/step
t_cc_2	Time needed for coarse calibration, **(Note 124)**	RFCAL_PERIOD = 2	-	**3.67**	-	µs/step
t_cc_3	Time needed for coarse calibration (most accurate), **(Note 124)**	RFCAL_PERIOD = 3	-	**4.83**	-	µs/step
t_lock_0	Time needed for fine tuning (fastest)	LOCK_TIME = 0	**30**	**42**	**55**	µs
t_lock_1	Time needed for fine tuning	LOCK_TIME = 1	**30**	**47**	**70**	µs
ACPR1	Adjacent channel power ratio (TBR06-TC9) **(Note 125)**	Y=M±1	-	**-35**	**-33**	dBc
ACPR2		Y=M±2	-	**-57**	**-55**	dBc
ACPR3		Y=M±3	-	**-68**	**-66**	dBc
ACPR4		Y=M±4	-	**-71**	**-69**	dBc
ACPR5		Y=M±5	-	**-71**	**-69**	dBc
FMres	Residual FM on LO signal, measured in RX mode, **(Note 126)**	RF_PADR_DCF_REG [RX_SENSITIVE] = 1, measurement bandwidth = 1.6MHz		**3**	**5**	kHz

36.0 Timing diagrams

Table 313: PLL lock time

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tlock_pll1	Baseband PLL Lock time	Xtal = 10.368 MHz Fpll = 165.888. MHz			**0.5**	**ms**

Table 314: Baseband PLL characteristics

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Fpll1_max_vco	Baseband PLL maximum frequency				**170**	**MHz**
Fpll1_min_vco	Baseband PLL minimum frequency		**80**			**MHz**

Table 315: FLASH characteristics

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tperased	Program FLASH page erase time (256/512 Dwords page)		**20**			**ms**
Tpme	Program FLASH mass erase time		**20**			**ms**
Tpprog	Program FLASH, program time for 1 Dword		**20**			**us**
Fendurance	Number of erase/write cycles of Program with 20ms erase and 20us program time. Writing 0xFFFFFFFF is not considered as a write cycle for lifetime point of view.		**500**			

Table 316: RSTn PIN

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tlow_rst_pu	Minimum low time to reset device	After power up.	**10**			**ms**
Tlow_rst_active		In active mode **(Note 127)**	**15**			**µs**

Note 127:spikes down to 100ns may reset the device. Shorter spikes are filtered (See **Figure 15 on page 30)**

Table 317: XTAL with external clock

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Fxtal_ext_10	Input frequency external clock on XTAL for guaranteed PLL operation			**10.368**		**MHz**
Fxtal_ext_20	Input frequency external clock on XTAL for guaranteed PLL operation	XTAL_DIV=1		**20.736**		**MHz**
Txtal_duty_ext	Duty cycle external clock on XTAL	Within Vil_xtal and Vih_xtal limits	**40**		**60**	**%**

Table 318: PON, CHARGE port pins

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Fpon_charge	Maximum switching frequency of PON, CHARGE pins				**100**	**kHz**

36.1 MICROWIRE TIMING DIAGRAMS

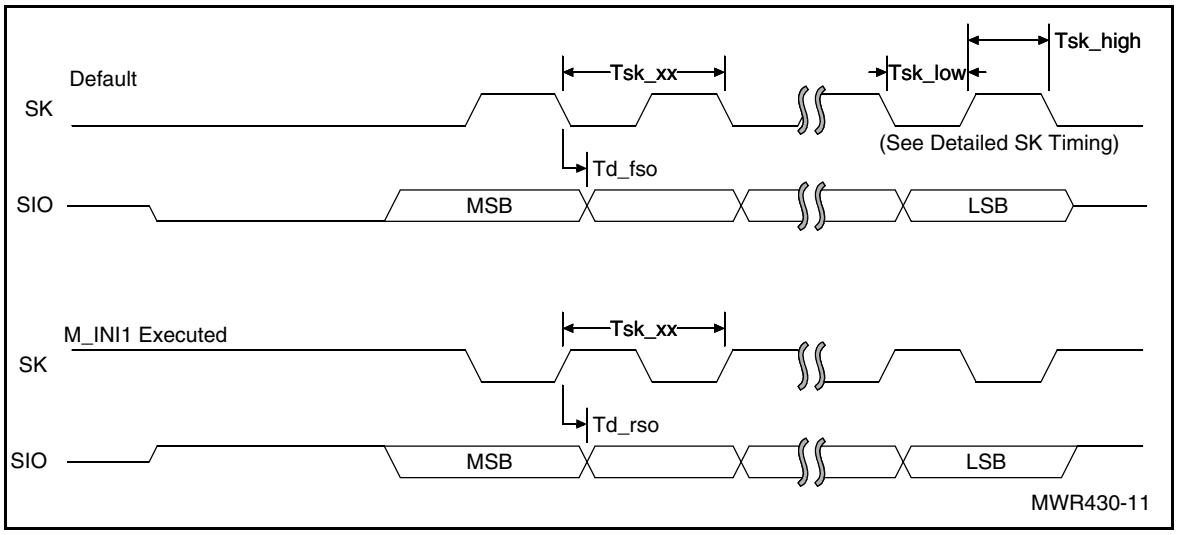

Figure 111 Microwire timing diagram (external RF mode)

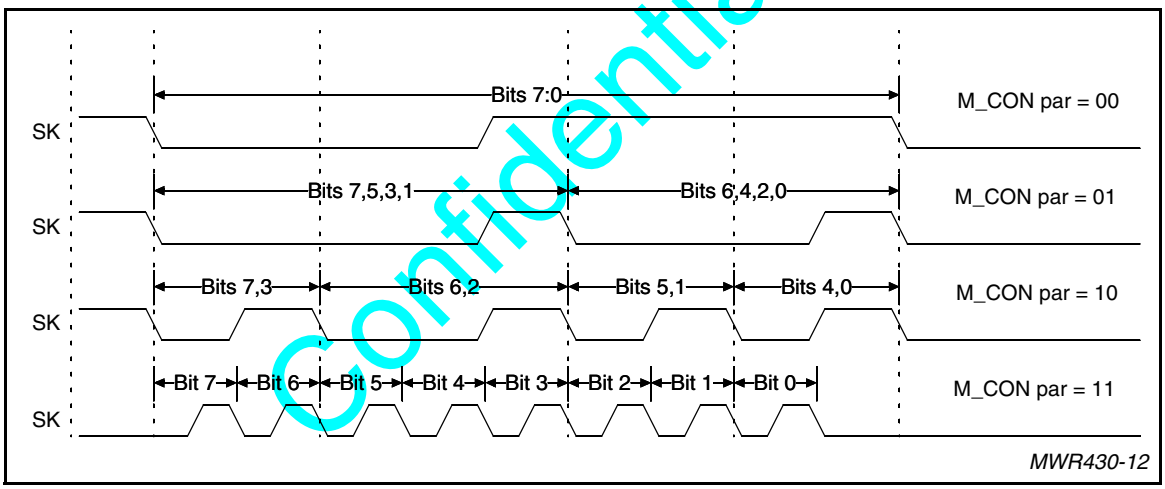

Figure 112 Detailed SK timing diagrams

Table 319: MICROWIRE interface (~~max~~ 50 pF load on all outputs, FDIP=10.368 MHz)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tsk_00	SK period time	M_CON par = 00		**9*96**		**ns**
Tsk_01	SK period time	M_CON par = 01	**4*96**		**5*96**	**ns**
Tsk_02	SK period time	M_CON par = 02	**2*96**		**3*96**	**ns**
Tsk_04	SK period time	M_CON par = 03	**1*96**		**2*96**	**ns**
Tsk_low_00	SK low time **(Note 128)**	M_CON par = 00	**4*96**			**ns**
Tsk_low_01	SK low time **(Note 128)**	M_CON par = 01	**3*96**			**ns**
Tsk_low_02	SK low time **(Note 128)**	M_CON par = 02	**96**			**ns**
Tsk_low_03	SK low time **(Note 128)**	M_CON par = 03	**48**			**ns**
Td_fso	Delay time SK falling edge to SO				**20**	**ns**
Td_rso	Delay time SK rising edge to SO				**20**	**ns**

Note 128: If M_INI0 or M_INI1 are applied, the SK clock is inverted and the SK high times have the same values as the SK low times as shown above.

36.2 UART IRDA TIMING DIAGRAMS

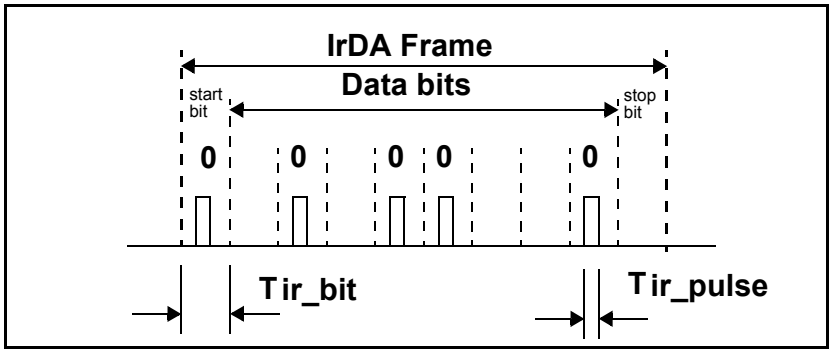

Figure 113 UART IrDA timing

Table 320: UART IrDA timing (capacitive load is 30 pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tir_pulse_96	Tx Pulse time	9600 baud (PER_DIV = 10.368 MHz)		**24/1.152**		**us**
Tir_pulse_192	Tx Pulse time	19.2 kbaud (PER_DIV = 10.368 MHz)		**12/1.152**		**us**
Tir_pulse_576	Tx Pulse time	57.6 kbaud (PER_DIV = 10.368 MHz)		**4/1.152**		**us**
Tir_pulse_115	Tx Pulse time	115.2 kbaud (PER_DIV = 10.368 MHz)		**2/1.152**		**us**
Tir_pulse	IrDA Receiver sensitivity	All baudrates (PER_DIV = 10.368 MHz)	**1**			**us**

36.3 ACCESS BUS TIMING DIAGRAM

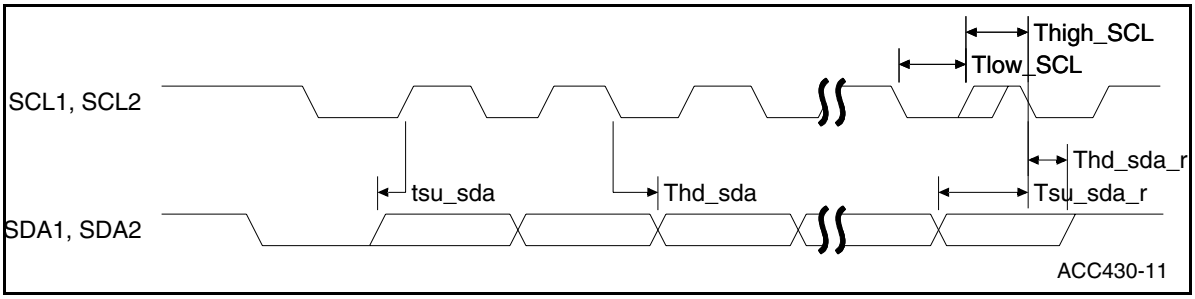

Figure 114 ACCESS bus timing

Table 321: ACCESS1, 2 bus timing (capacitive load is 30 pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tlow_scl	SCLx Low time **(Note 129)**	100 kHz mode		**5208**		**ns**
		400 kHz mode		**1543**		**ns**
		1.152 MHz mode		**290**		**ns**
Thigh_scl	SCLx high time **(Note 129)**	100 kHz mode		**4823**		**ns**
		400 kHz mode		**965**		**ns**
		1.152 MHz mode		**578**		**ns**
Tsu_sda	SDAx to SCLx setup time (transmission)	100 kHz mode	**2595**		**2615**	**ns**
		400 kHz mode	**760**		**780**	**ns**
		1.152 MHz mode	**89**		**109**	**ns**
Thd_sda	SCLx to SDAx hold time (transmission)	100 kHz mode	**2595**		**2615**	**ns**
		400 kHz mode	**760**		**780**	**ns**
		1.152 MHz mode	**185**		**205**	**ns**
Tsu_sda_r	SDAx to SCLx setup time (reception)	100 kHz mode	**120**			**ns**
		400 kHz mode	**120**			**ns**
		1.152 MHz mode	**120**			**ns**
Thd_sda_r	SCLx to SDAx hold time (reception)	100 kHz mode			**0**	**ns**
		400 kHz mode			**0**	**ns**
		1.152 MHz mode			**0**	**ns**

Note 129: The indicated values show the SCLx low and high time values if no clock stretching is applied.
If a slave device stretches the low time of SCL1 or SCL2 for less than 96 ns, the sum of Tlow_scl and Thigh_scl will stay the same. Else for every 96 ns longer stretch, the SCL clock period will increase with 96 ns.
The specified times are based on a PER_DIV output is 10.368. Refer to the clock divider overview

36.4 PCM INTERFACE TIMING DIAGRAM

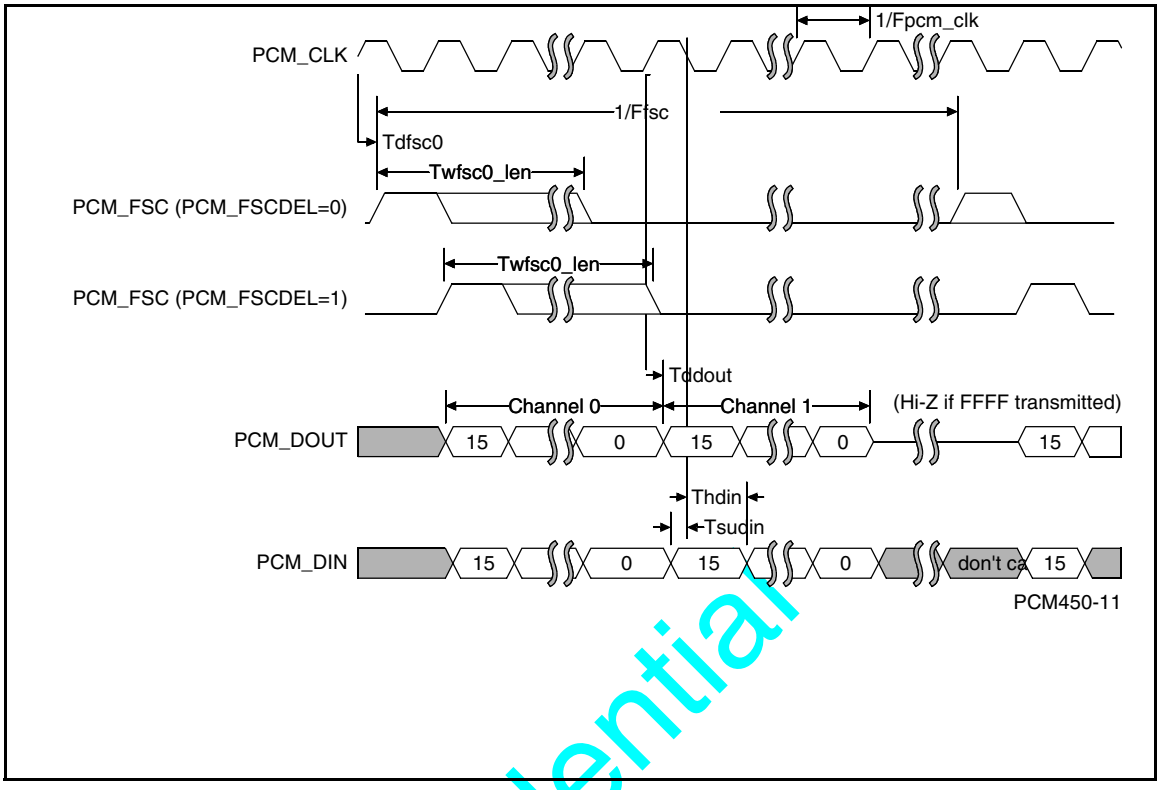

Figure 115 PCM interface timing master mode

Table 322: PCM bus timing master mode (Capacitive load is 30 pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Ffsc	PCM_FSC Frequency	DSP_MAIN_SYNC1_REG [PCM_SYNC] determines frequency	**8**		**32**	**kHz**
Fpcm_clk	PCM_CLK frequency	CLK_CODEC_REG [CLK_PCM_SEL] Determines frequency	**1.152**		**4.608**	**MHz**
Twfsc_len1	PCM_FSC duration	PCM_FSCLEN = 00		**1**		**bits**
Twfsc_len8	PCM_FSC duration	PCM_FSCLEN = 01		**8**		**bits**
Twfsc_len16	PCM_FSC duration	PCM_FSCLEN = 10		**16**		**bits**
Twfsc_len32	PCM_FSC duration	PCM_FSCLEN = 11		**32**		**bits**
Tdfsc	PCM_CLK to PCM_FSC delay				**20**	**ns**
Tddout	PCM_CLK to PCM_DOUT delay				**20**	**ns**
Tsudin	PCM_DIN to PCM_CLK setup time		**20**			**ns**
Thddin	PCM_DIN to PCM_CLK hold time		**20**			**ns**

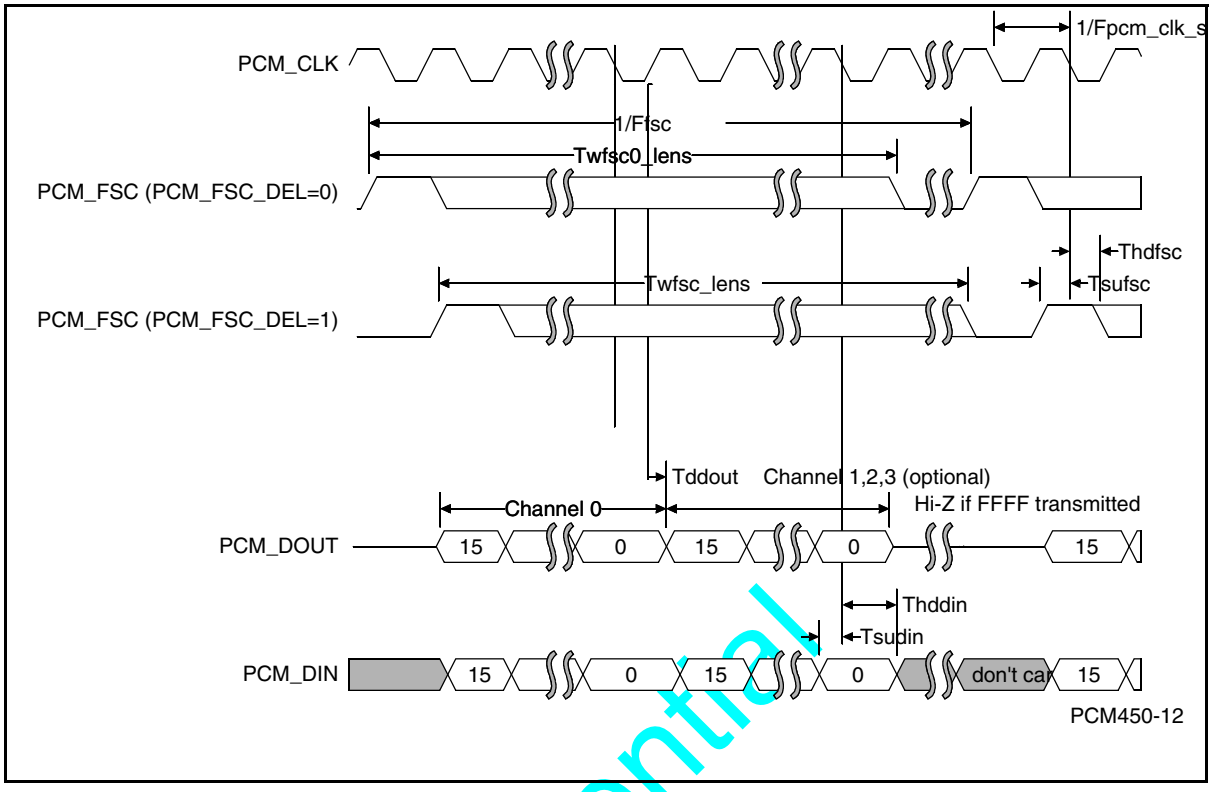

Figure 116 PCM interface timing slave mode

Table 323: PCM bus timing slave mode (capacitive load is 30 pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Ffsc_s	PCM_FSC frequency			**8**		**kHz**
Fpcm_clk_s	PCM_CLK frequency		**256**		**4096**	**kHz**
Twfsc_lens	PCM_FSC duration	**(Note 130)**	**1**			**bits**
Tddout	PCM_CLK to PCM_DOUT delay				**20**	**ns**
Tsufsc	PCM_FSC to PCM_CLK setup time		**20**			**ns**
Thdfsc	PCM_FSC to PCM_CLK hold time.		**20**			**ns**
Tsudin	PCM_DIN to PCM_CLK setup time		**20**			**ns**
Thddin	PCM_DIN to PCM_CLK hold time		**20**			**ns**

Note 130:PCM_FSC must be low for at least 1 PCM_CLK cycle

36.5 SPI BUS TIMING DIAGRAM

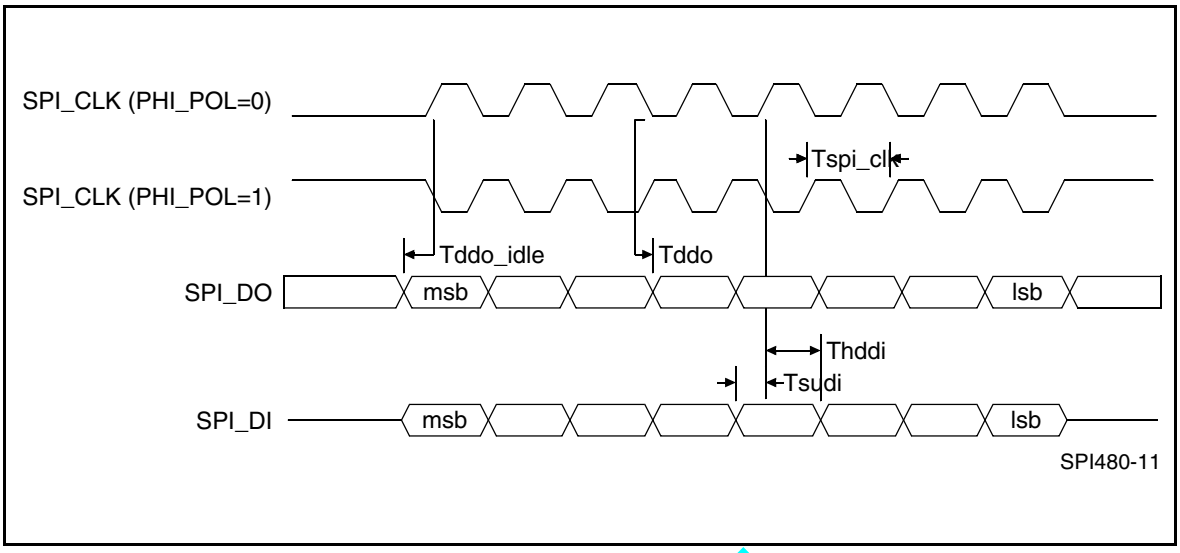

Figure 117 SPI timing

Table 324: SPI bus timing (capacitive load is 30 pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tspiclk	SPI _CLK cycle time	DIV2_CLK/ PER20_DIV = 41.476 MHz			**20.736**	**MHz**
Tddo_m	Delay time SPI_CLK master active edge to SPI_DO		**-5**		**5**	**ns**
Tddo_s	Delay time SPI_CLK slave active edge to SPI_DO		**0**		**10**	**ns**
Tddo_idle	Delay time SPI_CLK master active edge to first SPI_DO	SPI_PHA=0	**(1/2 * Tspiclk) -10**			**ns**
Tsudi_m	Setup time SPI_DI to SPI_CLK master		**10**			**ns**
Thddi_m	Hold time SPI_CLK to SPI_DI		**0**			**ns**
Tsudi_s	Setup time SPI_DI to SPI_CLK master		**5**			**ns**
Thddi_s	Hold time SPI_CLK to SPI_DI		**5**			**ns**

37.0 Package and KGD information

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37.1 MOISTURE SENSITIVITY LEVEL (MSL)

The MSL is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH. before the solder reflow process.

MSL Level	Floor Life Time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30°C/85%RH

37.2 SOLDERING INFORMATION

Refer to the JEDEC standard J-STD-020 for relevant soldering information.
This document can be downloaded from http://www.jedec.org

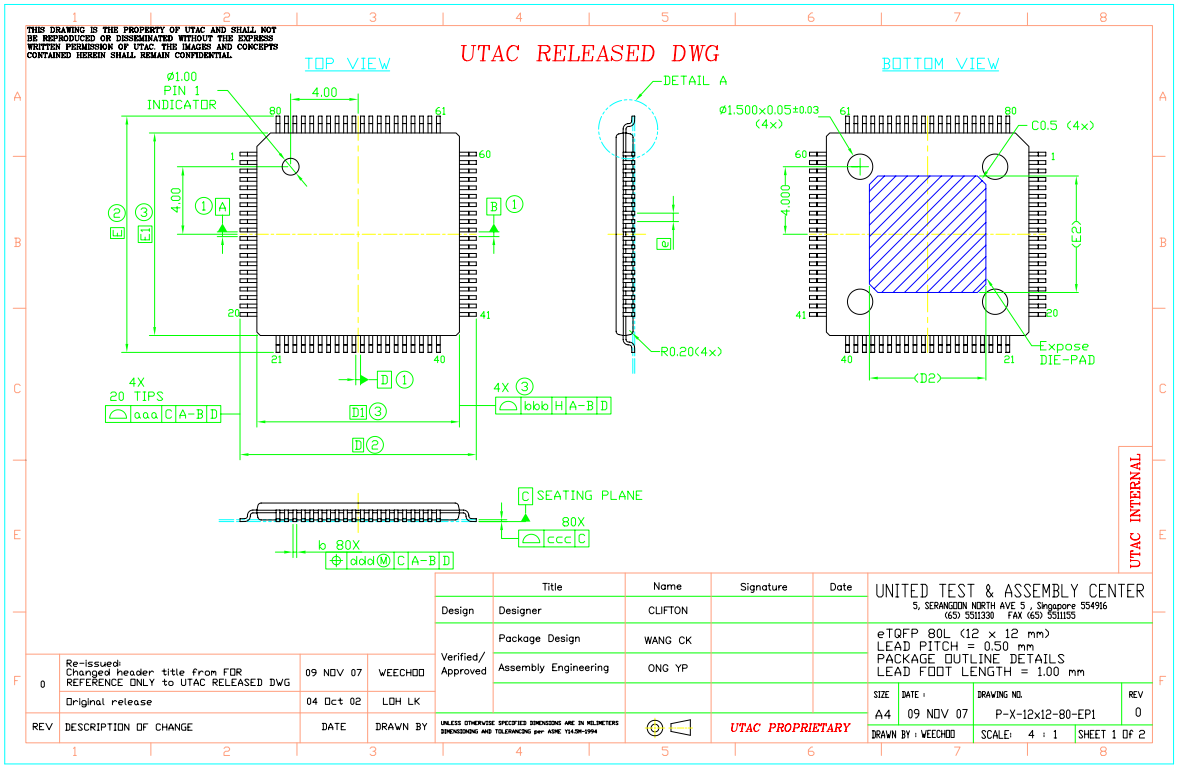
The eTQFP-80 and eLQFP-‘00 package is qualified to MSL 3.

37.3 KGD STORAGE INFORMATION

To be defined.

37.4 PACKAGE OUTLINES

see Figure 118 and see Figure 119



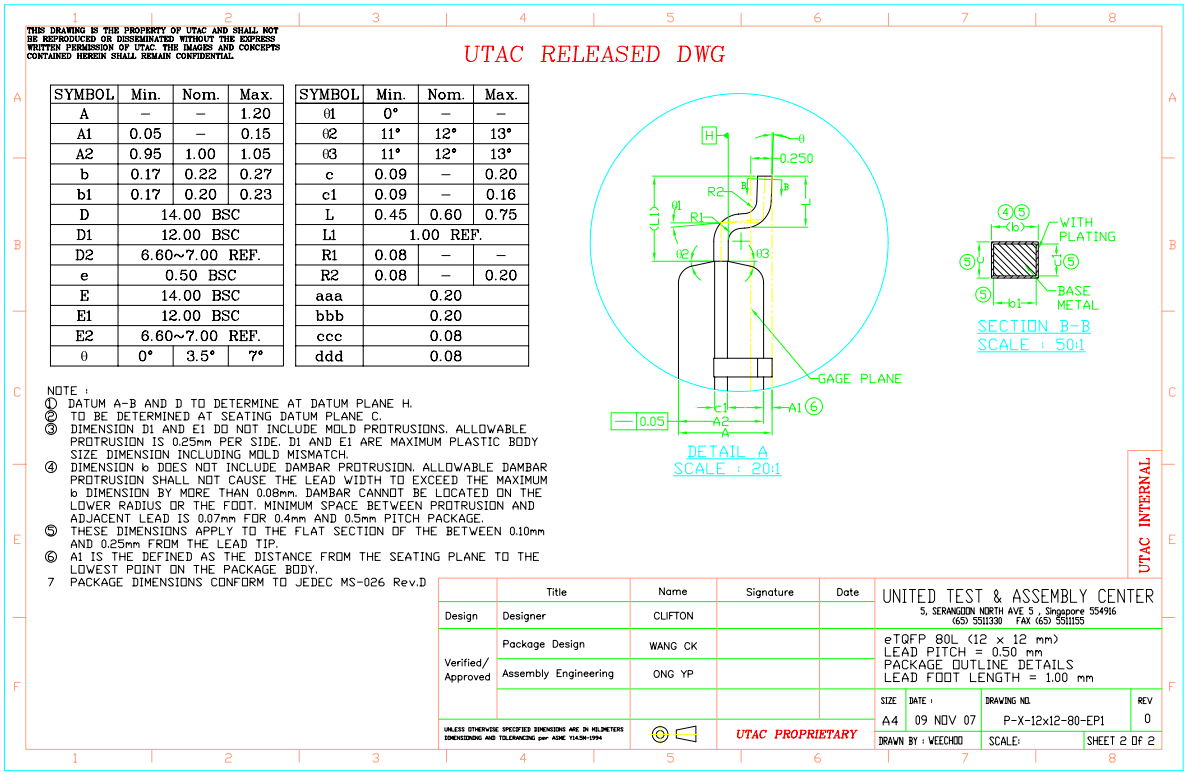
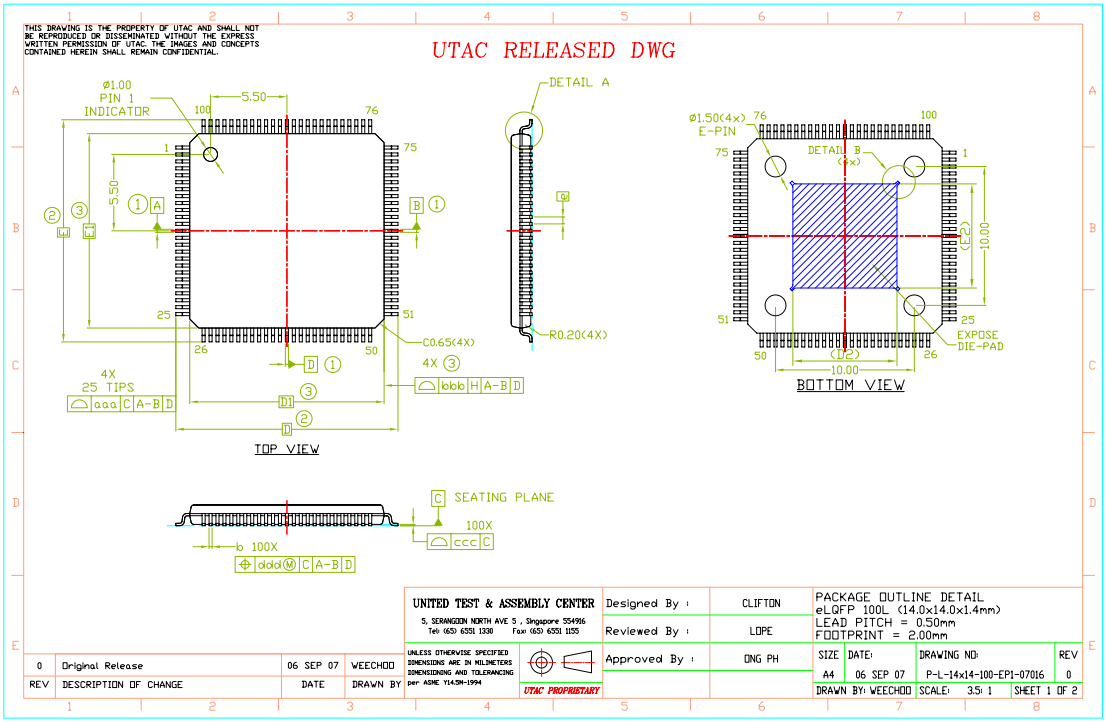
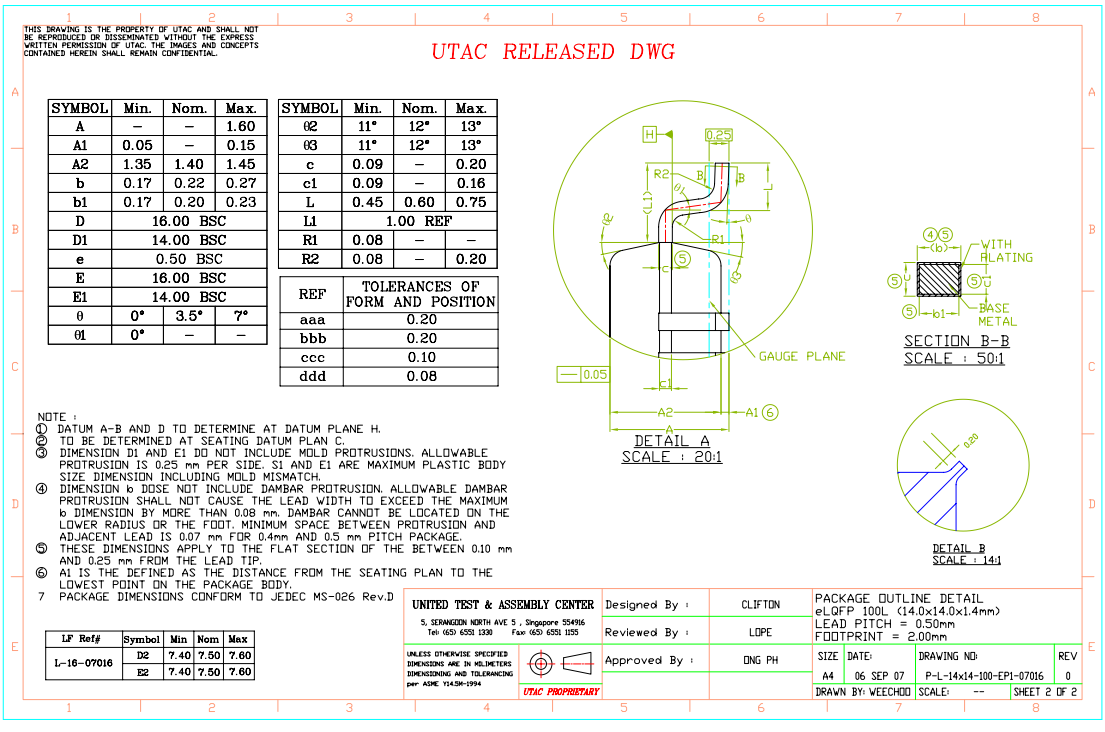


Figure 118 80 Pins e-TQFP Package Outline Drawings





SYMBOL	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
θ	0°	3.5°	7°
θ1	0°	–	–

SYMBOL	Min.	Nom.	Max.
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	–	0.20
c1	0.09	–	0.16
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	–	–
R2	0.08	–	0.20

REF	TOLERANCES OF FORM AND POSITION
aaa	0.20
bbb	0.20
ccc	0.10
ddd	0.08

LF Ref#	Symbol	Min	Nom	Max
L-16-07016	D2	7.40	7.50	7.60
	E2	7.40	7.50	7.60

Figure 119 100 Pins e-LQFP Package Outline Drawings

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Datasheet Status	Product Status	Definition
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No Identification Noted	Full production	This data sheet contains final specifications. SiTel Semiconductor BV reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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