

Section 15: SEMICELL[®] Power Semiconductor Chips

The following tables contain our standard types. Other types or selections are available on special request. Please contact your SEMIKRON office.

SEMICELL[®] Rectifier Diode Chips

Types  SKN ³⁾  SKR ⁴⁾	$\frac{V_{RRM}}{100}$ V	V_{RSM}, V_{RRM} 1) V	I_{FAV} max. A	at T_{case} (T_{amb}) °C	R_{thjc} (R_{thja}) °C/W	I_{FSM} 10 ms T_{vjmax} A	V_F $T_{vj} = 25^\circ C$ V	at I_F A	$V_{(TO)}$ V	r_T T_{vjmax} mΩ	T_{vjmax} 6) °C	Fig.	a mm
SKN-SW 2,5/..		200 ... 1600	1,3	(45)	(80)	50	1,6	10	0,85	90	150	1	2,5
SKN-SW 2,5/..		200 ... 800	1,4	(45)	(80)	100	1,3	10	0,85	50	150	1	2,5
SKN-SW 3,5/..		200 ... 1600	2,5	(45)	(40)	150	1,2	10	0,85	30	150	1	3,5
SKN-SW 5 /..		200 ... 1600	25	100	2	320	1,55	60	0,85	11	150	1	5
SKN-TABL 8H/..		200 ... 1600	50	100	1,1	640	1,8	150	0,85	8	180	2	8
SKN-TABL 9H/..		200 ... 1600	95	100	0,55	1000	1,5	200	0,85	3	180	2	9
SKN-TABL 11H/..		200 ... 1600	125	100	0,45	1500	1,55	400	0,85	1,8	180	2	11
SKN-TABL 8,3 QU/..		200 ... 1600	45	86	0,6	600	1,95	250	0,85	5	180		8,3
SKN-TABL 11,3 QU/..		200 ... 1600	100	85	0,35	2000	1,35	300	0,85	1,3	180		11,3
SKN-TABL 11RD/..		200 ... 1600	125	100	0,45	1500	1,55	400	0,85	1,8	180	3	11
SKN-TABL 13RD/..		200 ... 1600	160	100	0,35	2000	1,5	500	0,85	1,3	180	3	13,5
SKN-TABL 18RD/..		200 ... 1600	320	100	0,20	5000	1,4	750	0,85	0,6	180	3	19
SKN-TABL 23RD/..		200 ... 1600	420	100	0,16	8000	1,35	1000	0,85	1,45	180	3	24
SKR-TABL 4,2QU/.. ^{5,6)}		800 ... 1800	25	80	1,6	350	1,1	25	0,8	13	150	8	4,2
SKR-TABL 5,6QU/.. ^{5,6)}		800 ... 1800	35	80	1,2	750	1,1	35	0,8	11	150	8	5,6
SKR-TABL 6,2QU/.. ^{5,6)}		800 ... 1800	40	80	1,1	900	1,2	50	0,8	8,5	150	8	6,2
SKR-TABL 7,0QU/.. ^{5,6)}		800 ... 1800	75	80	0,7	1150	1,15	75	0,8	7	150	8	7,0
SKR-TABL 8,9QU/.. ^{5,6)}		800 ... 1800	90	80	0,5	1700	1,2	125	0,8	4	150	8	8,9
SKR-GSW18,2QU/.. ²⁾		800 ... 1800	250	80	0,18	6000	1,2	500	0,8	1	150	7	18,2

SEMICELL[®] Fast Rectifier Diode Chips

Types ¹⁾  SKN ...	V_{RSM}, V_{RRM} 1) V	I_{FAV} max. A	at T_{case} (T_{amb}) °C	R_{thjc} (R_{thja}) °C/W	I_{FSM} 10 ms T_{vjmax} A	V_F $T_{vj} = 25^\circ C$ V	at I_F A	$V_{(TO)}$ V	r_T T_{vjmax} mΩ	t_{rr} 25 °C μs	T_{vjmax} 6) °C	Fig.	a mm
SW 2,5 F/..	100 ... 800	1,2	(45)	(60)	60	1,5	10	1,0	50	0,45	130	1	2,5
SW 3,5 F/..	100 ... 800	2,0	(45)	(40)	200	1,25	10	1,0	20	0,45	130	1	3,5
SW 5 F/..	100 ... 1200	21	100	1,2	310	2,15	50	1,3	12	0,25	150	1	5
TABL 8 RDF	200 ... 1000	52	100	0,5	940	1,8	50	1,2	4	0,20	150	3	9
TABL11 RDF	200 ... 1500	60	100	0,5	1200	1,75	150	1,0	4	0,5	150	3	11
TABL14 RDF 1	600 ... 1500	140	100	0,2	2100	1,80	300	1,1	2	0,8	150	3	14
TABL14 RDF 2	600 ... 1200	135	100	0,2	2100	1,95	300	1,1	2,3	0,5	150	3	14
TABL18 RDM	200 ... 1500	170	85	0,2	3000	1,3	500	0,9	0,6	2	125	3	18

Remarks

¹⁾ Available selections for $V_{RRM} \geq 800$ V ... 1000 V; e.g. SKR-TABL 4,2 QU/08...10 ≥ 1200 V ... 1400 V; e.g. SKR-TABL 4,2 QU/12...14 ≥ 1600 V ... 1800 V; e.g. SKR-TABL 4,2 QU/16...18

²⁾ GSW = glass passivated sandwich: Molybdenum / Siliconchip/Molybdenum

³⁾ SKN-TABL = silicone passivated silicon diode chip, Mesa edge, Top = cathode (solderable); Bottom = anode (solderable)

⁴⁾ SKR-TABL = Glass passivated silicon diode chip; Bottom = cathode Mesa edge, Top = anode (solderable), Bottom = cathode (solderable)

⁵⁾ Metallisation of Version "B": Top = anode is bondable AL-contact; bondable area = (a - 1,4) x (a - 1,4); add suffix "B" (on request); I_{FSM} depends on number of bonds

⁶⁾ Soldering temperature = $255 \pm 5^\circ C$

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SEMICELL® Ultrafast Epitaxial Rectifier Diode Chips

Types 	V_{RSM}, V_{RRM} V	I_{FAV} max. A	at		I_{FSM} T_{vjmax} A	V_F $T_{vj} = 25\text{ }^{\circ}\text{C}$ V	at I_F A	$V_{(TO)}$ T_{vjmax} mΩ	r_T 25 °C ns	t_{rr} 25 °C ns	T_{vjmax} 8) °C	Fig.	a mm
			T_{case} °C	R_{thjc} °C/W									
SKCD 47E..B ⁹⁾	50 ... 400	40	100	0,85	700	1,6	120	0,8	6,5	60	150	4 a	7
SKR-Tabl.13.3QE..	50 ... 300	200	85	0,22	2800	1,55	500	0,75	1,5	100	150	4 b	13,3

SEMICELL® Thyristor Chips

Types 本	1)		2) 3) 4)		I _{TAV} at T _{case} = 85 °C		I _{TSM} at 10 ms		V _T at T _{vj} = 25 °C		V _{T(TO)}		r _T		(dv/dt) _{cr} 6)	(di/dt) _{cr}	V _{GT}	I _{GT}	V _{GD}	I _{GD}
	max		R _{thjc} °C/W	T _{vjmax} A	I _T		T _{vjmax}		T _{vjmax}		T _{vjmax}		25 °C		T _{vjmax}		25 °C		T _{vjmax}	
	V				V	A	V	mΩ	V	μs	A/μs	V	mA	V	mA					
SKT-GSW 5,6Q1/..	16	0,9	300	2,4	75	1,0	20	1000	125	3	100	0,25	3							
SKT-GSW 7 Q1/..	25	0,95	400	1,8	75	1,0	10	1000	125	3	100	0,25	3							
SKT-GSW 8,9Q1/..	45	0,60	1000	1,8	120	1,1	5	1000	125	3	150	0,25	5							
SKT-GSW 10,3Q1/..	50	0,60	1250	1,65	200	0,9	3,5	1000	100	3	150	0,25	6							
SKT-GSW 12,4Q1/..	90	0,30	1750	1,65	300	0,9	2	1000	100	3	150	0,25	6							
SKT-GSW 18,2QU/..	160	0,18	4000	1,80	500	0,85	1,5	1000	100	3	150	0,25	10							
SKT-TABL 5,6QU/.. 5)	16	0,9	370	2,4	75	1,0	20	1000	50	3	100	0,25	3							
SKT-TABL 7 QU/.. 5)	24	0,9	450	1,8	75	1,0	10	1000	50	3	100	0,25	3							
SKT-TABL 8,9QU/.. 5)	45	0,6	1050	1,8	120	1,1	5	1000	50	3	150	0,25	5							
SKT-TABL 8,9QU/.. ZG 7, 5)	45	0,6	1050	1,8	120	1,1	5	1000	50	3	150	0,25	5							
SKT-TABL 10,3QU/..	55	0,6	1250	1,65	200	0,9	3,5	1000	100	3	150	0,25	6							
SKT-TABL 10,3QU/.. ZG 7)	55	0,6	1250	1,65	200	0,9	3,5	1000	100	3	150	0,25	6							
SKT-TABL 12,4QU/..	95	0,3	1750	1,65	300	0,9	2	1000	100	3	150	0,25	6							
SKT-TABL 12,4QU/.. ZG 7)	95	0,3	1750	1,65	300	0,9	2	1000	100	3	150	0,25	6							
SKT-TABL C 24 N/..	160	0,18	3750	1,75	500	1	1,5	1000	125	3	200	0,25	8							
SKT-TABL C 30 N/..	300	0,11	7000	1,45	800	0,9	0,6	1000	125	3	200	0,25	8							

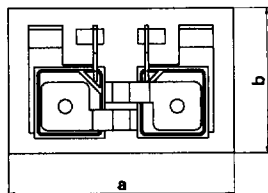
Remarks:

- Available selections for V_{DRM}, V_{RRM} : $\geq 800\text{ V} \dots 1000\text{ V}$; e.g. SKT-GSW 5,6 Q1/08
 $\geq 1200\text{ V} \dots 1600\text{ V}$; e.g. SKT-GSW 5,6 Q1/12..16
 ≥ 1600 ; e.g. SKT-GSW 5,6 Q1/16
- GSW = glass passivated sandwich: Molybdenum / Siliconchip/Molybdenum
- TABL = glass passivated silicon chip, Metallisation: Bottom = anode (solderable), Top = cathode (solderable) $\rightarrow$ 5)
- I_R, I_D ($V_R = V_{RRM}, V_D = V_{DRM}, T_j = 25^\circ C$) $\leq 0,3\text{ mA}$
 I_R, I_D ($V_R = V_{RRM}, V_D = V_{DRM}, T_j = 130^\circ C$) $\leq 8\text{ mA}$
- Metallisation of version "B" (add suffix B): Top = cath., bondable, on request
- $(dv/dt)_{cr}$ as per AQL 2,5
- ZG = Central gate (all others have "edge gate" see Fig. 5 and Fig. 6)
- Soldering temperature = $255 \pm 5^\circ C$
- Metallization of version "S": Top = anode is solderable contact (solderable area = $4,8\text{ mm}^2$) add suffix "S" (on request)

Fig. 4c

GMCL04C

GMCL04C



SEMICELL® Chips on Ceramic Substrate

Custom Designs on request

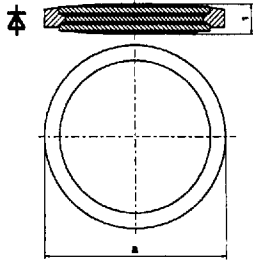
e.g. 2 antiparallel thyristor chips on ceramic substrate (in W1C circuit) $\rightarrow$ Fig. 4c

$I_{RMS} = 25 \dots 100\text{ A} / V_{DRM} = 800 \dots 1600\text{ V}$

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Fig. 1

GMCL01

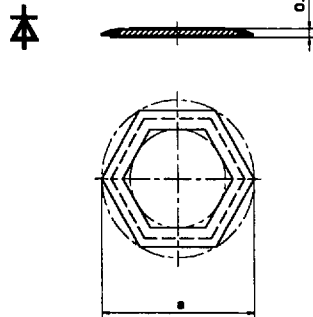


Silicone passivated

SKN-SW../

Fig. 2

GMCL02

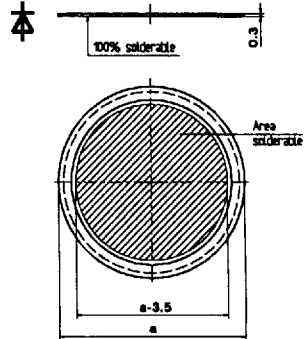


Silicone passivated

SKN-TABL..HEX

Fig. 3

GMCL03

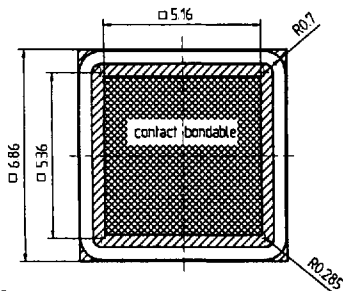


Silicone passivated

SKN-TABL..RD

Fig. 4 a

CD47E405



d = 0,6 mm

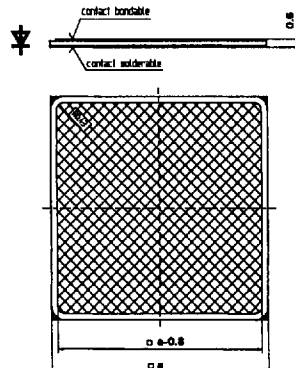
Glass passivated

SKCD 47E..B

Dimensions in mm

Fig. 4 b

GMCL04

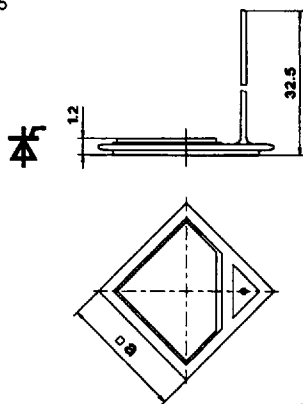


Glass passivated

SKR-TABL..EPI

Fig. 5

GMCL05

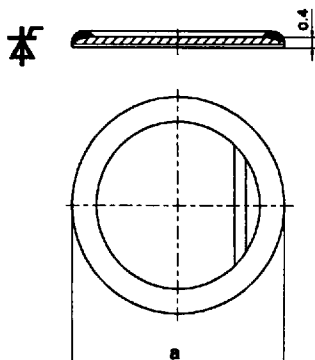


Glass passivated

SKT-GSW..QU/

Fig. 6

GMCL06

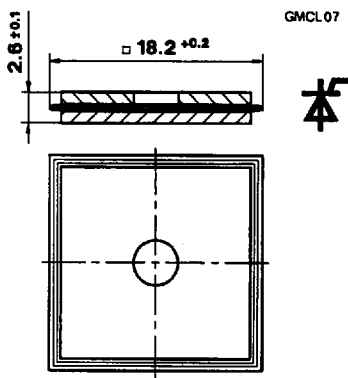


Silicone passivated

SKT-TABLC..RD

Fig. 7

GMCL07

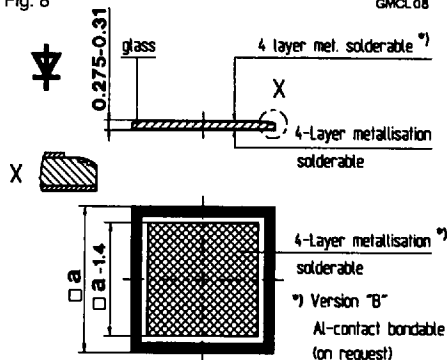


Glass passivated

SKR-GSW 18.2 QU

Fig. 8

GMCL08

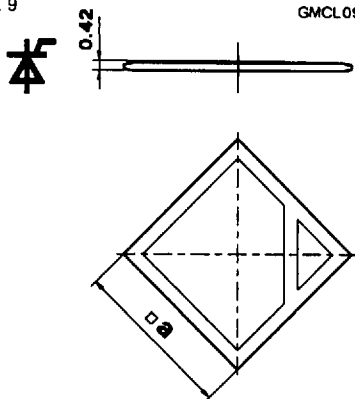


Glass passivated

SKR-TABL..QU/..(B)

Fig. 9

GMCL09

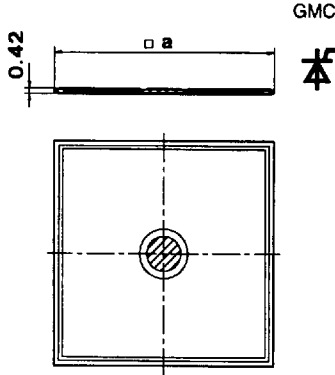


Glass passivated

SKT-TABL..QU/

Fig. 10

GMCL10



Glass passivated

SKT-TABL../. ZG

Dimensions in mm

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