PROGRAMMABLE 27-BIT SERIAL-TO-PARALLEL RECEIVER

FEATURES

- **Serial Interface Technology**
- **Compatible With FlatLink™ 3G Transmitters (E.g., SN65LVDS305 or SN65LVDS307)**
- **Supports Video Interfaces up to 24-Bit RGB Data and 3 Control Bits Received Over One SubLVDS Differential Data Line**
- **SubLVDS Differential Voltage Levels**
- **Up to 405-Mbps Data Throughput**
- **Three Operating Modes to Conserve Power**
  - **Active mode QVGA: 17 mW**
  - **Typical Shutdown: 0.7 μW**
  - **Typical Standby Mode: 67 μW Typical**
- **ESD Rating > 4 kV (HBM)**
- **Pixel-Clock Range of 4 MHz–15 MHz**
- **Failsafe on All CMOS Inputs**
- **Packaged in 4-mm × 4-mm MicroStar Junior™μBGA® With 0,5-mm Ball Pitch**
- **Very Low EMI**

APPLICATIONS

- **Small Low-Emission Interface Between Graphics Controller and LCD Display**
- **Mobile Phones and Smart Phones**
- **Portable Multimedia Players**

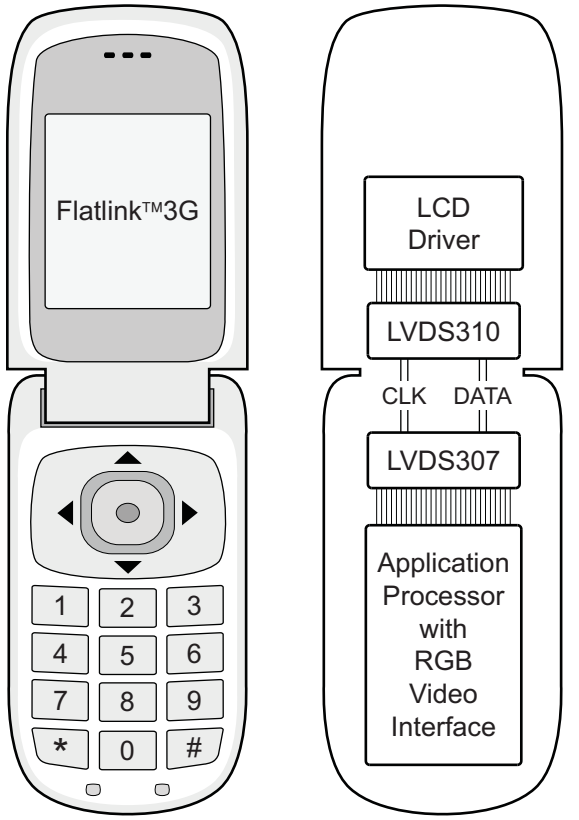
DESCRIPTION

The SN65LVDS310 receiver deserializes FlatLink 3G-compliant serial input data to 27 parallel data outputs. The SN65LVDS310 receiver contains one shift register to load 30 bits from one serial input and latches the 24 pixel bits and 3 control bits out to the parallel CMOS outputs after checking the parity bit. If a parity error is detected, the data output bus disregards the newly received pixel. Instead, the last data word is held on the output bus for another clock cycle.

The serial data and clock are received via sub-low-voltage differential signalling (SubLVDS) lines. The SN65LVDS310 supports three operating power modes (shutdown, standby, and active) to conserve power.

When receiving, the PLL locks to the incoming clock, CLK, and generates an internal high-speed clock at the line rate of the data lines. The data is serially loaded into a shift register using the internal high-speed clock. The deserialized data is presented on the parallel output bus with a recreation of the pixel clock, PCLK, generated from the internal high-speed clock. If no input CLK signal is present, the output bus is held static with PCLK and DE held low, while all other parallel outputs are pulled high.

The F/S conrol input selects between a slow CMOS bus output rise time for best EMI and power consumption and a fast CMOS output for increased speed or higher-load designs.



M0056-04

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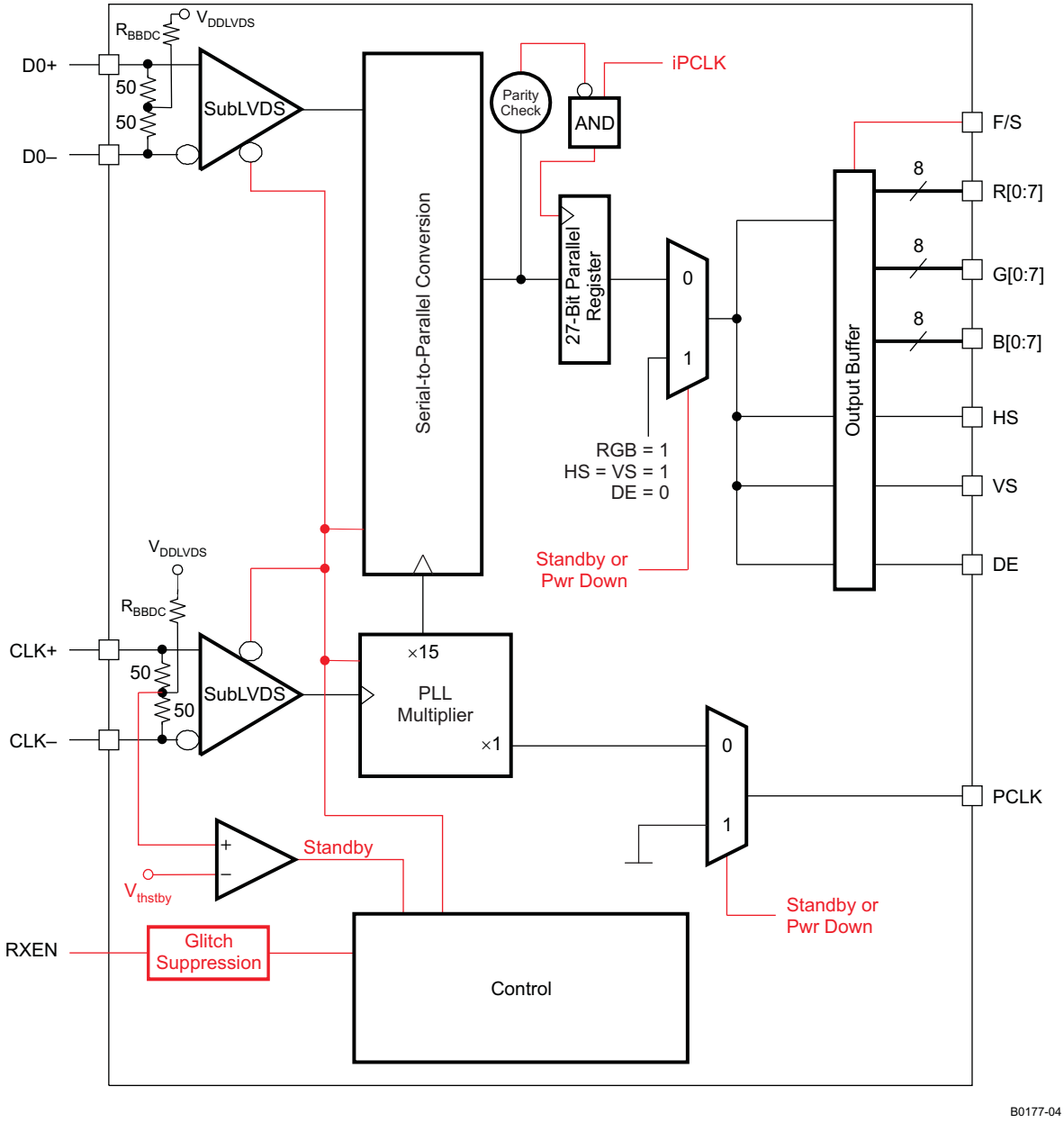
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The RXEN input can be used to put the SN65LVDS310 in a shutdown mode. The SN65LVDS310 enters an active standby mode if the common mode voltage of the CLK input becomes shifted to VDD_{LVDS} (e.g., transmitter releases CLK output into high-impedance). This minimizes power consumption without the need of switching an external control pin. The SN65LVDS310 is characterized for operation over ambient air temperatures of –40°C to 85°C. All CMOS and SubLVDS signals are 2-V tolerant with VDD = 0 V. This feature allows powering up I/Os before VDD is stabilized.

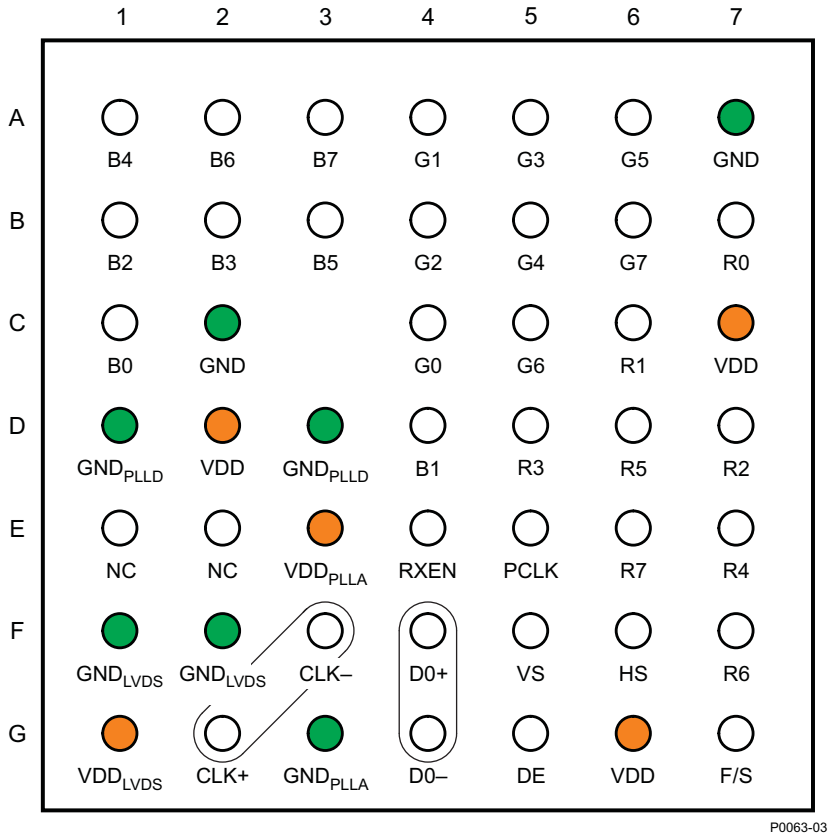
FUNCTIONAL BLOCK DIAGRAM



B0177-04

PINOUT – TOP VIEW

ZQC PACKAGE
(TOP VIEW)



P0063-03

PINOUT – TOP VIEW (continued)

Table 1. Numeric Terminal List

TERMINAL	SIGNAL	TERMINAL	SIGNAL	TERMINAL	SIGNAL	TERMINAL	SIGNAL
A1	B4	**B7**	R0	**D6**	R5	**F5**	VS
A2	B6	**C1**	B0	**D7**	R2	**F6**	HS
A3	B7	**C2**	GND	**E1**	NC	**F7**	R6
A4	G1	**C3**	–	**E2**	NC	**G1**	VDD_{LVDS}
A5	G3	**C4**	G0	**E3**	VDD_{PLLA}	**G2**	CLK+
A6	G5	**C5**	G6	**E4**	RXEN	**G3**	GND_{PLLA}
A7	GND	**C6**	R1	**E5**	PCLK	**G4**	D0–
B1	B2	**C7**	VDD	**E6**	R7	**G5**	DE
B2	B3	**D1**	GND_{PLLD}	**E7**	R4	**G6**	VDD
B3	B5	**D2**	VDD	**F1**	GND_{LVDS}	**G7**	F/S
B4	G2	**D3**	GND_{PLLD}	**F2**	GND_{LVDS}		
B5	G4	**D4**	B1	**F3**	CLK–		
B6	G7	**D5**	R3	**F4**	D0+		

Table 2. TERMINAL FUNCTIONS

NAME	I/O	DESCRIPTION
D0+, D0–	SubLVDS in	SubLVDS data link
CLK+, CLK–		SubLVDS input pixel clock; polarity is fixed.
R0–R7	CMOS out	Red-pixel data (8)
G0–G7		Green-pixel data (8)
B0–B7		Blue-pixel data (8)
HS		Horizontal sync
VS		Vertical sync
DE		Data enable
PCLK		Output pixel clock (rising clock polarity)
RXEN	CMOS In	Disables the CMOS drivers and turns off the PLL, putting device in shutdown mode 1 – Receiver enabled 0 – Receiver disabled (shutdown) Note: The RXEN input incorporates glitch suppression logic to avoid unwanted switching. The input must be pulled low for longer than 10 µs continuously to force the receiver to enter shutdown. The input must be pulled high for at least 10 µs continuously to activate the receiver. An input pulse shorter than 5 µs is interpreted as a glitch and becomes ignored. At power up, the receiver is enabled immediately if RXEN = H and disabled if RXEN = L.
F/S		CMOS bus rise time select 1 – fast output rise time 0 – slow output rise time
VDD	Power supply	Supply voltage
GND		Supply ground
VDD_{LVDS}		SubLVDS I/O supply voltage
GND_{LVDS}		SubLVDS ground
VDD_{PLLA}		PLL analog supply voltage
GND_{PLLA}		PLL analog GND
VDD_{PLLD}		PLL digital supply voltage
GND_{PLLD}		PLL digital GND

FUNCTIONAL DESCRIPTION

DESERIALIZATION MODE

The SN65LVDS310 receives payload data over a single SubLVDS data pair D0. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to shift in the data payload on D0 and deserialize the data. Figure 1 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and the data payload with the pixel clock is presented on the output bus. The reserved bits and parity bit are not output. The PLL can lock to a clock that is in the range of 4 MHz through 15 MHz.



Figure 1. Data and Clock Input

POWER-DOWN MODES

The SN65LVDS310 receiver has two power-down modes to facilitate efficient power management.

Shutdown Mode

A low input signal on the RXEN pin puts the SN65LVDS310 into shutdown mode. This turns off most of the receiver circuitry, including the SubLVDS receivers, PLL, and deserializers. The SubLVDS differential-input resistance remains 100 Ω, and any input signal is ignored. All outputs hold a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

The current draw in shutdown mode is nearly zero if the SubLVDS inputs are left open or pulled high.

Standby Mode

The SN65LVDS310 enters the standby mode when the SN65LVDS310 is not in shutdown mode but the SubLVDS clock-input common-mode voltage is above 0.9 × VDD_{LVDS}. The CLK input incorporates pullup circuitry. This circuit shifts the SubLVDS clock-input common-mode voltage to VDD_{LVDS} in the absence of an input signal. All circuitry except the SubLVDS clock-input standby monitor is shut down. The SN65LVDS310 also enters the standby mode when the input clock frequency on the CLK input is less than 500 kHz. The SubLVDS input resistance remains 100 Ω, and any input signal on the data inputs D0+ and D0– is ignored. All outputs hold a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

The current drawn in standby mode is very low.

ACTIVE MODES

A high input signal on RXEN combined with a CLK input signal switching faster than 3 MHz and V_{ICM} smaller than 1.3 V forces the SN65LVDS310 into the active mode. Current consumption in the active mode depends on operating frequency and the number of data transitions in the data payload. CLK-input frequencies between 3 MHz and 4 MHz activate the device, but proper PLL functionality is not assured.

Acquire Mode (PLL Approaches Lock)

When the SN65LVDS310 is enabled and a SubLVDS clock input is present, the PLL pursues lock to the input clock. While the PLL pursues lock, the output data bus holds a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

FUNCTIONAL DESCRIPTION (continued)

For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is higher than 3 MHz but lower than f_{PCLK}(MIN), the SN65LVDS310 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into the active receive mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

Receive Mode

After the PLL achieves lock, the device enters the normal receive mode. The output data bus presents the deserialized data. The PCLK output pin outputs the recovered pixel clock.

PARITY ERROR DETECTION AND HANDLING

The SN65LVDS310 receiver performs error checking on the basis of a parity bit that is transmitted across the LVDS interface from the transmitting device. Once the SN65LVDS310 detects the presence of the clock and the PLL has locked onto PCLK, then the parity is checked. Parity-error detection ensures detection of all single-bit errors in one pixel and 50% of all multibit errors.

The parity bit covers the 27-bit data payload consisting of 24 bits of pixel data plus VS, HS, and DE. Odd-parity bit signalling is used. If the sum of the 27 data bits and the parity bit is an odd number, the receive data are assumed to be valid. If the sum is an even number, parity error is declared.

If a parity error is detected, then the data on that PCLK cycle is not output. Instead, the last valid data from a previous PCLK cycle is repeated on the output bus. This is to prevent any bit error that occurs on the LVDS link from causing perturbations in VS, HS, or DE that might be visually disruptive to a display.

The reserved bits are not covered in the parity calculations.

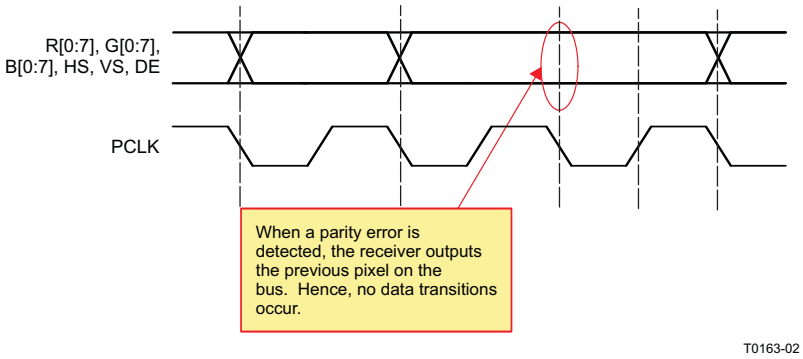


Figure 2. Output Response When Parity Error Is Detected

FUNCTIONAL DESCRIPTION (continued)

STATUS-DETECT AND OPERATING-MODES FLOW DIAGRAM

The SN65LVDS310 switches between the power-saving and active modes in the following way:

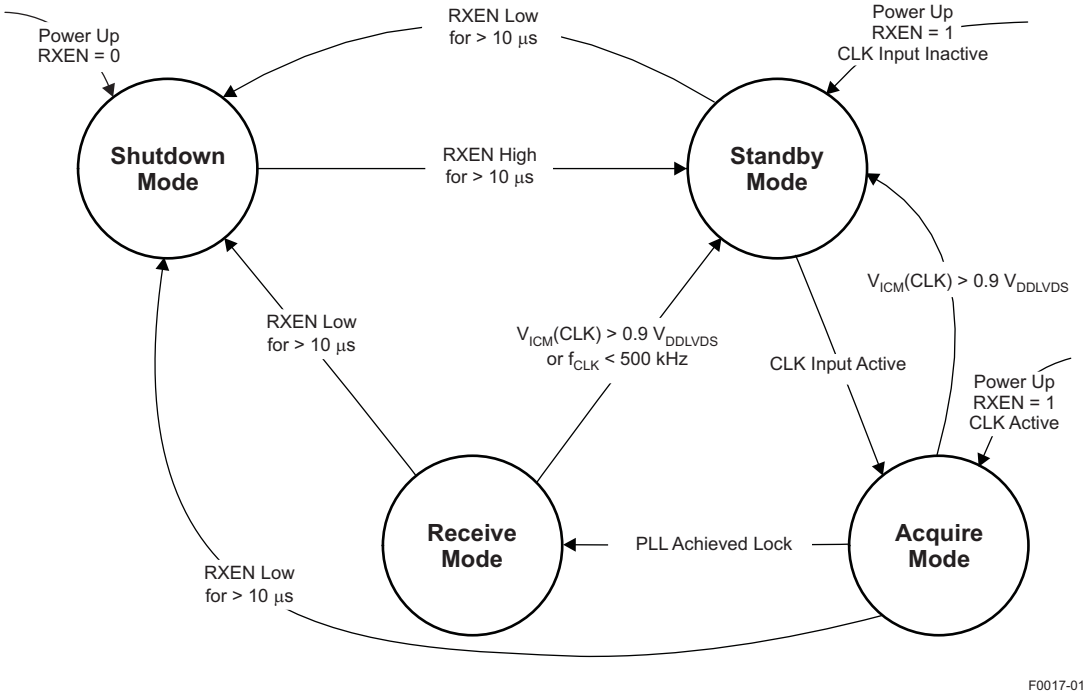


Figure 3. Operating Modes Flow Diagram

Table 3. Status Detect and Operating Modes Descriptions

MODE	CHARACTERISTICS	CONDITIONS
Shutdown mode	Least amount of power consumption (most circuitry turned off); all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low	RXEN is set low for longer than 10 µs. (1) (2)
Standby mode	Low power consumption (standby monitor circuit active; PLL is shut down to conserve power); All outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low	RXEN is high for longer than 10 µs and CLK inputs are common-mode, $V_{ICM(CLK)}$ is above 0.9 × VDD_{LVDS}, or CLK inputs are floating (2)
Acquire mode	PLL pursues lock; all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low	RXEN is high; CLK input monitor detected clock input common mode and woke up receiver from standby mode.
Receive mode	Data transfer (normal operation); receiver deserializes data and provides data on parallel output	RXEN is high and PLL is locked to incoming clock.

(1) In shutdown mode, all SN65LVDS310 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.

(2) Leaving CMOS control inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All CMOS inputs must be tied to a valid logic level, V_{IL} or V_{IH}, during shutdown or standby mode. Exceptions are the SubLVDS inputs CLK and D0, which can be left unconnected while not in use.

Table 4. Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → standby	Drive RXEN high to enable receiver.	1. RXEN high > 10 µs 2. Receiver enters standby mode. a. R[0:7] = G[0:7] = B[0:7] = VS = HS remain high and DE = PCLK low b. Receiver activates clock input monitor.
Standby → acquire	Transmitter activity detected	1. CLK input monitor detects clock input activity. 2. Outputs remain static. 3. PLL circuit is enabled.
Acquire → receive	Link is ready to receive data.	1. PLL is active and approaches lock. 2. PLL achieves lock within t_{wakeup}. 3. Input D0 becomes active. 4. First data word is recovered. 5. Parallel output bus turns on switching from a static output pattern to output the first valid data word.
Receive → standby	Receiver requested to enter standby mode by input common-mode voltage V_{ICM} > 0.9 VDD_{LVDS} (e.g., transmitter output clock enters high-impedance state)	1. Transmitter disables outputs within t_{sleep}. 2. RX Input monitor detects V_{ICM} > 0.9 VDD_{LVDS}. 3. R[0:7] = G[0:7] = B[0:7] = VS = HS transition to high and DE = PCLK to low on next falling PLL clock edge. 4. PLL shuts down. 5. Clock activity input monitor remains active.
Receive/standby → shutdown	Turn off receiver.	1. RXEN is pulled low for > t_{pwrdn}. 2. Receiver switches all outputs to the high-impedance state. 3. Most IC circuitry is shut down for least power consumption.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Supply voltage range, VDD(2), VDD_{PLLA}, VDD_{PLLD}, VDD_{LVDS}		–0.3 to 2.175	V
Voltage range at any input or output terminal	When VDD_x > 0 V	–0.5 to 2.175	V
	When VDD_x ≤ 0 V	–0.5 to VDD + 2.175	
Electrostatic discharge	Human body model(3) (all pins)	±4	kV
	Charged-device model(4) (all pins)	±1500	V
	Machine model(5) (all pins)	±200	
Continuous power dissipation		See Dissipation Ratings table	
Ouput current, I_O		±5	mA

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-B
(4) In accordance with JEDEC Standard 22, Test Method C101
(5) In accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
ZQC	Low-K(2)	496 mW	6.21 mW/°C	124 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-2.

DEVICE POWER DISSIPATION

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
P_D	Device power dissipation	VDD_x = 1.8 V, T_A = 25°C, all outputs terminated with 10 pF, f_{CLK} at 4 MHz	16.8		mW
		VDD_x = 1.95 V, T_A = –40°C, all outputs terminated with 10 pF, f_{CLK} at 15 MHz		48.8	

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	TYP	MAX	UNIT
VDD VDD_{PLLA} VDD_{PLLD} VDD_{LVDS}	Supply voltages		1.65	1.8	1.95	V
$VDD_{n(PP)}$	Supply voltage noise magnitude	Test set-up shown in Figure 5; f_{CLK} ≤ 50 MHz; f(noise) = 1 Hz to 2 GHz			100	mV
		f_{CLK} > 50 MHz; f(noise) = 1 Hz to 1 MHz			100	
		f_{CLK} > 50 MHz; f(noise) > 1 MHz			40	
T_A	Operating free-air temperature		–40		85	°C
CLK+ and CLK–						
$f_{CLK±}$	Input pixel clock frequency	See Figure 1	4		15	MHz
		Standby mode(2), see Figure 14			500	kHz
t_{DUTCLK}	CLK input duty cycle		35		65	%
D0+, D0–, CLK+, and CLK–						
$\|V_{ID}\|$	Magnitude of differential input voltage	$\|V_{D0+} – V_{D0–}\|$, $\|V_{CLK+} – V_{CLK–}\|$ during normal operation	70		200	mV
V_{ICM}	Input voltage common-mode range	Receive or acquire mode	0.6		1.2	V
		Standby mode	0.9 VDD_{LVDS}			
ΔV_{ICM}	Input voltage common-mode variation among all SubLVDS inputs	$V_{ICM(n)} – V_{ICM(m)}$ with n = D0 or CLK and m = D0 or CLK	–100		100	mV
ΔV_{ID}	Differential input voltage amplitude variation among all SubLVDS inputs	$V_{ID(n)} – V_{ID(m)}$ with n = D0 or CLK and m = D0 or CLK	–10%		10%	
$t_{r/f}$	Input rise or fall time	RXEN at VDD; see Figure 8			800	ps
$\Delta t_{r/f}$	Input rise or fall time mismatch among all SubLVDS inputs	$t_{r(n)} – t_{r(m)}$ and $t_{f(n)} – t_{f(m)}$ with n = D0 or CLK and m = D0 or CLK	–100		100	ps
RXEN, F/S						
V_{ICMOSH}	High-level input voltage		0.7 VDD		VDD	V
V_{ICMOSL}	Low-level input voltage		0		0.3 VDD	V
t_{inRXEN}	RXEN input pulse duration		10			µs
R[7:0], G[7:0], B[7:0], VS, HS, PCLK						
C_L	Output load capacitance			10		pF

(1) Unused single-ended inputs must be held high or low to prevent them from floating.
(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS310 into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS310. Input frequencies beyond 3 MHz activate the SN65LVDS310. Input frequencies between 500 kHz and 4 MHz are not recommended, and can cause PLL malfunction.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{DD}	RMS supply current	Alternating 1010 test pattern (see Table 7); all CMOS outputs terminated with 10 pF; F/S and RXEN at VDD; V_{IH} = VDD, V_{IL} = 0 V; VDD = VDD_{PLLA} = VDD_{PLLD} = VDD_{LVDS}	f_{PCLK} = 4 MHz		9.8	14	mA
			f_{PCLK} = 6 MHz		11.7	15.9	
			f_{PCLK} = 15 MHz		19.3	25	
		Typical power test pattern (see Table 6); V_{ID} = 70 mV, all CMOS outputs terminated with 10 pF; F/S at GND and RXEN at VDD; V_{IH} = VDD, V_{IL} = 0 V; VDD = VDD_{PLLA} = VDD_{PLLD} = VDD_{LVDS}	f_{PCLK} = 4 MHz		4.7		
			f_{PCLK} = 6 MHz		6		
			f_{PCLK} = 15 MHz		13.2		
		CLK and D inputs are left open; all control inputs held static high or low; All CMOS outputs terminated with 10 pF; V_{IH} = VDD, V_{IL} = 0 V; VDD = VDD_{PLLA} = VDD_{PLLD} = VDD_{LVDS}	Standby mode; RXEN = V_{IH}		15	100	µA
			Shutdown mode; RXEN = V_{IL}		0.4	10	

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.

INPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
D0+, D0–, CLK+, and CLK–						
V_{thstby}	Input voltage common-mode threshold to switch between receive/acquire mode and standby mode	RXEN at VDD	1.3		0.9 VDD_{LVDS}	V
V_{THL}	Low-level differential input voltage threshold	$V_{D0+} - V_{D0-}$, $V_{CLK+} - V_{CLK-}$	–40			mV
V_{THH}	High-level differential input voltage threshold				40	mV
I_{I+}, I_{I-}	Input leakage current	VDD = 1.95 V; $V_{I+} = V_{I-}$; V_I = 0.4 V or V_I = 1.5 V			75	µA
I_{IOFF}	Power-off input current	VDD = GND; V_I = 1.5 V			–75	µA
R_{ID}	Differential input termination resistor value		78	100	122	Ω
C_{IN}	Input capacitance	Measured between input terminal and GND		1		pF
ΔC_{IN}	Input capacitance variation	Within one signal pair			0.2	pF
		Between all signals			1	
R_{BBDC}	Pullup resistor for standby detection		21	30	39	kΩ
RXEN, F/S						
V_{IK}	Input clamp voltage	I_I = –18 mA, VDD = VDD(min)			–1.2	V
I_{ICMOS}	Input current(2)	0 V ≤ VDD ≤ 1.95 V; V_I = GND or V_I = 1.95 V			100	nA
C_{IN}	Input capacitance			2		pF
I_{IH}	High-level input current	V_{IN} = 0.7 VDD	–200		200	nA
I_{IL}	Low-level input current	V_{IN} = 0.3 VDD	–200		200	nA
V_{IH}	High-level input voltage		0.7 VDD		VDD	V
V_{IL}	Low-level input voltage		0		0.3 VDD	V

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.
(2) Do not leave any CMOS input unconnected or floating to minimize leakage currents. Every input must be connected to a valid logic level, V_{IH} or V_{OL}, while power is supplied to VDD.

OUTPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R[0:7], G[0:7], B[0:7], VS, HS, PCLK						
V_{OH}	High-level output current	F/S = L, I_{OH} = –250 µA	0.8 VDD		VDD	V
		F/S = H, I_{OH} = –500 µA				
V_{OL}	Low-level output current	F/S = L, I_{OL} = 250 µA	0		0.2 VDD	V
		F/S = H, I_{OL} = 500 µA				
I_{OH}	High-level output current	F/S = L	–250			µA
		F/S = H	–500			
I_{OL}	Low-level output current	F/S = L			250	µA
		F/S = H			500	

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
D0+, D0–, CLK+, and CLK–							
$t_{r/f}$	Input rise and fall times	RXEN at VDD; see Figure 8				800	ps
$\Delta t_{r/f}$	Input rise or fall time mismatch between all SubLVDS inputs	t_r(n) – tr(m) and t_f(n) – t_f(m) with n = D0 or CLK and m = D0 or CLK		–100		100	ps
R[7:0], G[7:0], B[7:0], VS, HS, PCLK							
$t_{r/f}$	Rise and fall time 20%–80% of VDD (2)	C_L = 10 pF(3); see Figure 7	F/S = L	8		16	ns
			F/S = H	4		8	
t_{OUTP}	PCLK output duty cycle			45%	50%	55%	
t_{OSK}	Output skew between PCLK and R[0:7], G[0:7], B[0:7], HS, VS, and DE	See Figure 7.		–500		500	ps
INPUT-TO-OUTPUT RESPONSE TIME							
$t_{PD(L)}$	Propagation delay time from CLK+ input to PCLK output	RXEN at VDD, V_{IH} = VDD, V_{IL} = GND, C_L = 10 pF, see Figure 12		1.4/f_{PCLK}	1.9/f_{PCLK}	2.5/f_{PCLK}	s
t_{GS}	RXEN glitch suppression pulse duration(4)	V_{IH} = VDD, V_{IL} = GND, RXEN toggles between V_{IL} and V_{IH}; see Figure 13 and Figure 14.				3.8	µs
t_{pwrup}	Enable time from power down (↑RXEN)	Time from RXEN pulled high to data outputs enabled and transmit valid data; see Figure 14.				2	ms
t_{pwrdn}	Disable time from active mode (↓RXEN)	RXEN is pulled low during receive mode; time measurement until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high, DE = PCLK = low and PLL is shut down; see Figure 14.				11	µs
t_{wakeup}	Enable time from standby (↑↓CLK)	RXEN at VDD; device is in standby; time measurement from CLK input starts switching to PCLK and data outputs enabled and transmit valid data; see Figure 15.				2	ms
t_{sleep}	Disable time from active mode (CLK transitions to high-impedance)	RXEN at VDD; device is receiving data; time measurement from CLK input signal stops (input open or input common mode V_{ICM} exceeds threshold voltage V_{thstby}) until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low and PLL is shut down; see Figure 15.				3	µs

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.
(2) $t_{r/f}$ depends on the F/S setting and the capacitive load connected to each output. Some application information of how to calculate $t_{r/f}$ based on the output load and how to estimate the timing budget to interconnect to an LCD driver are provided in the application section near the end of this data sheet.
(3) The output rise and fall times are optimized for an output load of 10 pF. The rise and fall times can be adjusted by changing the output load capacitance.
(4) The RXEN input incorporates glitch-suppression logic to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.

SWITCHING CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
f_{BW}	PLL bandwidth(5)		0.087 f_{PCLK}			MHz

(5) When using the SN65LVDS310 receiver in conjunction with the SN65LVDS307 transmitter in one link, the PLL bandwidth of the SN65LVDS310 receiver always exceeds the bandwidth of the SN65LVDS307 transmit PLL. This ensures stable PLL tracking under all operating conditions and maximizes the receiver skew margin.

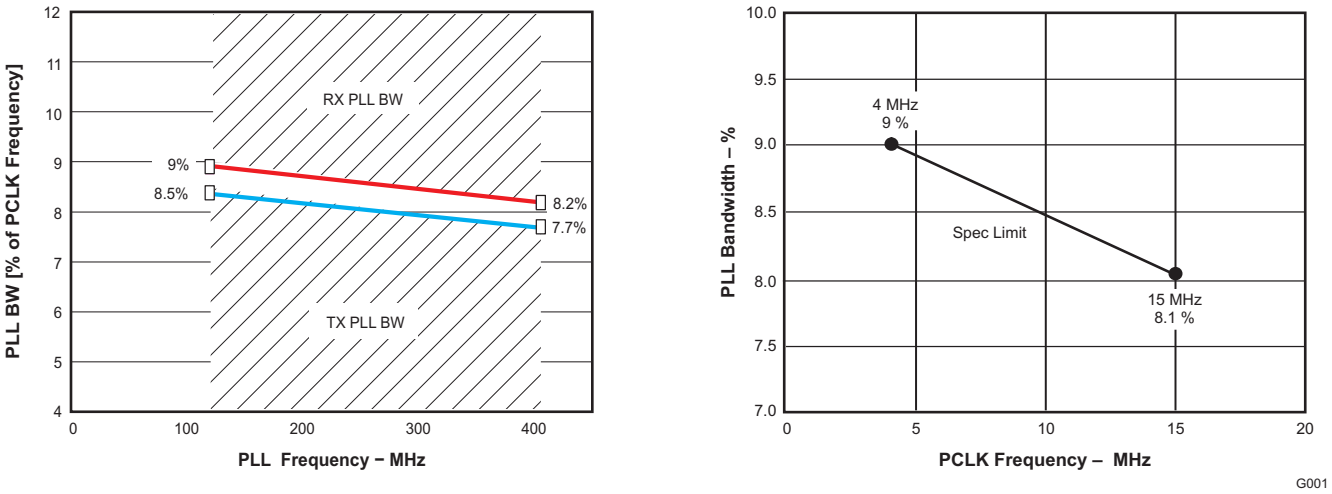


Figure 4. SN65LVDS310 PLL Bandwidth (Also Showing the SN65LVDS307 PLL Bandwidth)

TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{RSKMx} (1)(2)	Receiver input skew margin; see (3) and Figure 29	x = 0..29, f_{PCLK} = 15 MHz; RXEN at VDD, V_{IH} = VDD, V_{IL} = GND, R_L = 100 Ω, test setup as in Figure 6, test pattern as in Table 9	f_{CLK} = 15 MHz(4)	630		ps
			f_{CLK} = 4 MHz to 15 MHz(5)	$\frac{1}{2 \bullet 30 \bullet f_{CLK}} - 480\,ps$		

(1) Receiver input skew margin (t_{RSKM}) is the timing margin available for transmitter output pulse position (t_{PPOS}), interconnect skew, and interconnect inter-symbol interference. t_{RSKM} represents the remainder of the serial bit time not taken up by the receiver strobe uncertainty. t_{RSKM} assumes a bit error rate better than 10^{-12}.
(2) t_{RSKM} is inversely proportional to the internal setup and hold time uncertainty, ISI, and duty-cycle distortion from the front-end receiver, the skew missmatch between CLK and data D0, as well as the PLL cycle-to-cycle jitter.
(3) This includes the receiver internal setup and hold time uncertainty, all PLL-related high-frequency random and deterministic jitter components that impact the jitter budget, ISI and duty-cycle distortion from the front-end receiver, and the skew between CLK and data D0; the pulse position minimum/maximum variation is given with a bit error rate target of 10^{-12}; measurements of the total jitter are taken over $>10^{12}$ samples.
(4) The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges.
(5) These minimum and maximum limits are simulated only.

PARAMETER MEASUREMENT INFORMATION

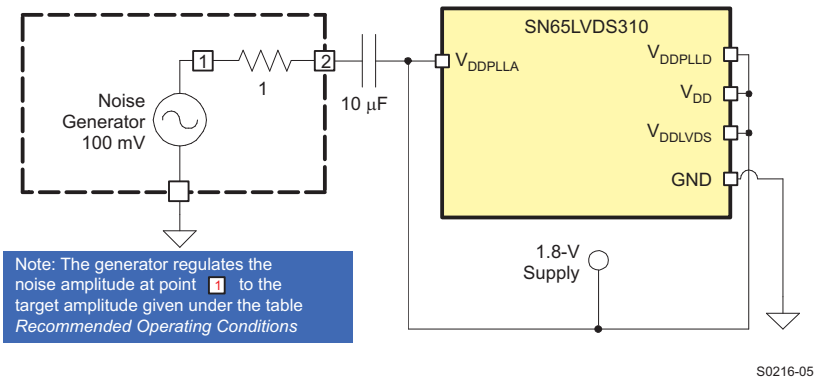


Figure 5. Power-Supply Noise Test Setup

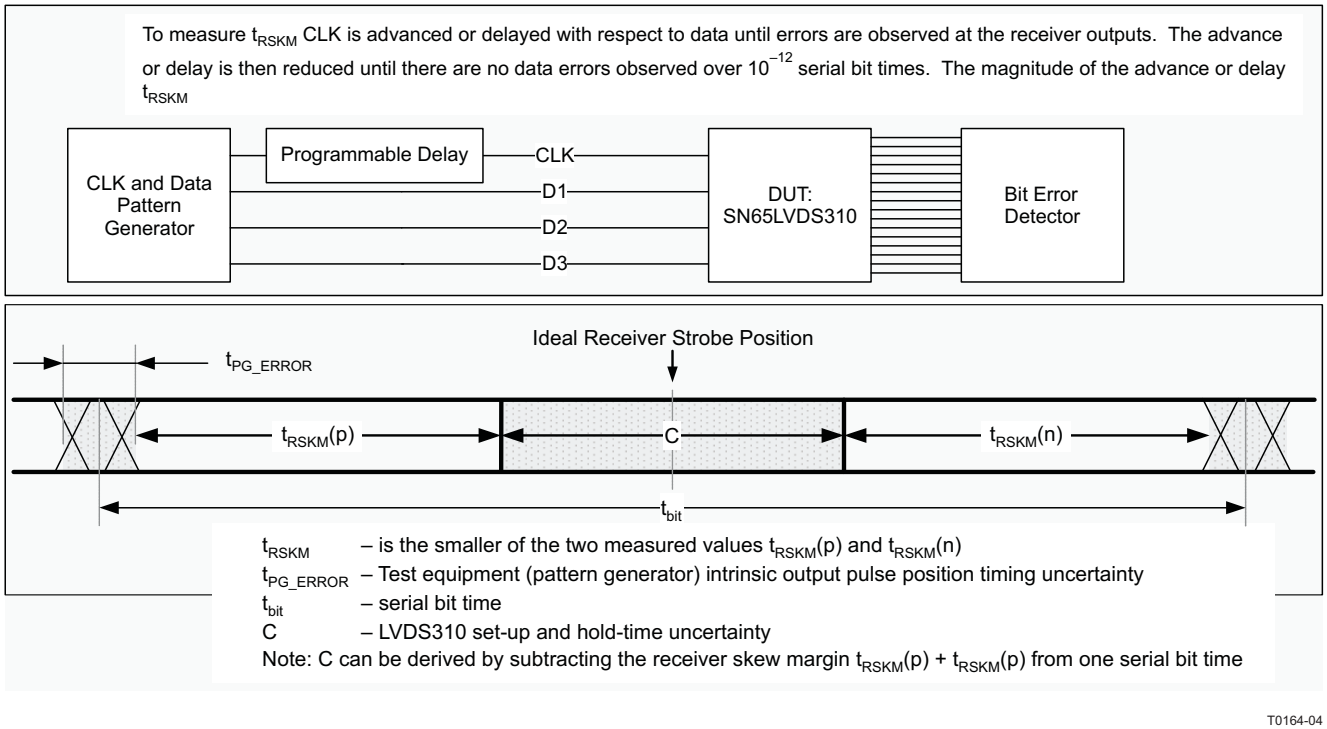


Figure 6. Receiver Jitter-Budget Test Setup

PARAMETER MEASUREMENT INFORMATION (continued)

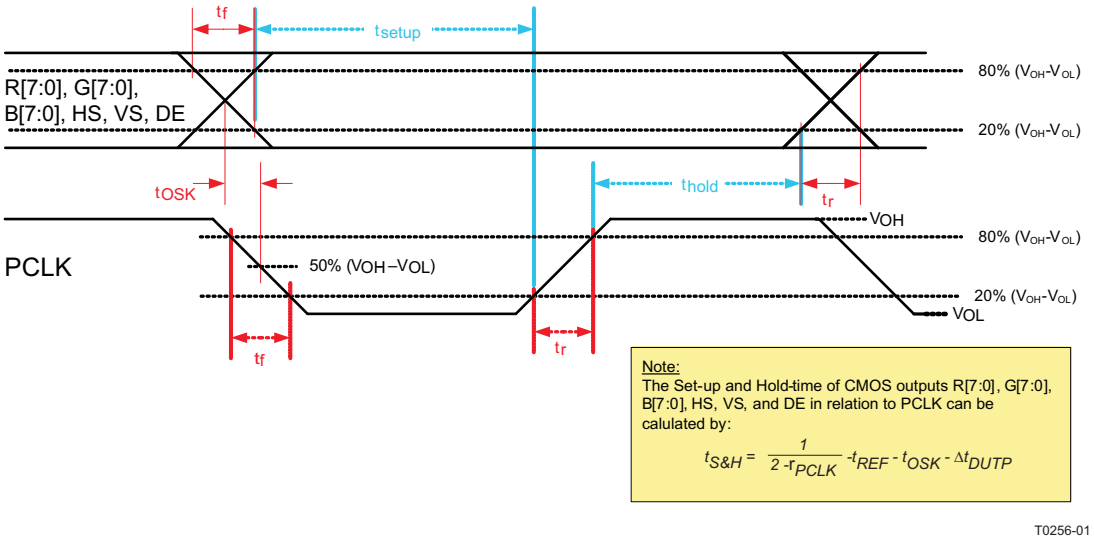


Figure 7. Output Rise/Fall, Setup/Hold Time

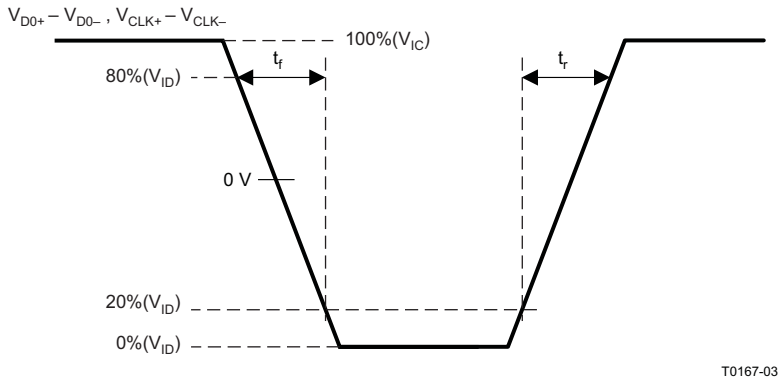


Figure 8. SubLVDS Differential Input Rise and Fall Time Defintion

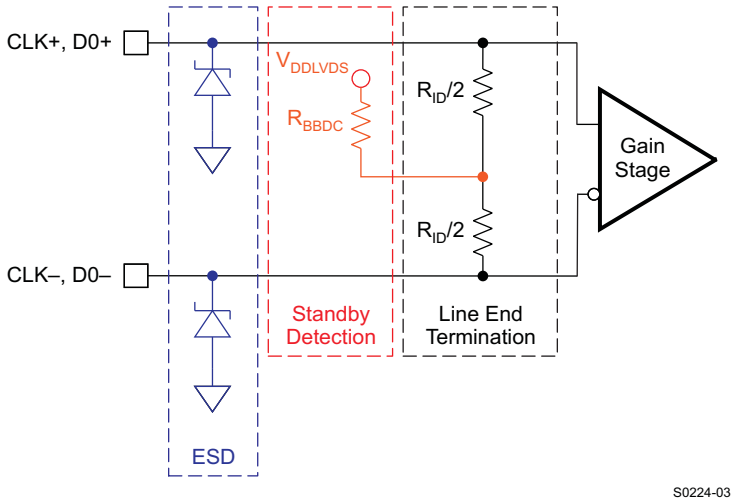


Figure 9. Equivalent Input Circuit Design

PARAMETER MEASUREMENT INFORMATION (continued)

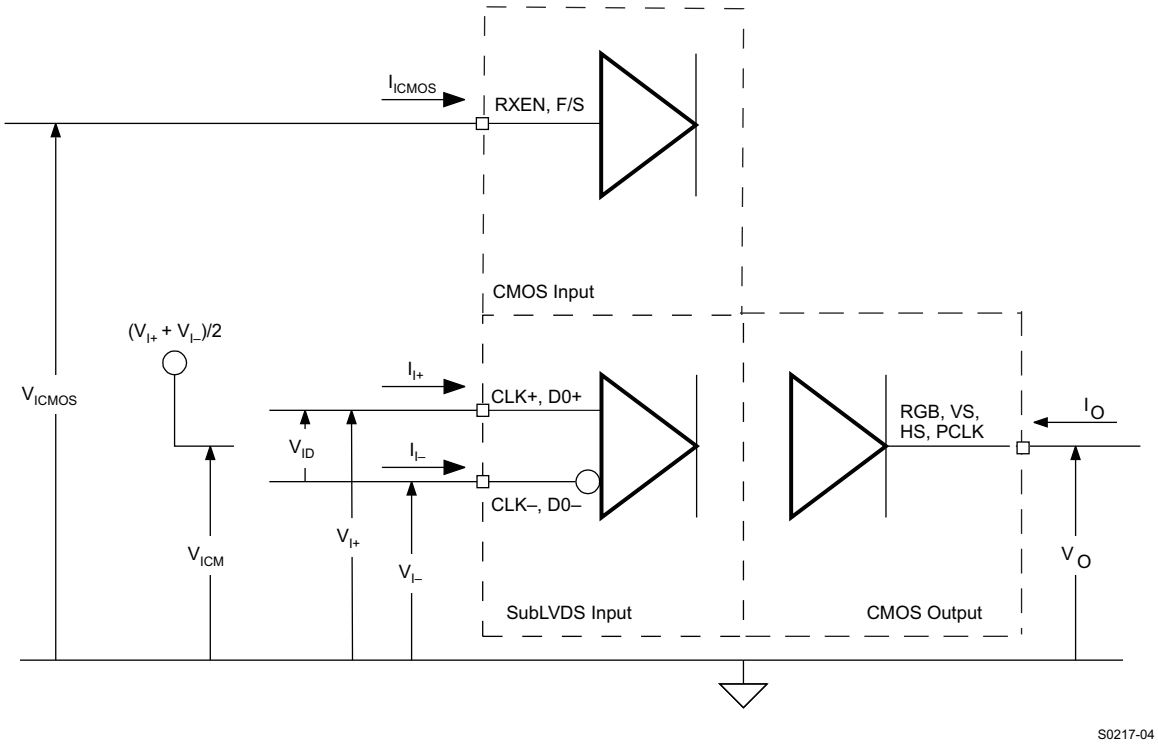


Figure 10. I/O Voltage and Current Definition

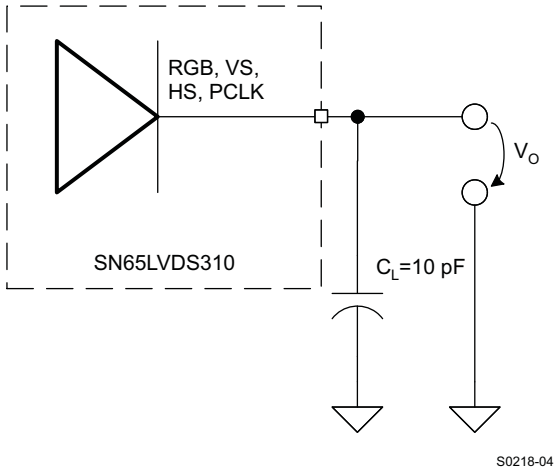


Figure 11. CMOS Output Test Circuit, Signal, and Timing Definition

PARAMETER MEASUREMENT INFORMATION (continued)

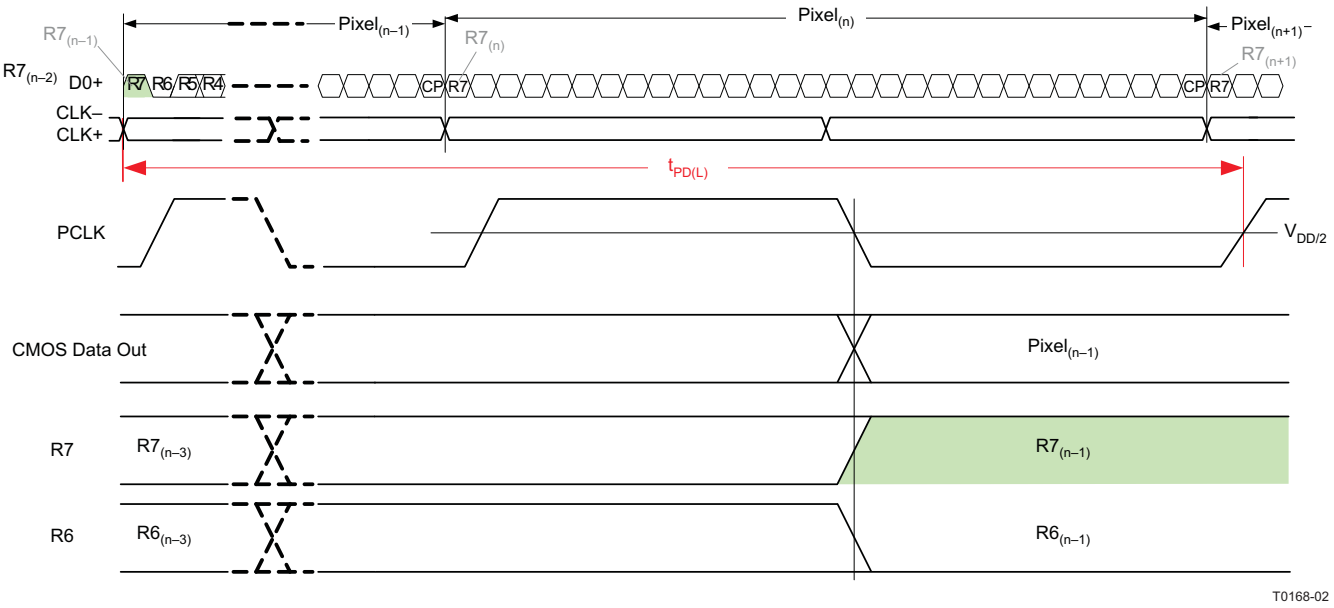


Figure 12. Propagation Delay, Input to Output

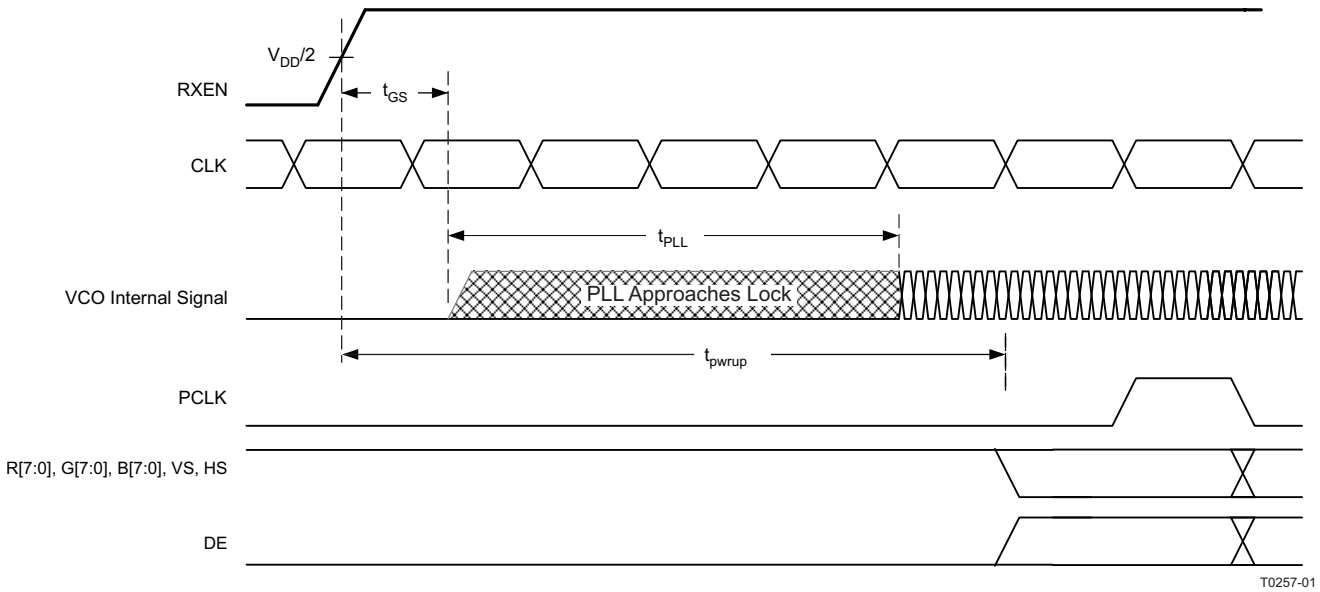


Figure 13. Receiver Phase-Locked Loop Set Time and Receiver Enable Time

PARAMETER MEASUREMENT INFORMATION (continued)

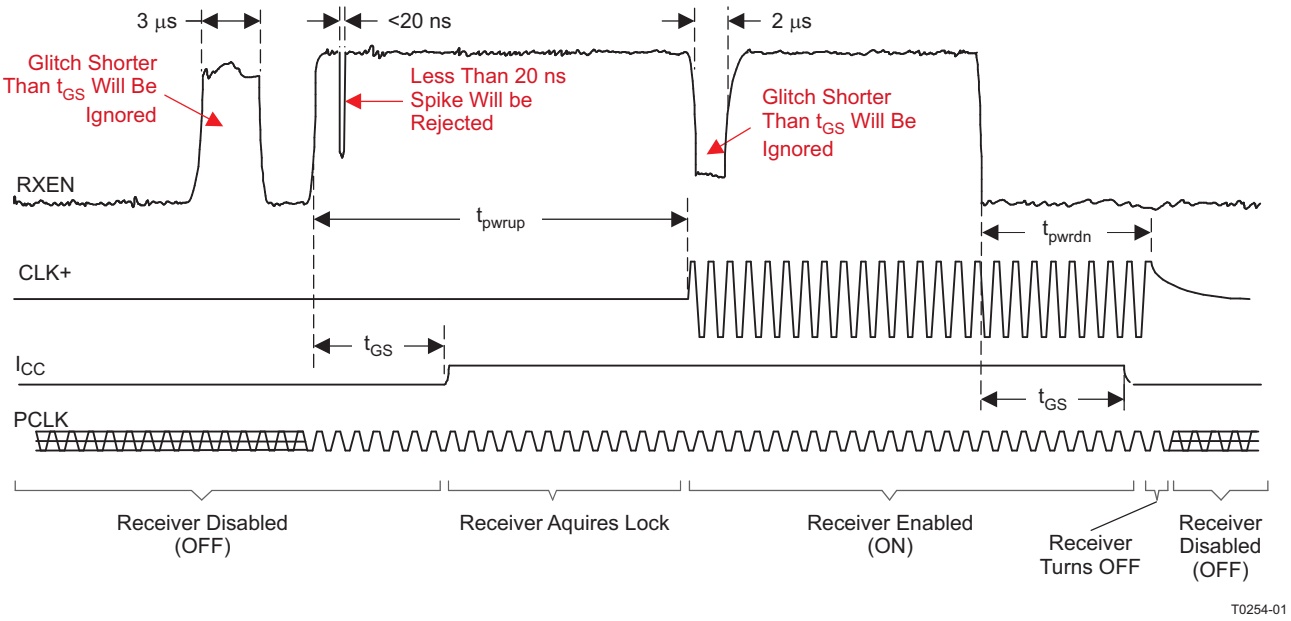


Figure 14. Receiver Enable/Disable Glitch Suppression Time

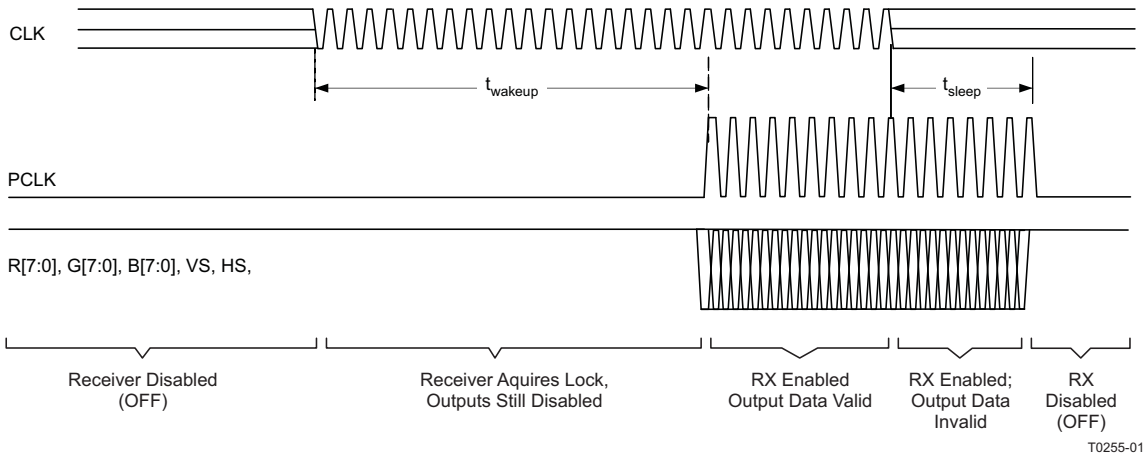


Figure 15. Standby Detection

POWER-CONSUMPTION TESTS

Table 5 shows an example test pattern word.

Table 5. Example Test Pattern Word

WORD	R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

TYPICAL IC POWER-CONSUMPTION TEST PATTERN

The typical power-consumption test pattern consists of 16 30-bit transmit words. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 6. Typical IC Power-Consumption Test Pattern

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000007
2	0xFFF0007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

MAXIMUM POWER-CONSUMPTION TEST PATTERNS

The maximum (or worst-case) power consumption of the SN65LVDS310 is tested using the two different test patterns shown in Table 7 and Table 8. Test patterns consist of 16 30-bit transmit words. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 7. Worst-Case Power-Consumption Test Pattern 1

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0xAAAAAA5
2	0x5555555

Table 8. Worst-Case Power-Consumption Test Pattern 2

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000000
2	0xFFFFFF7

OUTPUT SKEW PULSE POSITION and JITTER PERFORMANCE

The test pattern of Table 9 is used to measure the output skew pulse position and the jitter performance of the SN65LVDS310. The jitter test pattern stresses the interconnect, particularly to test for ISI, using very long run-lengths of consecutive bits, and incorporating very high and low data rates, maximizing switching noise. Each pattern is self-repeating for the duration of the test.

Table 9. Transmit Jitter Test Pattern

WORD	TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCCC1
20	0xEEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFF0001
27	0xFFFC001
28	0xFFFF001
29	0xFFFFC01
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFFF1

TYPICAL CHARACTERISTIC CURVES

Some of the plots in this section show more than one curve representing various device pin relationships. Taken together, they represent a working range for the tested parameter.

QUIESCENT SUPPLY CURRENT vs TEMPERATURE

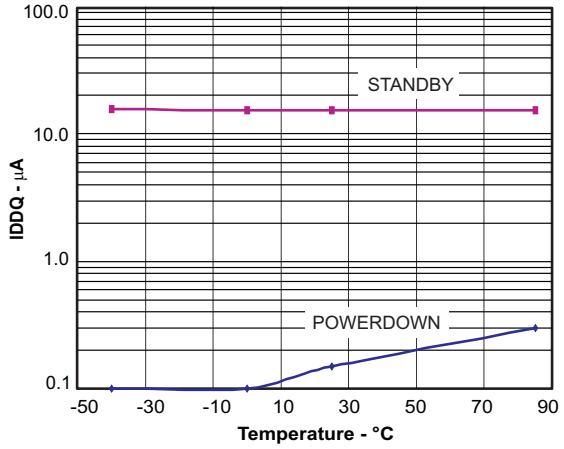


Figure 16.

SUPPLY CURRENT vs FREQUENCY

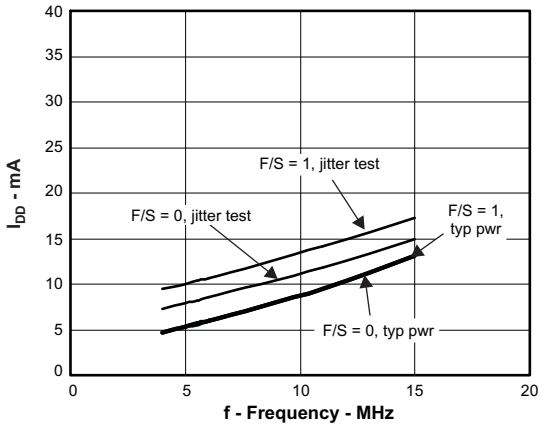


Figure 17.

RECEIVER STROBE POSITION vs TEMPERATURE

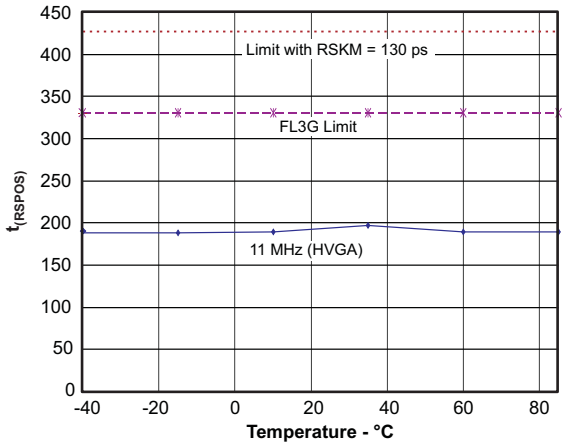


Figure 18.

PLL BANDWIDTH

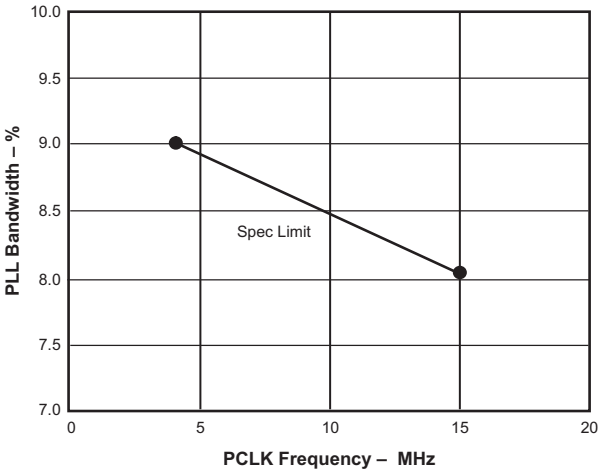


Figure 19.

TYPICAL CHARACTERISTIC CURVES (continued)

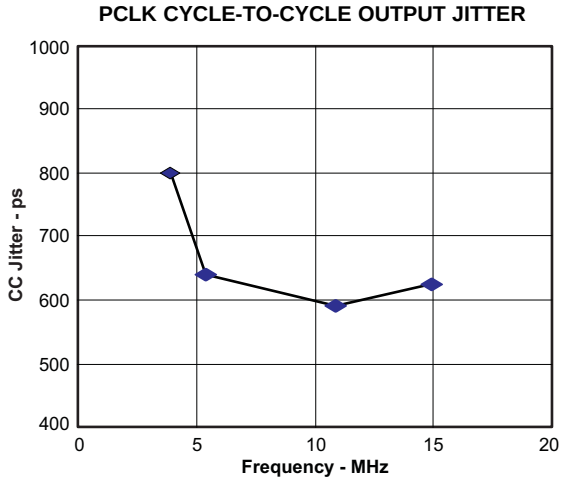


Figure 20.

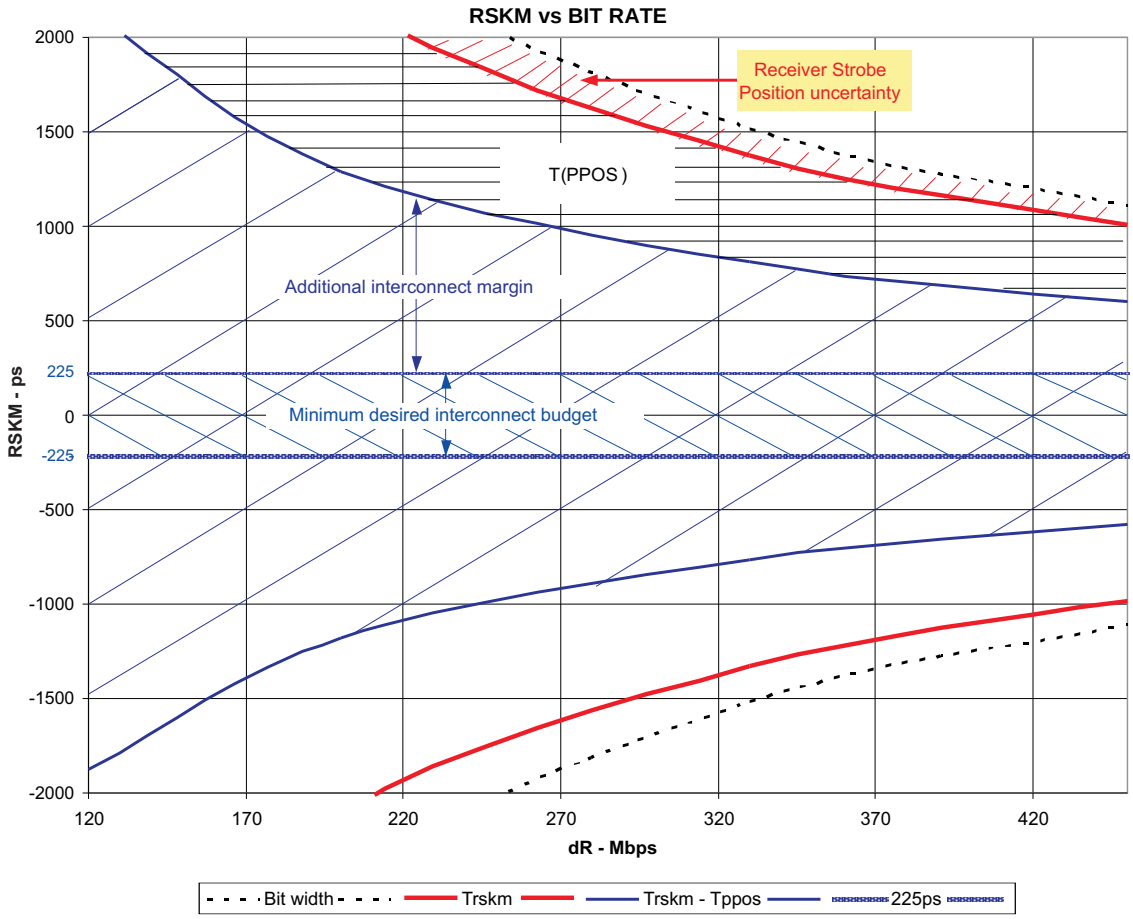


Figure 21.

TYPICAL CHARACTERISTIC CURVES (continued)

QVGA OUTPUT WAVEFORM

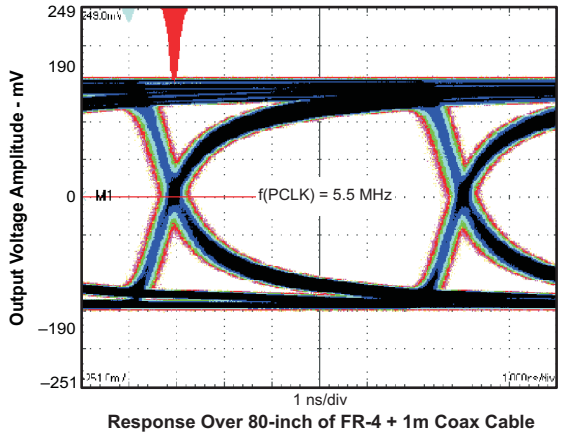


Figure 22.

INPUT COMMON-MODE NOISE REJECTION vs FREQUENCY

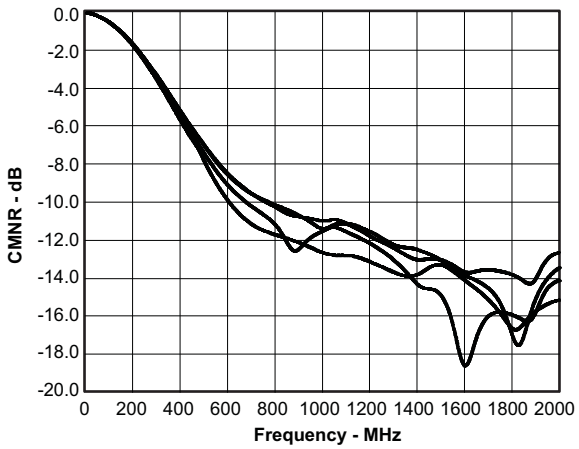


Figure 23.

INPUT RETURN LOSS

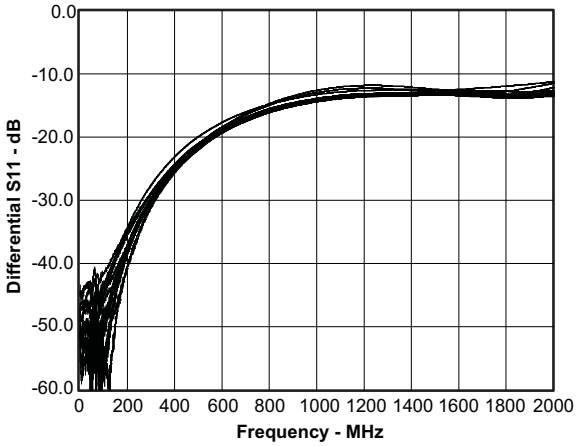


Figure 24.

INPUT DIFFERENTIAL CROSSTALK vs FREQUENCY

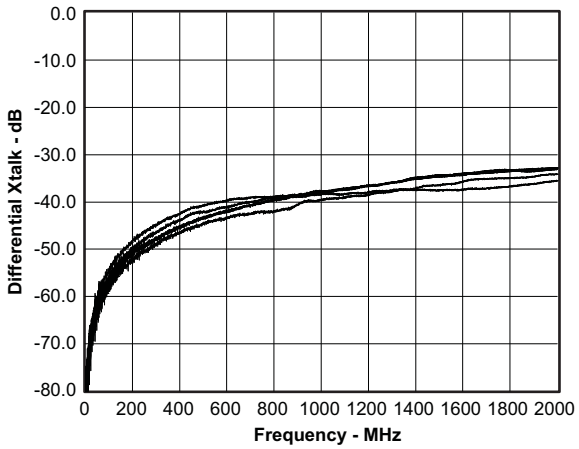


Figure 25.

PHASE NOISE

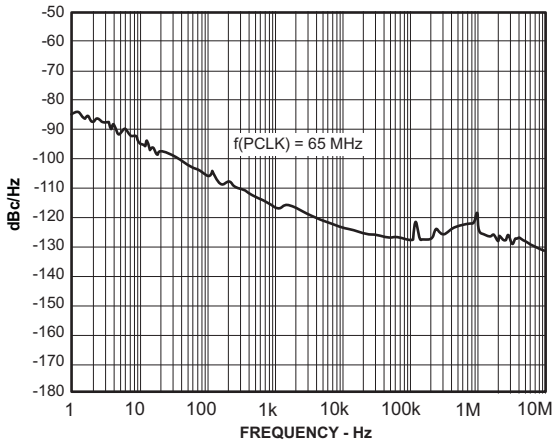


Figure 26.

APPLICATION INFORMATION

PREVENTING INCREASED LEAKAGE CURRENTS IN CONTROL INPUTS

A floating (left open) CMOS input allows leakage currents to flow from VDD to GND. Do not leave any CMOS input unconnected or floating. Every input must be connected to a valid logic level, V_{IH} or V_{OL}, while power is supplied to VDD. This also minimizes the power consumption of standby and power-down modes.

POWER-SUPPLY DESIGN RECOMMENDATION

For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

SN65LVDS310 DECOUPLING RECOMMENDATION

The SN65LVDS310 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS310 often shares a power supply with various other ICs. The SN65LVDS310 can operate with power-supply noise as specified in the (1) To minimize the power-supply noise floor, provide good decoupling near the SN65LVDS310 power pins. The use of four ceramic capacitors (two 0.01-µF and two 0.1-µF) provides good performance. At the very least, it is recommended to install one 0.1-µF and one 0.01-µF capacitor near the SN65LVDS310. To avoid large current loops and trace inductance, the trace length between the decoupling capacitors and IC power input pins must be minimized. Placing the capacitor underneath the SN65LVDS310 on the bottom of the PCB is often a good choice.

VGA APPLICATION

Figure 27 shows a possible implementation of a 640 × 480 VGA display. The SN65LVDS307 innterfaces to the SN65LVDS310, which is the corresponding receiver device, to deserialize the data and drive the display driver. The pixel-clock rate of 5.5 MHz assumes ~10% blanking overhead and a 60-Hz display refresh rate. The application assumes 24-bit color resolution. Also shown is how the application processor provides a power-down (reset) signal for both the serializer and the display driver. The signal count over the flexible printed circuit board (FPC) could be further decreased by using the automatic standby detection feature of the SN65LVDS310 and pulling RXEN permanently high.

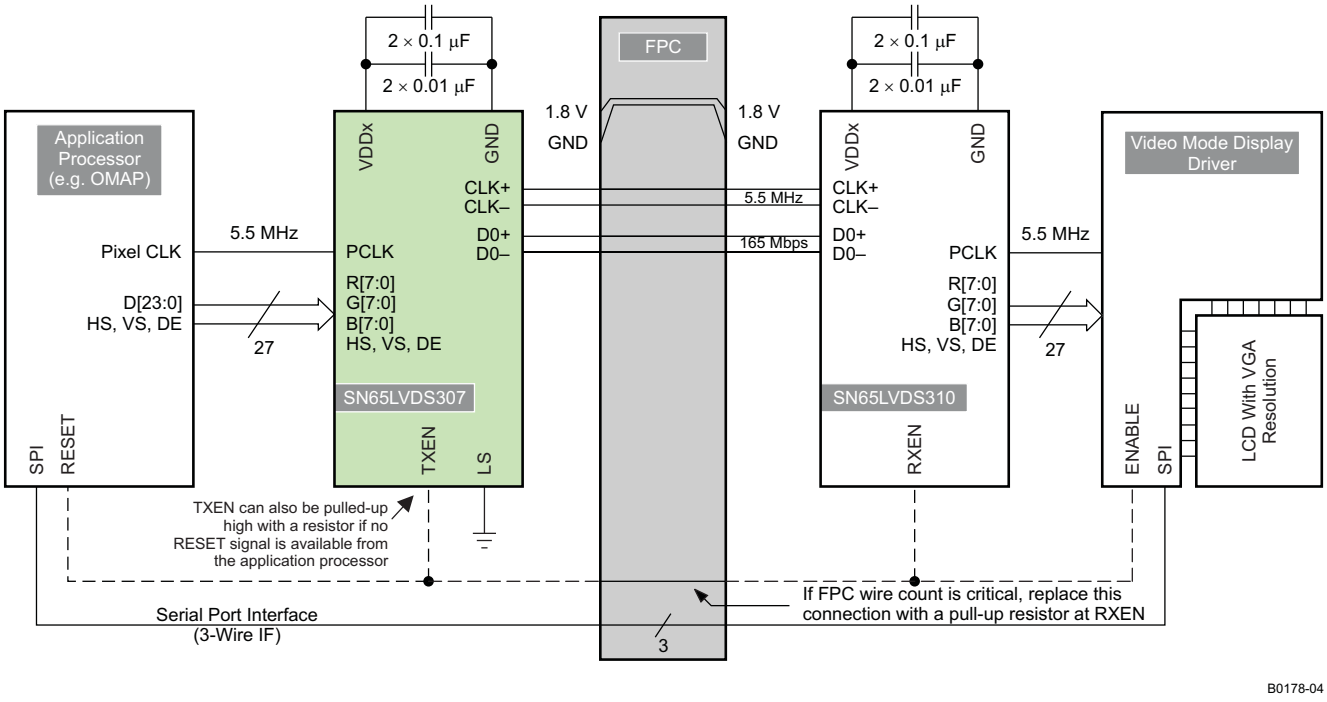


Figure 27. Typical VGA Display Application

(1) Unused single-ended inputs must be held high or low to prevent them from floating.

APPLICATION INFORMATION (continued)

TYPICAL APPLICATION FREQUENCIES

The SN65LVDS310 supports pixel clock frequencies from 4 MHz to 15 MHz. Table 10 provides a few typical display resolution examples. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate.

Table 10. Typical Application Data Rates and Serial Lane Usage

Display Screen Resolution	Visible Pixel Count	Blanking Overhead	Display Refresh Rate [Hz}	Pixel Clock Frequency on CLK [MHz]	Serial Data Rate [Mbps]
240 × 320 (QVGA)	76,800	20%	60	5.5	166
640 × 200	128,000			9.2	276
352 × 416 (CIF+)	146,432			10.5	316
352 × 440	154,880			11.2	335
320 × 480 (HVGA)	153,600		30	5.5	166
320 × 480 (HVGA)	153,600		60	11.1	332
800 × 250	200,000			14.4	432
640 × 320	204,800			14.7	442
640 × 480 (VGA)	307,200		30	11.1	332

CALCULATION EXAMPLE: HVGA DISPLAY

The following calculation shows an example for a half-VGA display with the following parameters:

Display resolution:	480 × 320
Frame refresh rate:	58.4 Hz
Vertical visible pixels:	320 lines
Vertical front porch:	10 lines
Vertical sync:	5 lines
Vertical back porch:	3 lines
Horizontal visible pixels:	480 columns
Horizontal front porch:	20 columns
Horizontal sync:	5 columns
Horizontal back porch:	3 columns

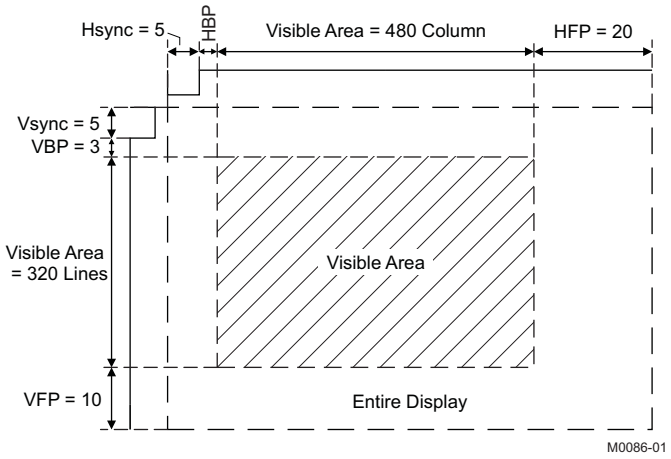


Figure 28. HVGA Display

Calculation of the total number of pixel and blanking overhead:

Visible area pixel count: 480 × 320 = 153,600 pixels

Total frame pixel count: (480 + 20 + 5 + 3) × (320 + 10 + 5 + 3) = 171,704 pixels

Blanking overhead: (171,704 – 153,600) ÷ 153,600 ≈ 11.8 %

The application requires the following serial-link parameters:

Pixel clock frequency: 171,704 × 58.4 Hz = 10 MHz

Serial data rate: 10 MHz × 30 bits = 300 Mbps

HOW TO DETERMINE INTERCONNECT SKEW AND JITTER BUDGET

Designing a reliable data link requires examining the interconnect skew and jitter budget. The sum of all transmitter, PCB, connector, FPC, and receiver uncertainties must be smaller than the available serial bit time. The highest pixel clock frequency defines the available serial bit time. The transmitter timing uncertainty is defined by t_{PPOS} in the transmitter data sheet. For a bit-error-rate target of $\leq 10^{-12}$, the measurement duration for t_{PPOS} is $\geq 10^{12}$. The SN65LVDS310 receiver can tolerate a maximum timing uncertainty defined by t_{RSKM}. The interconnect budget is calculated by:

$$t_{interconnect} = t_{RSKM} - t_{PPOS}$$

Example:

f_{PCLK}(max) = 11 MHz (HVGA display resolution, 60 Hz)

t_{PPOS}(SN65LVDS305) = 330 ps

Target bit error rate: 10^{-12}

t_{RSKM}(SN65LVDS310) = $1/(2 \times 30 \times f_{PCLK}) - 480$ ps = 1035 ps

The interconnect budget for cable skew and ISI must be smaller than:

$$t_{interconnect} = t_{RSKM} - t_{PPOS} = 1035 \text{ ps} - 330 \text{ ps} = 705 \text{ ps}$$

$$t_{interconnect} = t_{RSKM} - t_{PPOS}$$

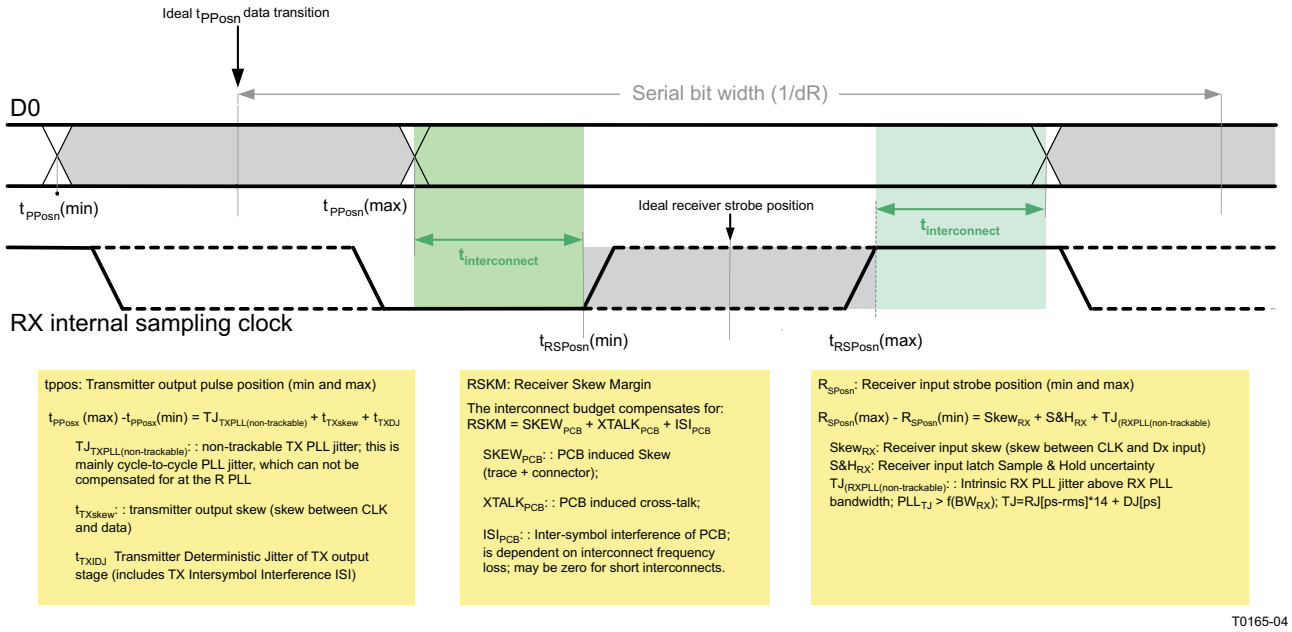


Figure 29. Jitter Budget

F/S-PIN SETTING AND CONNECTING THE SN65LVDS310 TO AN LCD DRIVER

NOTE:

Receiver PLL tracking: To maximize the design margin for the interconnect, good RX PLL tracking of the TX PLL is important. FlatLink 3G connection requires the RX PLL to have a bandwidth higher than the bandwidth of the TX PLL. The SN65LVDS310 PLL design is optimized to track the SN65LVDS307 PLL particularly well, thus providing a very large receiver skew margin. A FlatLink 3G-compliant link must provide at least ±225 ppm of receiver skew margin for the interconnect.

It is important to understand the tradeoff between power consumption, EMI, and maximum speed when selecting the F/S signal. It is beneficial to choose the slowest rise time possible to minimize EMI and power consumption. Unfortunately, a slower rise time also reduces the timing margin left for the LCD driver. Hence, it is necessary to calculate the timing margin to select the correct F/S pin setting.

The output rise time depends on the output driver strength and the output load. An LCD driver typical capacitive load is assumed with ~10 pF. The higher the capacitive load, the slower is the rise time. Rise time of the SN65LVDS310 is measured as the time duration it takes the output voltage to rise from 20% of VDD to 80% of VDD, and fall time is defined as the time for the output voltage to transition from 80% of VDD to 20% of VDD.

The rise time of the output stage is fixed and does not adjust to the pixel frequency. Only changing the F/S setting changes the output rise time. Due to the short bit time at very fast pixel clock speeds and the real capacitive load of the display driver, the output amplitude might not reach VDD and GND saturation fully. To ensure sufficient signal swing and verify the design margin, it is necessary to determine that the output amplitude under any circumstance reaches the display driver's input stage logic threshold (usually 30% and 70% of VDD).

HOW TO DETERMINE THE LCD DRIVER TIMING MARGIN

To determine the timing margin, it is necessary to specify the frequency of operation, identify the setup and hold times of the LCD driver, and specify the output load of the SN65LVDS310 as a combination of the LCD driver input parasitics plus any capacitance caused by the connecting PCB trace. Furthermore, the setting of pin F/S and the SN65LVDS310 output skew impact the margin. The total remaining design margin calculates as follows:

$$t_{DM} = \frac{1}{2 \times f_{PCLK}} - t_{DUTP(max_error)} - \frac{t_{rise(max)} \times C_{LOAD}}{10\ pF} - \left|t_{OSK}\right| \quad (2)$$

where:

t_{DM} – design margin
f_{PCLK} – pixel clock frequency
$t_{DUTP(max_error)}$ – maximum duty cycle error
$t_{rise(max)}$ – maximum rise or fall time; see $t_{r/f}$ under switching characteristics
C_L – parasitic capacitance (sum of LCD driver input parasitics + connecting PCB trace)
t_{skew} – clock-to-data output skew, SN65LVDS310

Example:

At a pixel clock frequeny of 11 MHz (HVGA), and an assumed LCD driver load of 15 pF, the remaining timing margin is:

$$t_{DUTP(max_error)} = \frac{\left|t_{DUTP}(max) - 50\%\right|}{100\%} \times t_{PCLK} = \frac{5\%}{100\%} \times \frac{1}{11\ MHz} = 4.5\ ns$$

$$t_{DM} = \frac{1}{2 \times 5.5\ MHz} - 9\ ns - \frac{16\ ns_{(F/S=GND)} \times 15\ pF}{10\ pF} - 500\ ps = 16\ ns$$

As long as the setup and hold times of the LCD driver are BOTJ less than 16 ns, the timing budget is met sufficiently.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LVDS310ZQCR	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS310	Samples
SN65LVDS310ZQCT	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS310	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

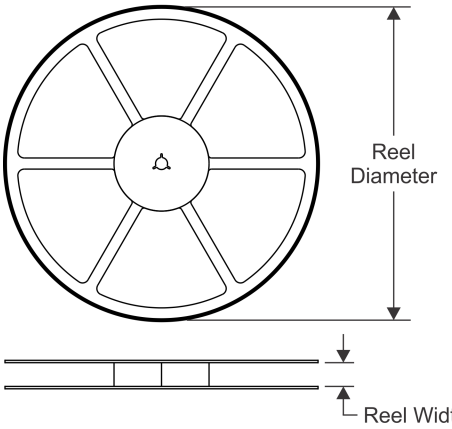
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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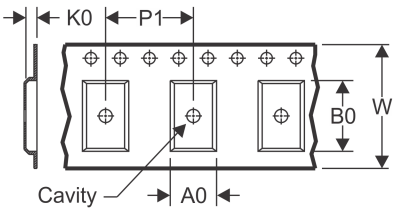
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

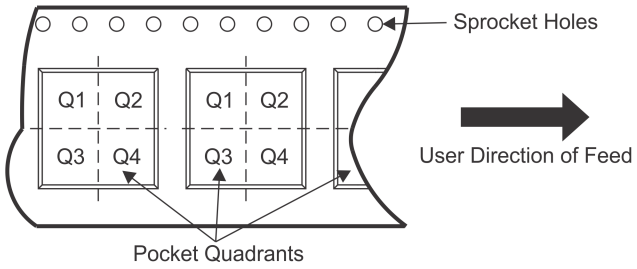


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

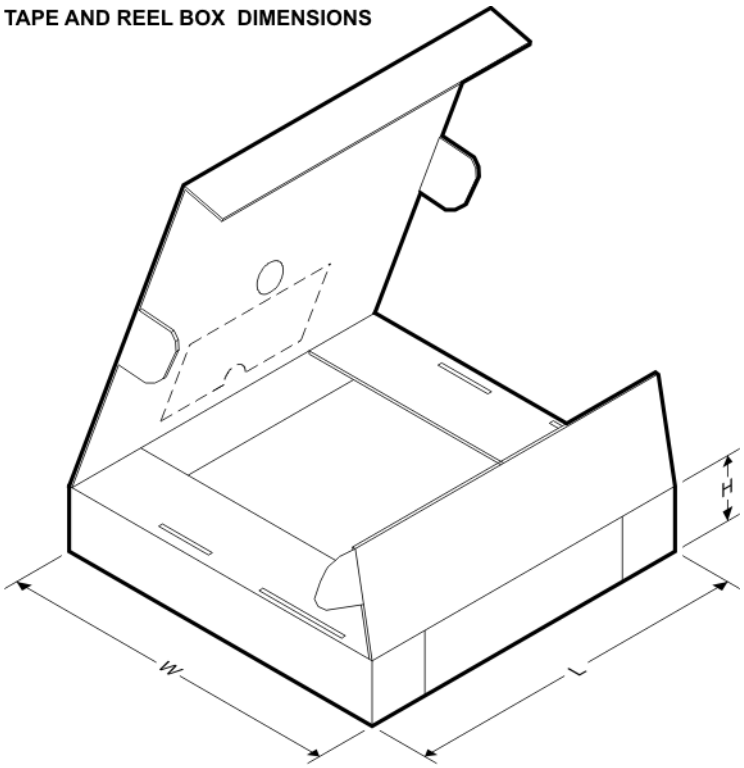
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS310ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1
SN65LVDS310ZQCT	BGA MICROSTAR JUNIOR	ZQC	48	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1

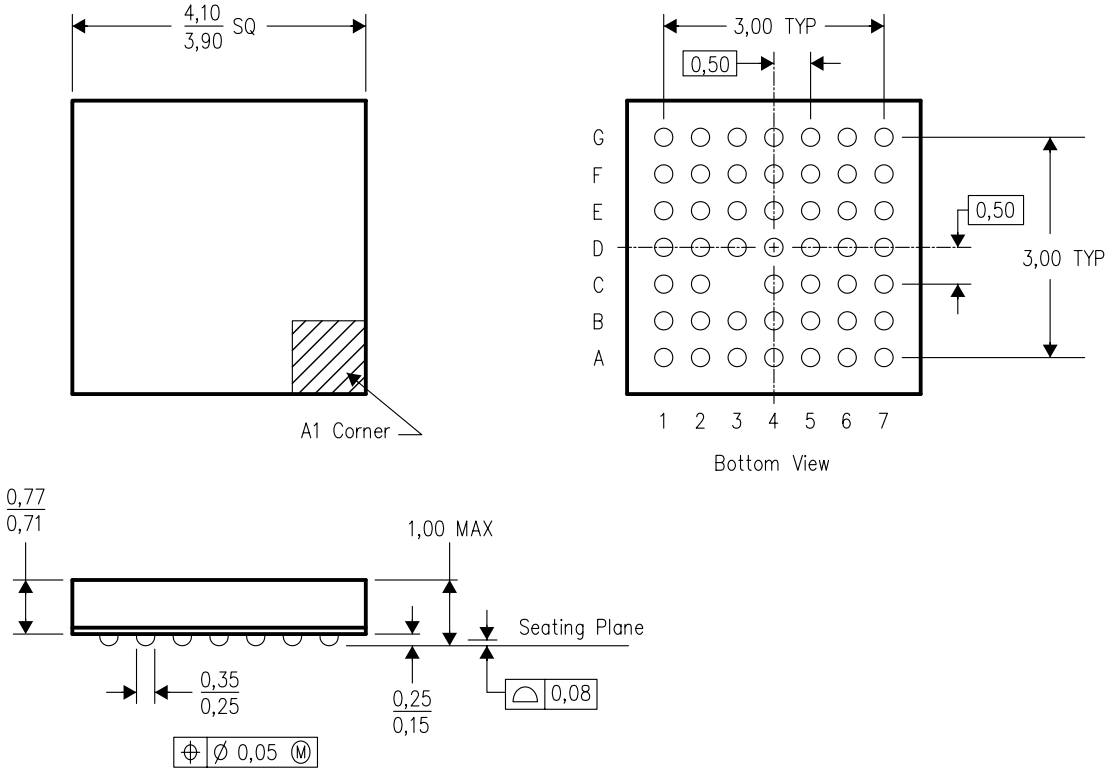
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS310ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	336.6	336.6	28.6
SN65LVDS310ZQCT	BGA MICROSTAR JUNIOR	ZQC	48	250	210.0	185.0	35.0

ZQC (S–PBGA–N48) PLASTIC BALL GRID ARRAY



4204659/A 09/02

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

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