# DATA SHEET

## SSTV16859

2.5 V 13-bit to 26-bit SSTL_2
registered buffer for stacked DDR DIMM

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PHILIPS

# 2.5 V 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM

# SSTV16859

## FEATURES

- Stub-series terminated logic for 2.5 V $V_{DD}$ (SSTL_2)
- Optimized for stacked DDR (Double Data Rate) SDRAM applications
- Supports SSTL_2 signal inputs as per JESD 8–9
- Flow-through architecture optimizes PCB layout
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Supports efficient low power standby operation
- Full DDR 200/266 solution for stacked DIMMs at 2.5 V when used with PCKV857
- See SSTV16857 for JEDEC compliant register support in unstacked DIMM applications
- See SSTV16856 for driver/buffer version with mode select.

## DESCRIPTION

The SSTV16859 is a 13-bit to 26-bit SSTL_2 registered driver with differential clock inputs, designed to operate between 2.3 V and 2.7 V. All inputs are compatible with the JEDEC standard for SSTL_2 with $V_{REF}$ normally at 0.5*$V_{DD}$, except the LVCMOS reset ($\overline{RESET}$) input. All outputs are SSTL_2, Class II compatible which can be used for standard stub-series applications or capacitive loads. Master reset ($\overline{RESET}$) asynchronously resets all registers to zero.

The SSTV16859 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JEDEC, such as DDR (Double Data Rate) SDRAM and SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 133 MHz will have a burst rate of 266 MHz.

The device data inputs consist of different receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

The clock input is fully differential (CK and $\overline{CK}$) to be compatible with DRAM devices that are installed on the DIMM. Data are registered at the crossing of CK going high, and $\overline{CK}$ going low. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device has an asynchronous input pin ($\overline{RESET}$), which when held to the LOW state, resets all registers and all outputs to the LOW state.

The device supports low-power standby operation. When $\overline{RESET}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ($V_{REF}$) inputs are allowed. In addition, when $\overline{RESET}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power-up.

In the DDR DIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering $\overline{RESET}$, the register will be cleared and the outputs will be driven low. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RESET}$ until the input receivers are fully enabled, the outputs will remain low.

Available in 64-pin plastic thin shrink small outline package.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.5$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay; CLK to Qn | $C_L$ = 30 pF; $V_{DD}$ = 2.5 V | 2.4 | ns |
| $C_I$ | Input capacitance | $V_{CC}$ = 2.5 V | 2.7 | pF |

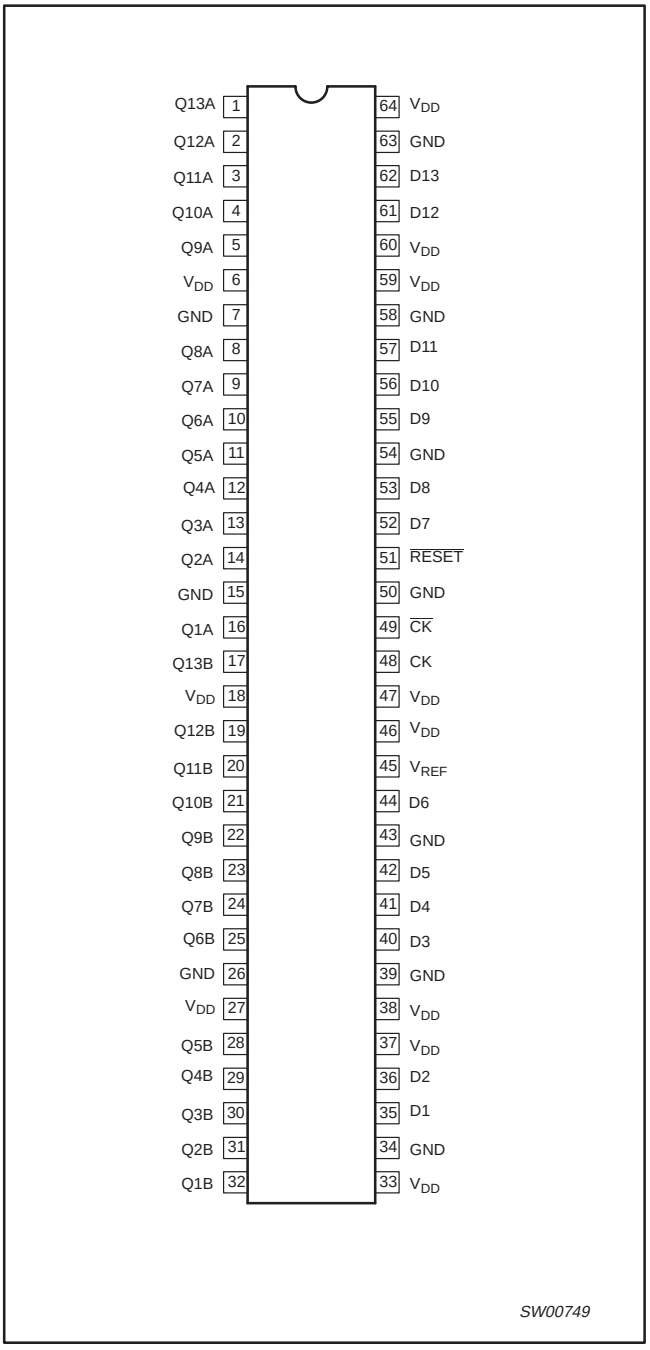
**NOTE:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i$ = input frequency in MHz; $C_L$ = output load capacity in pF; $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DWG NUMBER |
|---|---|---|---|
| 64-Pin Plastic TSSOP | 0 to +70 °C | SSTV16859DGG | SOT646AA1 |
| 96-Ball Plastic LFBGA | 0 to +70 °C | SSTV16859EC | SOT536-1 |
| 56-Terminal Plastic HVQFN | 0 to +70 °C | SSTV16859BS | SOT684-1 |

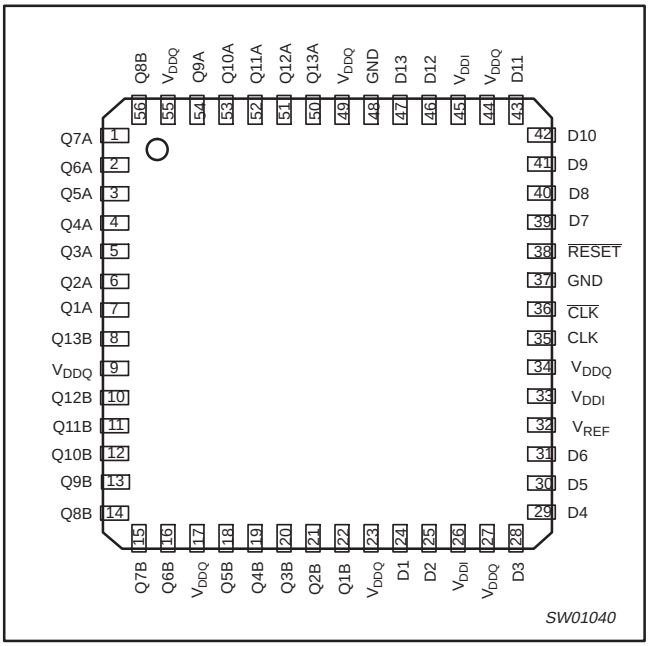
## PIN CONFIGURATION




## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 16 | Q13A–Q1A | Data output |
| 17, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31, 32 | Q13B–Q1B | Data output |
| 6, 18, 27, 33, 37, 38, 46, 47, 59, 60, 64 | $V_{DD}$ | Power supply voltage |
| 7, 15, 26, 34, 39, 43, 50, 54, 58, 63 | GND | Ground |
| 35, 36, 40, 41, 42, 44, 52, 53, 55, 56, 57, 61, 62 | D1–D13 | Data input: clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$ |
| 45 | $V_{REF}$ | Input reference voltage |
| 48, 49 | CK, $\overline{CK}$ | Positive and negative master clock input |
| 51 | $\overline{RESET}$ | Asynchronous reset input: resets registers and disables data and clock differential input receivers |

## 56-TERMINAL CONFIGURATION




## TERMINAL DESCRIPTION

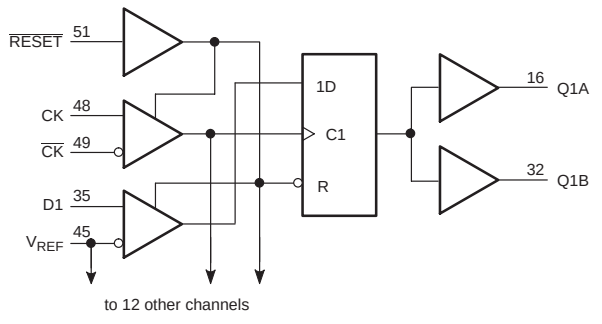
| TERMINAL NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 2, 3, 4, 5, 6, 7, 50, 51, 52, 53, 54, 56 | Q13A–Q1A | Data output |
| 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22 | Q13B–Q1B | Data output |
| 9, 17, 23, 27, 34, 44, 49, 55 | $V_{DDQ}$ | Power supply voltage |
| 26, 33, 45 | $V_{DDI}$ | Power supply voltage |
| 37, 48 | GND | Ground |
| 24, 25, 28, 29, 30, 31, 39, 40, 41, 42, 43, 46, 47 | D1–D13 | Data input: clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$ |
| 32 | $V_{REF}$ | Input reference voltage |
| 35, 36 | CK, $\overline{CK}$ | Positive and negative master clock input |
| 51 | $\overline{RESET}$ | Asynchronous reset input: resets registers and disables data and clock differential input receivers |

## BALL CONFIGURATION

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | — | — | — | — | — | — |
| B | Q12A | Q13A | GND | GND | — | — |
| C | Q10A | Q11A | GND | GND | — | — |
| D | Q8A | Q9A | $V_{DDQ}$ | $V_{DDQ}$ | D13 | D12 |
| E | Q6A | Q7A | $V_{DDQ}$ | $V_{DDQ}$ | D11 | D10 |
| F | Q4A | Q5A | $V_{DDQ}$ | $V_{DDQ}$ | D9 | D8 |
| G | Q2A | Q3A | GND | GND | D7 | $\overline{RESET}$ |
| H | Q1A | Q13B | GND | GND | — | $\overline{CK}$ |
| J | Q12B | Q11B | GND | $V_{REF}$ | — | CK |
| K | Q10B | Q9B | $V_{DDQ}$ | $V_{DDQ}$ | — | — |
| L | Q8B | Q7B | $V_{DDQ}$ | $V_{DDQ}$ | D5 | D6 |
| M | Q6B | Q5B | $V_{DDQ}$ | $V_{DDQ}$ | D3 | D4 |
| N | Q4B | Q3B | GND | GND | D1 | D2 |
| P | Q2B | Q1B | GND | GND | — | — |
| R | — | — | — | — | — | — |
| T | — | — | — | — | — | — |

*SW00944*

## LOGIC DIAGRAM




*SW00750*

| | | | | |
|---|---|---|---|---|
| H | ↑ | ↓ | L | L |
| H | ↑ | ↓ | H | H |
| H | L or H | L or H | X | $Q_0$ |
| L | X or floating | X or floating | X or floating | L |

H = High voltage level
L = Low voltage level
↓ = High-to-Low transition
↑ = Low-to-High transition
X = Don't care

## FUNCTION TABLE (each flip flop)

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{RESET}$ | CLK | $\overline{CLK}$ | D | Q |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | CONDITION | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{DD}$ | Supply voltage range | | –0.5 | +3.6 | V |
| $V_I$ | Input voltage range | Notes 2 and 3 | –0.5 | $V_{DD}$ + 0.5 | V |
| $V_O$ | Output voltage range | Notes 2 and 3 | –0.5 | $V_{DD}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ or $V_I > V_{DD}$ | — | ±50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ or $V_O > V_{DD}$ | — | ±50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{DD}$ | — | ±50 | mA |
| | Continuous current through each $V_{DD}$ or GND | | — | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | +150 | °C |

**NOTES:**
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
3. This value is limited to 3.6 V maximum.
4. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

## RECOMMENDED OPERATING CONDITIONS[1]

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | $V_{DD}$ | — | 2.7 | V |
| $V_{REF}$ | Reference voltage ($V_{REF} = V_{DD}/2$) | | 1.15 | 1.25 | 1.35 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 40 mV | $V_{REF}$ | $V_{REF}$ + 40 mV | V |
| $V_I$ | Input voltage | | 0 | — | $V_{DD}$ | V |
| $V_{IH}$ | AC HIGH-level input voltage | Data inputs | $V_{REF}$ + 310 mV | — | — | V |
| $V_{IL}$ | AC LOW-level input voltage | Data inputs | — | — | $V_{REF}$ – 310 mV | V |
| $V_{IH}$ | DC HIGH-level input voltage | Data inputs | $V_{REF}$ + 150 mV | — | — | V |
| $V_{IL}$ | DC LOW-level input voltage | Data inputs | — | — | $V_{REF}$ – 150 mV | V |
| $V_{IH}$ | HIGH-level input voltage | $\overline{\text{RESET}}$ | 1.7 | — | $V_{DD}$ | V |
| $V_{IL}$ | LOW-level input voltage | | 0.0 | — | 0.7 | V |
| $V_{ICR}$ | Common-mode input range | CK, $\overline{\text{CK}}$ | 0.97 | — | 1.53 | V |
| $V_{ID}$ | Differential input voltage | CK, $\overline{\text{CK}}$ | 360 | — | — | mV |
| $I_{OH}$ | HIGH-level output current | | — | — | –20 | mA |
| $I_{OL}$ | LOW-level output current | | — | — | 20 | mA |
| $T_{amb}$ | Operating free-air temperature range | | 0 | — | +70 | °C |

**NOTE:**
1. The $\overline{\text{RESET}}$ input of the device must be held at $V_{DD}$ or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS $T_{amb}$ = 0 to +70 °C MIN | LIMITS $T_{amb}$ = 0 to +70 °C TYP | LIMITS $T_{amb}$ = 0 to +70 °C MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $I_I$ = –18 mA, $V_{DD}$ = 2.3 V | | — | — | –1.2 | V |
| $V_{OH}$ | | $I_{OH}$ = –100 μA, $V_{DD}$ = 2.3 to 2.7 V | | $V_{DD}$ – 0.2 | — | — | V |
| | | $I_{OH}$ = –16 mA, $V_{DD}$ = 2.3 V | | 1.95 | — | — | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA, $V_{DD}$ = 2.3 to 2.7 V | | — | — | 0.2 | V |
| | | $I_{OL}$ = 16 mA, $V_{DD}$ = 2.3 V | | — | — | 0.35 | |
| $I_I$ | All inputs | $V_I = V_{DD}$ or GND, $V_{DD}$ = 2.7 V | | — | — | ±5 | μA |
| $I_{DD}$ | Static standby | $\overline{RESET}$ = GND | IO = 0, $V_{DD}$ = 2.7 V | — | — | 0.01 | mA |
| | Static operating | $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ | | — | — | 45 | |
| $I_{DDD}$ | Dynamic operating – clock only | $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. | IO = 0, $V_{DD}$ = 2.7 V | 90 | — | — | μA/ clock MHz |
| | Dynamic operating – per each data input | $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. | | 20 | — | — | μA/ clock MHz/ data input |
| $r_{OH}$ | Output high | $I_{OH}$ = –20 mA, $V_{DD}$ = 2.3 to 2.7 V | | 7 | — | 20 | Ω |
| $r_{OL}$ | Output low | $I_{OL}$ = 20 mA, $V_{DD}$ = 2.3 to 2.7 V | | 7 | — | 20 | Ω |
| $r_{O(\Delta)}$ | $\lvert r_{OH} - r_{OL} \rvert$ each separate bit | $I_O$ = 20 mA, $T_{amb}$ = 25°C, $V_{DD}$ = 2.5 V | | — | — | 4 | Ω |
| $C_i$ | Data inputs | $V_I = V_{REF} \pm 310$ mV, $V_{DD}$ = 2.5 V | | 2.5 | 2.74 | 3.5 | pF |
| | CK and $\overline{CK}$ | $V_{ICR}$ = 1.25 V, $V_{I(PP)}$ = 360 mV, $V_{DD}$ = 2.5 V | | 2.5 | 3.15 | 3.5 | |
| | $\overline{RESET}$ | $V_I = V_{DD}$ or GND, $V_{DD}$ = 2.5 V | | — | 2.27 | — | |

## TIMING REQUIREMENTS

Over recommended operating conditions; $T_{amb}$ = 0 to +70 °C (unless otherwise noted) (see Figure 1)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | $V_{DD}$ = 2.5 V ±0.2 V | | |
| | | | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | — | 200 | MHz |
| $t_w$ | Pulse duration, CK, $\overline{CK}$ HIGH or LOW | | 2.5 | — | ns |
| $t_{act}$ | Differential inputs active time | Notes 1, 2 | — | 22 | ns |
| $t_{inact}$ | Differential inputs inactive time | Notes 1, 3 | — | 22 | ns |
| $t_{su}$ | Setup time, fast slew rate (see Notes 4 and 6) | Data before CK↑, $\overline{CK}$↓ | 0.75 | | ns |
| | Setup time, slow slew rate (see Notes 5 and 6) | | 0.9 | | |
| $t_h$ | Hold time, fast slew rate (see Notes 4 and 6) | Data after CK↑, $\overline{CK}$↓ | 0.75 | | ns |
| | Hold time, slow slew rate (see Notes 5 and 6) | | 0.9 | | |
| $t_{SL}$ | Output slew | | 1 | 6 | V/ns |

**NOTES:**
1. This parameter is not necessarily production tested.
2. Data inputs must be below a minimum time of $t_{act}$ max, after $\overline{RESET}$ is taken high.
3. Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{inact}$ max, after $\overline{RESET}$ is taken low.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
6. CK, $\overline{CK}$ signals input slew rates are ≥ 1 V/ns.

## SWITCHING CHARACTERISTICS

Over recommended operating conditions; $T_{amb}$ = 0 to +70 °C; $V_{DD}$ = 2.3 – 2.7 V.
Class I, $V_{REF} = V_{TT} = V_{DD} \times 0.5$ and $C_L$ = 10 pF (unless otherwise noted) (see Figure 1)

| SYMBOL | FROM (INPUT) | TO (OUTPUT) | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | $V_{DD}$ = 2.5 V ±0.2 V | | |
| | | | MIN | MAX | |
| $f_{max}$ | | | 200 | — | MHz |
| $t_{pd}$ | CK and $\overline{CK}$ | Q | 1.1 | 2.8 | ns |
| $t_{PHL}$ | $\overline{RESET}$ | Q | 1.1 | 5 | ns |

## OUTPUT BUFFER CHARACTERISTICS

The following table describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these curves is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application.

| VOLTAGE (V) | PULL-DOWN | | PULL-UP | |
|---|---|---|---|---|
| | I (mA) MIN | I (mA) MAX | I (mA) MIN | I (mA) MAX |
| 0.0 | 0 | 0 | 0 | 0 |
| 0.1 | 7 | 11 | 7 | 10 |
| 0.2 | 14 | 23 | 14 | 20 |
| 0.3 | 21 | 34 | 21 | 30 |
| 0.4 | 28 | 44 | 27 | 40 |
| 0.5 | 33 | 54 | 33 | 49 |
| 0.6 | 39 | 64 | 38 | 59 |
| 0.7 | 44 | 74 | 44 | 68 |
| 0.8 | 48 | 83 | 49 | 76 |
| 0.9 | 52 | 91 | 53 | 84 |
| 1.0 | 56 | 99 | 57 | 93 |
| 1.1 | 59 | 107 | 61 | 100 |
| 1.2 | 61 | 114 | 64 | 108 |
| 1.3 | 63 | 121 | 67 | 115 |
| 1.4 | 64 | 127 | 69 | 121 |
| 1.5 | 66 | 133 | 70 | 128 |
| 1.6 | 66 | 138 | 72 | 134 |
| 1.7 | 67 | 142 | 73 | 139 |
| 1.8 | 67 | 146 | 74 | 144 |
| 1.9 | 67 | 149 | 74 | 148 |
| 2.0 | 67 | 151 | 75 | 152 |
| 2.1 | 68 | 153 | 75 | 156 |
| 2.2 | 68 | 154 | 75 | 159 |
| 2.3 | 68 | 155 | 76 | 161 |
| 2.4 | — | 156 | — | 163 |
| 2.5 | — | 157 | — | 165 |
| 2.6 | — | 157 | — | 167 |
| 2.7 | — | 157 | — | 168 |

## PARAMETER MEASUREMENT INFORMATION

### TEST CIRCUIT

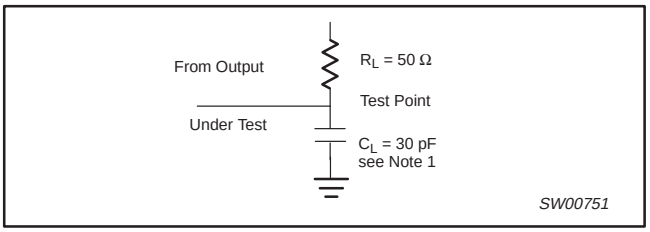
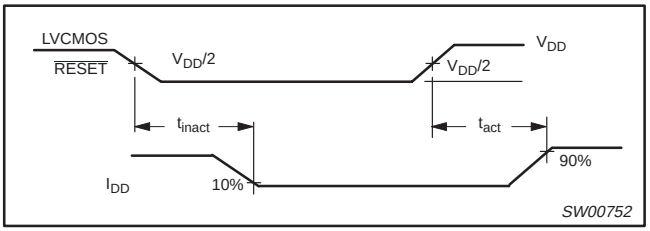


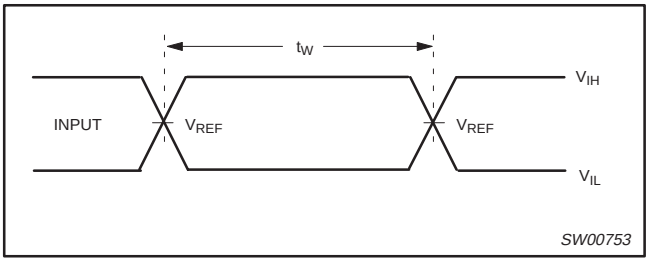

**Figure 1. Load circuitry**

**NOTE:**
1. $C_L$ includes probe and jig capacitance.

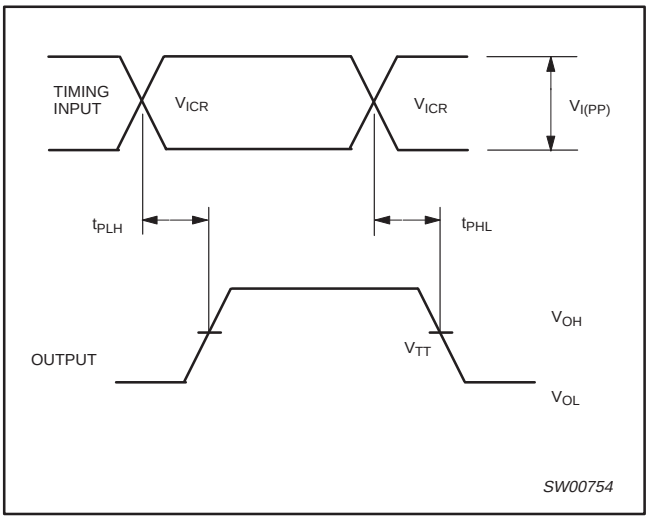
## AC WAVEFORMS



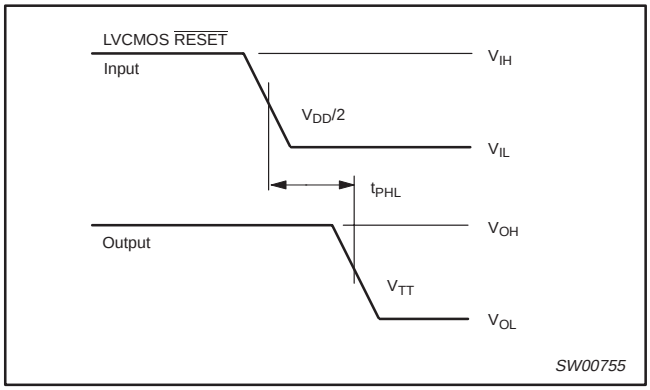

**Waveform 1. Inputs active and inactive times (see Note 1)**



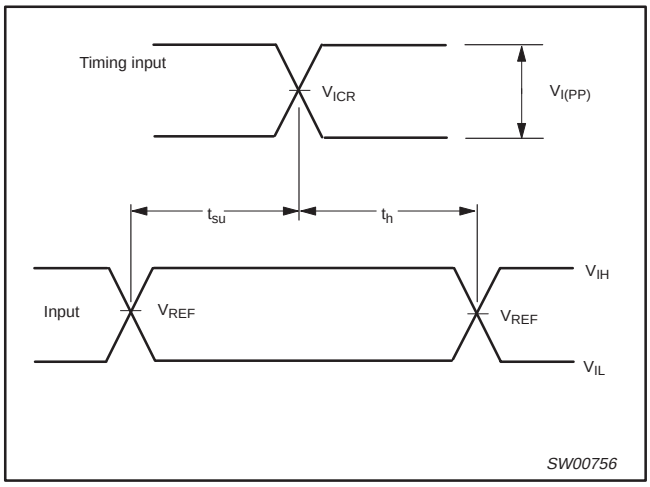

**Waveform 2. Pulse duration**




**Waveform 3. Propagation delay times**



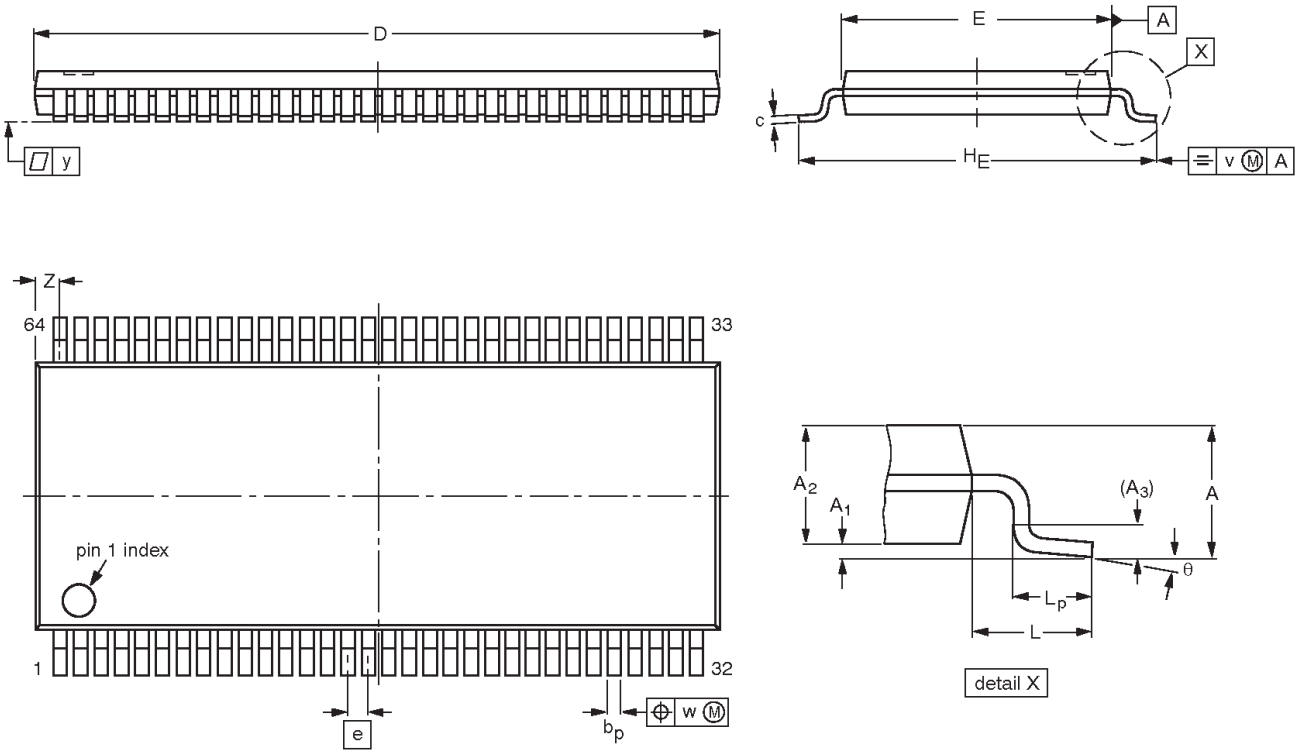

**Waveform 4. Propagation delay times**




**Waveform 5. Setup and hold times**

**NOTES:**
1. $I_{DD}$ tested with clock and data inputs held at $V_{DD}$ or GND, and $I_O$ = 0 mA.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).
3. The outputs are measured one at a time with one transition per measurement.
4. $V_{TT} = V_{REF} = V_{DD}/2$
5. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
6. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. $V_{IL}$ = GND for LVCMOS input.
7. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**TSSOP64: plastic thin shrink small outline package; 64 leads; body width 6.1 mm SOT646-1**




**DIMENSIONS (mm are the original dimensions).**

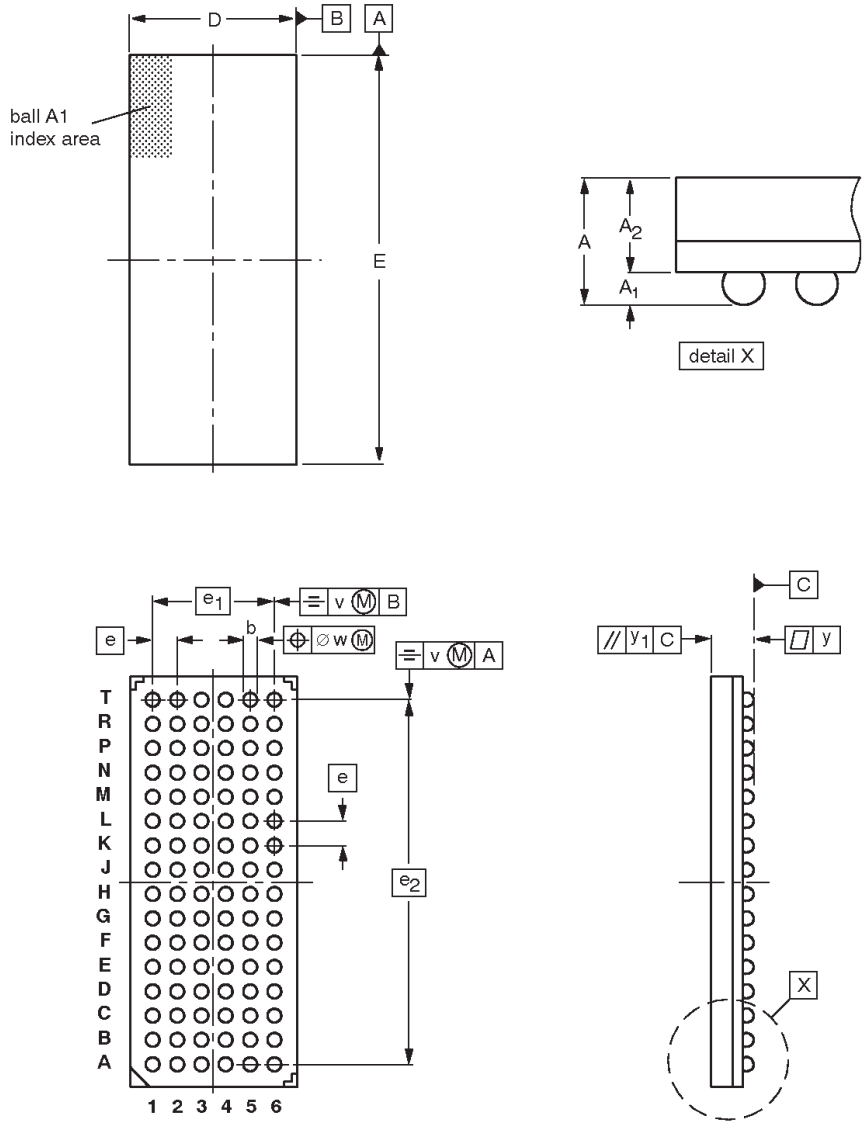
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.27<br>0.17 | 0.2<br>0.1 | 17.1<br>16.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1.0 | 0.75<br>0.45 | 0.2 | 0.08 | 0.1 | 0.89<br>0.61 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

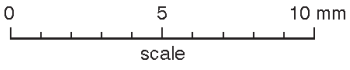
| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT646-1 | | MO-153 | | | | | 00-08-21 |

**LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm** **SOT536-1**



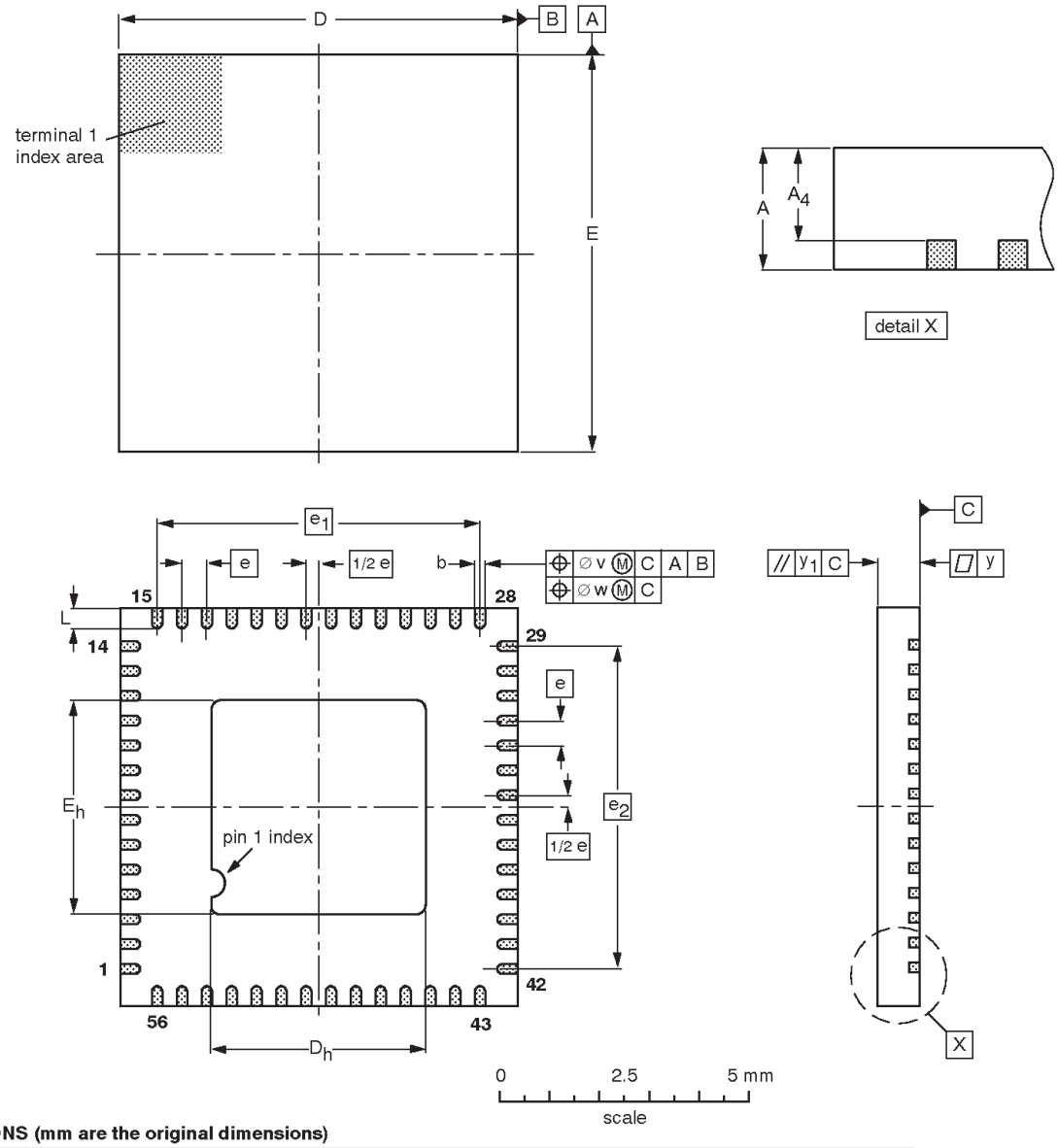

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.5 | 0.41<br>0.31 | 1.2<br>0.9 | 0.51<br>0.41 | 5.6<br>5.4 | 13.6<br>13.4 | 0.8 | 4.0 | 12.0 | 0.15 | 0.1 | 0.1 | 0.2 |




| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT536-1 | | | | | | ~~99-12-02~~<br>00-03-04 |

**HVQFN56: plastic, heatsink very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm** **SOT684-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_4$ max. | b | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.00 | 0.80 | 0.35<br>0.18 | 8.05<br>7.95 | 4.45<br>4.15 | 8.05<br>7.95 | 4.45<br>4.15 | 0.5 | 6.5 | 6.5 | 0.50<br>0.30 | 0.10 | 0.10 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT684-1 | | MO-220 | | | | ~~01-06-12~~<br>01-08-08 |

# 2.5 V 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM

SSTV16859

## Data sheet status

| Data sheet status [1] | Product status [2] | Definitions |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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