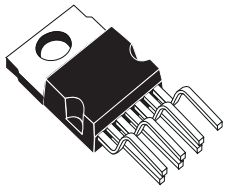
STV8172A

Vertical deflection booster for 3 App TV/monitor applications with 70 V flyback generator

Features

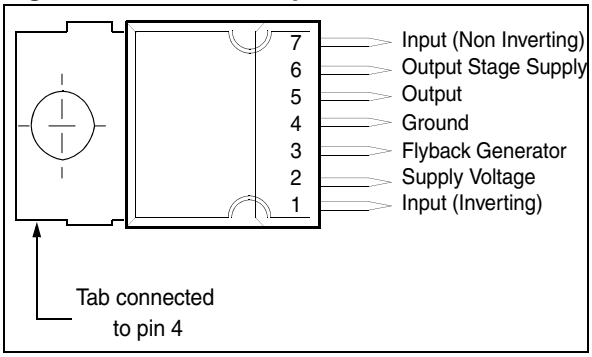
- Power amplifier
- Flyback generator
- Stand-by control
- Output current up to 3.0 App
- Thermal protection

Figure 1. Heptawatt package



Heptawatt
(Plastic Package)
ORDER CODE: STV8172A

Figure 2. STV8172A pin detail



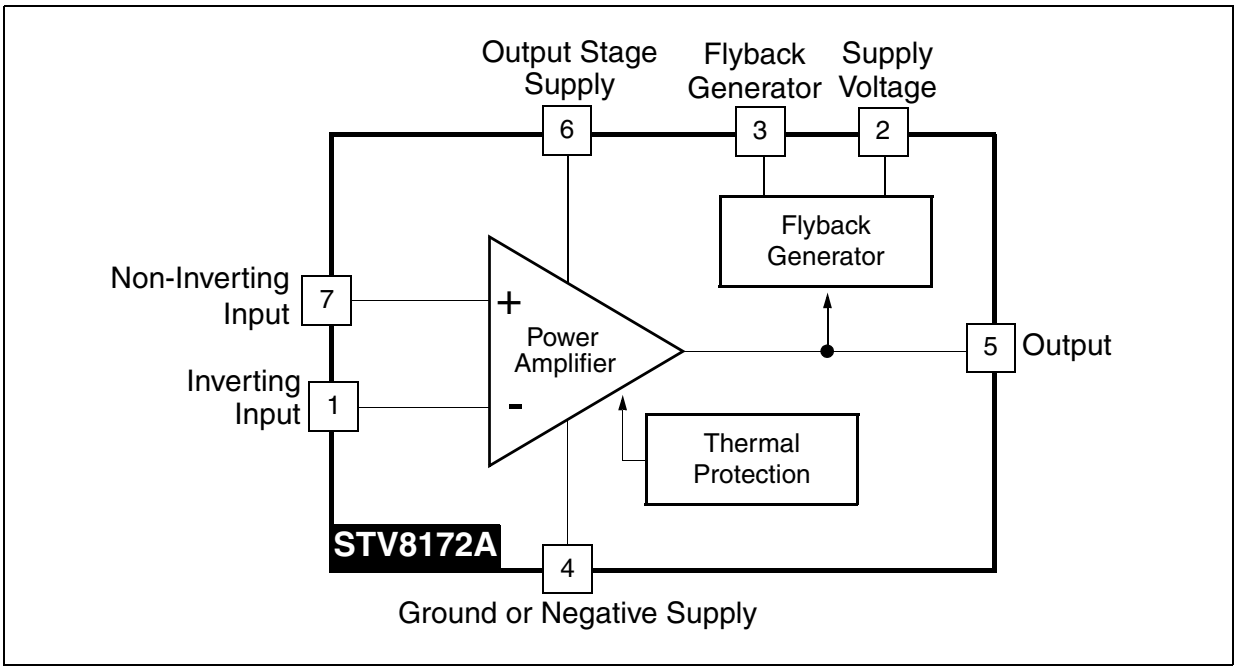
Description

Designed for monitors and high performance TVs, the STV8172A vertical deflection booster delivers flyback voltages up to 70V.

The STV8172A operates with supplies up to 35V and provides up to 3 A_{PP} output current to drive the yoke.

The STV8172A is offered in a Heptawatt plastic package.

In double-supply applications, a stand-by state will be reached by stopping the (+) supply alone.



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1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
Voltage			
V_S	Supply voltage (pin 2) - Note 1 and Note 2	40	V
V_5, V_6	Flyback peak voltage - Note 2	70	V
V_3	Voltage at Pin 3 - Note 2, Note 3 and Note 6	-0.4 to (V_S + 3)	V
V_1, V_7	Amplifier input voltage - Note 2, Note 6 and Note 7	- 0.4 to (V_S + 2) or +40	V
Current			
I_0 (1)	Output peak current at f = 50 to 200 Hz, t ≤10µs - Note 4	±5	A
I_0 (2)	Output peak current non-repetitive - Note 5	±2	A
I_3 Sink	Sink current, t<1ms - Note 3	2	A
I_3 Source	Source current, t < 1ms	2	A
I_3	Flyback pulse current at f=50 to 200 Hz, t≤10µs - Note 4	±5	A
ESD Susceptibility			
ESD1	Human body model (100 pF discharged through 1.5 kΩ)	2	kV
ESD2	EIAJ standard (200 pF discharged through 0 Ω)	300	V
Temperature			
T_s	Storage temperature	-40 to 150	°C
T_j	Junction temperature	+150	°C

Note: 1 Usually the flyback voltage is slightly more than 2 x VS. This must be taken into consideration when setting V_S.

2 Versus pin 4

3 V3 is higher than V_S during the first half of the flyback pulse.

4 Such repetitive output peak currents are usually observed just before and after the flyback pulse.

5 This non-repetitive output peak current can be observed, for example, during the Switch-On/Switch-Off phases. This peak current is acceptable providing the SOA is respected (Figure 10 and Figure 11).

6 All pins have a reverse diode towards pin 4, these diodes should never be forward-biased.

7 Input voltages must not exceed the lower value of either V_S + 2 or 40 volts.

2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-to-case thermal resistance	3	°C/W
T_T	Temperature for thermal shutdown	150	°C
T_J	Recommended max. junction temperature	120	°C

3 Electrical characteristics

V_S = 34 V, T_{AMB} = 25°C, unless otherwise specified.

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Figure
Supply							
V_S	Operating supply voltage range (V_2-V_4)	See note below(1)	10		35	V	
I_2	Pin 2 quiescent current	I_3 = 0, I_5 = 0		5	20	mA	*Figure 3*
I_6	Pin 6 quiescent current	I_3 = 0, I_5 = 0, V_6 =35v	8	19	50	mA	*Figure 3*
Input							
I_1	Input bias current	V_1 = 1 V, V_7 = 2.2 V		- 0.6	-1.5	µA	*Figure 3*
I_7	Input bias current	V_1 = 2.2 V, V_7 = 1 V		- 0.6	-1.5	µA	
V_{IR}	Operating input voltage range		0		V_S - 2	V	
V_{I0}	Offset voltage			2		mV	
$\Delta V_{I0}/dt$	Offset drift versus temperature			10		µV/°C	
Output							
I_0	Operating peak output current	$0^o<T_{case}<125^oC$			±1.25	A	
V_{5L}	Output saturation voltage to pin 4	I_5 = 1.25 A		0.9	1.6	V	*Figure 5*
V_{5H}	Output saturation voltage to pin 6	I_5 = -1.25 A		1.5	2.2	V	*Figure 4*
Standby							
V_{5STBY}	Output voltage in standby	$V_1 = V_7 = V_s = 0$(2)					*Figure 6*
Miscellaneous							
G	Voltage gain		80			dB	
V_{D5-6}	Diode forward voltage between pins 5-6	I_5 = 1.25 A		1.5	2.1	V	
V_{D3-2}	Diode forward voltage between pins 3-2	I_3 = 1.25 A		1.5	2.1	V	
V_{3SL}	Saturation voltage on pin 3	I_3 = 20 mA		0.4	1	V	*Figure 5*
V_{3SH}	Saturation voltage to pin 2 (2nd part of flyback)	I_3 = -1.25 A		1.8	2.6	V	

1. In normal applications, the peak flyback voltage is slightly greater than 2 x (V_S - V_4). Therefore, (V_S - V_4) = 35 V is not allowed without special circuitry.
2. Refer to *Figure 6*, standby condition.

Figure 3. Measurement of I_1, I_2 and I_6

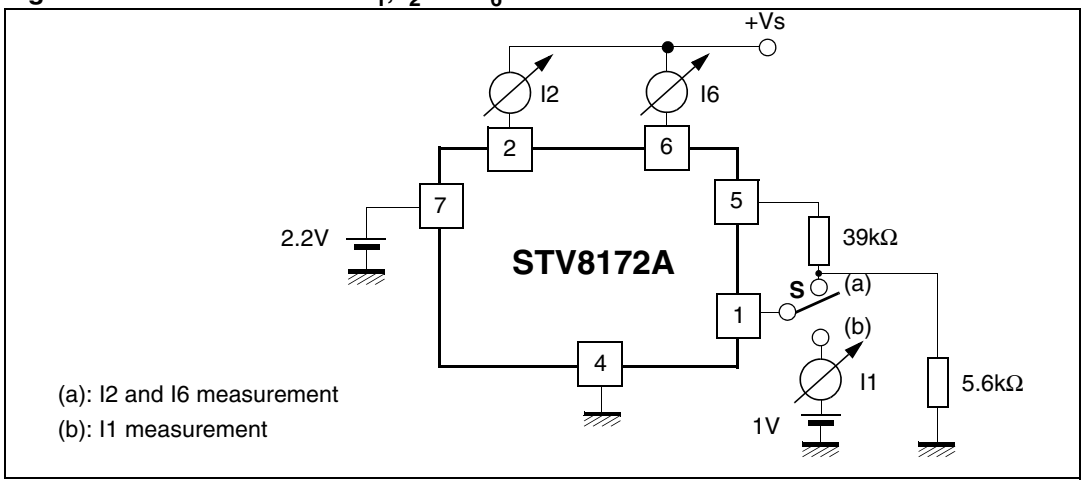


Figure 4. Measurement of V_{5H}

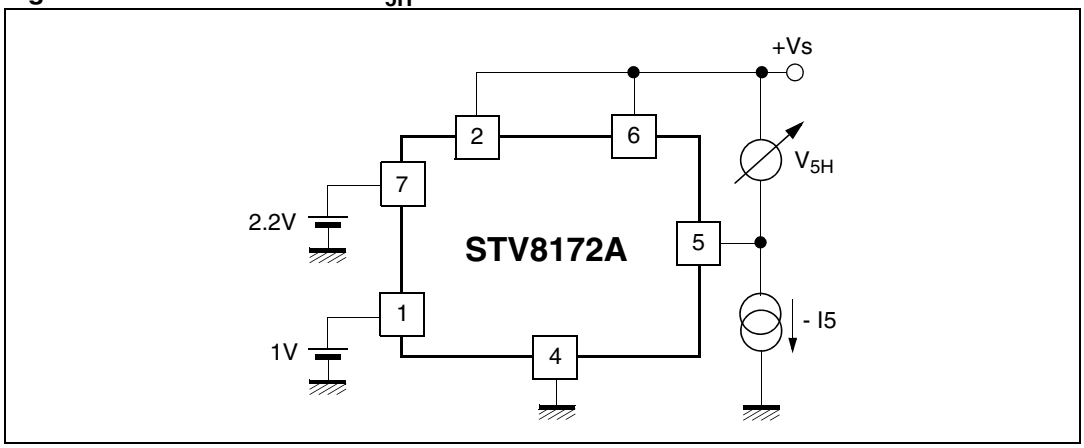
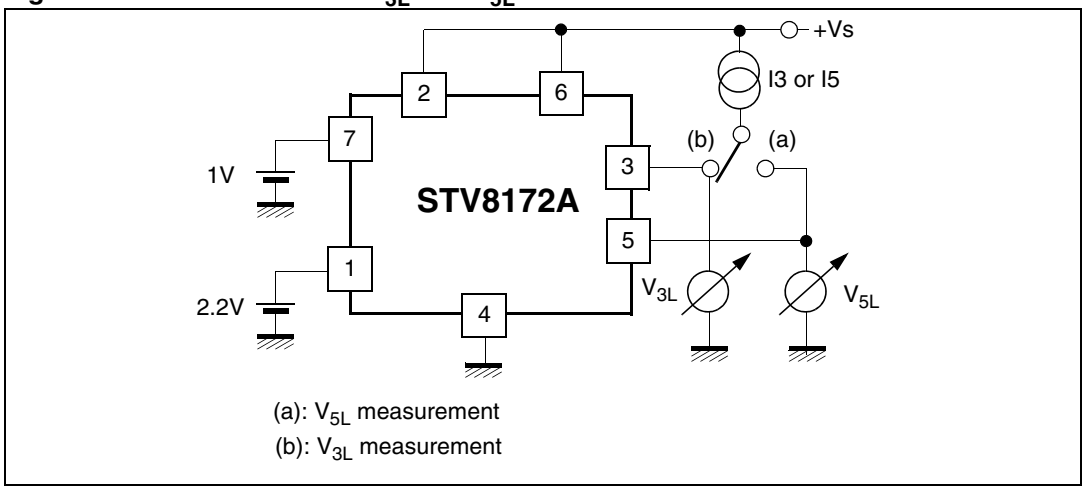


Figure 5. Measurement of V_{3L} and V_{5L}



4 Application hints

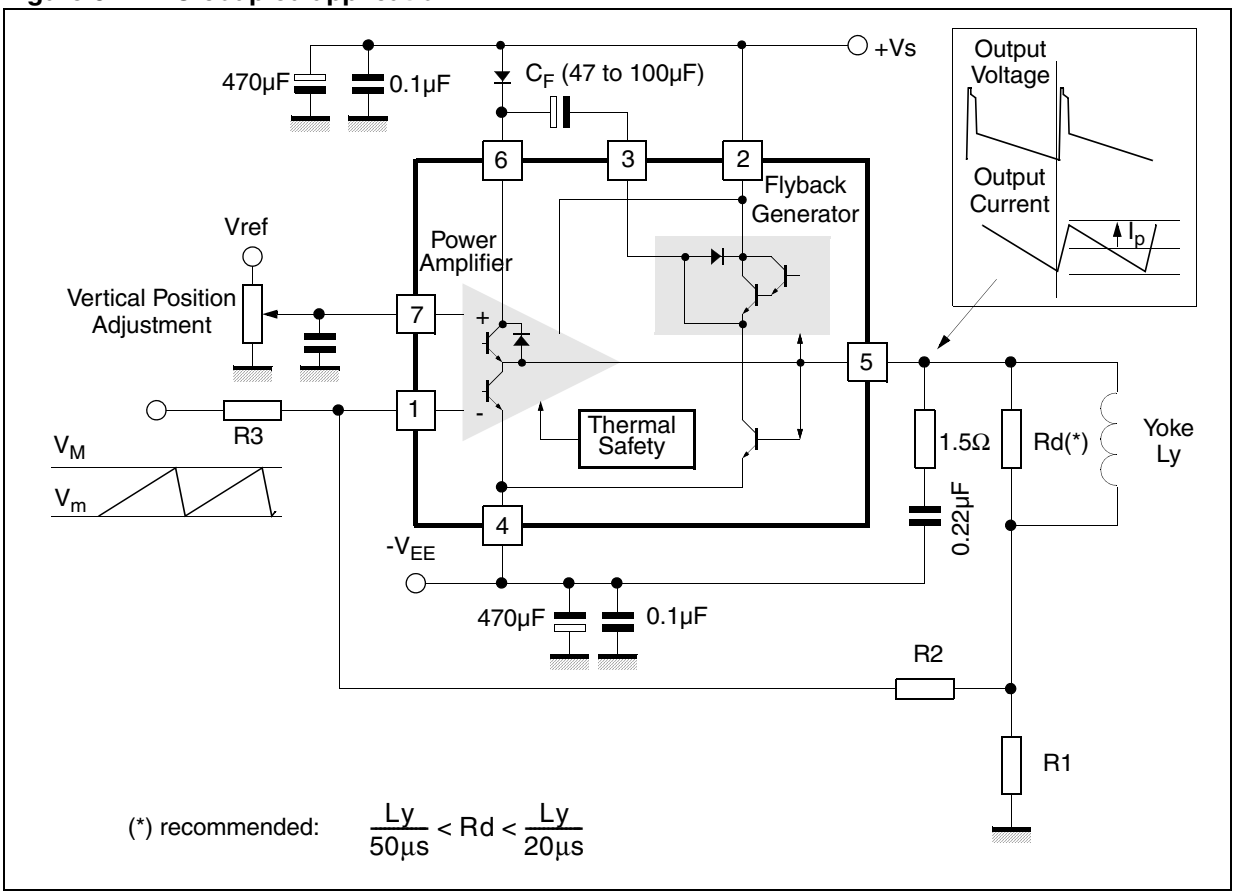
The yoke can be coupled either in AC or DC.

4.1 DC-coupled application

When DC coupled (see *Figure 6*), the display vertical position can be adjusted with input bias. On the other hand, 2 supply sources (V_S and $-V_{EE}$) are required.

A standby state will be reached by switching OFF the positive supply alone. In this state, where both inputs are the same voltage as pin 2 or higher, the output will sink negligible current from the deviation coil.

Figure 6. DC-coupled application



4.1.1 Application hints

For calculations, treat the IC as an op-amp, where the feedback loop maintains $V_1 = V_7$.

Centering

Display will be centered (null mean current in yoke) when voltage on pin 7 is (R_1 is negligible):

$$V_7 = \frac{V_M + V_m}{2} \times \left(\frac{R_2}{R_2 + R_3} \right)$$

Peak current

$$I_P = \frac{(V_M - V_m)}{2} \times \frac{R_2}{R_1 x R_3}$$

Example: for $V_m = 2$ V, $V_M = 5$ V and $I_P = 1$ A

Choose R_1 in the1 Ω range, for instance R_1=1 Ω

From equation of peak current:

$$\frac{R_2}{R_3} = \frac{2 \times I_P \times R_1}{V_M - V_m} = \frac{2}{3}$$

Then choose R_2 or R_3. For instance, if $R_2 = 10$ kΩ, then $R_3 = 15$ kΩ

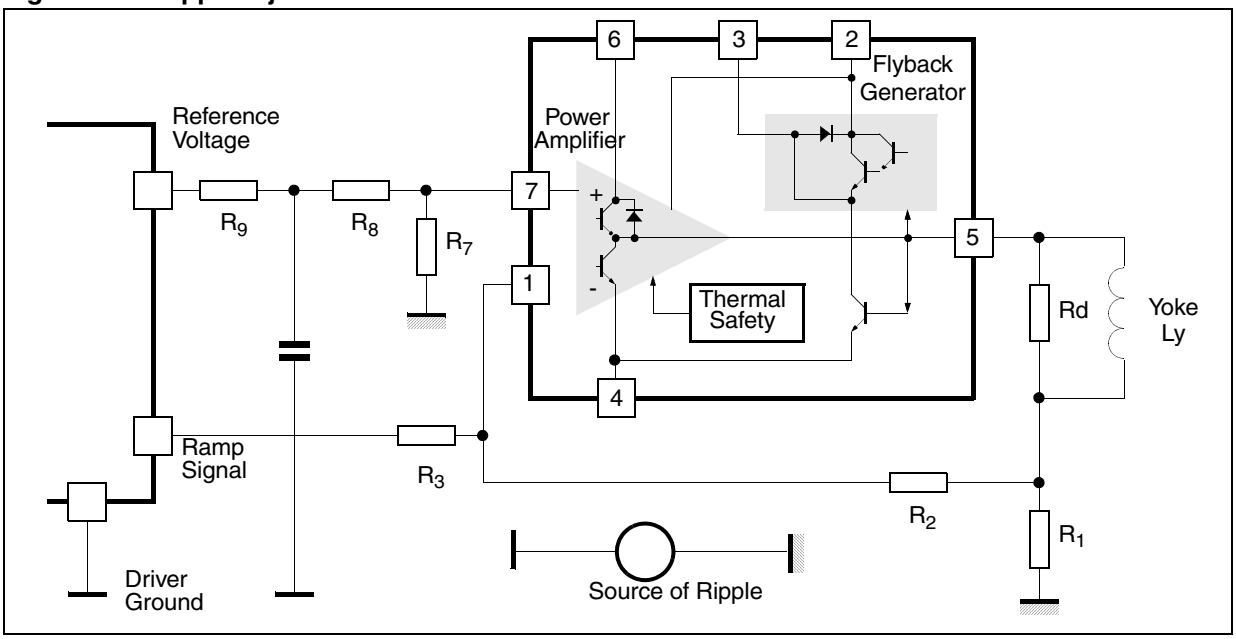
Finally, the bias voltage on pin 7 should be:

$$V_7 = \frac{V_M + V_m}{2} \times \frac{1}{1 + \frac{R_3}{R_2}} = \frac{7}{2} \times \frac{1}{2.5} = 1.4V$$

4.1.2 Ripple rejection

When both ramp signal and bias are provided by the same driver IC, you can gain natural rejection of any ripple caused by a voltage drop in the ground (see *Figure 7*), if you manage to apply the same fraction of ripple voltage to both booster inputs. For that purpose, arrange an intermediate point in the bias resistor bridge, such that (R_8 / R_7) = (R_3 / R_2), and connect the bias filtering capacitor between the intermediate point and the local driver ground. Of course, R_7 should be connected to the booster reference point, which is the ground side of R_1.

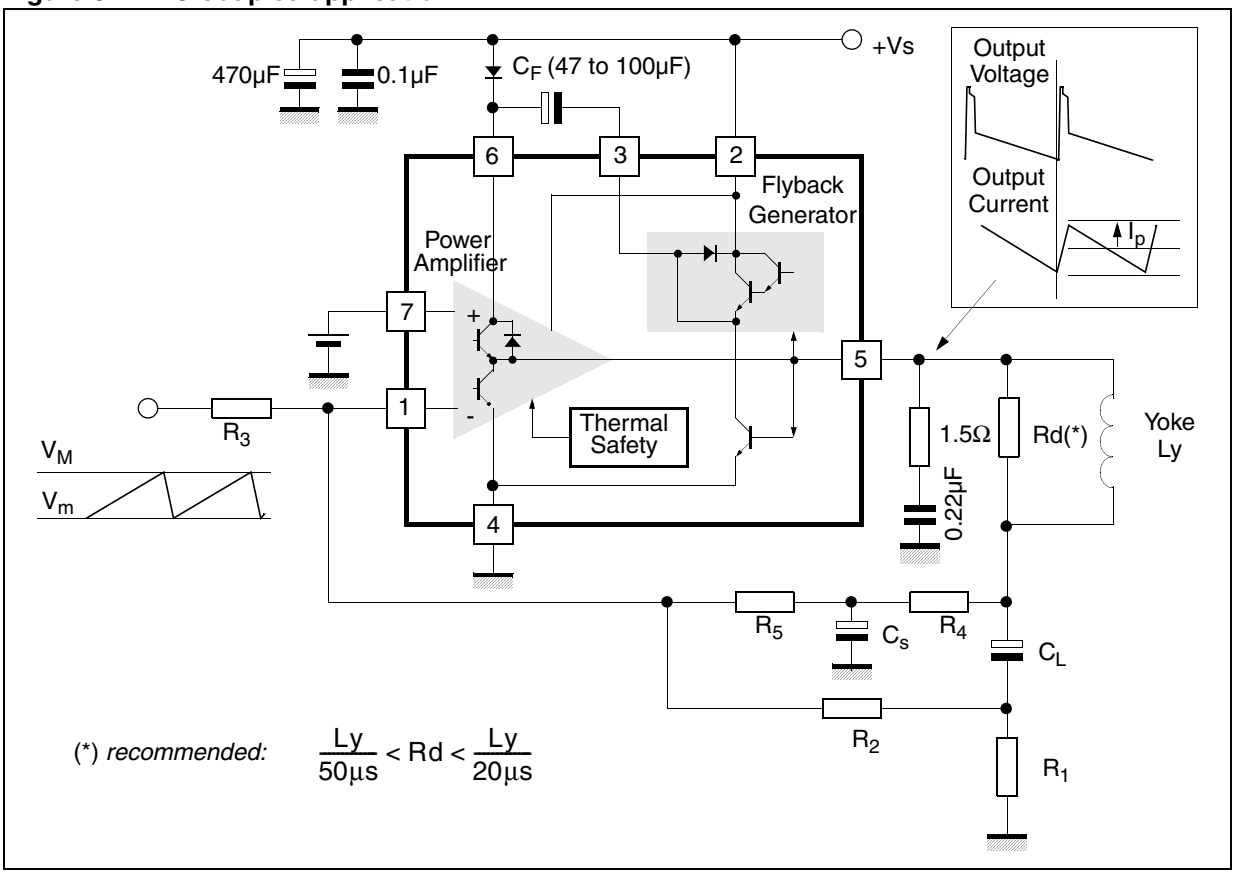
Figure 7. Ripple rejection



4.2 AC-coupled applications

In AC-coupled applications (see *Figure 8*), only one supply (V_S) is needed. The vertical position of the scanning cannot be adjusted with input bias (for that purpose, usually some current is injected or sunk with a resistor in the low side of the yoke).

Figure 8. AC-coupled application



4.2.1 Application hints

Gain is defined as in the previous case:

$$I_p = \frac{V_M - V_m}{2} \times \frac{R_2}{R_1 \times R_3}$$

Choose R_1 then either R_2 or R_3. For good output centering, V_7 must fulfill the following equation:

$$\frac{\frac{V_S}{2} - V_7}{R_4 + R_5} = \frac{V_7 - \frac{V_M + V_m}{2}}{R_3} + \frac{V_7}{R_2}$$

or

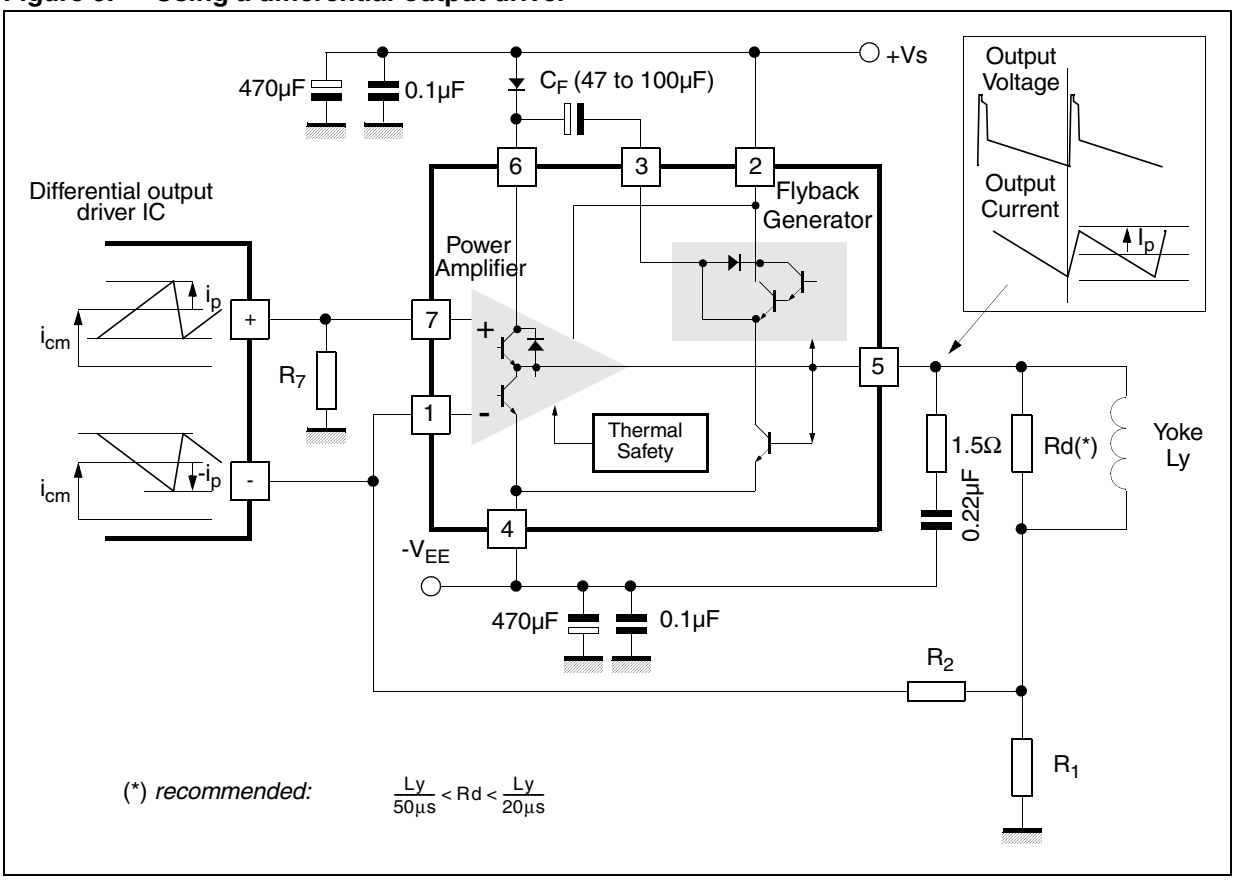
$$V_7 \times \left(\frac{1}{R_3} + \frac{1}{R_2} + \frac{1}{R_4 + R_5}\right) = \left(\frac{V_S}{2(R_4 + R_5)} + \frac{V_M + V_m}{2 \times R_3}\right)$$

C_S performs an integration of the parabolic signal on C_L, therefore the amount of S correction is set by the combination of C_L and C_s.

4.3 Application with differential-output drivers

Certain driver ICs provide the ramp signal in differential form, as two current sources i_+ and i_with opposite variations.

Figure 9. Using a differential-output driver



Some definitions:

- i_{cm} is the common-mode current: $i_{cm} = \frac{1}{2}(i_+ + i_-)$
- at peak of signal, $i_+ = i_{cm} + i_p$ and $i_- = i_{cm} - i_p$, therefore the peak differential signal is $i_p - (-i_p) = 2\,i_p$, and the peak-peak differential signal, $4i_p$.

The application is described in *Figure 9* with DC yoke coupling. The calculations still rely on the fact that V_1 remains equal to V_7.

4.3.1 Centering

When idle, both driver outputs provide i_{cm} and the yoke current should be null (R_1 is negligible), hence:

$$i_{cm} \cdot R_7 = i_{cm} \cdot R_2 \quad \text{therefore} \quad R_7 = R_2$$

4.3.2 Peak current

Scanning current should be I_P when positive and negative driver outputs provide respectively i_{cm} - i_p and i_{cm} + i_p, therefore

$$(i_{cm} - i) \cdot R_7 = I_p \cdot R_1 + (i_{cm} + i) \cdot R_2$$

and since $R_7 = R_2$

$$\frac{I_p}{i} = -\frac{2R_7}{R_1}$$

Choose R_1 in the 1Ω range, the value of $R_2 = R_7$ follows. Remember that i is one-quarter of driver peak-peak differential signal! Also check that the voltages on the driver outputs remain inside allowed range.

Example:

for i_{cm} = 0.4mA, i = 0.2mA (corresponding to 0.8mA of peak-peak differential current), I_p = 1A

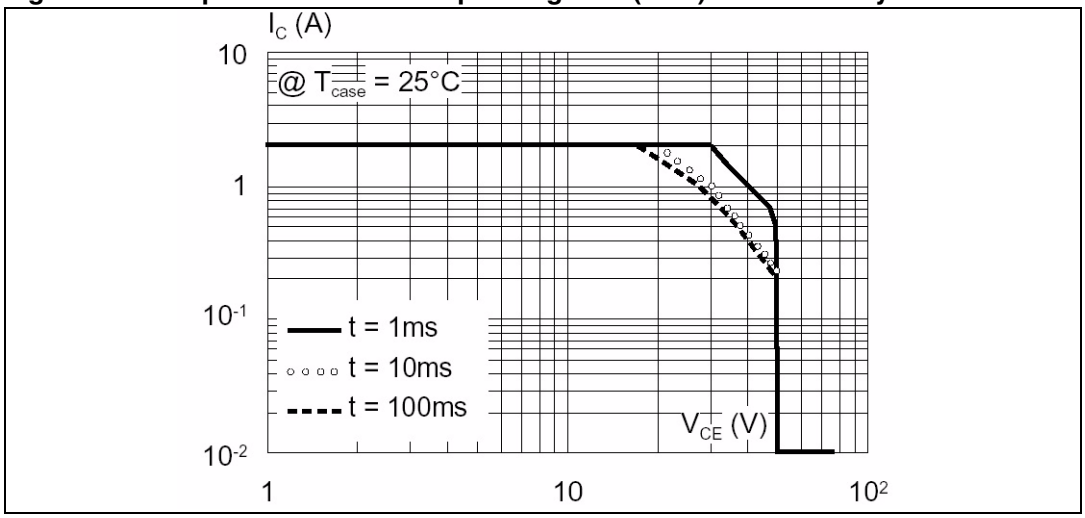
Choose R_1 = 0.75Ω, it follows $R_2 = R_7$ = 1.875kΩ

4.3.3 Ripple rejection

Make sure to connect R_7 directly to the ground side of R_1.

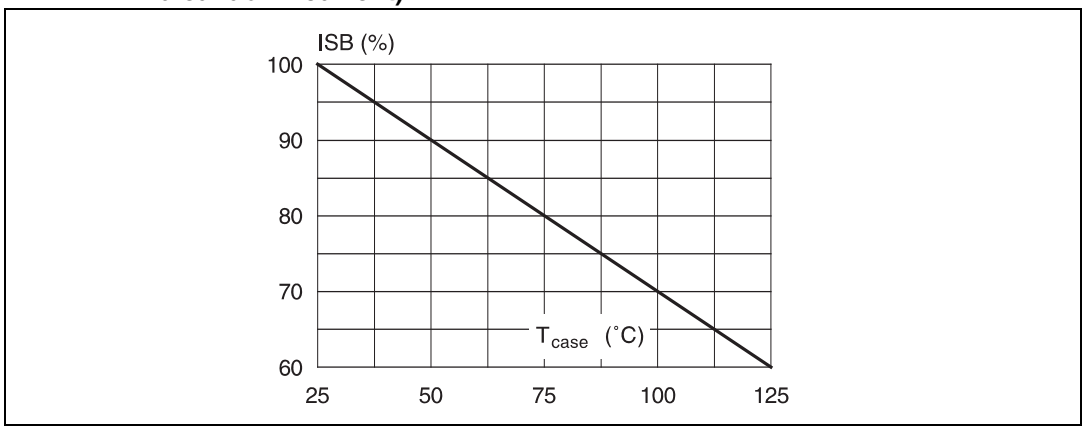
4.3.4 Secondary breakdown diagrams

Figure 10. Output transistor safe operating area (SOA) for secondary breakdown



The diagram has been arbitrarily limited to max I0 (2A).

Figure 11. Secondary breakdown temperature derating curve (ISB = secondary breakdown current)

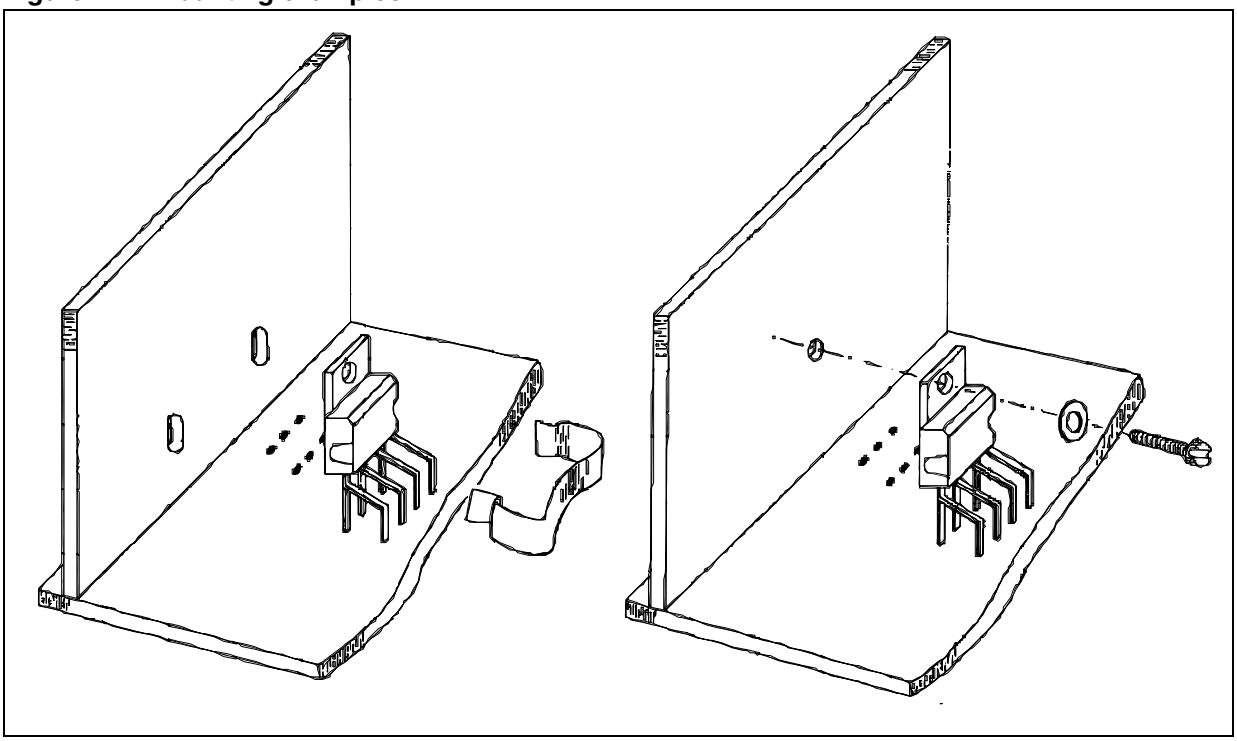


5 Mounting instructions

The power dissipated in the circuit is removed by adding an external heatsink. With the Heptawatt package, the heatsink is simply attached with a screw or a compression spring (clip).

A layer of silicon grease inserted between heatsink and package optimizes thermal contact. In DC-coupled applications we recommend to use a silicone tape between the device tab and the heatsink to electrically isolate the tab.

Figure 12. Mounting examples



6 Pin configuration

Figure 13. Pins 1 and 7

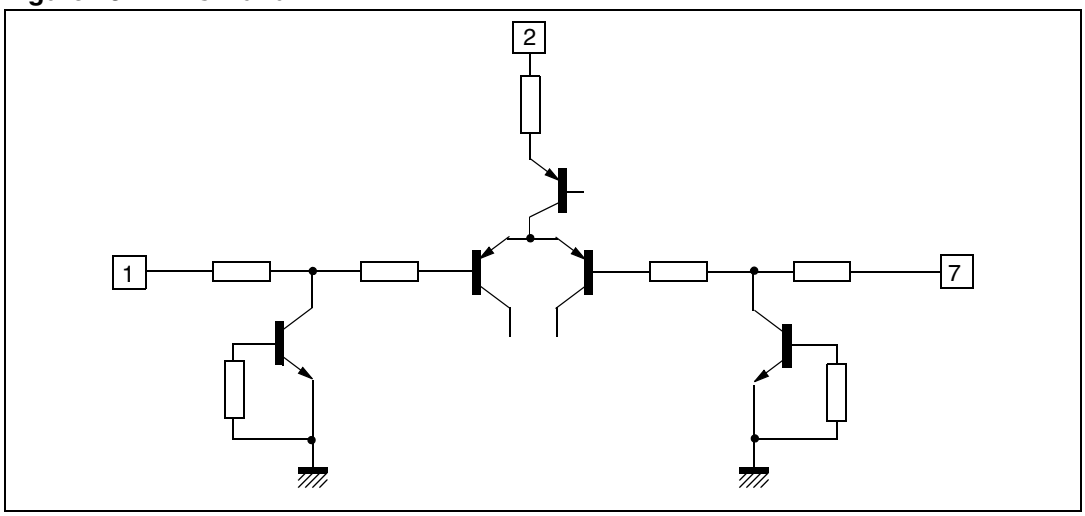
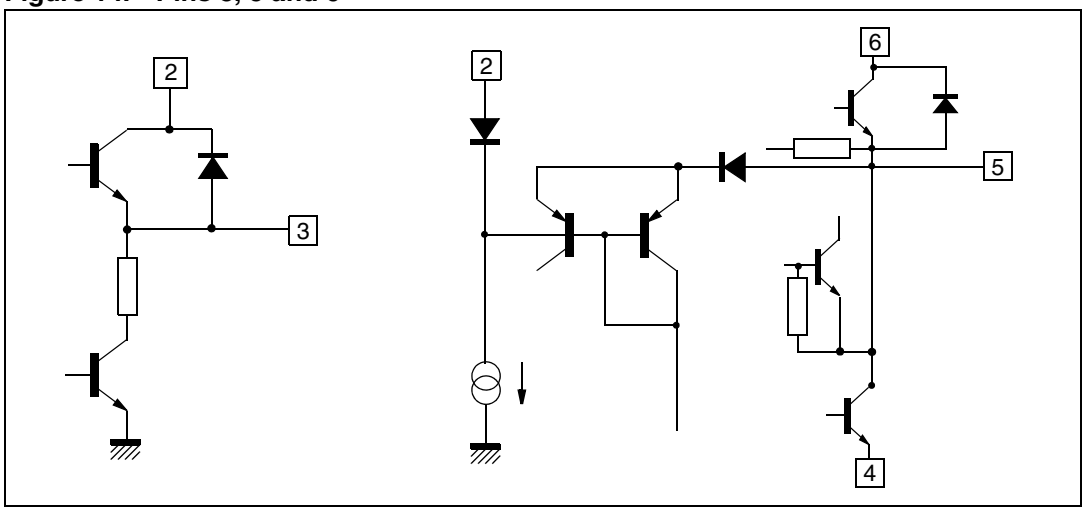


Figure 14. Pins 3, 5 and 6



7 Package mechanical data

Figure 15. 7-pin Heptawatt package

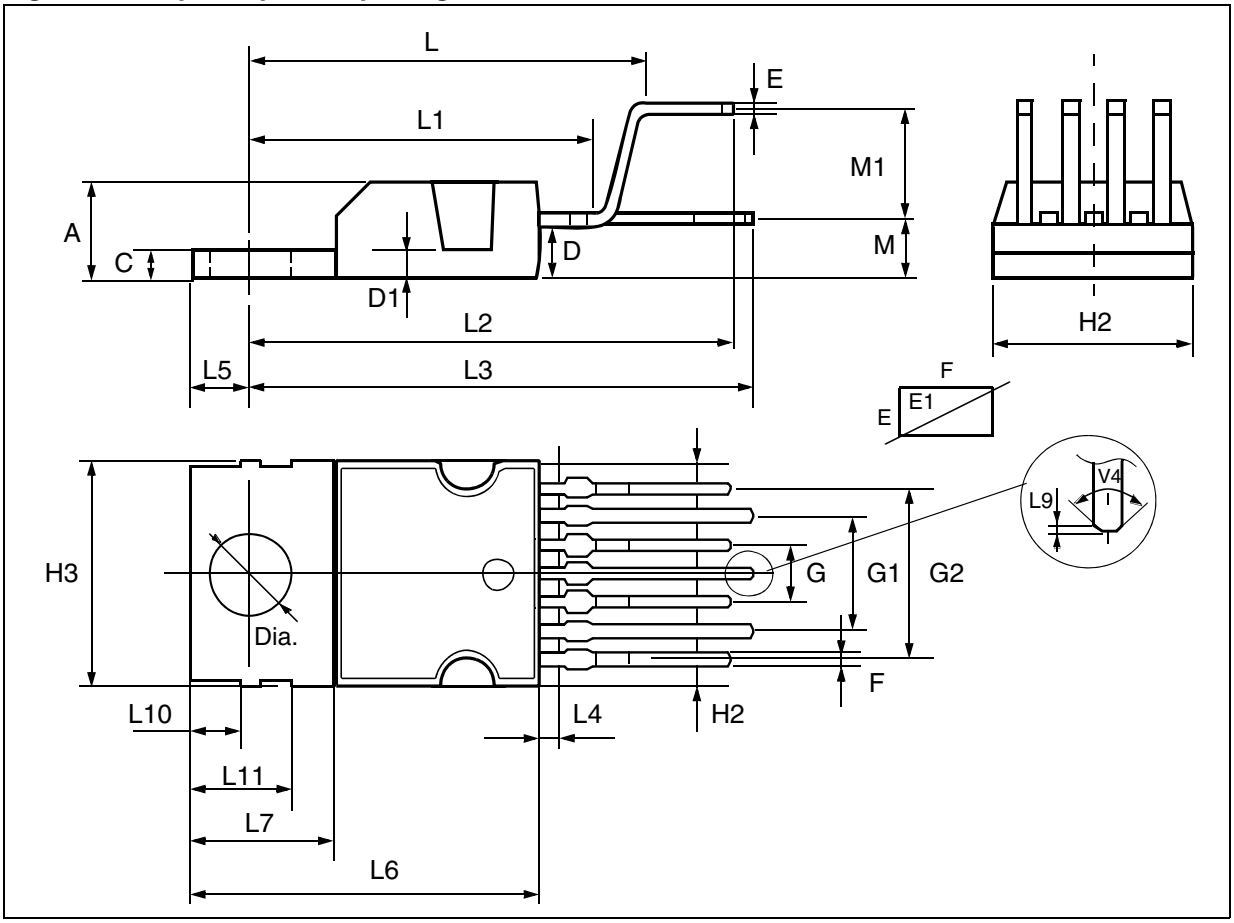


Table 4. Heptawatt package

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.40		2.80	0.094		0.110
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.70		0.97	0.028		0.038
F	0.60		0.80	0.024		0.031

Table 4. Heptawatt package (continued)

Dim.	mm			inches		
G	2.34	2.54	2.74	0.095	0.100	0.105
G1	4.88	5.08	5.28	0.193	0.200	0.205
G2	7.42	7.62	7.82	0.295	0.300	0.307
H2			10.40			0.409
H3	10.05		10.40	0.396		0.409
L	16.70	16.90	17.10	0.657	0.668	0.673
L1		14.92			0.587	
L2	21.24	21.54	21.84	0.386	0.848	0.860
L3	22.27	22.52	22.77	0.877	0.891	0.896
L4			1.29			0.051
L5	2.60	2.80	3.00	0.102	0.110	0.118
L6	15.10	15.50	15.80	0.594	0.610	0.622
L7	6.00	6.35	6.60	0.0236	0.250	0.260
L9		0.20			0.008	
L10	2.10		2.70	0.082		0.106
L11	4.30		4.80	0.169		0.190
M	2.55	2.80	3.05	0.100	0.110	0.120
M1	4.83	5.08	5.33	0.190	0.200	0.210
V4	40 (Typ.)					
Dia.	3.65		3.85	0.144		0.152

7.1 Lead-free packaging

To meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com.*

8 Revision history

Table 5. Document revision history

Date	Revision	Changes
August 2003	1	First issue.
November 2003	1.1	Datasheet status changed to preliminary data.
December 2003	1.2	Modification to *Figure 13*.
June 2004	1.3	Datasheet status changed to datasheet.
February 2005	2	Updated *Figure 9*.
March 2005	3	Status changed to datasheet.
13-Nov-2008	4	*Section 7.1* added, new template applied.

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