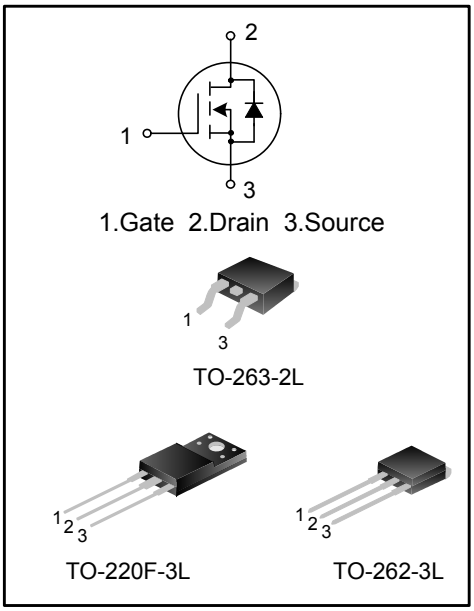
12A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF12N60F/S/K is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 12A,600V,$R_{DS(on)(typ.)}$=0.58Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF12N60F	TO-220F-3L	SVF12N60F	Pb free	Tube
SVF12N60S	TO-263-2L	SVF12N60S	Halogen free	Tube
SVF12N60STR	TO-263-2L	SVF12N60S	Halogen free	Tape&Reel
SVF12N60K	TO-262-3L	SVF12N60K	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVF12N60F	SVF12N60S	SVF12N60K	
Drain-Source Voltage		V_{DS}	600			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	12			A
	T_C=100°C		7.6			
Drain Current Pulsed		I_{DM}	48			A
Power Dissipation(T_C=25°C)		P_D	51	180	213	W
-Derate above 25°C			0.41	1.44	1.7	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	798			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF12N60F	SVF12N60S	SVF12N60K	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.44	0.69	0.59	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=6.0A	--	0.58	0.75	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	--	1367	--	pF
Output Capacitance	C_{oss}		--	152	--	
Reverse Transfer Capacitance	C_{rss}		--	14.0	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=12A, V_{GS}=10V ,R_G=24Ω (Note 2,3)	--	24.33	--	ns
Turn-on Rise Time	t_r		--	51.93	--	
Turn-off Delay Time	$t_{d(off)}$		--	87.93	--	
Turn-off Fall Time	t_f		--	47.73	--	
Total Gate Charge	Q_g	V_{DS}=480V, I_D=12A, V_{GS}=10V (Note 2,3)	--	33..5	--	nC
Gate-Source Charge	Q_{gs}		--	7.57	--	
Gate-Drain Charge	Q_{gd}		--	15.2	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	12	A
Pulsed Source Current	I_{SM}		--	--	48	
Diode Forward Voltage	V_{SD}	I_S=12A,V_{GS}=0V	--	--	1.3	V
Reverse Recovery Time	T_{rr}	I_S=12A,V_{GS}=0V, dI_F/dt=100A/μS (Note 2)	--	530	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.8	--	μC

Notes:

1. L=30mH, I_{AS}=6.66A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

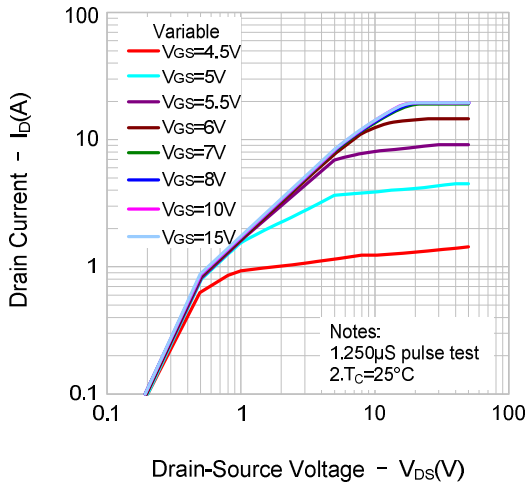


Figure 2. Transfer Characteristics

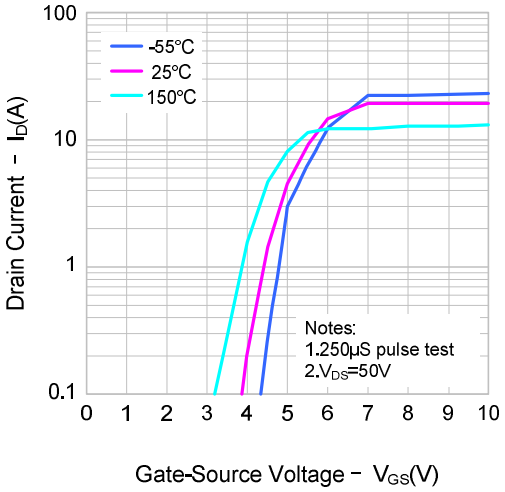


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

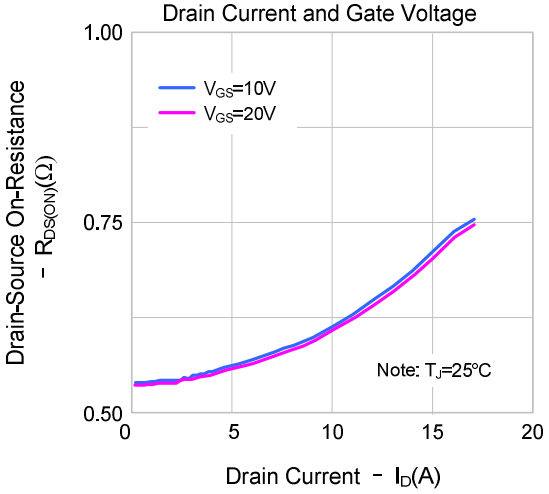
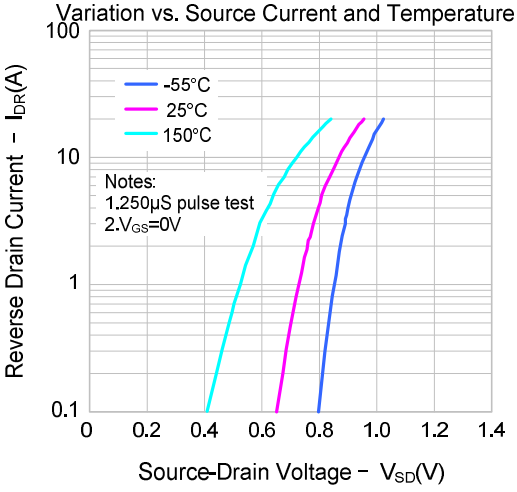


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

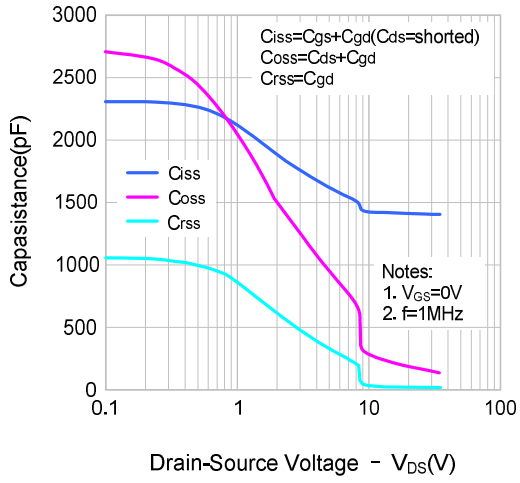


Figure 6. Gate Charge Characteristics

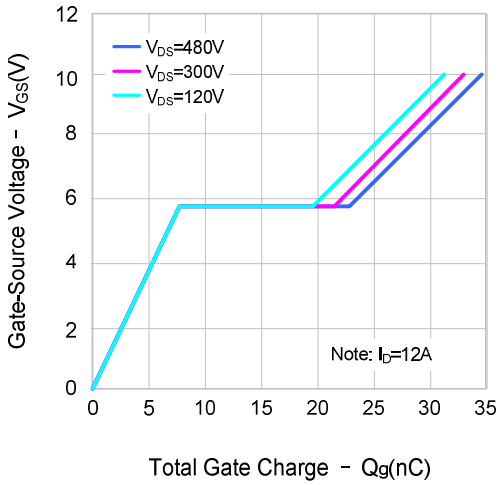


Figure 7. Breakdown Voltage Variation vs. Temperature

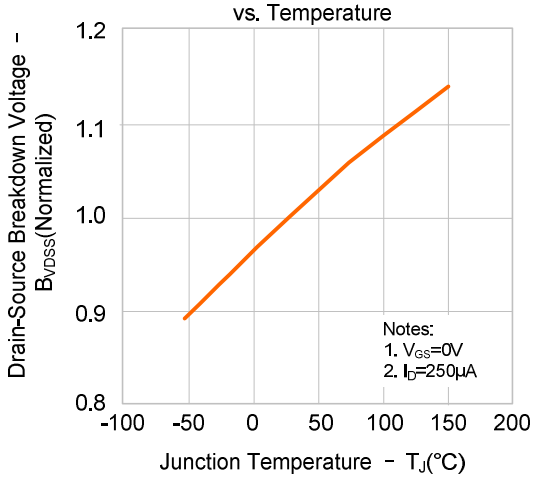


Figure 8. On-resistance Variation vs. Temperature

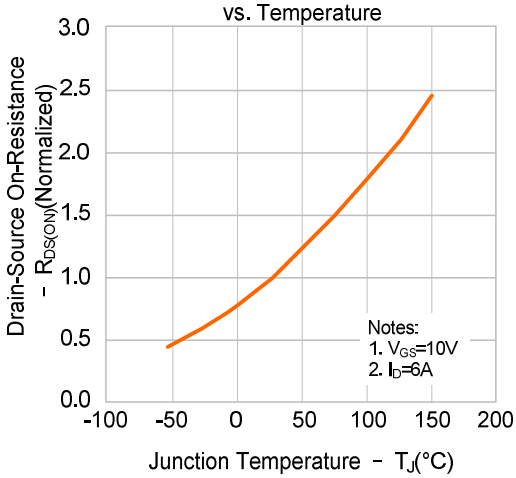


Figure 9-1. Max. Safe Operating Area(SVF12N60F)

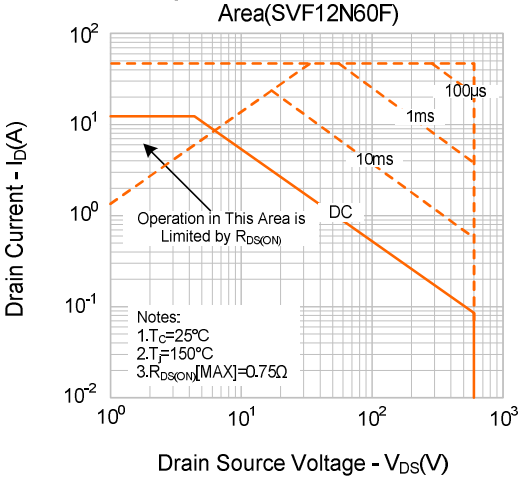
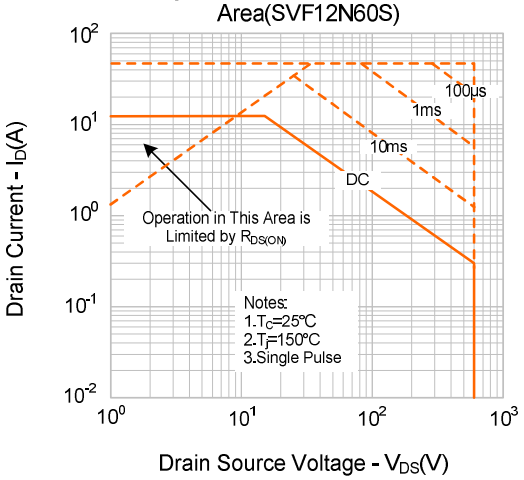


Figure 9-2. Max. Safe Operating Area(SVF12N60S)



TYPICAL CHARACTERISTICS(continued)

Figure 9-3. Max. Safe Operating Area(SVF12N60K)

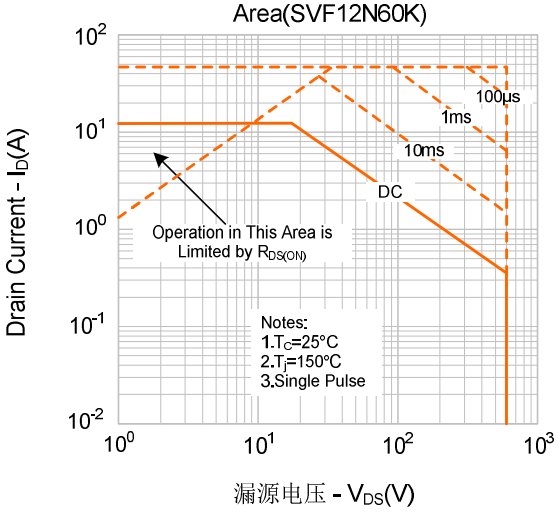
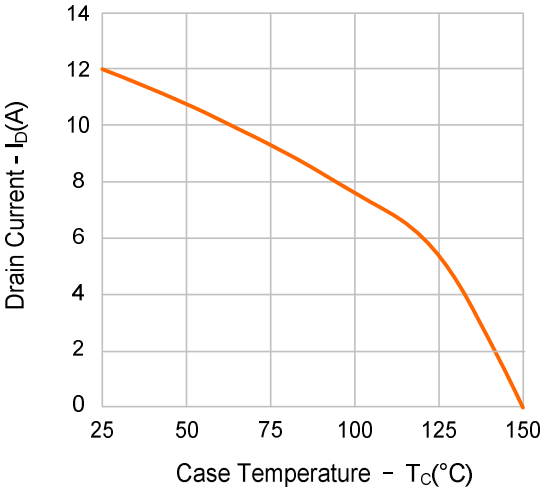
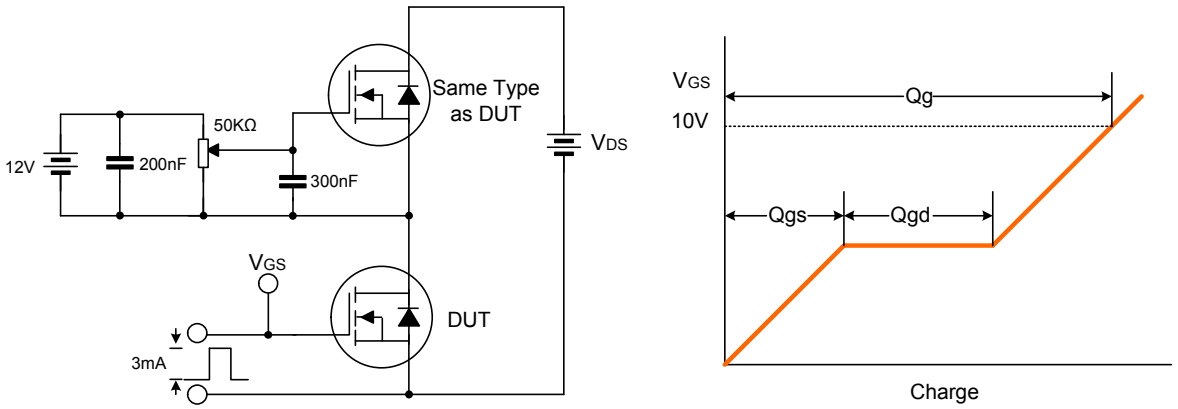


Figure 10. Maximum Drain Current vs. Case Temperature

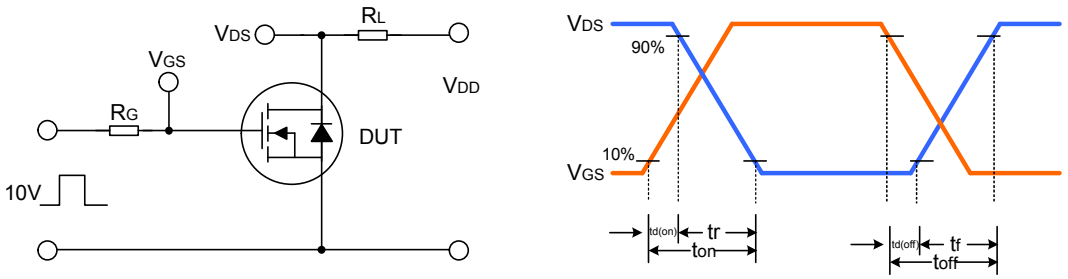


TYPICAL TEST CIRCUIT

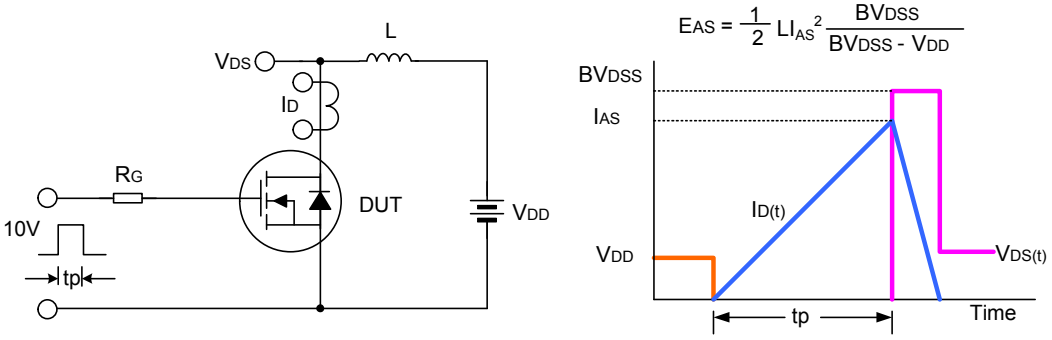
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



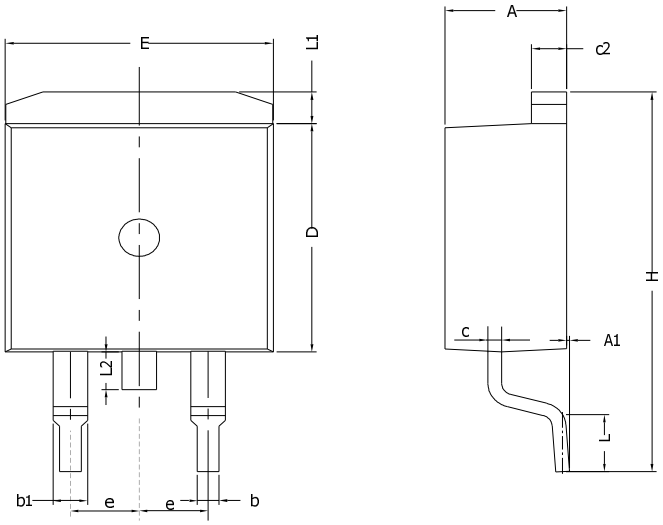
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-263-2L

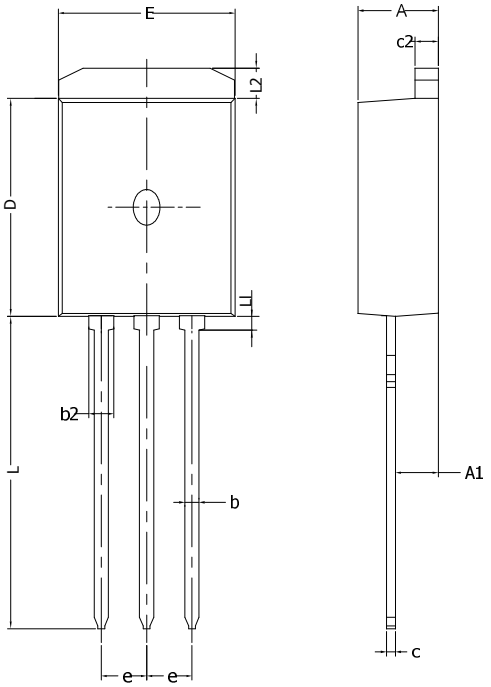
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

TO-262-3L

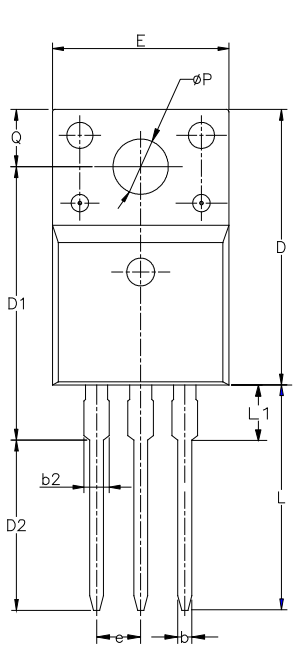
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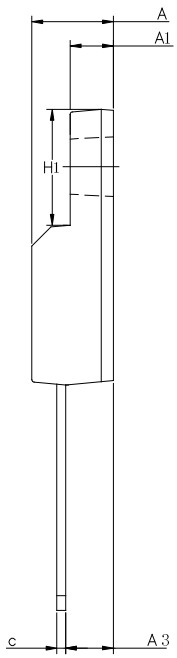


SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	---	2.92
b	0.71	0.80	0.90
b2	1.20	---	1.50
c	0.34	---	0.65
c2	1.22	1.30	1.35
D	8.38	---	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	---	14.10
L1	---	---	0.75
L2	1.12	---	1.42

PACKAGE OUTLINE(continued)

TO-220F-3L **UNIT: mm**





SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Part No.:	SVF12N60F/S/K	Document Type:	Datasheet
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Rev.: 2.5
Revision History:
1. Update the package outline of TO-262-3L

Rev.: 2.4
Revision History:
1. Delete the package outline of TO-220-3L

Rev.: 2.3
Revision History:
1. Add another solid figure of TO-220-3L
2. Update the package outline of TO-262-3L and TO-263-2L

Rev.: 2.2
Revision History:
1. Modify the Electrical characteristics

Rev.: 2.1
Revision History:
1. Modify the ordering information
2. Modify the package information of TO-220-3L

Rev.: 2.0
Revision History:
1. Modify the package information

Rev.: 1.9
Revision History:
1. Modify the thermal characteristics

Rev.: 1.8
Revision History:
1. Modify the ordering information

Rev.: 1.7
Revision History:
1. Change the schematic diagram of MOS

Rev.: 1.6
Revision History:
1. Modify “PACKAGE OUTLINE”

Rev.: 1.5
Revision History:
1. Add the package of TO-262-3L

Rev.: 1.4
Revision History:

1. Modify the typ. value of $R_{DS(on)}$

Rev.: 1.3

Revision History:

1. Modify the value of T_{rr} and Q_{rr}
2. Modify the value of capacitance
3. Modify the figure 5

Rev.: 1.2

Revision History:

1. Add the halogen free information of SVF12N60F

Rev.: 1.1

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.0

Revision History:

1. Original