TDA8768A

12-bit, 70 Msps Analog-to-Digital Converter (ADC)

Rev. 02 — 03 July 2002 **Product data**

1. Description

The TDA8768AH is a biCMOS 12-bit Analog-to-Digital Converter (ADC) optimized for GSM and EDGE cellular infrastructures, professional telecommunications and imaging, and advanced FM radio. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 70 MHz. All static digital inputs (SH, $\overline{CE}$ and OTC) are TTL and CMOS compatible and all outputs are CMOS compatible. A sine wave clock input signal can also be used.

2. Features

- 12-bit resolution
- Sampling rate up to 70 MHz
- –3 dB bandwidth of 245 MHz
- 5 V power supplies and 3.3 V output power supply
- Binary or twos complement CMOS outputs
- In-range CMOS compatible output
- TTL and CMOS compatible static digital inputs
- TTL and CMOS compatible digital outputs
- Differential AC or PECL clock input; TTL compatible
- Power dissipation 550 mW (typical)
- Low analog input capacitance (typical 2 pF), no buffer amplifier required
- Integrated sample-and-hold amplifier
- Differential analog input
- External amplitude range control
- Voltage controlled regulator included
- –40 °C to +85 °C ambient temperature.

3. Applications

- High-speed analog-to-digital conversion for:
  - Cellular infrastructure (GSM and EDGE)
  - Professional telecommunication
  - Advanced FM radio
  - Radar
  - Imaging (camera scanner)
  - Set Top Box (STB)
  - Medical imaging.

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4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	3.6	V
I_{CCA}	analog supply current		-	78	87	mA
I_{CCD}	digital supply current		-	27	30	mA
I_{CCO}	output supply current	f_{CLK} = 20 MHz f_i = 400 kHz	-	3	4	mA
INL	integral non-linearity	f_{CLK} = 20 MHz f_i = 400 kHz	-	±2.6	±4.5	LSB
DNL	differential non-linearity (no missing code)	f_{CLK} = 20 MHz f_i = 400 kHz	-	±0.5	+1.1 – 0.95	LSB
$f_{CLK(max)}$	maximum clock frequency		-	-	-	-
	TDA8768AH/4		40	-	-	MHz
	TDA8768AH/5		55		-	MHz
	TDA8768AH/7		70	-	-	MHz
P_{tot}	total power dissipation	f_{CLK} = 55 MHz f_i = 20 MHz	-	550	660	mW

5. Ordering information

Table 2: Ordering information

Type number	Package			Sampling frequency (MHz)
	Name	Description	Version	
TDA8768AH/4	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	40
TDA8768AH/5				55
TDA8768AH/7				70

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6. Block diagram

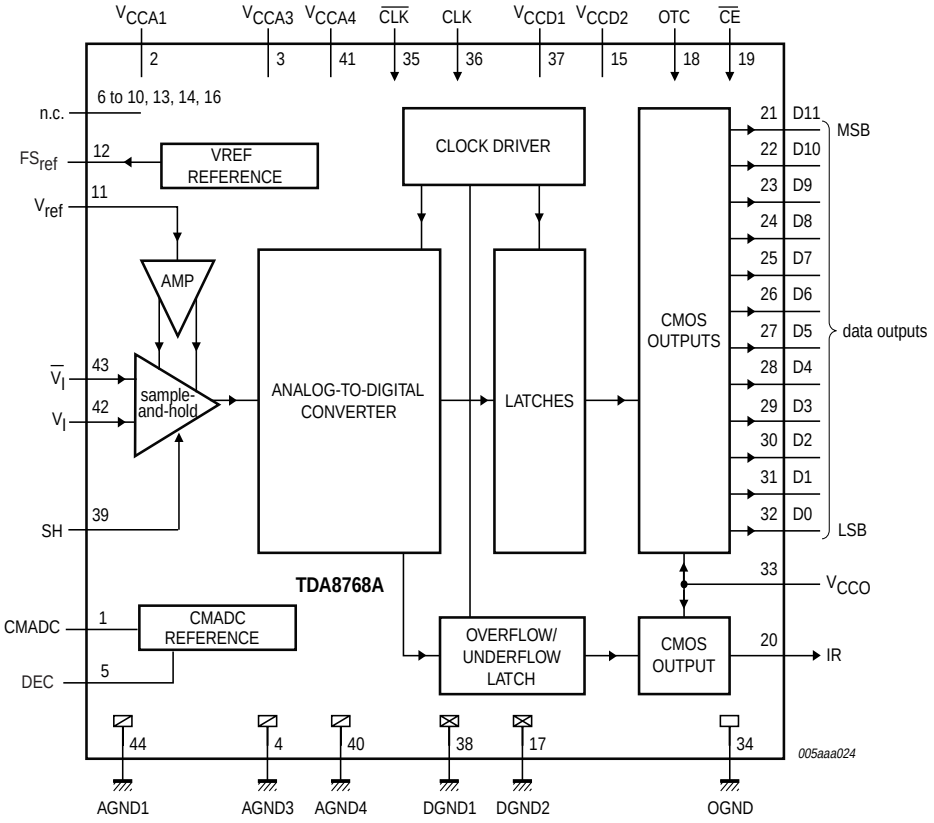


Fig 1. Block diagram.

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7. Pinning information

7.1 Pinning

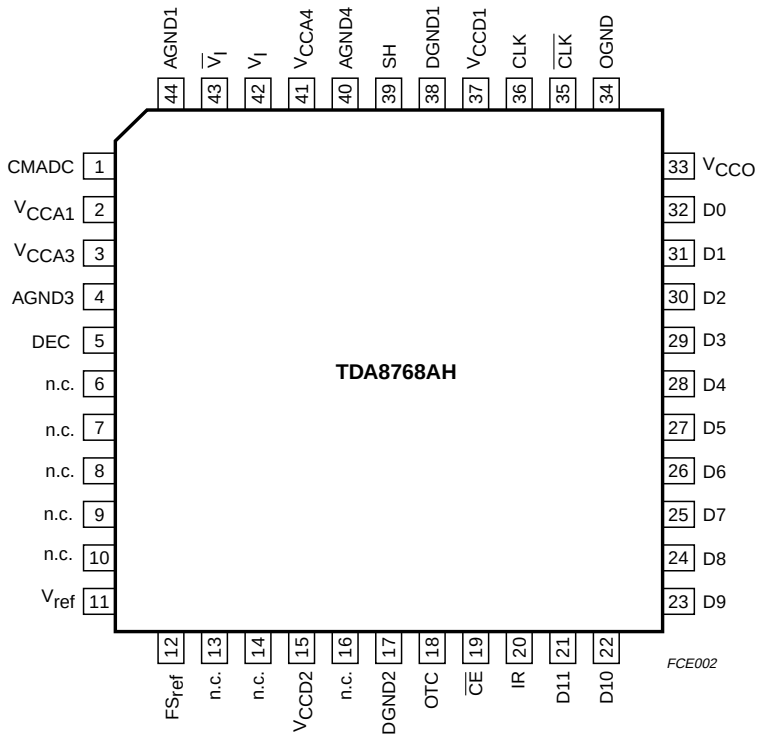


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CMADC	1	regulator output common mode ADC input
V_{CCA1}	2	analog supply voltage 1 (+5 V)
V_{CCA3}	3	analog supply voltage 3 (+5 V)
AGND3	4	analog ground 3
DEC	5	decoupling node
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
VREF	11	reference voltage input
FSREF	12	full-scale reference output

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Table 3: Pin description *...continued*

Symbol	Pin	Description
n.c.	13	not connected
n.c.	14	not connected
V_{CCD2}	15	digital supply voltage 2 (+5 V)
n.c.	16	not connected
DGND2	17	digital ground 2
OTC	18	control input twos complement output; active HIGH
$\overline{CE}$	19	chip enable input (CMOS level; active LOW)
IR	20	in-range output
D11	21	data output; bit 11 (MSB)
D10	22	data output; bit 10
D9	23	data output; bit 9
D8	24	data output; bit 8
D7	25	data output; bit 7
D6	26	data output; bit 6
D5	27	data output; bit 5
D4	28	data output; bit 4
D3	29	data output; bit 3
D2	30	data output; bit 2
D1	31	data output; bit 1
D0	32	data output; bit 0 (LSB)
V_{CCO}	33	output supply voltage (+3.3 V)
OGND	34	output ground
$\overline{CLK}$	35	complementary clock input
CLK	36	clock input
V_{CCD1}	37	digital supply voltage 1 (+5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V_{CCA4}	41	analog supply voltage 4 (+5 V)
V_I	42	analog input voltage
$\overline{V_I}$	43	complementary analog input voltage
AGND1	44	analog ground 1

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	–0.3	+7.0	V
V_{CCD}	digital supply voltage		[1]	–0.3	+7.0	V
V_{CCO}	output supply voltage		[1]	–0.3	+7.0	V

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Table 4: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		–1.0	+1.0	V
	$V_{CCD} - V_{CCO}$		–1.0	+4.0	V
	$V_{CCA} - V_{CCO}$		–1.0	+4.0	V
V_I, $\overline{V}_I$	input voltage at pins 42 and 43	referenced to AGND	0.3	V_{CCA}	V
$V_{CLK(p-p)}$	input voltage at pins 35 and 36 for differential clock drive (peak-to-peak value)		-	V_{CCD}	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C

[1] The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

9. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

10. Characteristics

Table 6: Characteristics

$V_{CCA} = V_2$ to V_{44}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; $V_{CCD} = V_{37}$ to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; $V_{CCO} = V_{33}$ to V_{34} = 3.0 to 3.6 V; AGND and DGND shorted together; T_{amb} = –40 to 85 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3}$–1.75 V; $V_{I(CM)} = V_{CCA3}$–1.6V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			4.75	5.0	5.25	V
V_{CCD}	digital supply voltage			4.75	5.0	5.25	V
V_{CCO}	output supply voltage			3.0	3.3	3.6	V
I_{CCA}	analog supply current		I	-	78	87	mA
I_{CCD}	digital supply current		I	-	27	30	mA
I_{CCO}	output supply current	f_{CLK} = 20 MHz; f_i = 400 kHz	I	-	3	4	mA
		f_{CLK} = 40 MHz; f_i = 4.43 MHz	C	-	6.2	9	mA
		f_{CLK} = 55 MHz; f_i = 20 MHz	I	-	9.5	12	mA
Inputs							

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Table 6: Characteristics…*continued*

V_{CCA} = V_2 to V_{44}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 to 85 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3}$−1.75 V; $V_{I(CM)} = V_{CCA3}$−1.6V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
CLK and $\overline{CLK}$ (referenced to DGND)[2]							
V_{IL}	LOW-level input voltage	PECL mode; V_{CCD} = 5 V	I	3.19	-	3.52	V
		TTL mode	C	0	-	0.8	V
V_{IH}	HIGH-level input voltage	PECL mode; V_{CCD} = 5 V	I	3.83	-	4.12	V
		TTL mode	C	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} or $V_{\overline{CLK}}$ = 3.19 V	C	−10	-	-	µA
I_{IH}	HIGH-level input current	V_{CLK} or $V_{\overline{CLK}}$ = 3.83 V	C	-	-	10	µA
$\Delta V_{CLK(p-p)}$	differential AC input voltage for switching ($V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$)	AC driving mode; DC voltage level = 2.5 V	C	1	1.5	2.0	V
R_i	input resistance	f_{CLK} = 55 MHz	D	2	-	-	kΩ
C_i	input capacitance	f_{CLK} = 55 MHz	D	-	-	2	pF
OTC, SH and $\overline{CE}$ (referenced to DGND); see Tables 7 and 8							
V_{IL}	LOW-level input voltage		I	0	-	0.8	V
V_{IH}	HIGH-level input voltage		I	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	I	−20	-	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	I	-	-	20	µA
V_I and $\overline{V}_I$ (referenced to AGND); see Table 7, $V_{ref} = V_{CCA3}$ − 1.75 V							
I_{IL}	LOW-level input current	SH = HIGH	C	-	10	-	µA
I_{IH}	HIGH-level input current	SH = HIGH	C	-	10	-	µA
R_i	input resistance	f_i = 20 MHz	D	-	14	-	MΩ
C_i	input capacitance	f_i = 20 MHz	D	-	450	-	fF
$V_{I(CM)}$	common mode input voltage	$V_I = \overline{V}_I$; output code 2047	C	V_{CCA3} − 1.7	V_{CCA3} − 1.6	V_{CCA3} − 1.2	V
Voltage controlled regulator output CMADC							
$V_{o(CM)}$	common mode output voltage		I	-	V_{CCA3} − 1.6	-	V
I_L	load current		I	-	1	2	mA
Voltage input V_{ref} [3]							
V_{ref}	full-scale fixed voltage	f_i = 20 MHz; f_{CLK} = 55 Msps	C	-	V_{CCA3} − 1.75	-	V
I_{ref}	input current at V_{ref}		C	-	0.3	10	µA
$V_{I(p-p)} - \overline{V}_{I(p-p)}$	input voltage amplitude (peak-to-peak value)	$V_{ref} = V_{CCA3}$ − 1.75 V $V_{I(CM)} = V_{CCA3}$ − 1.6 V	C	-	1.9	-	V
Voltage controlled regulator output FS_{ref}							
$V_{o(ref)}$	1.9 V full-scale output voltage		I	-	V_{CCA3} − 1.75	-	V
Outputs (referenced to OGND)							
Digital outputs D11 to D0 and IR (referenced to OGND)							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	I	0	-	0.5	V

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Table 6: Characteristics…*continued*

V_{CCA} = V_2 to V_{44}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 3.6 V; AGND and DGND shorted together; T_{amb} = –40 to 85 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 1.9 V; V_{ref} = V_{CCA3}–1.75 V; $V_{I(CM)}$ = V_{CCA3}–1.6V; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = – 0.4 mA	I	V_{CCO} – 0.5	-	V_{CCO}	V
I_o	output current in 3-state	output level between 0.5 V and V_{CCO}	I	–20	-	+20	µA
Switching characteristics							
Clock frequency f_{CLK}; see Figure 3							
$f_{CLK(min)}$	minimum clock frequency	SH = HIGH	C	-	-	7	MHz
$f_{CLK(max)}$	maximum clock frequency						
	TDA8768AH/4		C	40	-	-	MHz
	TDA8768AH/5		I	55	-	-	MHz
	TDA8768AH/7		C	70	-	-	MHz
t_{CLKH}	clock pulse width HIGH	f_i = 20 MHz	C	6.8	-	-	ns
t_{CLKL}	clock pulse width LOW	f_i = 20 MHz	C	6.8	-	-	ns
Analog signal processing; 50% clock duty factor; $V_I - \overline{V}_I$ = 1.9 V; V_{ref} = V_{CCA3} – 1.75 V; see Table 7							
Linearity							
INL	integral non-linearity	f_{CLK} = 20 MHz; f_i = 400 kHz	I	-	±2.6	4.5	LSB
DNL	differential non-linearity	f_{CLK} = 20 MHz; f_i = 400 kHz (no missing code guaranteed)	I	-	±0.5	+1.1 – 0.95	LSB
O_{err}	offset error	V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C; output code = 2047	C	–25	5	25	mV
E_G	gain error amplitude; spread from device to device	V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C	C	–7	-	+7	%FS
Bandwidth (f_{CLK} = 55 MHz) [4]							
B	analog bandwidth	–3 dB; full-scale input	C	220	245	-	MHz
Harmonics							
H_2	second harmonic TDA8768AH/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	C	-	–78	-	dBFS
		f_i = 10 MHz	C	-	–77	-	dBFS
		f_i = 15 MHz	C	-	–74	-	dBFS
		f_i = 20 MHz	C	-	–71	-	dBFS
	second harmonic TDA8768AH/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	C	-	–77	-	dBFS
		f_i = 10 MHz	C	-	–77	-	dBFS
		f_i = 15 MHz	C	-	–76	-	dBFS
		f_i = 20 MHz	I	-	– 73	-	dBFS
	second harmonic TDA8768AH/7 (f_{CLK} = 70 MHz)	f_i = 4.43 MHz	C	-	–76	-	dBFS
		f_i = 10 MHz	C	-	–74	-	dBFS
		f_i = 15 MHz	C	-	–70	-	dBFS

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Table 6: Characteristics…*continued*

V_{CCA} = V_2 to V_{44}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 to 85 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 1.9 V; V_{ref} = V_{CCA3}−1.75 V; $V_{I(CM)}$ = V_{CCA3}−1.6V; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
H_3	third harmonic TDA8768AH/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	C	-	−74	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−74	-	dBFS
		f_i = 20 MHz	C	-	−73	-	dBFS
	third harmonic TDA8768AH/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	C	-	−74	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−74	-	dBFS
		f_i = 20 MHz	I	-	−72	-	dBFS
	third harmonic TDA8768AH/7 (f_{CLK} = 70 MHz)	f_i = 4.43 MHz	C	-	−74	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−73	-	dBFS
Total harmonic distortion[5]							
THD	total harmonic distortion TDA8768AH/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−68	-	dBFS
		f_i = 15 MHz	C	-	−68	-	dBFS
		f_i = 20 MHz	C	-	−68	-	dBFS
	total harmonic distortion TDA8768AH/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−68	-	dBFS
		f_i = 15 MHz	C	-	−68	-	dBFS
		f_i = 20 MHz	I	-	−68	-	dBFS
	total harmonic distortion TDA8768AH/7 (f_{CLK} = 70 MHz)	f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−67	-	dBFS
		f_i = 15 MHz	C	-	−67	-	dBFS
Thermal noise (f_{CLK} = 55 MHz)							
$N_{th(rms)}$	thermal noise (RMS value)	shorted input; SH = HIGH; f_{CLK} = 55 MHz	C	-	0.45	-	LSB
Signal-to-noise ratio [6]							
SNR	signal-to-noise ratio TDA8768AH/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	C	-	64	-	dBFS
		f_i = 10 MHz	C	-	64	-	dBFS
		f_i = 15 MHz	C	-	64	-	dBFS
		f_i = 20 MHz	C	-	64	-	dBFS
	signal-to-noise ratio TDA8768AH/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	C	-	64	-	dBFS
		f_i = 10 MHz	C	-	64	-	dBFS
		f_i = 15 MHz	C	-	64	-	dBFS
		f_i = 20 MHz	I	-	64	-	dBFS
	signal-to-noise ratio TDA8768AH/7 (f_{CLK} = 70 MHz)	f_i = 4.43 MHz	C	-	64	-	dBFS
		f_i = 10 MHz	C	-	64	-	dBFS
		f_i = 15 MHz	C	-	63	-	dBFS

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Table 6: Characteristics…*continued*

V_{CCA} = V_2 to V_{44}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 to 85 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 1.9 V; V_{ref} = V_{CCA3}−1.75 V; $V_{I(CM)}$ = V_{CCA3}−1.6V; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Spurious free dynamic range; see Figure 7, 13 and 14							
SFDR	spurious free dynamic range TDA8768AH/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	C	-	72	-	dBFS
		f_i = 10 MHz	C	-	71	-	dBFS
		f_i = 15 MHz	C	-	71	-	dBFS
		f_i = 20 MHz	C	-	69	-	dBFS
	spurious free dynamic range TDA8768AH/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	C	-	72	-	dBFS
		f_i = 10 MHz	C	-	71	-	dBFS
		f_i = 15 MHz	C	-	71	-	dBFS
		f_i = 20 MHz	I	-	69	-	dBFS
	spurious free dynamic range TDA8768AH/7 (f_{CLK} = 70 MHz)	f_i = 4.43 MHz	C	-	70	-	dBFS
		f_i = 10 MHz	C	-	69	-	dBFS
		f_i = 15 MHz	C	-	69	-	dBFS
Effective number of bits [7]							
ENOB	effective number of bits TDA8768AH/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	C	-	10.1	-	bits
		f_i = 10 MHz	C	-	10.1	-	bits
		f_i = 15 MHz	C	-	10.1	-	bits
		f_i = 20 MHz	C	-	10	-	bits
	effective number of bits TDA8768AH/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	C	-	10.1	-	bits
		f_i = 10 MHz	C	-	10.1	-	bits
		f_i = 15 MHz	C	-	10	-	bits
		f_i = 20 MHz	I	-	10	-	bits
	effective number of bits TDA8768AH/7 (f_{CLK} = 70 MHz)	f_i = 4.43 MHz	C	-	10	-	bits
		f_i = 10 MHz	C	-	10	-	bits
		f_i = 15 MHz	C	-	10	-	bits
Intermodulation; (f_{CLK} = 55 MHz; f_i = 20 MHz)[8]							
TTIR	two-tone intermodulation rejection		C	-	−68	-	dB
d_3	third-order intermodulation distortion		C	-	−70	-	dB
Bit error rate (f_{CLK} = 55 MHz)							
BER	bit error rate	f_i = 20 MHz; V_I = ±16 LSB at code 2047	C	-	10^{-14}	-	times/ sample
Timing (C_L = 10 pF)[9]							
$t_{d(s)}$	sampling delay time		C	-	0.25	1	ns
$t_{h(o)}$	output hold time		C	4	6.4	-	ns
$t_{d(o)}$	output delay time		C	-	9.0	13	ns

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Table 6: Characteristics…*continued*

V_{CCA} = V_2 to V_{44}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 to 85 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 1.9 V; V_{ref} = V_{CCA3}−1.75 V; $V_{I(CM)}$ = V_{CCA3}−1.6V; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
3-state output delay times; see Figure 4							
t_{dZH}	enable HIGH		C	-	5.1	9.0	ns
t_{dZL}	enable LOW		C	-	7.0	11	ns
t_{dHZ}	disable HIGH		C	-	9.7	14	ns
t_{dLZ}	disable LOW		C	-	9.5	13	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100% industrially tested.

[2] The circuit has two clock inputs: CLK and $\overline{CLK}$. There are 5 modes of operation:

a) PECL mode 1: (DC level vary 1:1 with V_{CCD}) CLK and $\overline{CLK}$ inputs are at differential PECL levels.

b) PECL mode 2: (DC level vary 1:1 with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on $\overline{CLK}$ decoupled to GND via a 100 nF capacitor.

c) PECL mode 3: (DC level vary 1:1 with V_{CCD}) $\overline{CLK}$ input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.

d) Differential AC driving mode 4: When driving the CLK input directly and with any AC signal of minimum 1 V (p-p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal.
When driving the $\overline{CLK}$ input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the $\overline{CLK}$ or CLK input to DGND via a 100 nF capacitor.

e) TTL mode 1: CLK input is at TTL level and sampling is taken on the falling edge of the clock input signal.
In that case $\overline{CLK}$ pin has to be connected to the ground.

[3] The ADC input range can be adjusted with an external reference connected to V_{ref} pin. This voltage has to be referenced to V_{CCA}; see Figure 12.

[4] The −3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.

[5] Total Harmonic Distortion (THD) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \sqrt{\frac{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}{F^2}}$$

where F is the fundamental harmonic referenced at 0 dB for a full-scale sine wave input; see Figure 6.

[6] Signal-to-noise ratio (SNR) takes into account all harmonics above five and noise up to nyquist frequency; see Figure 8.

[7] Effective number of bits are obtained via a Fast Fourier Transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to SINAD is given by SINAD = ENOB × 6.02 + 1.76 dB; see Figure 5.

[8] Intermodulation measured relative to either tone with analog input frequencies of 20 and 20.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (−6 dB below full scale for each input signal). $d3_{(IM3)}$ is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.

[9] Output data acquisition: the output data is available after the maximum delay of t_d; see Figure 3.

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Table 7: Output coding with differential inputs (typical values to AGND); $V_{i(p-p)} - \overline{V}_{i(p-p)} = 1.9$ V, $V_{ref} = V_{CCA3} - 1.75$ V

Code	$V_{i(p-p)}$	$\overline{V}_{i(p-p)}$	IR	Binary outputs	Twos complement outputs[1]
				D11 to D0	D11 to D0
Underflow	<3.125	>4.075	0	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
0	3.125	4.075	1	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
1	–	–	1	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1
↓	–	–	↓	↓	↓
2047	3.6	3.6	1	0 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1
↓	–	–	↓	↓	↓
4094	–	–	1	1 1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 1 0
4095	4.075	3.125	1	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1
Overflow	>4.075	<3.125	0	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1

[1] Twos complement reference is inverted MSB.

Table 8: Mode selection

OTC	$\overline{CE}$	D0 to D11 and IR
0	0	binary; active
1	0	twos complement; active
X[1]	1	high-impedance

[1] X = don't care.

Table 9: Sample-and-hold selection

SH	Sample-and-hold
1	active
0	inactive; tracking mode

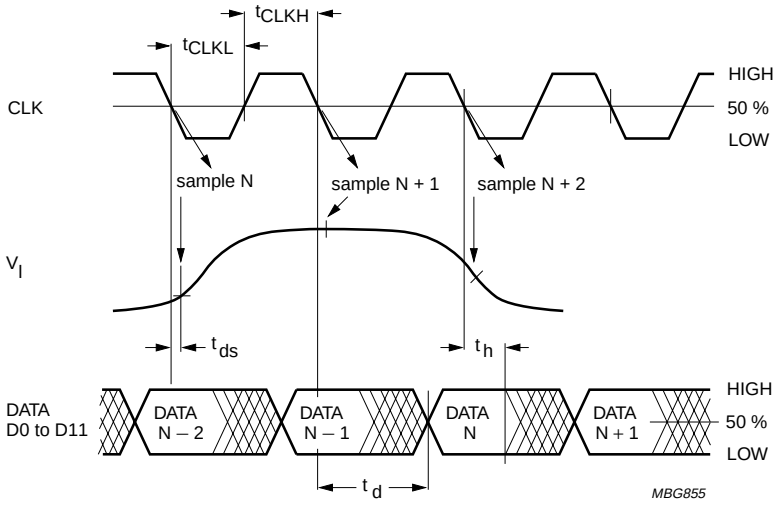
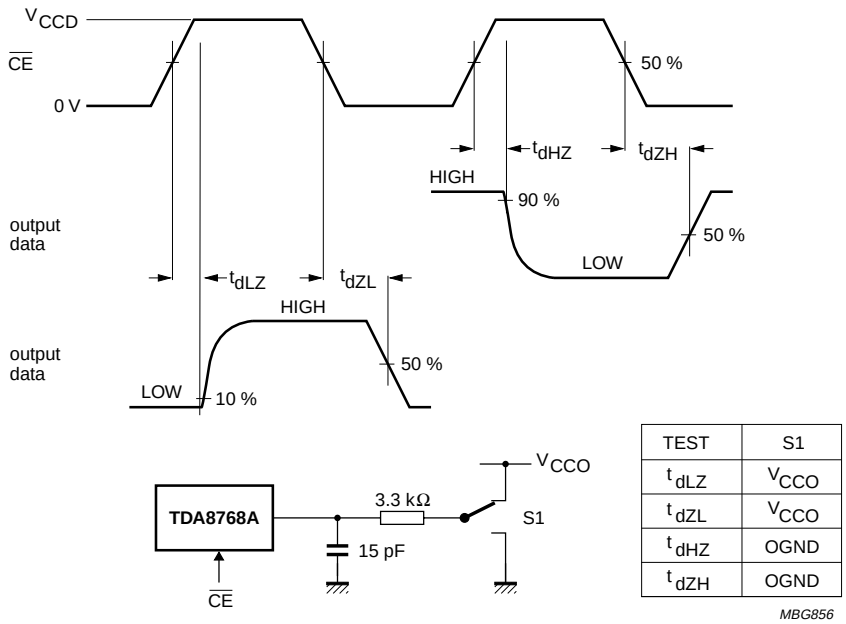


Fig 3. Timing diagram.

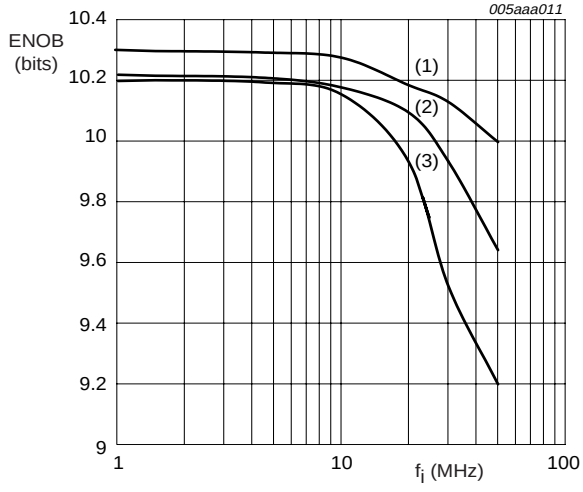
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TEST	S1
t_{dLZ}	V_{CCO}
t_{dZL}	V_{CCO}
t_{dHZ}	OGND
t_{dZH}	OGND

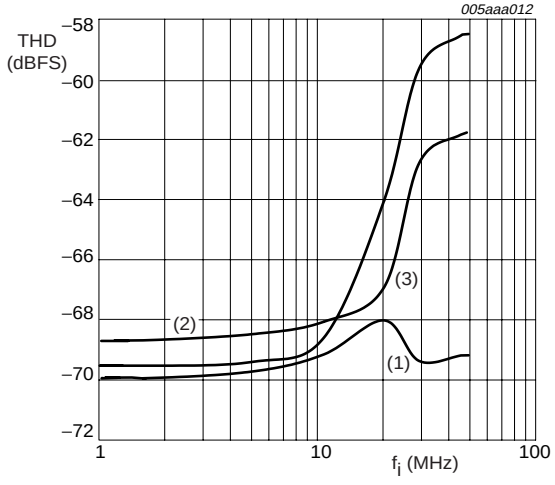
$f_{\overline{CE}}$ = 100 kHz.

Fig 4. Timing diagram and test conditions of 3-state output delay time.



(1) 40 Msps
(2) 55 Msps
(3) 70 Msps

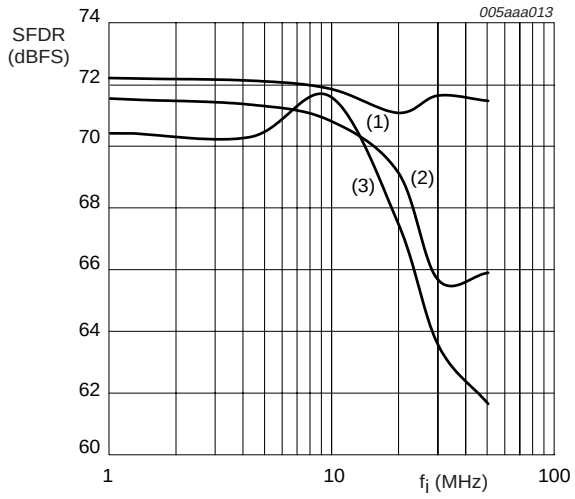
Fig 5. Effective number of bits (ENOB) as a function of input frequency (sample device).



(1) 40 Msps
(2) 55 Msps
(3) 70 Msps

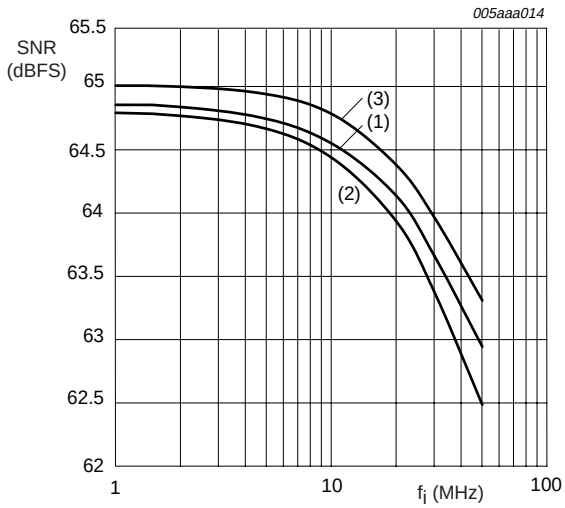
Fig 6. Total harmonic distortion (THD) as a function of input frequency (sample device).

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(1) 40 Msps
(2) 55 Msps
(3) 70 Msps

Fig 7. Spurious free dynamic range (SFDR) as a function of input frequency (sample device).



(1) 40 Msps
(2) 55 Msps
(3) 70 Msps

Fig 8. Signal-to-noise ratio (SNR) as a function of input frequency (sample device).

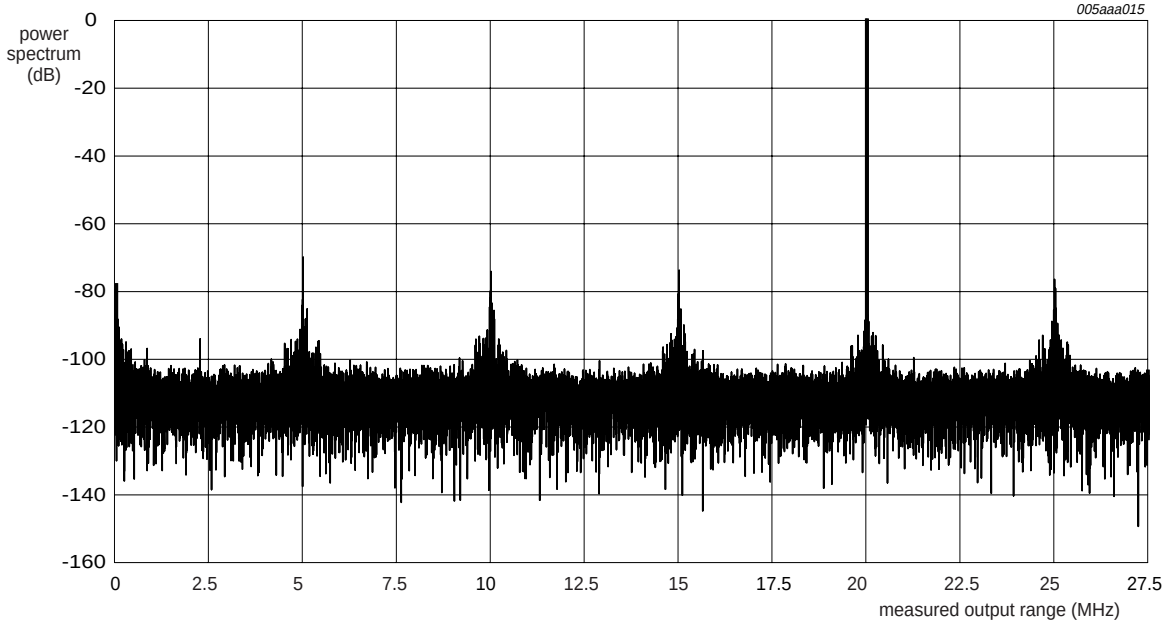


Fig 9. Single-tone; f_i = 20 MHz; f_{CLK} = 55 Msps.

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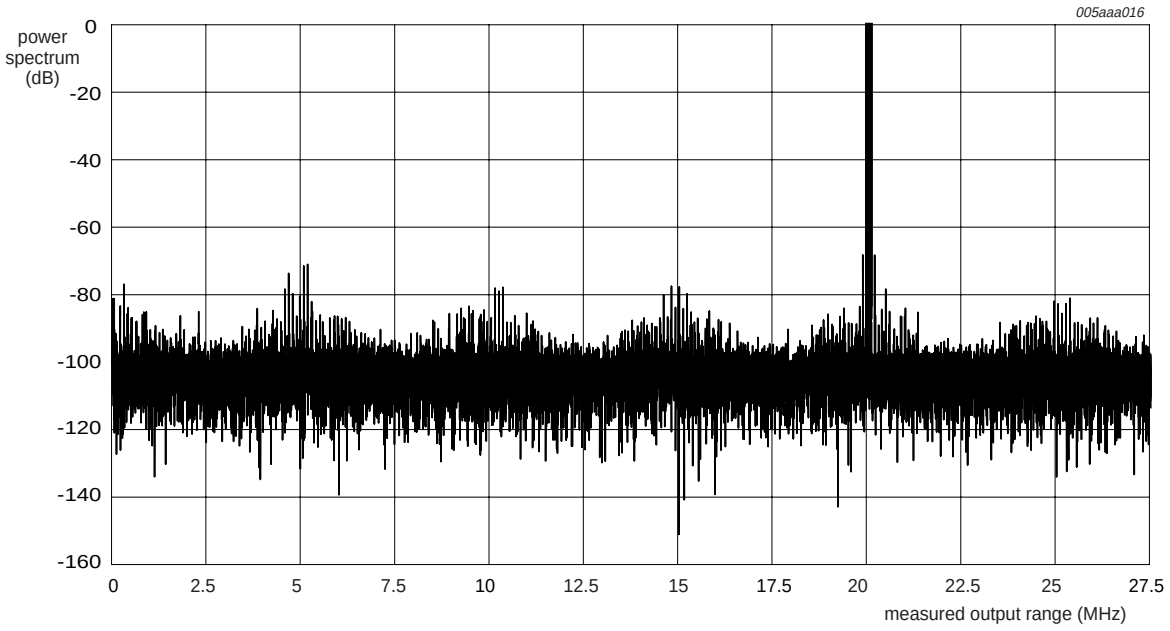


Fig 10. Two-tone; f_{i1} = 20 MHz; f_{i2} = 20.1 MHz; f_{CLK} = 55 Msps.

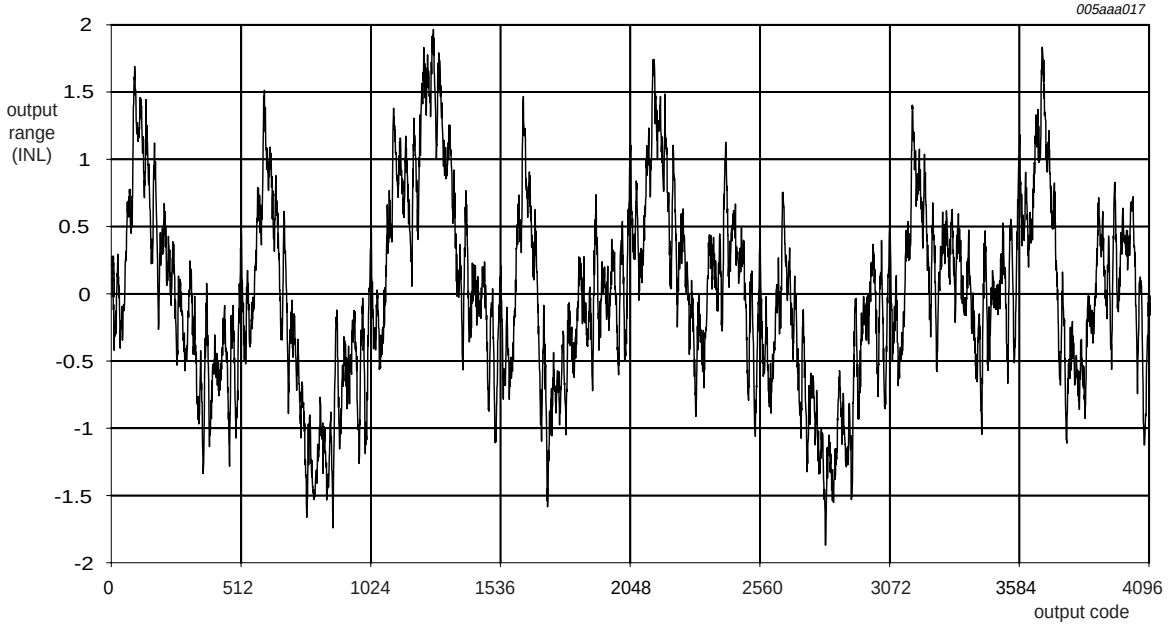


Fig 11. Integral non-linearity (INL).

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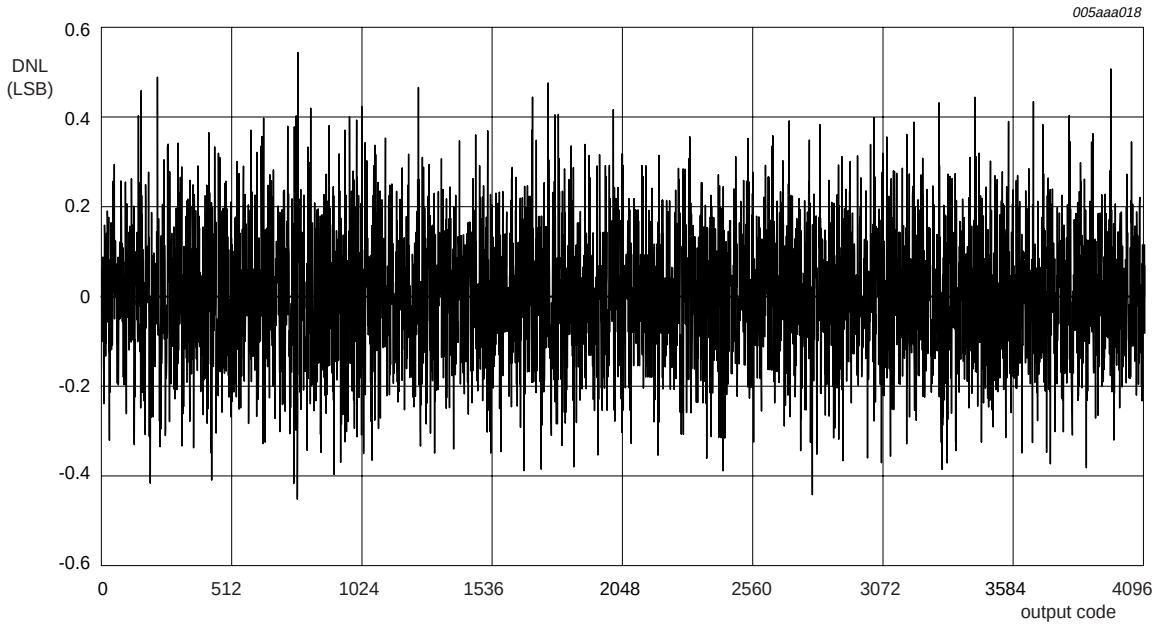
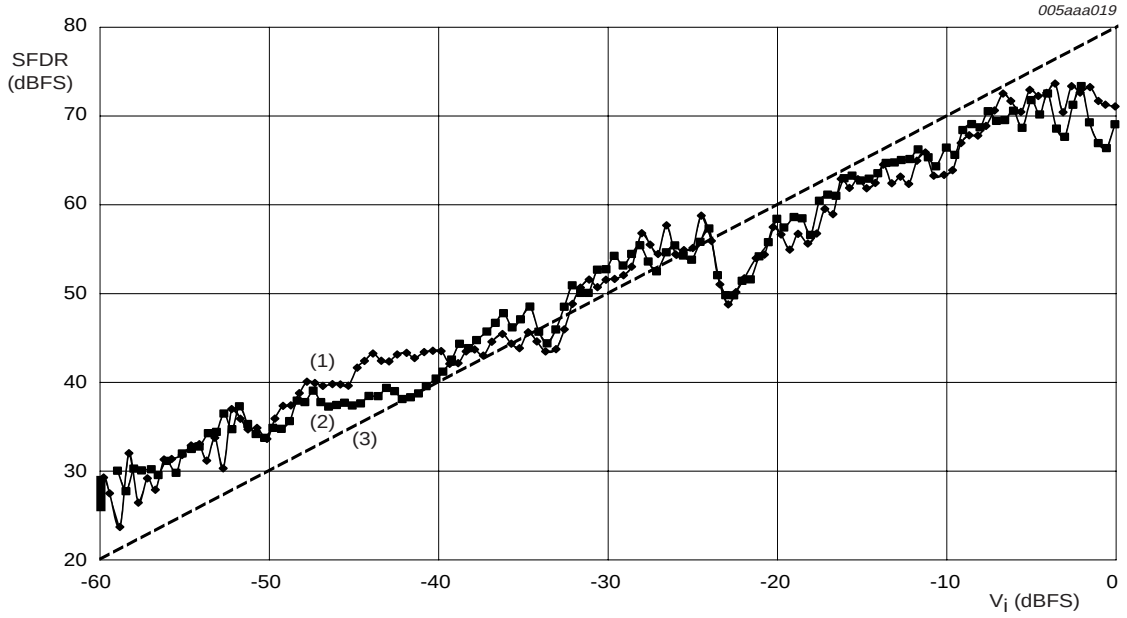


Fig 12. Differential non-linearity (DNL).



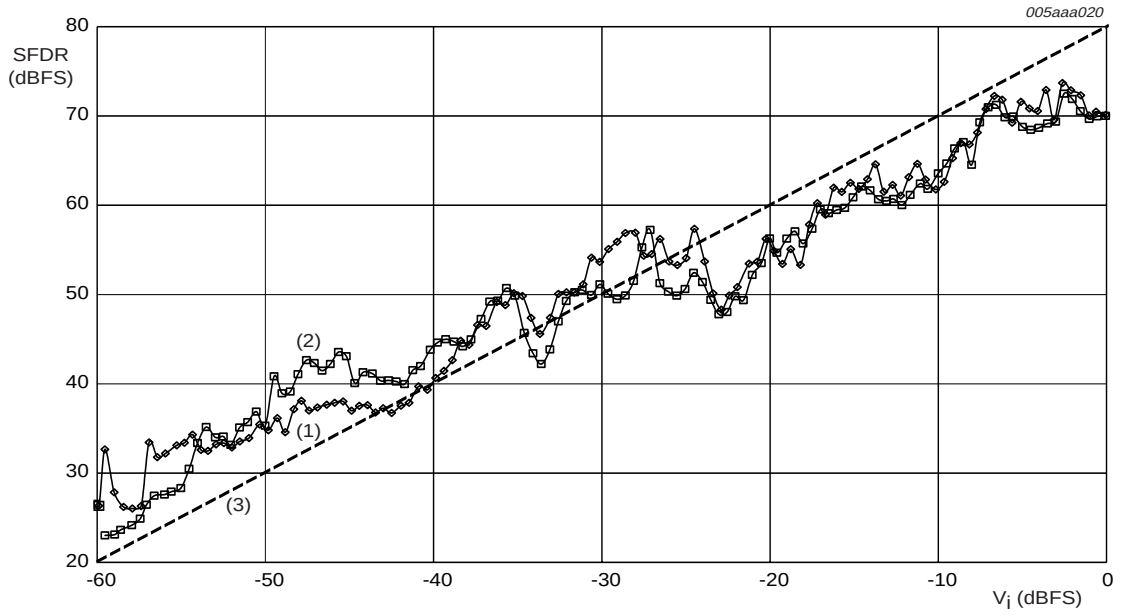
(1) f_i = 4.43 MHz

(2) f_i = 20 MHz

(3) SFDR = 80 dB

Fig 13. SFDR as a function of input amplitude; FS = 1.9 V; f_{CLK} = 40 MHz.

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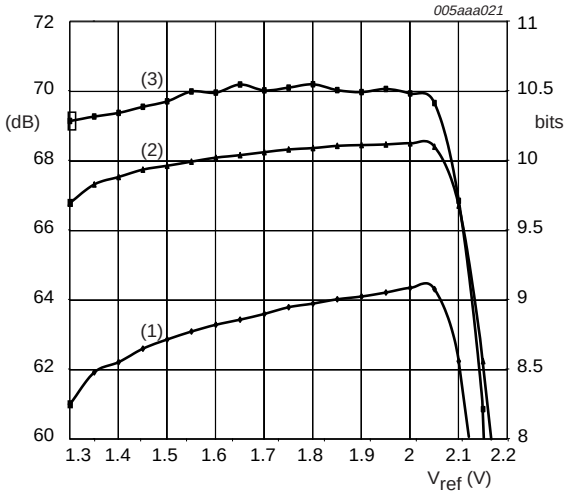


(1) f_i = 4.43 MHz

(2) f_i = 20 MHz

(3) SFDR = 80 dB

Fig 14. Spurious free dynamic range (SFDR) as a function of input amplitude; FSREF = 1.9 V; f_{CLK} = 55 MHz.



(1) = SNR

(2) = ENOB

(3) = SFDR

Fig 15. ENOB, SFDR and SNR as a function of V_{ref}; f_{CLK} = 55 MHz; f_i = 4.43 MHz.

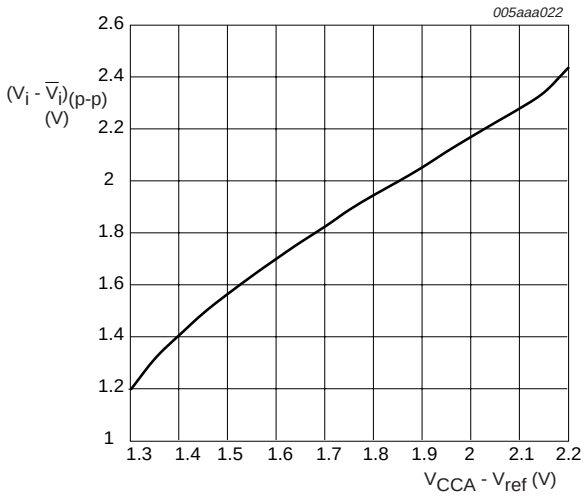
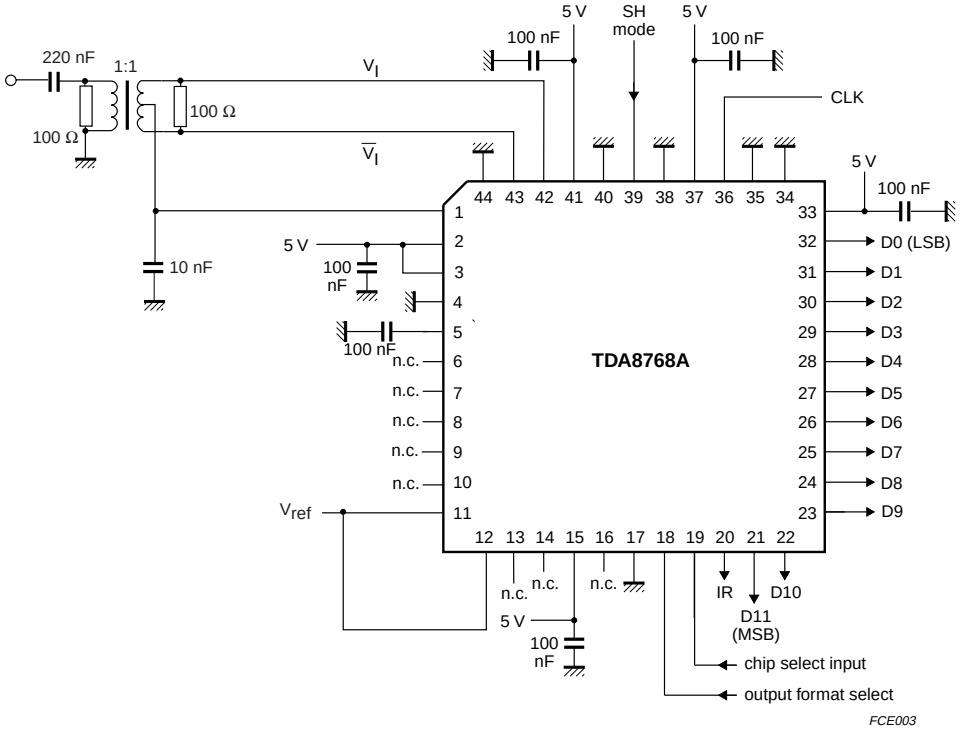


Fig 16. ADC full-scale; $V_{I(p-p)} - V_{I(p-p)}$ as a function of $V_{CCA} - V_{ref}$.

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11. Application information

11.1 Application diagrams



The analog, digital and output supplies should be separated and decoupled.

Fig 17. Application diagram.

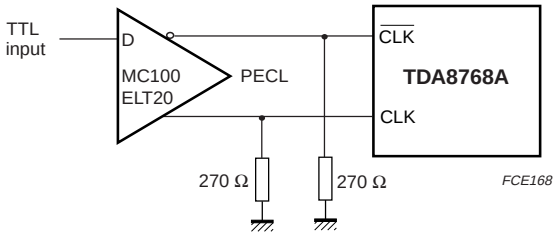


Fig 18. Application diagram for differential clock input PECL compatible using a TTL to PECL translator.

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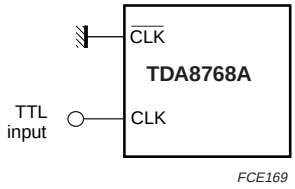
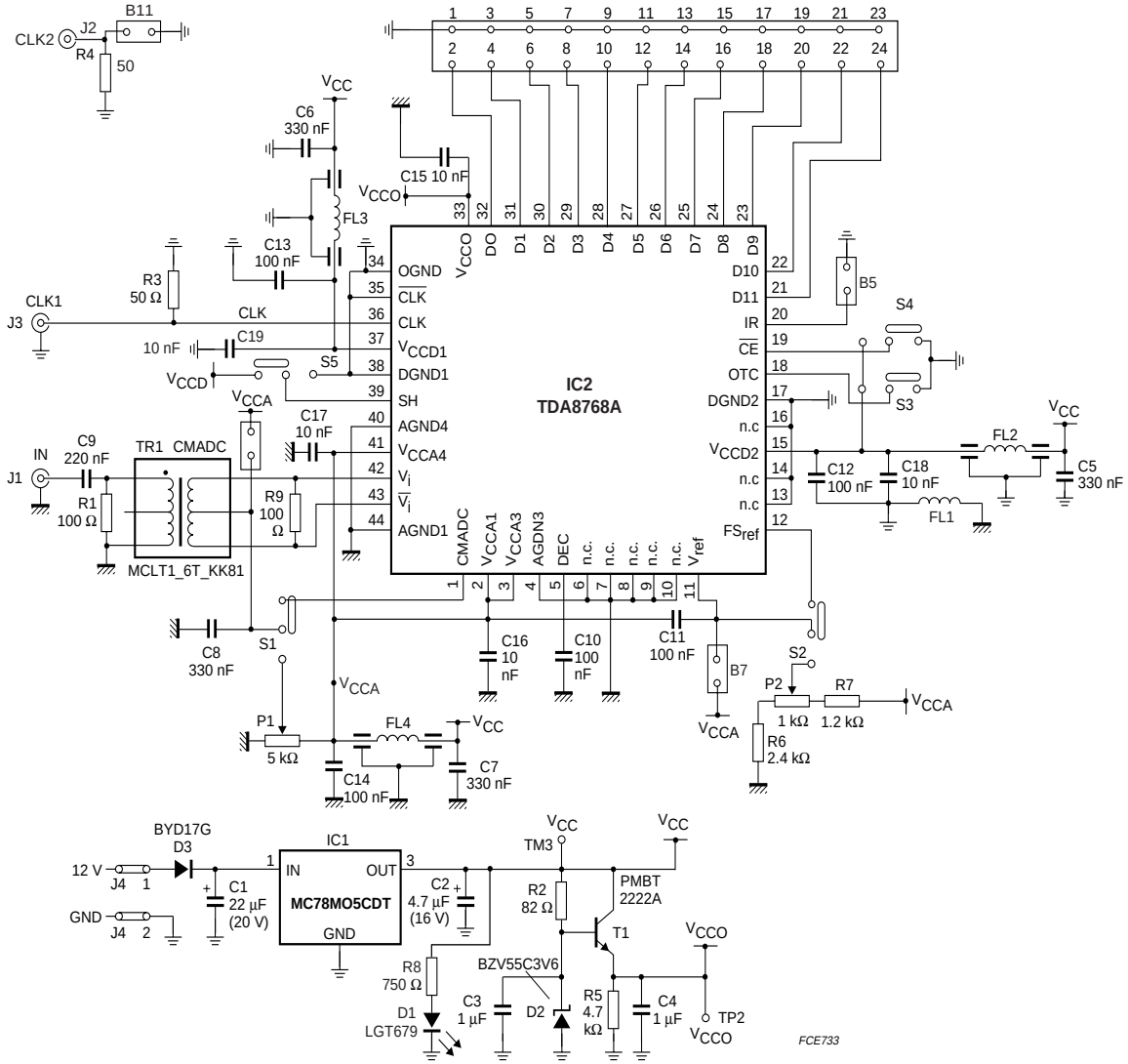


Fig 19. Application diagram for TTL single-ended clock.

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11.2 Demonstration board



C8 = close to TR1 pin.

Fig 20. Demonstration board schematic.

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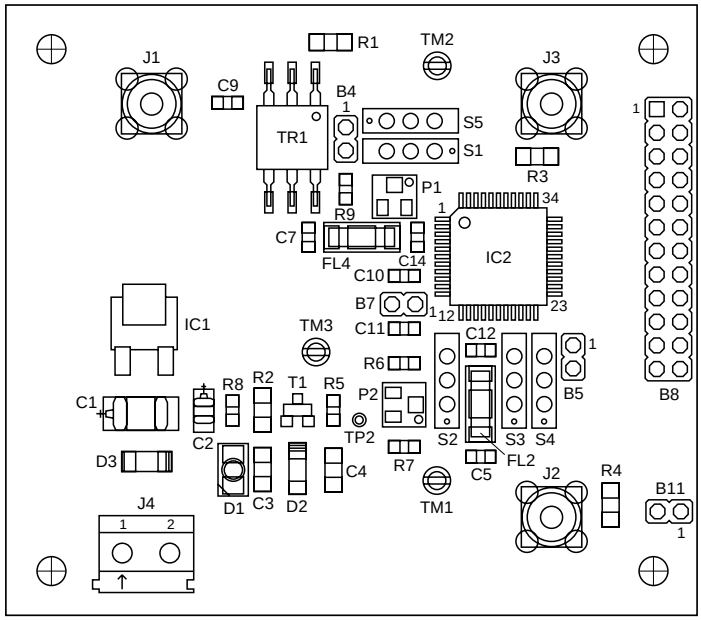


Fig 21. Component placement (top side).

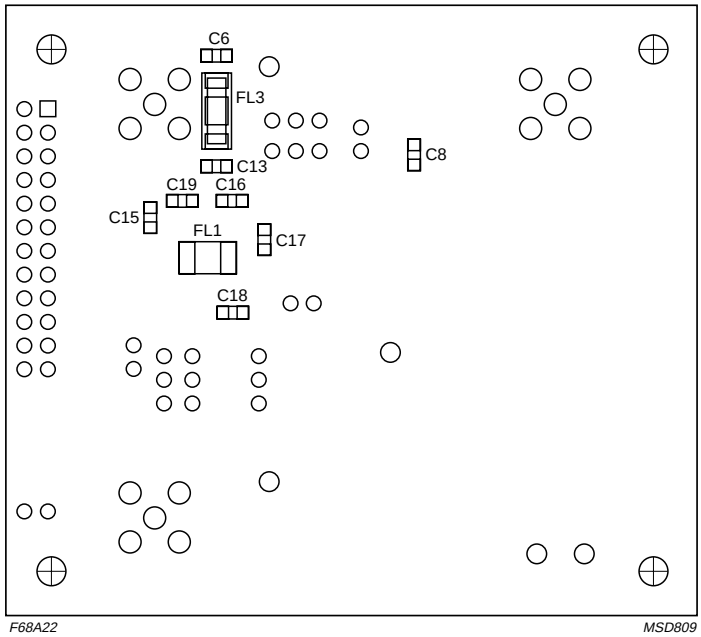
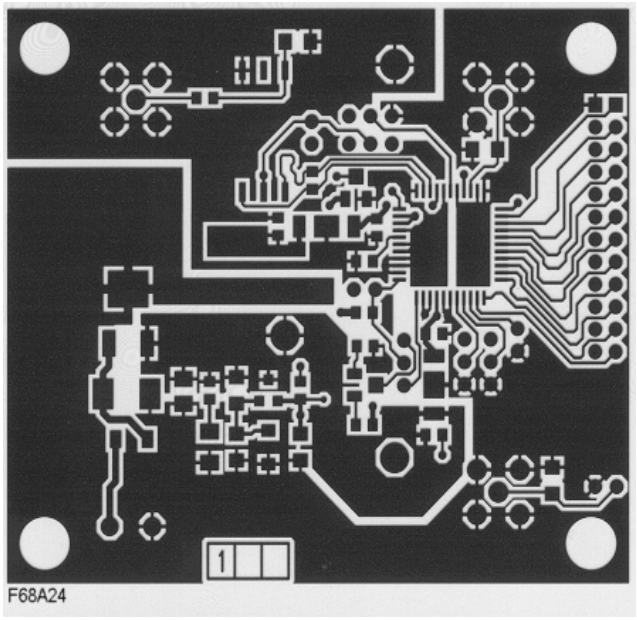


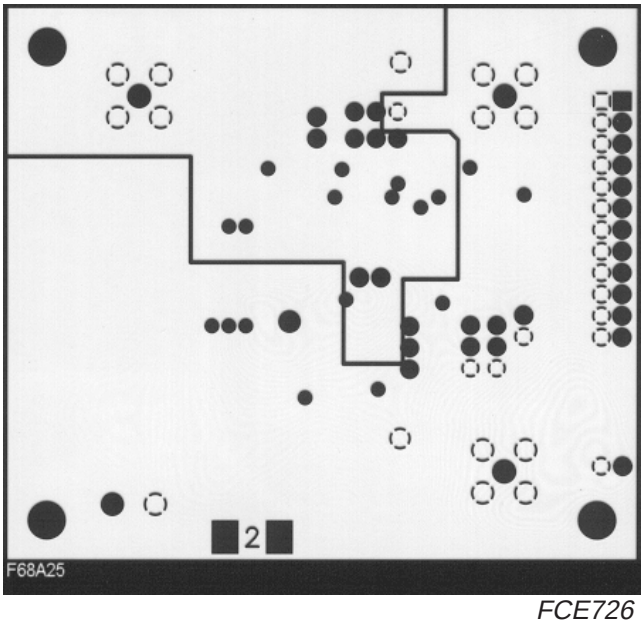
Fig 22. Component placement (underside).

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FCE725

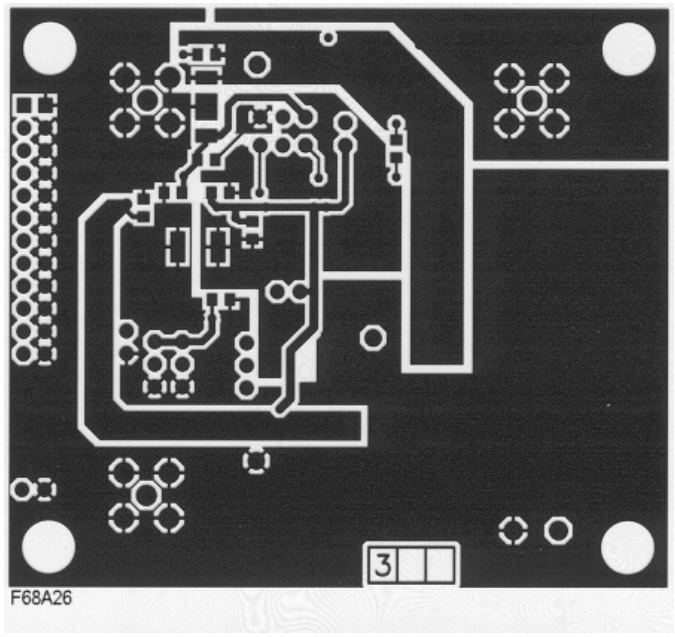
Fig 23. PCB layout (top layer).



FCE726

Fig 24. PCB layout (ground layer).

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FCE727

Fig 25. PCB layout (power plane).

12. Support information

12.1 Definitions

12.1.1 Non-linearities

Integral Non-Linearity (INL).: It is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of the code i is obtained from the equation:

$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S}$$

where

$i = 0 \cdot (2^n - 1)$ and

S = slope of the ideal straight line = code width; i = code value.

Differential Non-Linearity (DNL).: It is the deviation in code width from the value of 1LSB.

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S} - 1$$

where

$i = 0 \cdot (2^n - 2)$

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12.1.2 Dynamic parameters (single tone)

Figure 26 shows the spectrum of a full-scale input sine wave with frequency f_t, conforming to coherent sampling (f_t/f_s = M/N, where M is the number of cycles and N is number of samples, M and N being relatively prime), and digitized by the ADC under test.

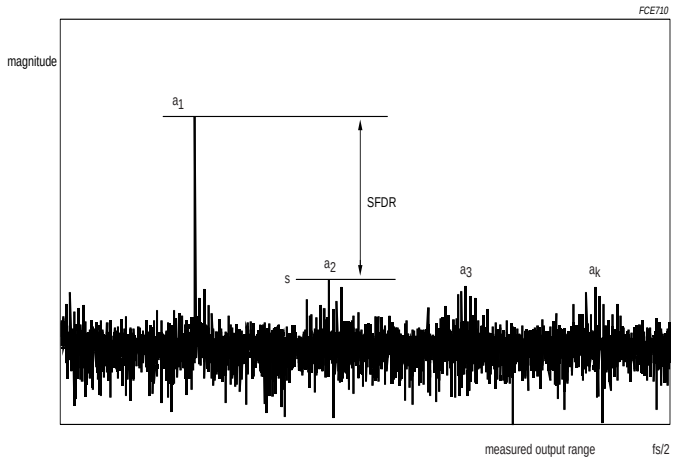


Fig 26. Spectrum of full-scale input sine wave with frequency f_t.

Remark: in the following equations, P_{noise} is the power of the terms which include the effects of random noise, non-linearities, sampling time errors, and “quantization noise”.

Signal-to-noise and distortion (SINAD): The ratio of the output signal power to the noise plus distortion power for a given sample rate and input frequency, excluding the DC component:

$$SINAD[db] = 10log\left[\frac{P_{signal}}{P_{noise+distortion}}\right]$$

Effective Number of Bits (ENOB): It is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$ENOB = (SINAD[dB] - (1 \cdot 76))/(6 \cdot 02)$$

Total Harmonic Distortion (THD): The ratio of the power of the harmonics to the power of the fundamental. For k-1 harmonics the THD is:

$$THD[dB] = 10log\left[\frac{P_{harmonics}}{P_{signal}}\right]$$

where

$$P_{harmonics} = a|_2^2 + a|_3^2 + a|_k^2$$

$$P_{signal} = a|_1^2$$

The value of k is usually 6 (i.e. calculation of THD is done on the first 5 harmonics).

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Signal-to-Noise Ratio (SNR): The ratio of the output signal power to the noise power, excluding the harmonics and the DC component.

$$SNR[dB] = 10log\left[\frac{P_{signal}}{P_{noise}}\right]$$

Spurious Free Dynamic Range (SFDR): The number SFDR specifies available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious (harmonic and non-harmonic, excluding DC component.

$$SFDR[dB] = 20log\frac{a_1}{max(s)}$$

12.1.3 Intermodulation distortion

Spectral analysis (dual-tone)

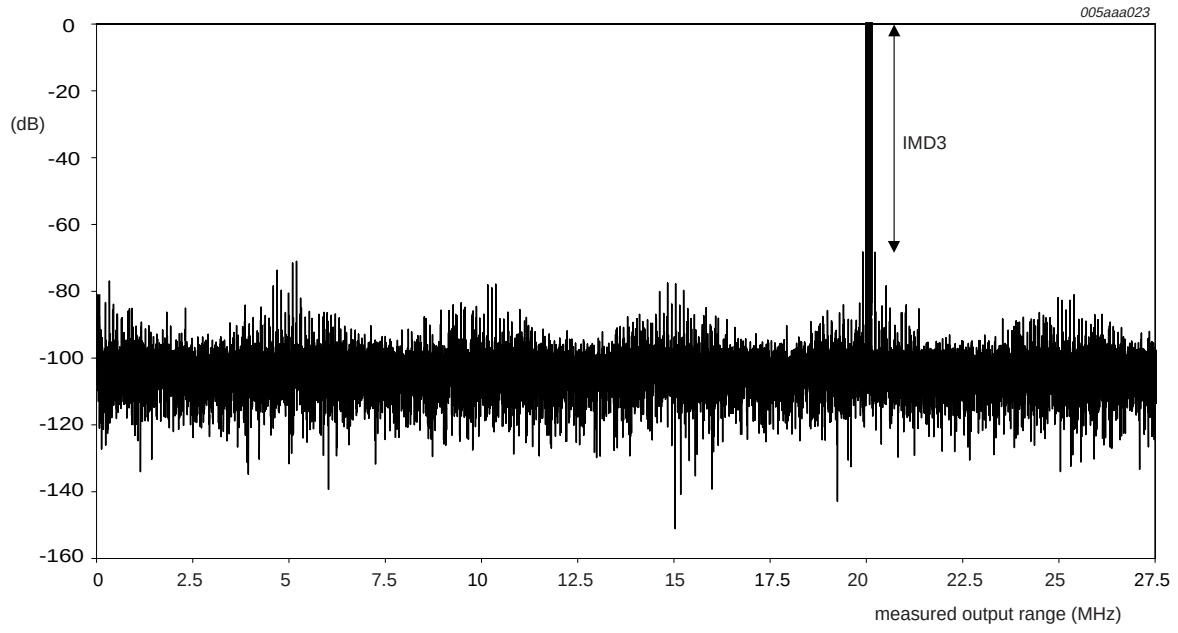


Fig 27. Spectral analysis (dual-tone)

From a dual-tone input sinusoid (f_{t1} and f_{t2}, these frequencies being chosen according to the coherence criterion), the intermodulation distortion products IMD2 and IMD3 (respectively, 2nd and 3rd-order components) are defined, as follows.

IMD2 (IMD3): The ratio of the RMS value of either tone to the RMS value of the worst second (third) order intermodulation product.

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The total intermodulation distortion IMD is given by

$$IMD[dB] = 10log\left[\frac{P_{intermod}}{P_{signal}}\right]$$

where,

$$P_{intermod} = a|_{im}^{2}(f_{t1} - f_{t2}) - a|_{im}^{2}(f_{t1} + f_{t2}) + a|_{im}^{2}(f_{t1} - 2f_{t2}) + a|_{im}^{2}(f_{t1} + 2f_{t2}) + a|_{im}^{2}(2f_{t1} - f_{t2}) + a|_{im}^{2}(2f_{t1} + f_{t2})$$

$$P_{signal} = a^{2}(f_{t1}) + a^{2}(f_{t2})$$

and

$$a|_{im}^{2}(f_{t})$$

is the power in the intermodulation component at frequency f_t.

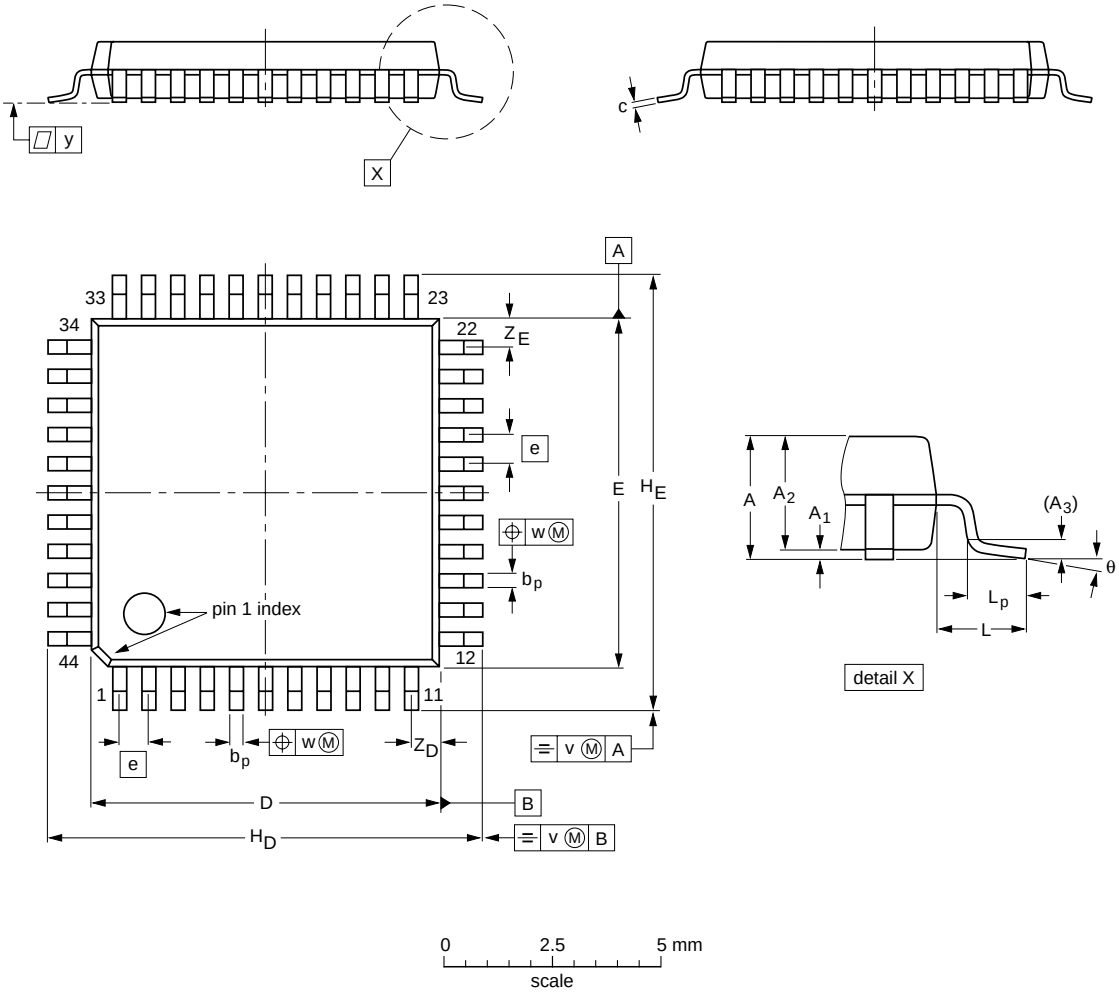
12.1.4 Noise Power Ratio (NPR)

When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample set.

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13. Package outline

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

Fig 28. SOT307-2.

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14. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

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The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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16. Revision history

Table 11: Revision history

Rev	Date	CPCN	Description
02	20020703	-	**Product data (9397 750 09656); supersedes Preliminary specification TDA8768A_1 of 20020409 (9397 750 08323)** Modifications: • Raise to Product • Features list corrected • Change value of INL in Table 6.
01	20020409	-	**Preliminary data; initial version.**

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17. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

18. Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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