

- High-Performance Static CMOS Technology
- Includes the T320C2xLP Core CPU
 - Object Compatible With the TMS320C2xx
 - Source Code Compatible With TMS320C25
 - Upwardly Compatible With TMS320C5x
 - 132-Pin Plastic Quad Flat Package (PQ Suffix)
 - 50-ns Instruction Cycle Time
- Industrial and Automotive Temperature Available
- Memory
 - 544 Words × 16 Bits of On-Chip Data/Program Dual-Access RAM
 - 16K Words × 16 Bits of On-Chip Program Flash EEPROM
 - 224K Words × 16 Bits of Total Memory Address Reach (64K Data, 64K Program and 64K I/O, and 32K Global Memory Space)
- Event-Manager Module
 - 12 Compare/Pulse-Width Modulation (PWM) Channels
 - Three 16-Bit General-Purpose Timers With Six Modes, Including Continuous Up and Up/Down Counting
 - Three 16-Bit Full-Compare Units With Deadband
 - Three 16-Bit Simple-Compare Units
 - Four Capture Units (Two With Quadrature Encoder-Pulse Interface Capability)
- Dual 10-Bit Analog-to-Digital Conversion Module
- 28 Individually Programmable, Multiplexed I/O Pins
- Phase-Locked-Loop (PLL)-Based Clock Module
- Watchdog Timer Module (With Real-Time Interrupt)
- Serial Communications Interface (SCI) Module
- Serial Peripheral Interface (SPI) Module
- Six External Interrupts (Power Drive Protect, Reset, NMI, and Three Maskable Interrupts)
- Four Power-Down Modes for Low-Power Operation
- Scan-Based Emulation
- Development Tools Available:
 - Texas Instruments (TI) ANSI C Compiler, Assembler/Linker, and C-Source Debugger
 - Scan-Based Self-Emulation (XDS510™)
 - Third-Party Digital Motor Control and Fuzzy-Logic Development Support

description

The TMS320F240 (F240) device is a member of a family of DSP controllers based on the TMS320C2xx generation of 16-bit fixed-point digital signal processors (DSPs). This family is optimized for digital motor/motion control applications. The DSP controllers combine the enhanced TMS320 architectural design of the C2xLP core CPU for low-cost, high-performance processing capabilities and several advanced peripherals optimized for motor/motion control applications. These peripherals include the event manager module, which provides general-purpose timers and compare registers to generate up to 12 PWM outputs, and a dual10-bit analog-to-digital converter (ADC), which can perform two simultaneous conversions within 6.1 μ s. See the functional block diagram.



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REVISION HISTORY

REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
E	November 2002	Production Data	Removed TMS320C240 as it is an obsolete device. Updated descriptions of the following pins in the Terminal Functions table: – PWM1/CMP1–PWM6/CMP6 – <u>OSCBYP</u> – TRST Updated the following figures: – Figure 3, Shared Pin Configuration – Figure 6, System Module Interrupt Structure – Figure 12, Analog-to-Digital Converter Module – Figure 16, TMS320 Device Nomenclature – Figure 20, Recommended Crystal/Clock Connection Added the following figures: – Figure 31, Case With Crystal – Figure 32, Case With External Oscillator Updated the following tables: – Table 15, Development Support Tools – Table 16, TMS320F240-Specific Development Tools – Table 20, Register File Compilation [ADCTRL1 and ADCTRL2] Updated the following sections: – Low-Power Modes – Flash EEPROM – Capture Unit – Analog-to-Digital Converter (ADC) Module [Digital Value equation] – Development Support – External Reference Crystal With PLL-Circuit-Enabled Clock Option – 10-Bit Dual Analog-to-Digital Converter (ADC)

Terminal Functions

TERMINAL NAME	NO.	TYPE†	DESCRIPTION
EXTERNAL INTERFACE DATA/ADDRESS SIGNALS			
A0 (LSB)	110	O/Z	Parallel address bus A0 [least significant bit (LSB)] through A15 [most significant bit (MSB)]. A15–A0 are multiplexed to address external data/program memory or I/O. A15–A0 are placed in high-impedance state when EMU1/ÖFF is active low and hold their previous states in power-down modes.
A1	111		
A2	112		
A3	114		
A4	115		
A5	116		
A6	117		
A7	118		
A8	119		
A9	122		
A10	123		
A11	124		
A12	125		
A13	126		
A14	127		
A15 (MSB)	128		
D0 (LSB)	9	I/O/Z	Parallel data bus D0 (LSB) through D15 (MSB). D15–D0 are multiplexed to transfer data between the TMS320F240 and external data/program memory and I/O space (devices). D15–D0 are placed in the high-impedance state when not outputting, when in power-down mode, when reset (RS) is asserted, or when EMU1/ÖFF is active low.
D1	10		
D2	11		
D3	12		
D4	15		
D5	16		
D6	17		
D7	18		
D8	19		
D9	22		
D10	23		
D11	24		
D12	25		
D13	26		
D14	27		
D15 (MSB)	28		
EXTERNAL INTERFACE CONTROL SIGNALS			
DS	129	O/Z	Data, program, and I/O space select signals. DS, PS, and IS are always high unless low-level asserted for communication to a particular external space. They are placed in the high-impedance state during reset, power down, and when EMU1/ÖFF is active low.
PS	131		
IS	130		
READY	36	I	Data ready. READY indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again.
RW	4	O/Z	Read/write signal. RW indicates transfer direction during communication to an external device. It is normally in read mode (high), unless low level is asserted for performing a write operation. It is placed in the high-impedance state during reset, power down, and when EMU1/ÖFF is active low.
STRB	6	O/Z	Strobe. STRB is always high unless asserted low to indicate an external bus cycle. It is placed in the high-impedance state during reset, power down, and when EMU1/ÖFF is active low.
WE	1	O/Z	Write enable. The falling edge of WE indicates that the device is driving the external data bus (D15–D0). Data can be latched by an external device on the rising edge of WE. WE is active on all external program, data, and I/O writes. WE goes in the high-impedance state following reset and when EMU1/ÖFF is active low.
WR	132	O/Z	Write/read. WR is an inverted form of RW and can connect directly to the output enable of external devices. WR is placed in the high-impedance state following reset and when EMU1/ÖFF is active low.

† I = input, O = output, Z = high impedance

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Terminal Functions (Continued)

TERMINAL NAME	NO.	TYPE†	DESCRIPTION
EXTERNAL INTERFACE CONTROL SIGNALS (CONTINUED)			
$\overline{\text{BR}}$	5	O/Z	Bus request. $\overline{\text{BR}}$ is asserted during access of external global data memory space. $\overline{\text{BR}}$ can be used to extend the data memory address space by up to 32K words. $\overline{\text{BR}}$ goes in the high-impedance state during reset, power down, and when EMU1/ $\overline{\text{OFF}}$ is active low.
V _{CCP} /WDDIS	50	I	Flash-programming voltage supply. If V _{CCP} = 5 V, then WRITE/ERASE can be made to the ENTIRE on-chip flash memory block—that is, for programming the flash. If V _{CCP} = 0 V, then WRITE/ERASE of the flash memory is not allowed, thereby protecting the entire memory block from being overwritten. V _{CCP} /WDDIS also functions as a hardware watchdog disable. The watchdog timer is disabled when V _{CCP} /WDDIS = 5 V and bit 6 in WDCR is set to 1.
ADC INPUTS (UNSHARED)			
ADCIN2	74	I	Analog inputs to the first ADC
ADCIN3	75	I	
ADCIN4	76	I	
ADCIN5	77	I	
ADCIN6	78	I	
ADCIN7	79	I	
ADCIN10	89	I	Analog inputs to the second ADC
ADCIN11	88	I	
ADCIN12	83	I	
ADCIN13	82	I	
ADCIN14	81	I	
ADCIN15	80	I	
BIT I/O AND SHARED FUNCTIONS PINS			
ADCIN0/IOPA0	72	I/O	Bidirectional digital I/O. Analog input to the first ADC. ADCIN0/IOPA0 is configured as a digital input by all device resets.
ADCIN1/IOPA1	73	I/O	Bidirectional digital I/O. Analog input to the first ADC. ADCIN1/IOPA1 is configured as a digital input by all device resets.
ADCIN9/IOPA2	90	I/O	Bidirectional digital I/O. Analog input to the second ADC. ADCIN9/IOPA2 is configured as a digital input by all device resets.
ADCIN8/IOPA3	91	I/O	Bidirectional digital I/O. Analog input to the second ADC. ADCIN8/IOPA3 is configured as a digital input by all device resets.
PWM7/CMP7/IOPB0	100	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 1 output. The state of PWM7/CMP7/IOPB0 is determined by the simple compare/PWM and the simple action control register (SACTR). It goes to the high-impedance state when unmasked PDPINT goes active low. PWM7/CMP7/IOPB0 is configured as a digital input by all device resets.
PWM8/CMP8/IOPB1	101	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 2 output. The state of PWM8/CMP8/IOPB1 is determined by the simple compare/PWM and the SACTR. It goes to the high-impedance state when unmasked PDPINT goes active low. PWM8/CMP8/IOPB1 is configured as a digital input by all device resets.
PWM9/CMP9/IOPB2	102	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 3 output. The state of PWM9/CMP9/IOPB2 is determined by the simple compare/PWM and SACTR. It goes to the high-impedance state when unmasked PDPINT goes active low. PWM9/CMP9/IOPB2 is configured as a digital input by all device resets.

† I = input, O = output, Z = high impedance



Terminal Functions (Continued)

TERMINAL NAME	NO.	TYPE†	DESCRIPTION
BIT I/O AND SHARED FUNCTIONS PINS (CONTINUED)			
T1PWM/T1CMP/ IOPB3	105	I/O/Z	Bidirectional digital I/O. Timer 1 compare output. T1PWM/T1CMP/IOPB3 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
T2PWM/T2CMP/ IOPB4	106	I/O/Z	Bidirectional digital I/O. Timer 2 compare output. T2PWM/T2CMP/IOPB4 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
T3PWM/T3CMP/ IOPB5	107	I/O/Z	Bidirectional digital I/O. Timer 3 compare output. T3PWM/T3CMP/IOPB5 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
TMRDIR/IOPB6	108	I/O	Bidirectional digital I/O. Direction signal for the timers. Up-counting direction if TMRDIR/IOPB6 is low, down-counting direction if this pin is high. This pin is configured as a digital input by all device resets.
TMRCLK/IOPB7	109	I/O	Bidirectional digital I/O. External clock input for general-purpose timers. This pin is configured as a digital input by all device resets.
ADCSOC/IOPC0	63	I/O	Bidirectional digital I/O. External start of conversion input for ADC. This pin is configured as a digital input by all device resets.
CAP1/QEP1/IOPC4	67	I/O	Bidirectional digital I/O. Capture 1 or QEP 1 input. This pin is configured as a digital input by all device resets.
CAP2/QEP2/IOPC5	68	I/O	Bidirectional digital I/O. Capture 2 or QEP 2 input. This pin is configured as a digital input by all device resets.
CAP3/IOPC6	69	I/O	Bidirectional digital I/O. Capture 3 input. This pin is configured as a digital input by all device resets.
CAP4/IOPC7	70	I/O	Bidirectional digital I/O. Capture 4 input. This pin is configured as a digital input by all device resets.
XF/IOPC2	65	I/O	Bidirectional digital I/O. External flag output (latched software-programmable signal). XF is used for signaling other processors in multiprocessing configurations or as a general-purpose output pin. This pin is configured as an external flag output by all device resets.
$\overline{\text{BIO}}$ /IOPC3	66	I/O	Bidirectional digital I/O. Branch control input. $\overline{\text{BIO}}$ is polled by the BIOZ instruction. If $\overline{\text{BIO}}$ is low, the CPU executes a branch. If $\overline{\text{BIO}}$ is not used, it should be pulled high. This pin is configured as a branch-control input by all device resets.
CLKOUT/IOPC1	64	I/O	Bidirectional digital I/O. Clock output. Clock output is selected by the CLKSRC bits in the SYSCR register. This pin is configured as a DSP clock output by a power-on reset.
SERIAL COMMUNICATIONS INTERFACE (SCI) AND BIT I/O PINS			
SCITXD/IO	44	I/O	SCI asynchronous serial port transmit data, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SCIRXD/IO	43	I/O	SCI asynchronous serial port receive data, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.

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Terminal Functions (Continued)

TERMINAL NAME	NO.	TYPE†	DESCRIPTION
SERIAL PERIPHERAL INTERFACE (SPI) AND BIT I/O PINS			
SPISIMO/I/O	45	I/O	SPI slave in, master out , or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPISOMI/I/O	48	I/O	SPI slave out, master in, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPICLK/I/O	49	I/O	SPI clock, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPISTE/I/O	51	I/O	SPI slave transmit enable (optional), or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
COMPARE SIGNALS			
PWM1/CMP1 PWM2/CMP2 PWM3/CMP3 PWM4/CMP4 PWM5/CMP5 PWM6/CMP6	94 95 96 97 98 99	O/Z	Compare or PWM outputs. The state of these pins is determined by the compare/PWM and the full action control register (ACTR). CMP1–CMP6 go to the high-impedance state when unmasked PDPINT goes active low. After power up and PORESET is high, the PWM/CMP pins are high-impedance once the internal clock is stable (see Figure 31 and Figure 32).
INTERRUPT AND MISCELLANEOUS SIGNALS			
RS	35	I/O	Reset input. RS causes the TMS320F240 to terminate execution and sets PC = 0. When RS is brought to a high level, execution begins at location zero of program memory. RS affects (or sets to zero) various registers and status bits.
MP/MC	37	I	MP/MC (microprocessor/microcomputer) select. If MP/MC is low, internal program memory is selected. If it is high, external program memory is selected.
NMI	40	I	Nonmaskable interrupt. When NMI is activated, the device is interrupted regardless of the state of the INTM bit of the status register. NMI has programmable polarity.
PORESET	41	I	Power-on reset. PORESET causes the TMS320F240 to terminate execution and sets PC = 0. When PORESET is brought to a high level, execution begins at location zero of program memory. PORESET affects (or sets to zero) the same registers and status bits as RS. In addition, PORESET initializes the PLL control registers.
XINT1	53	I	External user interrupt no. 1
XINT2/I/O	54	I/O	External user interrupt no. 2. General-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
XINT3/I/O	55	I/O	External user interrupt no. 3. General-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
PDPINT	52	I	Maskable power-drive protection interrupt. If PDPINT is unmasked and it goes active low, the timer compare outputs immediately go to the high-impedance state.
CLOCK SIGNALS			
XTAL2	57	O	PLL oscillator output. XTAL2 is tied to one side of a reference crystal when the device is in PLL mode (CLKMD[1:0] = 1x, CKCR0.7–6). This pin can be left unconnected in oscillator bypass mode (OSCBYP ≤ VIL). This pin goes in the high-impedance state when EMU1/OFF is active low.
XTAL1/CLKIN	58	I/Z	PLL oscillator input. XTAL1/CLKIN is tied to one side of a reference crystal in PLL mode (CLKMD[1:0] = 1x, CKCR0.7–6), or is connected to an external clock source in oscillator bypass mode (OSCBYP ≤ VIL).
OSCBYP	56	I	Bypass on-chip oscillator if low

[†] I = input, O = output, Z = high impedance



Terminal Functions (Continued)

TERMINAL NAME	NO.	TYPE†	DESCRIPTION
SUPPLY SIGNALS			
CVSS	8	I	Digital core logic ground reference
VSS	3 14 20 29 46 59 61 71 92 104 113 120	I	Digital logic ground reference
VSSA	87	I	Analog ground reference
DVDD	2 13 21 47 62 93 103 121	I	Digital I/O logic supply voltage
CVDD	7 60	I	Digital core logic supply voltage
VCCA	84	I	Analog supply voltage
VREFHI	85	I	ADC analog voltage reference high
VREFLO	86	I	ADC analog voltage reference low
TEST SIGNALS			
TCK	30	I	JTAG test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test-access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register of the C2xx core on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	31	I	JTAG test data input (TDI). TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	34	O/Z	JTAG test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state when $\overline{\text{OE}}$ is active low.
TMS	33	I	JTAG test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.

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Terminal Functions (Continued)

TERMINAL NAME	NO.	TYPE†	DESCRIPTION
TEST SIGNALS (CONTINUED)			
$\overline{\text{TRST}}$	32	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored.
EMU0	38	I/O/Z	Emulator pin 0. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output through the scan.
EMU1/ $\overline{\text{OFF}}$	39	I/O/Z	Emulator pin 1/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/ $\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output through JTAG scan. When $\overline{\text{TRST}}$ is driven low, this pin is configured as $\overline{\text{OFF}}$. When EMU1/ $\overline{\text{OFF}}$ is active low, it puts all output drivers in the high-impedance state. $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications); therefore, for $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}}$ = low, EMU0 = high, EMU1/ $\overline{\text{OFF}}$ = low
RESERVED	42	I	Reserved for test. This pin has an internal pulldown and must be left unconnected.

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description (continued)

Table 1. Characteristics of the TMS320F240 DSP Controller

ON-CHIP MEMORY (WORDS)			POWER SUPPLY (V)	CYCLE TIME (ns)	PACKAGE TYPE PIN COUNT
RAM		FLASH EEPROM			
DATA	DATA/PROG	PROG			
288	256	16K	5	50	PQ 132-P

architectural overview

The functional block diagram provides a high-level description of each component in the F240 DSP controller. The TMS320F240 device is composed of three main functional units: a C2xx DSP core, internal memory, and peripherals. In addition to these three functional units, there are several system-level features of the F240 that are distributed. These system features include the memory map, device reset, interrupts, digital input/output (I/O), clock generation, and low-power operation.

system-level functions

device memory map

The TMS320F240 implements three separate address spaces for program memory, data memory, and I/O. Each space accommodates a total of 64K 16-bit words. Within the 64K words of data space, the 256 to 32K words at the top of the address range can be defined to be external global memory in increments of powers of two, as specified by the contents of the global memory allocation register (GREG). Access to global memory is arbitrated using the global memory bus request (BR) signal.

On the F240, the first 96 (0–5Fh) data memory locations are either allocated for memory-mapped registers or are reserved. This memory-mapped register space contains various control and status registers including those for the CPU.

All the on-chip peripherals of the F240 device are mapped into data memory space. Access to these registers is made by the CPU instructions addressing their data-memory locations. Figure 1 shows the memory map.

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hardware-generated interrupts (continued)

Table 7. Interrupt Locations and Priorities

INTERRUPT NAME	OVERALL PRIORITY	DSP-CORE INTERRUPT, AND ADDRESS	PERIPHERAL VECTOR ADDRESS	PERIPHERAL VECTOR ADDRESS OFFSET	MASKABLE?	SOURCE PERIPHERAL MODULE	FUNCTION INTERRUPT
$\overline{\text{RS}}$	1 Highest	$\overline{\text{RS}}$ 0000h	N/A		N	Core, SD	External, system reset (RESET)
RESERVED	2	INT7 0026h	N/A	N/A	N	DSP Core	Emulator trap
NMI	3	NMI 0024h	N/A	0002h	N	Core, SD	External user interrupt
XINT1 XINT2 XINT3	4 5 6	INT1 0002h (System)	SYSIVR (701Eh)	0001h 0011h 001Fh	Y	SD	High-priority external user interrupts
SPIINT	7			0005h	Y	SPI	High-priority SPI interrupt
RXINT	8			0006h	Y	SCI	SCI receiver interrupt (high priority)
TXINT	9			0007h	Y	SCI	SCI transmitter interrupt (high priority)
WDTINT	10			0010h	Y	WDT	Watchdog timer interrupt
PDPINT	11	INT2 0004h (Event Manager Group A)	EVIVRA (7432h)	0020h	Y	External	Power-drive protection Int.
CMP1INT	12			0021h	Y	EV.CMP1	Full Compare 1 interrupt
CMP2INT	13			0022h	Y	EV.CMP2	Full Compare 2 interrupt
CMP3INT	14			0023h	Y	EV.CMP3	Full Compare 3 interrupt
SCMP1INT	15			0024h	Y	EV.CMP4	Simple compare 1 interrupt
SCMP2INT	16			0025h	Y	EV.CMP5	Simple compare 2 interrupt
SCMP3INT	17			0026h	Y	EV.CMP6	Simple compare 3 interrupt
TPINT1	18			0027h	Y	EV.GPT1	Timer1-period interrupt
TCINT1	19			0028h	Y	EV.GPT1	Timer1-compare interrupt
TUFINT1	20			0029h	Y	EV.GPT1	Timer1-underflow interrupt
TOFINT1	21			002Ah	Y	EV.GPT1	Timer1-overflow interrupt
TPINT2	22	INT3 0006h (Event Manager Group B)	EVIVRB (7433h)	002Bh	Y	EV.GPT2	Timer2-period interrupt
TCINT2	23			002Ch	Y	EV.GPT2	Timer2-compare interrupt
TUFINT2	24			002Dh	Y	EV.GPT2	Timer2-underflow interrupt
TOFINT2	25			002Eh	Y	EV.GPT2	Timer2-overflow interrupt
TPINT3	26			002Fh	Y	EV.GPT3	Timer3-period interrupt
TCINT3	27			0030h	Y	EV.GPT3	Timer3-compare interrupt
TUFINT3	28			0031h	Y	EV.GPT3	Timer3-underflow interrupt
TOFINT3	29			0032h	Y	EV.GPT3	Timer3-overflow interrupt
CAPINT1	30	INT4 0008h (Event Manager Group C)	EVIVRC (7434h)	0033h	Y	EV.CAP1	Capture 1 interrupt
CAPINT2	31			0034h	Y	EV.CAP2	Capture 2 interrupt
CAPINT3	32			0035h	Y	EV.CAP3	Capture 3 interrupt
CAPINT4	33			0036h	Y	EV.CAP4	Capture 4 interrupt

hardware-generated interrupts (continued)

Table 7. Interrupt Locations and Priorities (Continued)

INTERRUPT NAME	OVERALL PRIORITY	DSP-CORE INTERRUPT, AND ADDRESS	PERIPHERAL VECTOR ADDRESS	PERIPHERAL VECTOR ADDRESS OFFSET	MASKABLE?	SOURCE PERIPHERAL MODULE	FUNCTION INTERRUPT
SPIINT	34	INT5 000Ah (System)	SYSIVR (701Eh)	0005h	Y	SPI	Low-priority SPI interrupt
RXINT	35			0006h	Y	SCI	SCI receiver interrupt (low priority)
TXINT	36			0007h	Y	SCI	SCI transmitter interrupt (low priority)
ADCINT	37	INT6	SYSIVR	0004h	Y	ADC	Analog-to-digital interrupt
XINT1	38	000Ch (System)	(701Eh)	0001h	Y	External pins	Low-priority external user interrupts
XINT2	39			0011h	Y		
XINT3	40			001Fh	Y		
RESERVED	41	000Eh	N/A		Y	DSP Core	Used for analysis
TRAP	N/A	0022h	N/A		N/A		TRAP instruction vector

external interrupts

The F240 has five external interrupts. These interrupts include:

- **XINT1.** Type A interrupt. The XINT1 control register (at 7070h) provides control and status for this interrupt. XINT1 can be used as a high-priority (Level 1) or low-priority (Level 6) maskable interrupt or as a general-purpose input pin. XINT1 can also be programmed to trigger an interrupt on either the rising or the falling edge.
- **NMI.** Type A interrupt. The NMI control register (at 7072h) provides control and status for this interrupt. NMI is a nonmaskable external interrupt or a general-purpose input pin. NMI can also be programmed to trigger an interrupt on either the rising or the falling edge.
- **XINT2.** Type C interrupt. The XINT2 control register (at 7078h) provides control and status for this interrupt. XINT2 can be used as a high-priority (Level 1) or low-priority (Level 6) maskable interrupt or a general-purpose I/O pin. XINT2 can also be programmed to trigger an interrupt on either the rising or the falling edge.
- **XINT3.** Type C interrupt. The XINT3 control register (at 707Ah) provides control and status for this interrupt. XINT3 can be used as a high-priority (Level 1) or low-priority (Level 6) maskable interrupt or as a general-purpose I/O pin. XINT3 can also be programmed to trigger an interrupt on either the rising or the falling edge.
- **PDPINT.** This interrupt is provided for safe operation of the power converter and motor drive. This maskable interrupt can put the timers and PWM output pins in the high-impedance state and inform the CPU in case of motor drive abnormalities such as overvoltage, overcurrent, and excessive temperature rise. PDPINT is a Level 2 interrupt.

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external interrupts (continued)

Table 8 is a summary of the external interrupt capability of the F240.

Table 8. External Interrupt Types and Functions

EXTERNAL INTERRUPT	CONTROL REGISTER NAME	CONTROL REGISTER ADDRESS	INTERRUPT TYPE	CAN DO NMI?	DIGITAL I/O PIN	MASKABLE?
XINT1	XINT1CR	7070h	A	No	Input only	Yes (Level 1 or 6)
NMI	NMICR	7072h	A	Yes	Input only	No
XINT2	XINT2CR	7078h	C	No	I/O	Yes (Level 1 or 6)
XINT3	XINT3CR	707Ah	C	No	I/O	Yes (Level 1 or 6)
PDPIINT	EVIMRA	742Ch	N/A	N/A	N/A	Yes (Level 2)

clock generation

The TMS320F240 has an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The only external component necessary for this module is an external fundamental crystal, or oscillator.

The PLL-based clock module provides two basic modes of operation: oscillator mode and clock-in mode.

- oscillator mode
This mode allows the use of a 4-, 6-, or 8-MHz external reference crystal to provide the time base to the device. The internal oscillator circuitry is initialized by software to select the desired CPUCLK frequency, which can be the input clock frequency, the input clock frequency divided by 2 (default), or a clock frequency determined by the PLL.
- Clock-in mode
This mode allows the internal crystal oscillator circuitry to be bypassed. The device clocks are generated from an external clock source input on the XTAL1/CLKIN pin. The device can be configured by software to operate on the input clock frequency, the input clock frequency divided by 2, or a clock frequency determined by the PLL.

The F240 runs on two clock frequencies: the CPU clock (CPUCLK) frequency, and the system clock (SYSCLK) frequency. The CPU, memories, external memory interface, and event manager run at the CPUCLK frequency. All other peripherals run at the SYSCLK frequency. The CPUCLK runs at 2x or 4x the frequency of the SYSCLK; for example, for 2x, CPUCLK = 20 MHz and SYSCLK = 10 MHz. There is also a clock for the watchdog timer, WDCLK. This clock has a nominal frequency of 16384 Hz (214 Hz) when XTAL1/CLKIN is a power of two or a sum of two powers of two; for example, 4194304 Hz (222 Hz), 6291456 (222 + 221 Hz), or 8388608 Hz (223 Hz).

The clock module includes three external pins:

1. XTAL1/CLKIN clock source/crystal input
2. XTAL2 output to crystal
3. $\overline{\text{OSCBYP}}$ oscillator bypass

For the external pins, if $\overline{\text{OSCBYP}} \geq V_{IH}$, then the oscillator is enabled and if $\overline{\text{OSCBYP}} \leq V_{IL}$, then the oscillator is bypassed and the device is in clock-in mode. In clock-in mode, an external TTL clock must be applied to the XTAL1/CLKIN pin. The XTAL2 pin can be left unconnected.



output current variation with output voltage: SPICE simulation results

Condition: Temperature : 150° C
Voltage : 4.5 V

Table 17. Typical Output Source Current vs. Output Voltage High

	2.4 V	3.0 V	3.5 V	4.0 V
RS	–19 mA	–16 mA	–12 mA	–6 mA
See complete listing of pin names [†]	–16 mA	–13.5 mA	–9.5 mA	–5.0 mA
All other inputs	–23 mA	–18.5 mA	–13 mA	–6.5 mA

[†] IOPA[0:3], SCIRXD/IO, SCITXD/IO, XINT2/IO, XINT3/IO, ADCSOC/IOPC0, TMRDIR/IOPB6, TMRCLK/IOPB7 EMU0, EMU1/OFF

Table 18. Typical Output Sink Current vs. Output Voltage Low

	0.6 V	0.4 V	0.2 V
RS	8 mA	6 mA	3 mA
See complete listing of pin names [†]	7.5 mA	5 mA	2.5 mA
All other inputs	14.5 mA	10 mA	5.0 mA

[†] IOPA[0:3], SCIRXD/IO, SCITXD/IO, XINT2/IO, XINT3/IO, ADCSOC/IOPC0, TMRDIR/IOPB6, TMRCLK/IOPB7 EMU0, EMU1/OFF

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	5-V operation, I _{OH} = MAX	2.4			V
V _{OL}	Low-level output voltage	5-V operation, I _{OL} = MAX			0.6	V
I _I	Input current (V _I = V _{SS} or V _{DD})	TRST pin with internal pulldown	–10		500	μA
		EMU0, EMU1/OFF, TMS, TCK, and TDI, with internal pullup	–500		10	
		All other input pins	–10		10	
I _{OZ}	Output current, high-impedance state (off-state)	V _O = V _{DD} or 0 V	–5		5	μA
I _{DD}	Supply current, operating mode	5-V operation, t _c (CO) = 50 ns		80		mA
	Supply current, Idle 1 low-power mode	5-V operation, t _c (CO) = 50 ns		50		
	Supply current, Idle 2 low-power mode	5-V operation, t _c (CO) = 50 ns		7		
	Supply current, PLL power-down mode	5-V operation, t _c (CO) = 50 ns		1		
	Supply current, OSC power-down mode	5-V operation, t _c (CO) = 50 ns		400		μA
C _i	Input capacitance			15		pF
C _o	Output capacitance			15		pF
I _{DDP}	Flash programming supply current	5-V operation, t _c (CO) = 50 ns		10		mA

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TMS320F240PQ	ACTIVE	BQFP	PQ	132	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72HR
TMS320F240PQA	ACTIVE	BQFP	PQ	132	36	TBD	CU SNPB	Level-4-220C-72HR
TMS320F240PQG4	ACTIVE	BQFP	PQ	132	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72HR
TMS320F240PQS	ACTIVE	BQFP	PQ	132	36	TBD	CU SNPB	Level-4-220C-72HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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