

1A Peak Sink/Source PCDDR3 Termination Regulator with Integrated Isolation Switch and Low Power Mode Operation

Check for Samples: [TS3DDR32611](#)

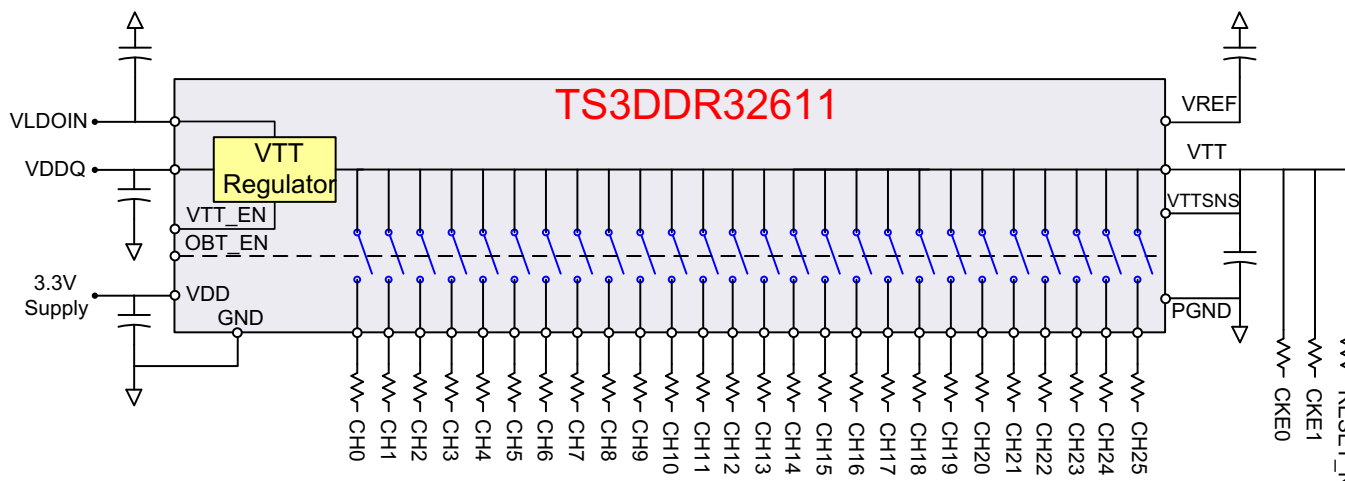
FEATURES

- **VDD Range** – 3.0V to 3.6V
- **R_{ON}** 1.75Ω typical
- **Channel Count** – 26
- **V_{DDQ}** – Input Voltage 1.2V to 3.5V
- **V_{TT}** – $V_{DDQ}/2 \pm 1\% \times V_{DDQ}$ with 60mA Sink or Source
- **V_{REF}** – $V_{DDQ}/2 \pm 1\% \times V_{DDQ}$
- **Switch Time** – (T_{ON/OFF}) 100ns Max
- **I_{DD}** Supply Current
 - High Speed Mode (I_{DD,HS}) 220 μA Max
 - Low Speed Mode (I_{DD,LS}) 220 μA Max
 - Power Down Mode (I_{DD,PD}) 5 μA Max
- **Special Features**
 - 1.8-V Compatible Control Inputs (V_{TT_EN}, ODT_EN)
 - High current Sinking/Sourcing Capability: 1A Max
- **48-Ball ZQC Package** (4mm x 4mm, 0.5mm pitch)

APPLICATIONS

- Double Data Rate type 3 (PCDDR3) termination and regulation in mobile devices

SWITCH DIAGRAM



DESCRIPTION

The TS3DDR32611 is a sink/source double data rate type III (PCDDR3) termination regulator with a 1% accuracy buffered reference output. It has built-in termination SPST switches that can be disconnected when the memory system undergoes lower speed operation without the need of voltage termination. Turning off these switches enables significant power saving on the memory system. The switches on-state resistance has a typical value of only 1.75Ω which helps retain signal integrity on the signal lines.

The TS3DDR32611 is powered from a 3.3V supply. The V_{DDQ} pin takes 1.2V to 1.8V input while the output voltage at V_{TT} pin is $1/2V_{DDQ} \pm 1\% \times V_{DDQ}$. The regulator's V_{TT} output is capable of sinking/sourcing up to 1A current, while the V_{REF} pin output is $1/2V_{DDQ} \pm 1\% \times V_{DDQ}$ with 10mA current sinking/sourcing capability. The TS3DDR32611 has 4 modes of operation: high speed, low speed, V_{REF} mode and power down mode, depending on the control signals V_{TT_EN} and ODT_EN. These different modes of operation provide flexibility to establish a memory system's performance and power consumption.

The TS3DDR32611 is situated within a small 48 balls BGA package with only 4mm x 4mm in size, which makes it a perfect candidate to be used in mobile applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

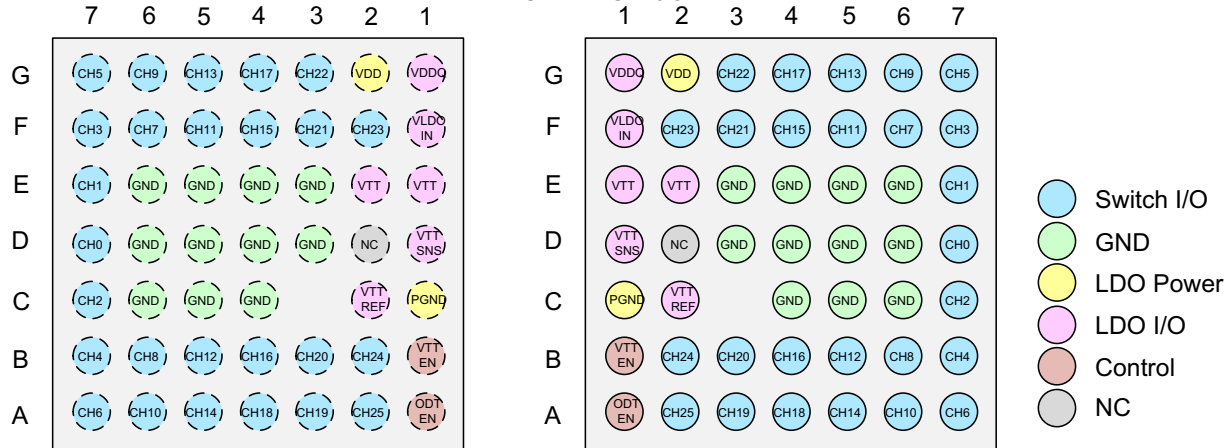
TS3DDR32611

SCDS347 –AUGUST 2013

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DIE SIZE: 4.0 mm × 4.0 mm
BUMP PITCH: 0.5 mm



TS3DDR32611 Pin Mapping⁽¹⁾

	7	6	5	4	3	2	1
G	CH5	CH9	CH13	CH17	CH22	VDD	VDDQ
F	CH3	CH7	CH11	CH15	CH21	CH23	VLODIN
E	CH1	GND	GND	GND	GND	VTT	VTT
D	CH0	GND	GND	GND	GND	NC	VTTSENS
C	CH2	GND	GND	GND		VREF	PGND
B	CH4	CH8	CH12	CH16	CH20	CH24	VTT_EN
A	CH6	CH10	CH14	CH18	CH19	CH25	ODT_EN

(1) The NC must be floating, and cannot be connected to anything.

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NO.	NAME		
C4, C5, C6, D3, D4, D5, D6, E3, E4, E5, E6	GND	—	Signal Ground
E1, E2	VTT	O	Power output for VTT LDO, need to connect 10-μF or greater MLCC for stability
C1	PGND	—	Power GND for VTT LDO
D1	VTTSENS	I	VTT LDO voltage sense input
F1	VLDOIN	I	Power supply input for VTT/ VTTREF
C2	VREF	O	VREF buffered reference output. Need to connect 0.22-μF or greater MLCC for stability.
B1	VTT_EN	I	Enable signal for VTT and VREF output
A1	ODT_EN	I	Enable signal for Switch
G1	VDDQ	I	VDDQ input, reference input for VREF
G2	VDD	I	Device power supply input 3.3 V typical
D7, E7, C7, F7, B7, G7, A7, F6, B6, G6, A6, F5, B5, G5, A5, F4, B4, G5, A4, A3, B3, F3, G3, F2, B2, A2	CH0-CH25	I/O	Switch input or output
D2	NC	—	Not connected, must be floating and cannot be connected to any signal

FUNCTION TABLE

STATE	VTT_EN ⁽¹⁾	ODT_EN ⁽¹⁾	VTT	VREF	SWITCH
Power Down mode ⁽²⁾	L	L	OFF(Discharge)	OFF(Discharge)	Disabled
Low Speed mode	H	L	ON	ON	Disabled
High Speed mode	H	H	ON	ON	Enabled

- (1) The VTT_EN and ODT_EN pins has 6MΩ weak pull-down resistor to GND to make its default value to be LOW.
(2) For VTT_EN= L and ODE_EN= H, the TS3DDR32611 will also stays in the power down mode. However, there will be an increased leakage current of up to max 25μA depending on the voltage level of ODT_EN and is thus not a recommended setting to use.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{DD}	Supply voltage range ⁽³⁾	−0.3	5.5	V
V _{CTRL}	Control input (VTT_EN, ODT_EN) voltage range ⁽³⁾	−0.3	5.5	V
V _{DDQ}	V _{DDQ} input voltage range ⁽³⁾	−0.3	3.6	V
V _{LDOIN}	V _{LDOIN} input voltage range ⁽³⁾	−0.3	3.6	V
V _{TT} , V _{REF}	V _{TT} , V _{REF} output voltage range ⁽³⁾	−0.3	3.6	V
V _{TTSNS}	V _{TTSNS} input voltage range ⁽³⁾	−0.3	3.6	V
PGND	PGND input voltage range ⁽³⁾	−0.3	0.3	V
HBM	Electrostatic discharge QSS 009-105 (JESD22-A114A)		2	kV
CDM	Electrostatic discharge QSS 009-147 (JESD22-C101B.01)		500	V
T _J	Junction temperature	−40	125	°C
T _A	Operating free-air temperature	−55	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to GND, unless otherwise specified.

PACKAGE THERMAL IMPEDANCE⁽¹⁾

		TYP	UNIT
θ _{JA}	Package thermal impedance	101 ⁽²⁾	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.
(2) 69.2°C/W With 4 Central GND vias when layout.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{DD}	Supply voltage range ⁽¹⁾	3.0	3.6	V
V _{CTRL}	Control input (VTT_EN, ODT_EN) voltage range ⁽¹⁾	0	3.6	V
V _{DDQ}	V _{DDQ} input voltage range ⁽¹⁾	1.2	1.5	V
V _{LDOIN}	V _{LDOIN} input voltage range ⁽¹⁾	VTT+0.4	1.5	V
V _{TT} , V _{REF}	V _{TT} , V _{REF} output voltage range ⁽¹⁾	0.6	0.75	V
V _{TTSNS}	V _{TTSNS} input voltage range ⁽¹⁾	0.6	0.75	V
PGND	PGND input voltage range ⁽¹⁾	−0.1	0.1	V
T _A	Operating free-air temperature	−40	85	°C

- (1) All voltages are with respect to GND, unless otherwise specified.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, Typical values are at V_{DD} = 3.3V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I _{VDD(HS)}	V _{DD} supply current in high speed mode ⁽¹⁾	V _{DD} = 3.3V	No load, VTT_EN=ODT_EN= 1.8V, V _{DDQ} =1.5 V		150		μA
I _{VDD(LS)}	V _{DD} supply current in low speed mode ⁽¹⁾	V _{DD} = 3.3V	No load, VTT_EN=1.8V, ODT_EN= 0V, V _{DDQ} =1.5V		150		μA
I _{VDD(PD)}	V _{DD} supply current in power down mode ⁽¹⁾	V _{DD} = 3.3V	No load, VTT_EN=0V,ODT_EN= 0V, V _{DDQ} =1.5V		1		μA
I _{VLDIOIN}	V _{LDOIN} supply current in high or low speed mode	V _{DD} = 3.3V	No load, VTT_EN=H, ODT_EN= H or L, V _{DDQ} =1.5V		1		μA
I _{VLDIOIN(PD)}	V _{LDOIN} supply current in power down mode	V _{DD} = 3.3V	No load, VTT_EN=L, ODT_EN=H or L, V _{DDQ} =1.5V		1		μA
V _{TT} OUTPUT							
V _{TT}	Output voltage			V _{DDQ} /2			V
V _{TTTOL}	Output voltage tolerance to 1/2V _{DDQ}	V _{DDQ} = 1.25V, 1.35V, 1.5V	I _{VTT} < 60 mA	−0.01×V _{DDQ} 0.01×V _{DDQ}			mV
			I _{VTT} < 550 mA	±20			
			I _{VTT} < 1 A	±30			
I _{VTT(SRC)}	Source current limit	V _{DDQ} = 1.5 V	V _{TT} =V _{TTSNS} =0.6 V	1000			mA
I _{VTT(SINK)}	Sink current limit	V _{DDQ} = 1.5 V	V _{TT} =V _{TTSNS} =0.9 V	1000			mA
I _{VTT(max)}	Max Source or Sink current capability	V _{DDQ} = 1.5 V	V _{TT} =V _{TTSNS} =0 V			1.5	A
I _{VTT(DIS)}	V _{TT} Discharge current	V _{DDQ} = 0 V	VTT_EN=L, ODT_EN=H or L, V _{TT} = 0.5 V, T _A =25°C			10	mA
I _{VTTSNS(BIAS)}	V _{TTSNS} Input Bias current	V _{TTSNS} =V _{REF}	No load, VTT_EN=H, ODT_EN= H	−0.1		0.1	μA
V _{REF} OUTPUT							
V _{REF}	Output voltage			V _{DDQ} /2			V
V _{REFTOL}	Output voltage tolerance to 1/2V _{DDQ}	V _{DDQ} = 1.25V, 1.35V, 1.5V	I _{VREF} < 10 mA	V _{DDQ} /2−1.25%*V _{DDQ} V _{DDQ} /2+1.25%*V _{DDQ}			mV
I _{VREF(SRC)}	Source current limit	V _{DDQ} = 1.5V	V _{REF} =0 V	10			mA
I _{VREF(SINK)}	Sink current limit	V _{DDQ} = 0V	V _{REF} =1.5 V	10			mA
V _{VREF(DIS)}	VREF Discharge current	V _{DDQ} = 0V	VTT_EN=L,ODT_EN=H or L, V _{REF} =0.5 V, T _A = 25°C			1	mA
V _{DDQ} INPUT							
I _{VDDQ}	V _{DDQ} input current	V _{DDQ} = 1.5V		30			μA
ISOLATION SWITCH							
R _{ON}	ON-state resistance	V _{DD} = 3.3V	V _{I/O} = 0.75 V, I _{VTT} = 18 mA	1.75			Ω
R _{ON, FLAT}	ON-state resistance flatness	V _{DD} = 3.3V	V _{I/O} = 0 V to 0.75 V, I _{VTT} = 18 mA	0.2			Ω
ΔR _{ON}	ON-state resistance match between channels	V _{DD} = 3.3V	V _{I/O} = 0.75 V, I _{VTT} = 18 mA	0.2			Ω
DIGITAL CONTROL INPUTS (VTT_EN, ODT_EN)							
V _{IH}	Input logic high	V _{DD} = 3.0 V to 3.6 V		1.3			V
V _{IL}	Input logic low	V _{DD} = 3.0 V to 3.6 V				0.6	V
V _{LHYST}	Hysteresis voltage			0.22			V
I _{LK}	Input leak current			−1		1	μA
OVER-TEMPERATURE PROTECTION							
T _{OTP}	Over temperature protection	Shutdown temperature		150			°C
		Hysteresis		30			

- (1) For ODT_EN and VTT_EN, If the V_{IH} is less than 1.8V but more than Max V_{IH}, or V_{IL} is more than 0V but less than Max V_{IL}, it will cause the I_{VDD} has the max 25μA increase based on the voltage at ODT_EN and VTT_EN.

DYNAMIC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{ON/OFF}$	Switching time between low speed and high speed mode	$R_L = 50\Omega$, $C_L = 5\text{pF}$	$V_{DD} = 3.0\text{ V to }3.6\text{ V}$		100		ns
$t_{RAMP(VTT)}$	V_{TT} ramp time	$C_{VTT} = 20\text{ }\mu\text{F}$	$V_{DD} = 3.0\text{V to }3.6\text{V}$, $I_{VTT} = 0$		50		μs
$t_{RAMP(VREF)}$	V_{REF} ramp time	$C_{VREF} = 220\text{ nF}$	$V_{DD} = 3.0\text{V to }3.6\text{V}$, $I_{VREF} = 0$		30		μs
C_{ON}	Switch input ON capacitance	$V_{DD} = 3.3\text{V}$, $V_{I/O} = 0$ or 0.75V , $f = 1066\text{MHz}$	Switch ON		TBD		pF
C_{OFF}	Switch input OFF capacitance	$V_{DD} = 3.3\text{V}$, $V_{I/O} = 0$ or 0.75V , $f = 400\text{MHz}$, 667MHz , 933MHz and 1066MHz	Switch OFF		TBD		pF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DDR32611ZQCR	PREVIEW	BGA MICROSTAR JUNIOR	ZQC	48	2500	TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

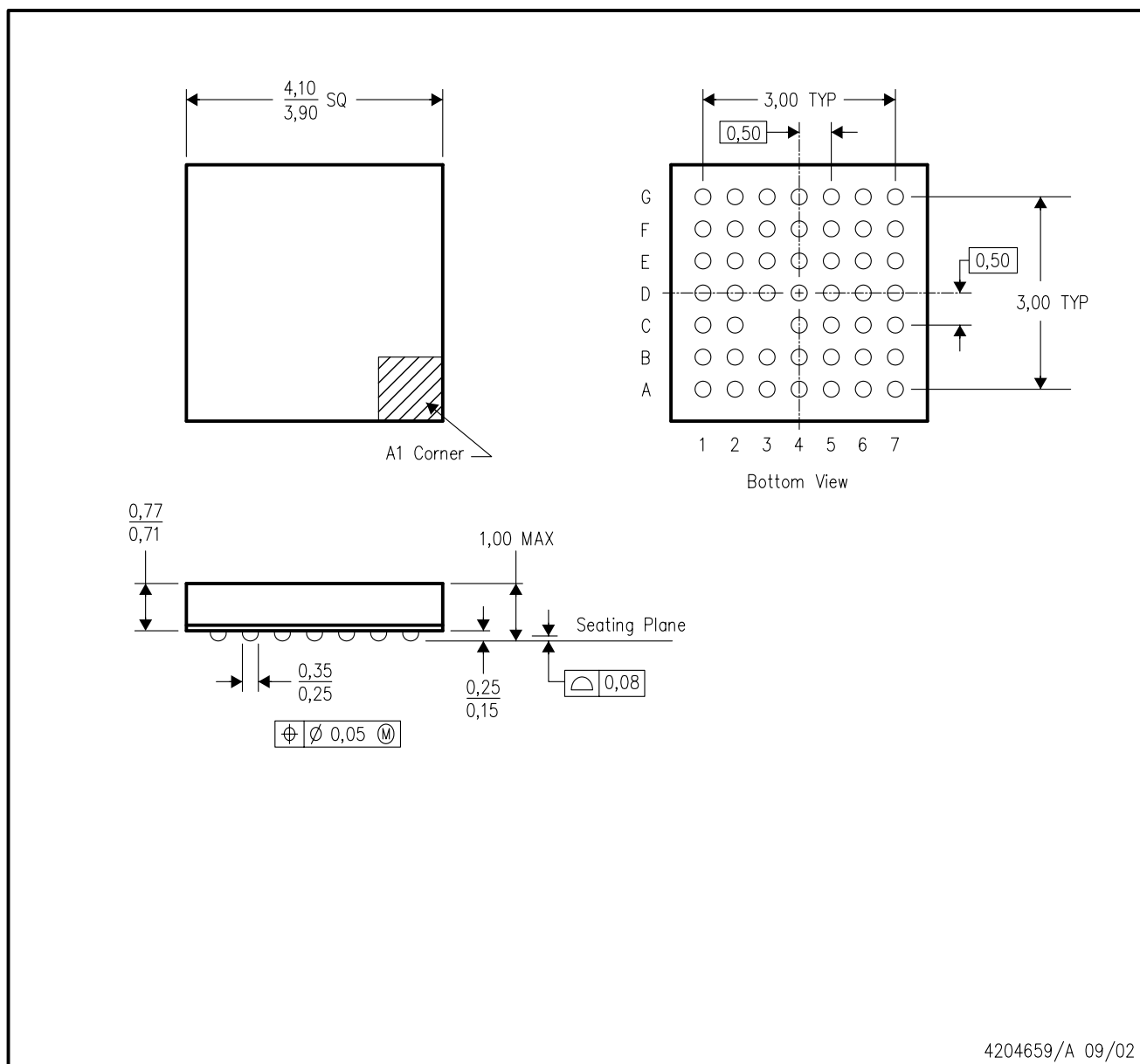
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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ZQC (S-PBGA-N48)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ BGA configuration
 - D. Falls within JEDEC MO-225
 - E. This package is lead-free.

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