



UTRON

Rev. 1.1

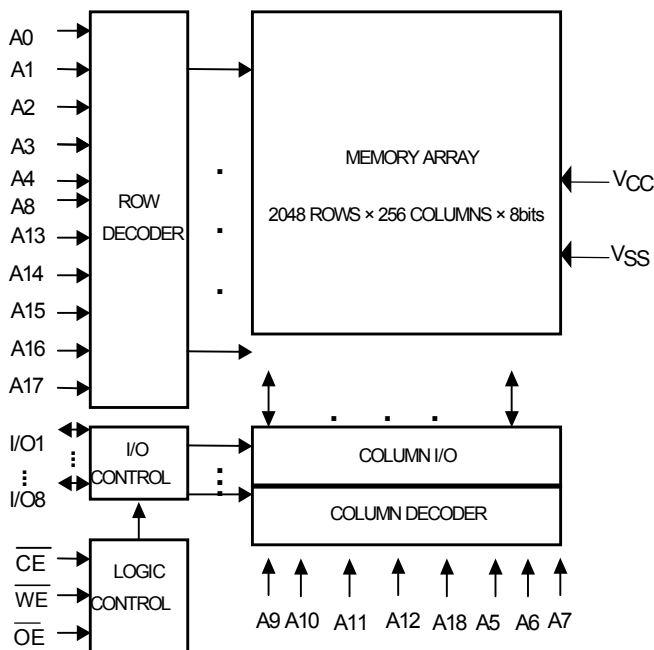
UT62L5128

512K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time: 55ns(max) for $V_{CC}=3.0V\sim 3.6V$
70/100ns(max) for $V_{CC}=2.7V\sim 3.6V$
- CMOS Low operating power
Operating : 45/35/25mA (I_{CC} max)
Standby : 20 μ A (TYP.) L-version
3 μ A (TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operating Temperature:
Commercial : 0°C~70°C
Extended : -20°C~80°C
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Package : 32-pin 8mm×20mm TSOP-I
32-pin 8mm×13.4mm STSOP
36-pin 6mm×8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

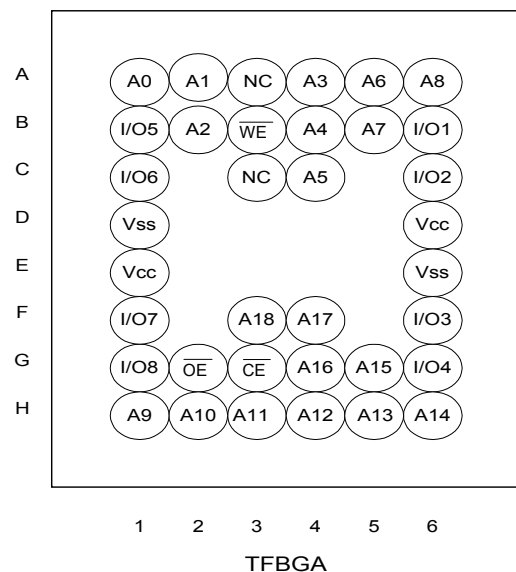
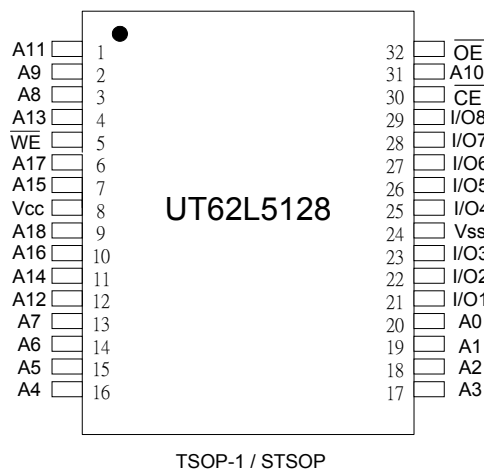
GENERAL DESCRIPTION

The UT62L5128 is a 4,194,304-bit high speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT62L5128 is designed for high speed system applications. It is particularly well suited for battery back-up nonvolatile memory applications.

The UT62L5128 operates from a single 2.7V~3.6V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



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TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	SUPPLY CURRENT
Standby	X	H	X	High – Z	I_{SB}, I_{SB1}
Output Disable	H	L	H	High – Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70	$^{\circ}C$
	Extended	T_A	-20 to 80	$^{\circ}C$
Storage Temperature		T_{STG}	-65 to 150	$^{\circ}C$
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		T_{solder}	260	$^{\circ}C$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7V \sim 3.6V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$ / $-20^{\circ}C$ to $80^{\circ}C(E)$)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	V _{CC}			2.7	3.0	3.6	V
Input High Voltage	V _{IH}			2.0	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL}			- 0.2	-	0.6	V
Input Leakage Current	I _{LI}	V _{SS} ≤ V _{IN} ≤ V _{CC}		- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{SS} ≤ V _{I/O} ≤ V _{CC} , Output Disabled		- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = - 1mA		2.2	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA		-	-	0.4	V
Operating Power Supply Current	I _{CC}	Cycle time=Min.100% duty, CE = V _{IL} , I _{I/O} =0mA ,	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
	I _{CC1}	Cycle time = 1μs,100% duty, CE ≤ 0.2,I _{I/O} =0mA, other pins at 0.2V or V _{CC} -0.2V,	-	4	5	mA	
	I _{CC2}	Cycle time =500ns,100% duty, CE ≤ 0.2,I _{I/O} =0mA other pins at 0.2V or V _{CC} -0.2V,	-	8	10	mA	
Standby Current(TTL)	I _{SB1}	CE =V _{IH}		-	0.3	0.5	mA
Standby Current(CMOS)	I _{SB1}	CE ≥ V _{CC} -0.2V	-L	-	20	80	μA
		other pins at 0.2V or V _{CC} -0.2V,	-LL	-	3	25	μA



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CAPACITANCE (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V, TA = 0°C to 70°C / -20°C to 80°C(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L5128-55*		UT62L5128-70		UT62L5128-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	100	-	ns
Address Access Time	t _{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t _{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t _{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t _{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t _{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t _{OHZ*}	-	20	-	25	-	35	ns
Output Hold from Address Change	t _{OH}	5	-	5	-	5	-	ns

(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L5128-55*		UT62L5128-70		UT62L5128-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t _{WHZ*}	-	30	-	30	-	40	ns

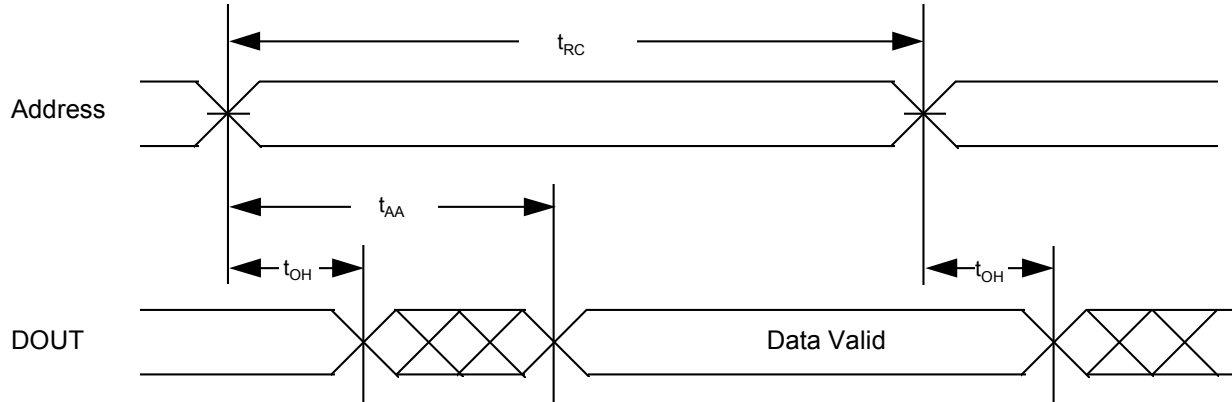
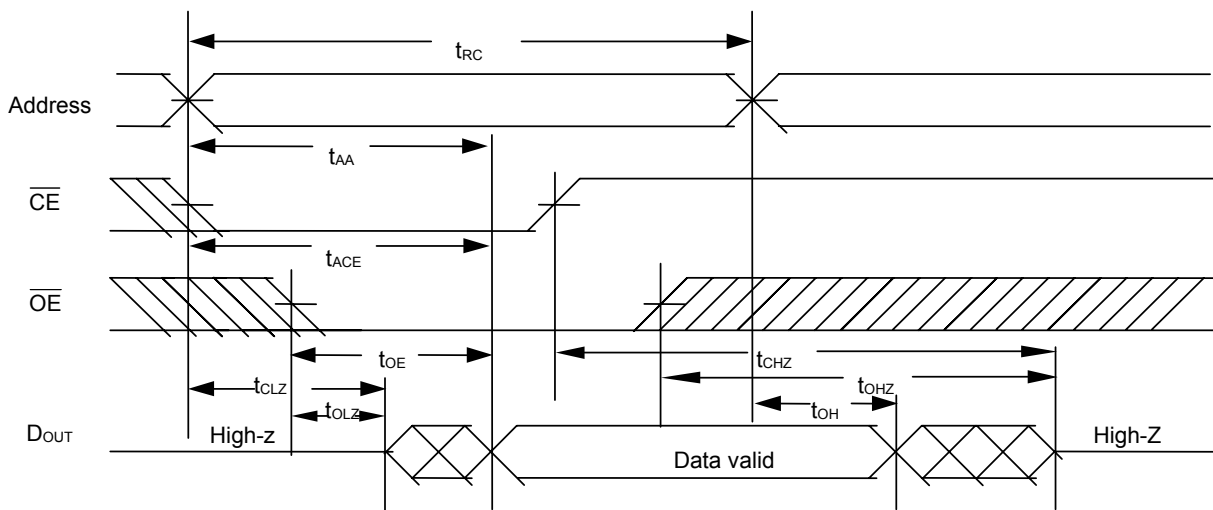
*These parameters are guaranteed by device characterization, but not production tested.

*55ns for V_{CC}=3.0V~3.6V



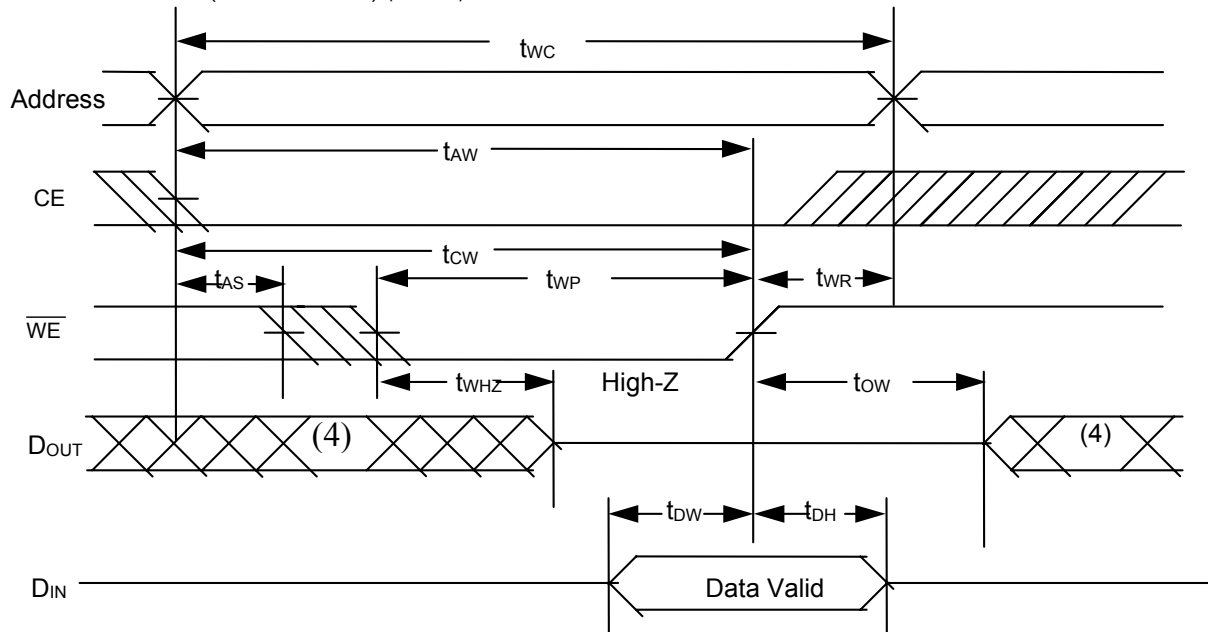
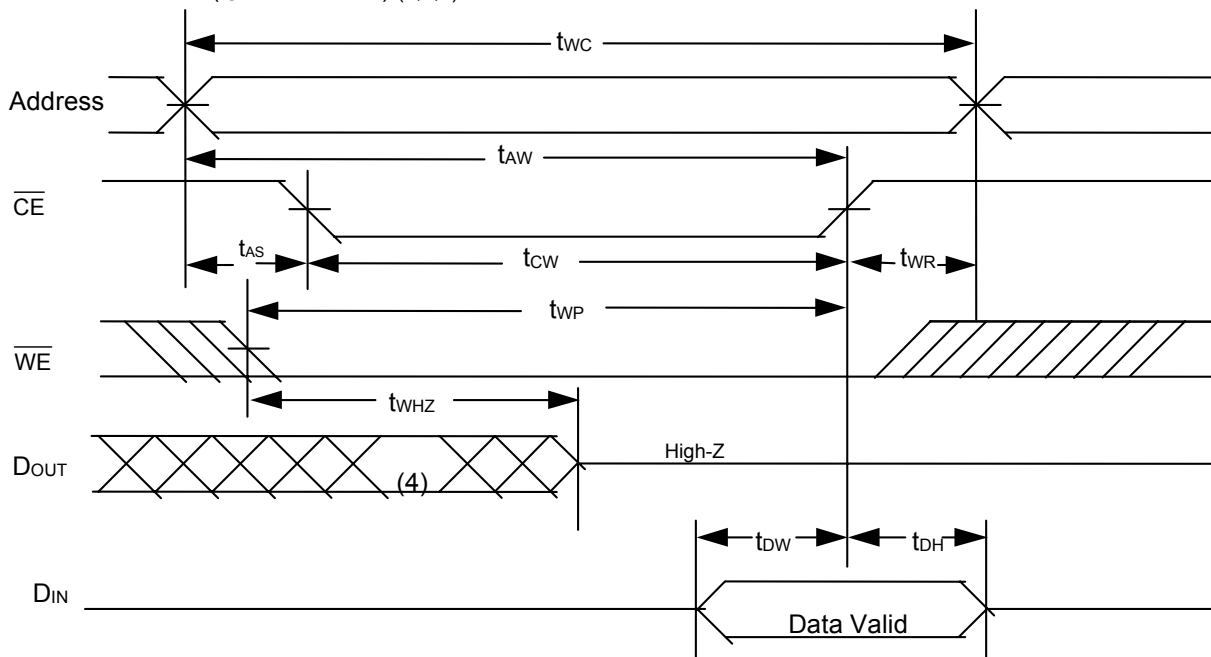
TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)

Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

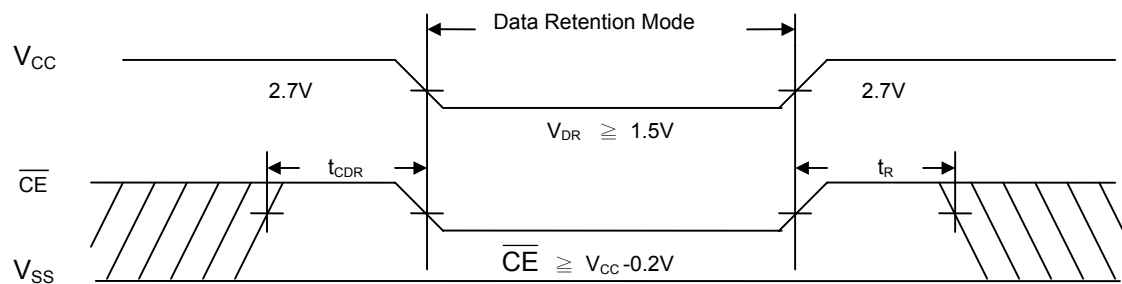
**WRITE CYCLE 1** ($\overline{WE}$ Controlled) (1,2,3,5)**WRITE CYCLE 2** ($\overline{CE}$ Controlled) (1,2,5)

Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ} + t_{OW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

**DATA RETENTION CHARACTERISTICS** ($T_A = 0^{\circ}\text{C}$ to 70°C / -20°C to 80°C (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	$\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =1.5V $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$	- L	1	50	μA
			- LL	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t _R		5	-	-	ms

DATA RETENTION WAVEFORM



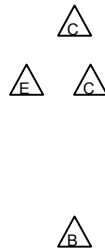
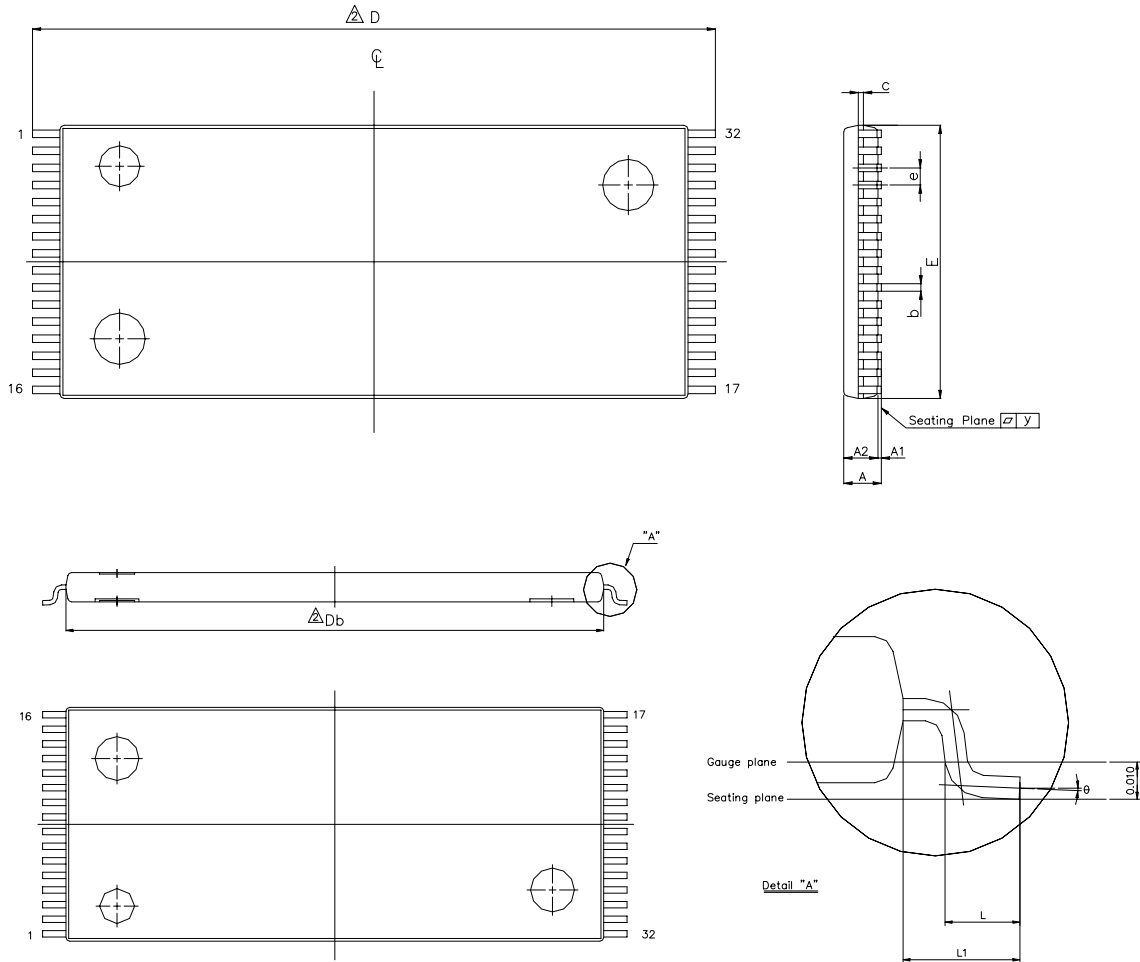
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PACKAGE OUTLINE DIMENSION

32 pin 8mm × 20mm TSOP-I PACKAGE OUTLINE DIMENSION



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 + 0.002	0.20 + 0.05
c		0.005 (TYP)	0.127 (TYP)
D		0.724 ±0.004	18.40 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.08 ±0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°



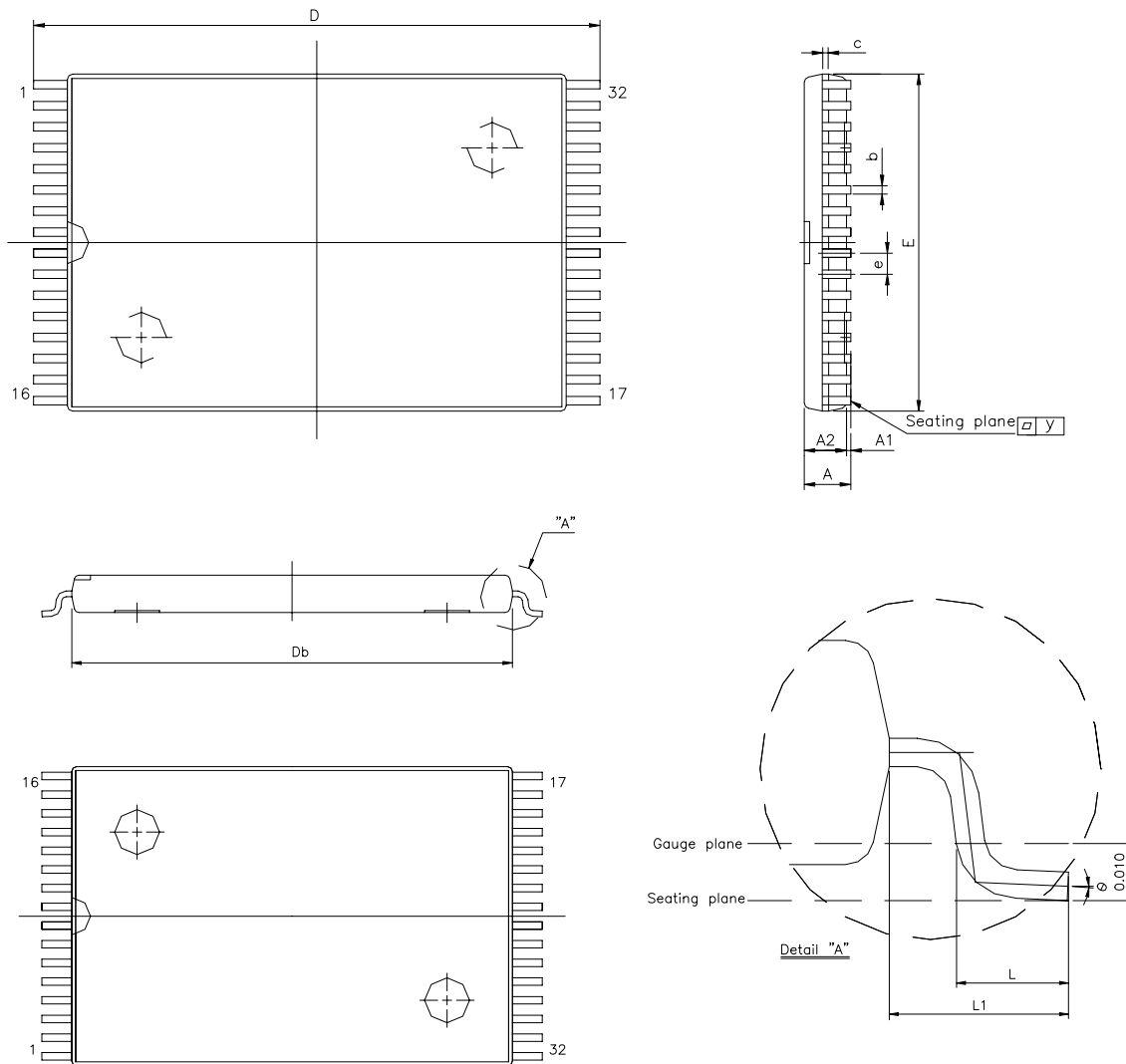
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512K X 8 BIT LOW POWER CMOS SRAM

32 pin 8mm x 13.4mm STSOP PACKAGE OUTLINE DIMENSION



Note :

- 1.E dimension is not including end flash.
- 2.The total of both sides' end flash is not above 0.3mm.

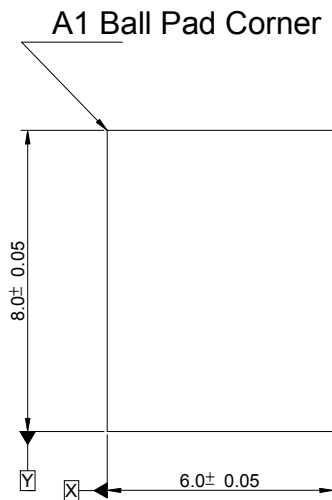
SYMBOL	UNIT	MM(REF)	INCH(BASE)
A		1.20(Max.)	0.047(Max.)
A1		0.1060.05	0.00460.002
A2		1.0060.05	0.03960.002
b		0.20(typ.)	0.006(typ.)
c		0.15(typ.)	0.006(typ.)
D		13.4060.20	0.52660.006
Db		11.8060.10	0.46560.004
E		8.00060.10	0.31560.004
e		0.50(typ.)	0.020(typ.)
L		0.5060.10	0.02060.004
L1		0.8060.10	0.031560.004
y		0.08(Max.)	0.003(Max.)
e		08~58	08~58

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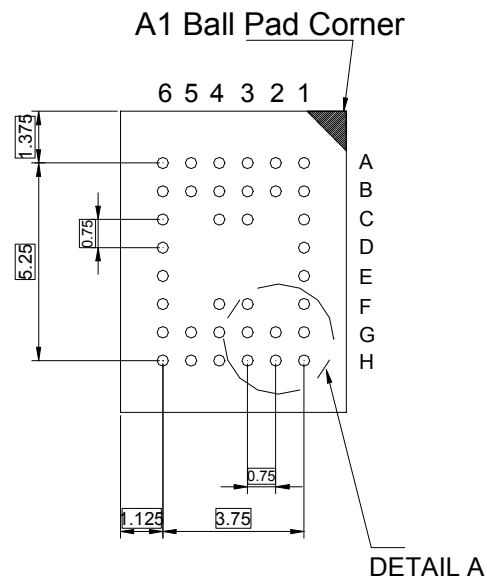
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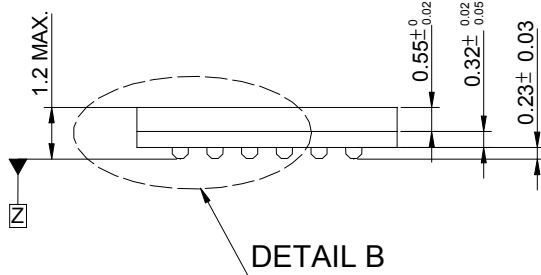
36 pin 6mm×8mm TFBGA PACKAGE OUTLINE DIMENSION



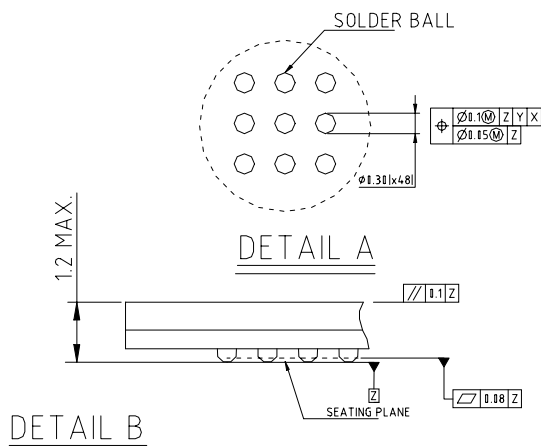
TOP VIEW (DIE VIEW)



BOTTOM VIEW (BALL SIDE)



SIDE VIEW



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UT62L5128**512K X 8 BIT LOW POWER CMOS SRAM****ORDERING INFORMATION****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L5128LC-55L	55	20	32 PIN TSOP- I
UT62L5128LC-55LL	55	3	32 PIN TSOP- I
UT62L5128LC-70L	70	20	32 PIN TSOP- I
UT62L5128LC-70LL	70	3	32 PIN TSOP- I
UT62L5128LS-55L	55	20	32 PIN STSOP
UT62L5128LS-55LL	55	3	32 PIN STSOP
UT62L5128LS-70L	70	20	32 PIN STSOP
UT62L5128LS-70LL	70	3	32 PIN STSOP
UT62L5128BS-55L	55	20	36 PIN TFBGA
UT62L5128BS-55LL	55	3	36 PIN TFBGA
UT62L5128BS-70L	70	20	36 PIN TFBGA
UT62L5128BS-70LL	70	3	36 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L5128LC-55LE	55	20	32 PIN TSOP- I
UT62L5128LC-55LLE	55	3	32 PIN TSOP- I
UT62L5128LC-70LE	70	20	32 PIN TSOP- I
UT62L5128LC-70LLE	70	3	32 PIN TSOP- I
UT62L5128LS-55LE	55	20	32 PIN STSOP
UT62L5128LS-55LLE	55	3	32 PIN STSOP
UT62L5128LS-70LE	70	20	32 PIN STSOP
UT62L5128LS-70LLE	70	3	32 PIN STSOP
UT62L5128BS-55LE	55	20	36 PIN TFBGA
UT62L5128BS-55LLE	55	3	36 PIN TFBGA
UT62L5128BS-70LE	70	20	36 PIN TFBGA
UT62L5128BS-70LLE	70	3	36 PIN TFBGA



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REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev. 1.0	1. The symbols CE# and OE# and WE# are revised as $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2. Separate Industrial and Consumer SPEC. 3. Add access time 55ns range.	Jun 21,2001
Rev. 1.1	Add STSOP package	Aug 3,2001



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