XPT2046 Data Sheet

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General Description

The XPT2046 is a 4-wire resistive touch screen controller that incorporates a 12-bit 125 kHz sampling SAR type A/D converter.
The XPT2046 operates down to 2.2V supply voltage and supports digital I/O interface voltage from 1.5V to VCC in order to connect low voltage uP.
The XPT2046 can detect the pressed screen location by performing two A/D conversions. In addition to location, the XPT2046 also measures touch screen pressure.On-chip VREF can be utilized for analog auxiliary input, temperature measurement and battery monitoring withthe ability to measure voltage from 0V to 5V.
The XPT2046 also has an on-chip temperature sensor
The XPT2046 is available in 16pin QFN thin package(0.75mm in height) and has the operating temperature range of -40°C to +85°C

Features

12 bit SAR type A/D converter with S/H circuit
Low voltage operation (VCC = 2.2V ~ 3.6V)
Low voltage digital I/F (1.5V ~ VCC)
4-wire I/F
Sampling frequency: 125 kHz (max)
On-Chip voltage reference (2.5V)
Pen pressure measurement
On-chip thermo sensor
Direct battery masurement
Low power consumption (260μA)
Package 16pin QFN

Applications

Personal digital assistants
Portable instruments
Point -of-sale terminals
Pagers
Touch screen monitors
Cellular phones

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Block Diagram

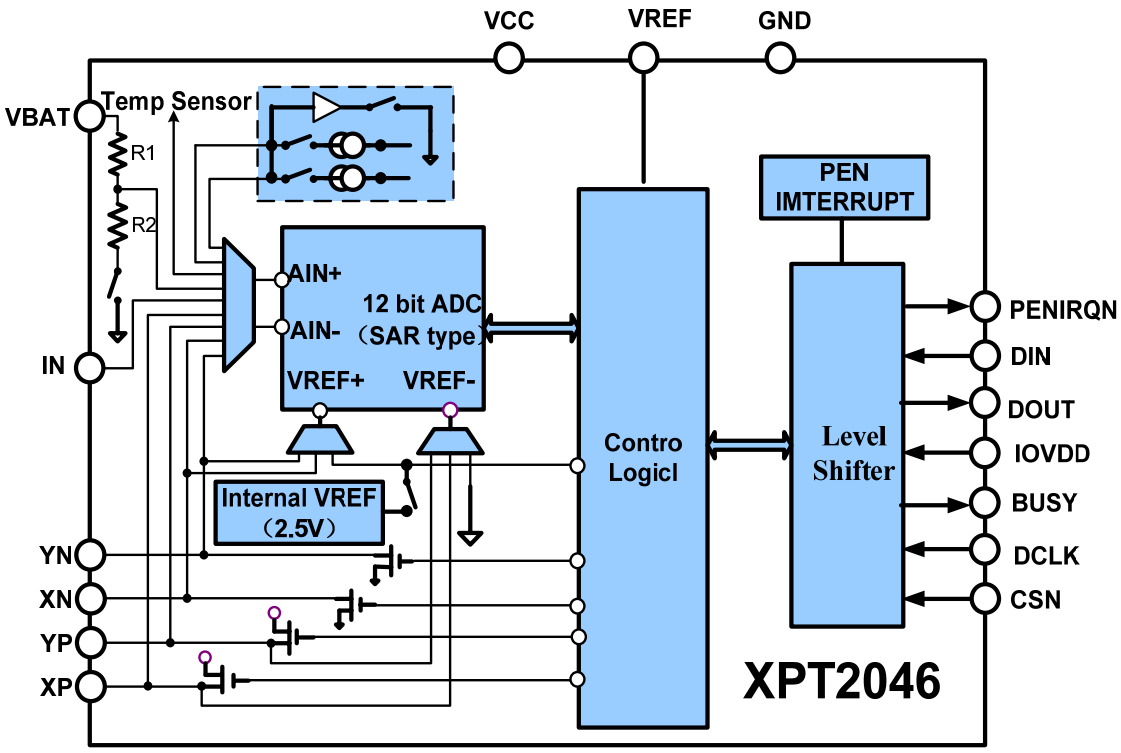


Figure 1. Block Diagram

Absolute Maximum Ratings

+VCC and IOVDD to GND	−0.3V to +6V
Analog Inputs to GND	−0.3V to +VCC + 0.3V
Digital Inputs to GND	−0.3V to IOVDD + 0.3V
Power Dissipation	. 250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	. −40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Table 1. Absolute Maximum Ratings

WARNING: Stresses above these ratings may cause permanent damage.Exposure to absolute maximum conditions for xtended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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Electrical Characteristics: VS = +2.7V to +5.5V

At TA = −40°C to +85°C, +VCC = +2.7V, VREF = 2.5V internal voltage, fSAMPLE = 125kHz, fCLK = 16 • fSAMPLE = 2MHz, 12-bit mode, digital inputs = GND or IOVDD, and +VCC must be • IOVDD.

PARAMETER	CONDITION	XPT2046			UNITS
		MIN	TYP	MAX	
ANALOG INPUT					
Full-Scale Input Span	Positive Input−Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	-0.2		+VCC+0.2	V
	Negative Input	-0.2		+0.2	V
Capacitance			25		pF
Leakage Current			0.1		μA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB[1]
Offset Error				±6	LSB
Gain Error	External VREF			±4	LSB
Noise	Including Internal VREF		70		μV_{rms}
Power-Supply Rejection			70		dB
SAMPLING DYNAMICS					
Conversion Time				12	CLK
Acquisition Time		3			Cycles
Throughput Rate				125	CLK
Multiplexer Settling Time			500		Cycles
Aperture Delay			30		KHz
Aperture Jitter			100		ns
Channel-to-Channel Isolation	V_{IN}=2.5V_{pp}, fs=50KHz		100		ns
					ps
					dB
SWITCH DRIVERS					
On-Resistance					
YP、XP			5		Ω
YN、XN			6		Ω
Drive Current(2)	Duration 100ms			50	mA
REFERENCE OUTPUT					
Internal Reference Voltage		2.45	2.50	2.55	V
Internal Reference Drift			15		ppm/℃
Quiescent Current			500		μA

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REFERENCE INPUT					
Range		1.0		VCC	V
Input Impedance			1		GΩ
	SER/$\overline{DFR}$=0，PD1=0				
	Internal Reference Off		250		Ω
	Internal Reference On				
BATTERY MONITOR					
Input Voltage Range		0.5		6.0	V
Input Impedance					
Sampling Battery			10		KΩ
Battery Monitor Off			1		GΩ
Accuracy	V_{BAT}=0.5V~5.5V, ExternalV_{REF}=2.5V	-2		+2	%
	V_{BAT}=0.5V~5.5V, Internal Reference	-3		+3	%
TEMPERATURE ASUREMENT					
Temperature Range		-40		+85	℃
Resolution	Differential Method(3)		1.6		℃
	TEMP0(4)		0.3		℃
Accuracy	Differential Method(3)		±2		℃
	TEMP0(4)		±3		℃
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Capacitance	All Digital Control Input Pins		5	15	pF
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	IOVDD*0.7		IOVDD+0.3	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	-0.3		0.3*IOVDD	V
V_{OH}	I_{OH}=-250μA	IOVDD*0.8			V
V_{OL}	I_{OL}=250μA			0.4	V
Data Format			Straight Binary		
POWER-SUPPLYREQUIREMENTS					
+VCC (5)	Specified Performance	2.7		3.6	V
	Operating Range	2.2		5.25	V
IOVDD (6)		1.5		VCC	V
Quiescent Current (7)	Internal Reference Off		280	650	μA
	Internal Reference On		780		μA
	fSAMPLE = 12.5kHz		220		μA
	Power-Down Mode with (CS=DCLK=DIN=IOVDD)			3	μA
Power Dissipation	VCC=+2.7V			1.8	mW

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TEMPERATURE RANGE Specified Performance		-40		+85	℃

Table 2. Electrical Characteristics

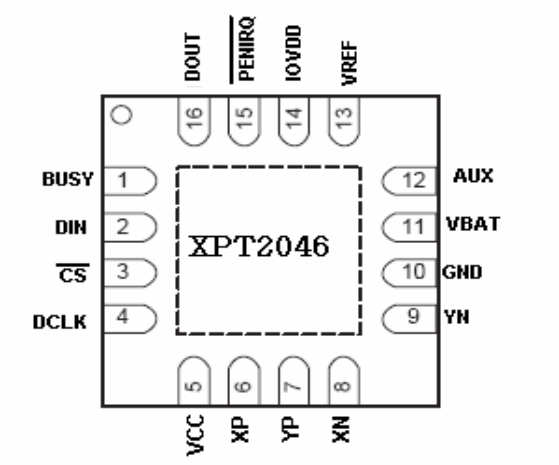
(1) LSB means *Least Significant Bit*. With VREF = +2.5V, one LSB is 610 V.
(2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP0 and TEMP1 measurement, no calibration necessary.
(4) Temperature drift is −2.1mV/ C.
(5) XPT2046 operates down to 2.2V.
(6) IOVDD must be − (+VCC).
(7) Combined supply current from +VCC and IOVDD. Typical values obtained from conversions on AUX input with PD0 = 0.

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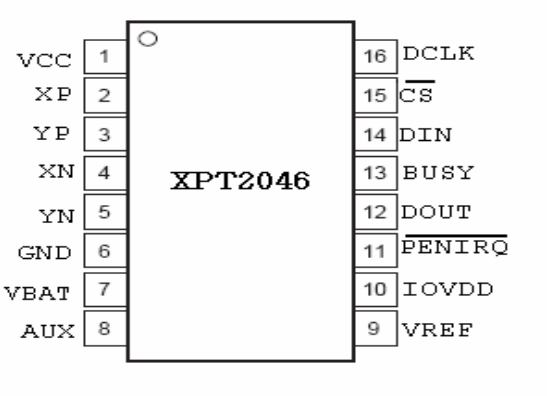
Pin Configuration

Pin Layout

QFN-16



TSSOP－16



VFBGA-16

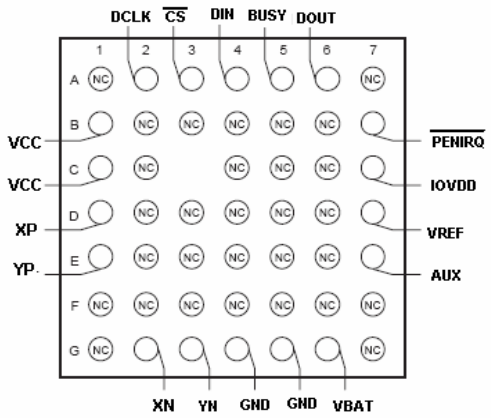


Figure 2. Pin Layout

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Pin Description

QFN PIN #	TSSOP PIN#	VFBGA PIN #	NAME	DESCRIPTION
1	13	A5	BUSY	Busy Output. This output is high impedance when CS is high.
2	14	A4	DIN	Serial Data Input. If CS is low, data is latched on the rising edge of DCLK.
3	15	A3	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output
4	16	A2	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes
5	1	B1和C1	VCC	Power Supply
6	2	D1	XP	XP Position Input
7	3	E1	YP	YP Position Input
8	4	G2	XN	XN Position Input
9	5	G3	YN	YN Position Input
10	6	G4和G5	GND	Ground
11	7	G6	VBAT	Battery Monitor Input
12	8	E7	AUX	Auxiliary Input to ADC
13	9	D7	VREF	Voltage Reference Input/Output
14	10	C7	IOVDD	Digital I/O Power Supply
15	11	B7	$\overline{PENIRQ}$	Pen Interrupt
16	12	A6	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high

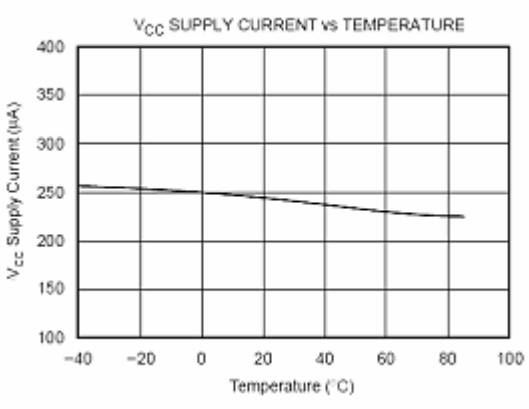
Table 3. Pin Description

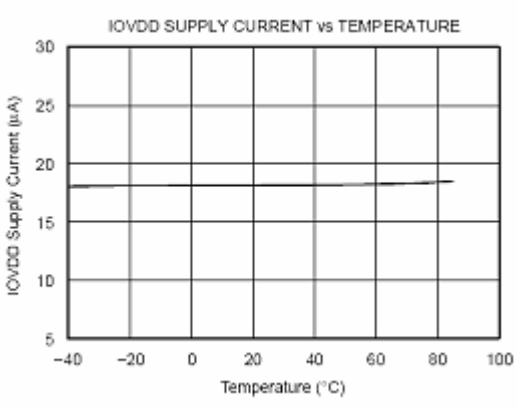
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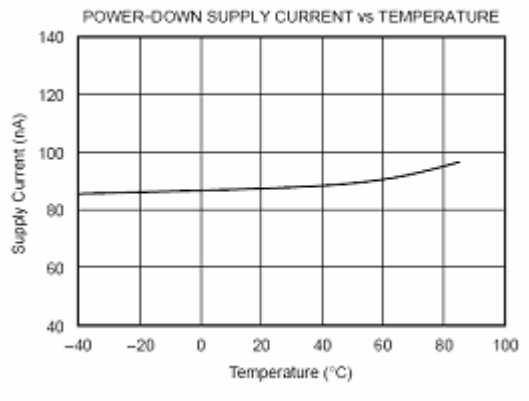
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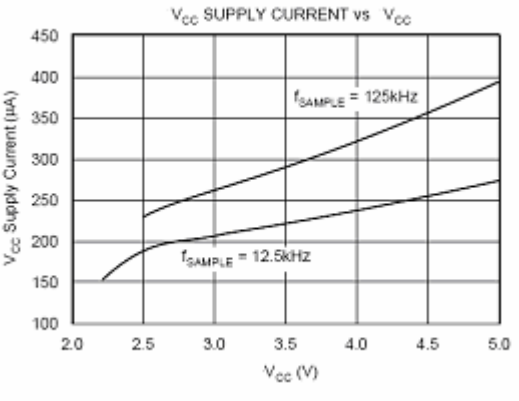
Typical Characteristics

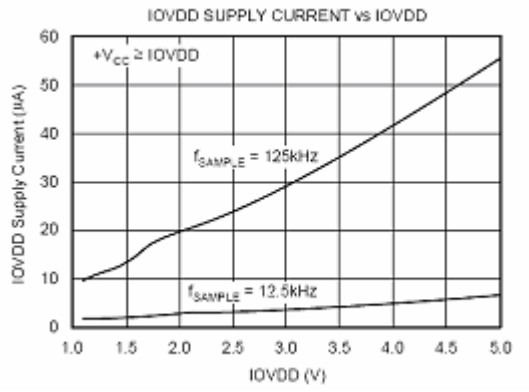
At TA = +25 C, +VCC = +2.7V, IOVDD = +1.8V, VREF = External +2.5V, 12-bit mode, PD0 = 0, fSAMPLE = 125kHz, and fCLK = 16 . fSAMPLE = 2MHz,

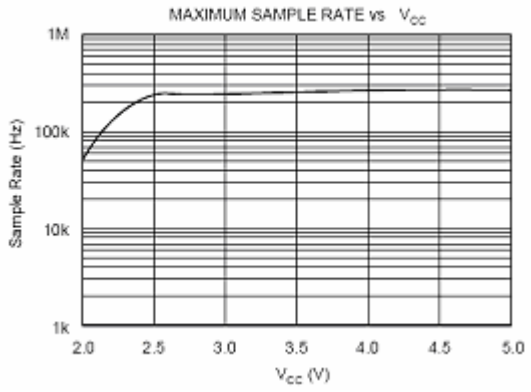






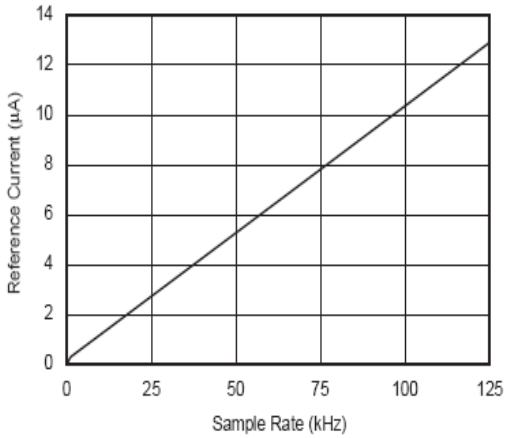




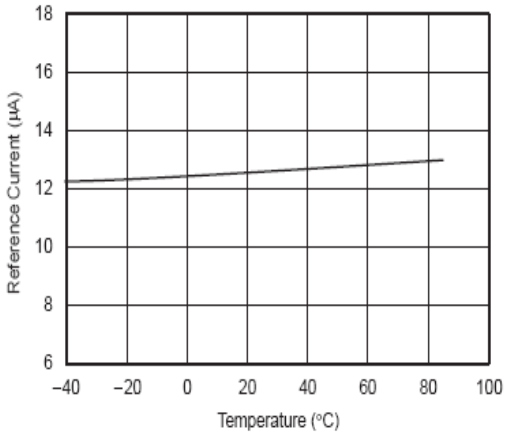


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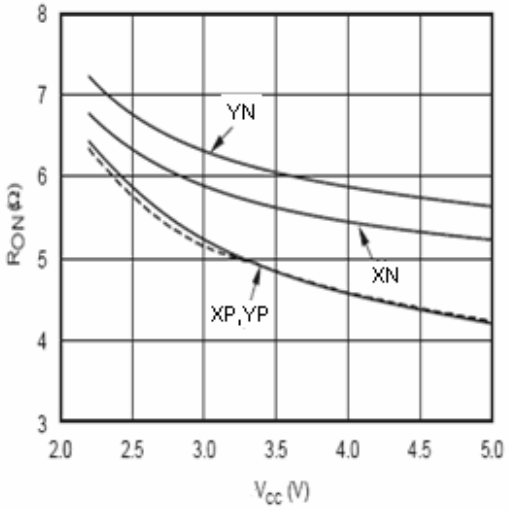
REFERENCE CURRENT vs SAMPLE RATE



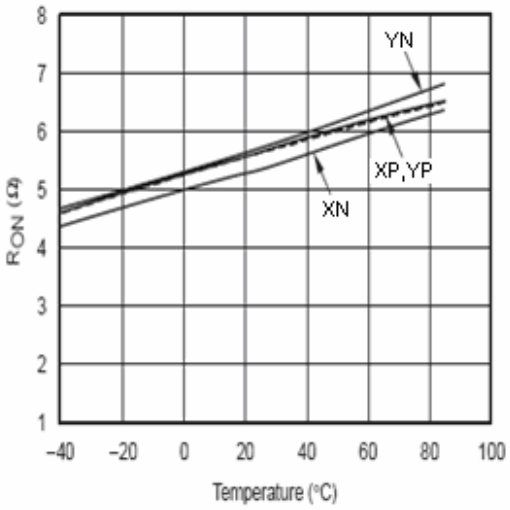
REFERENCE CURRENT vs TEMPERATURE



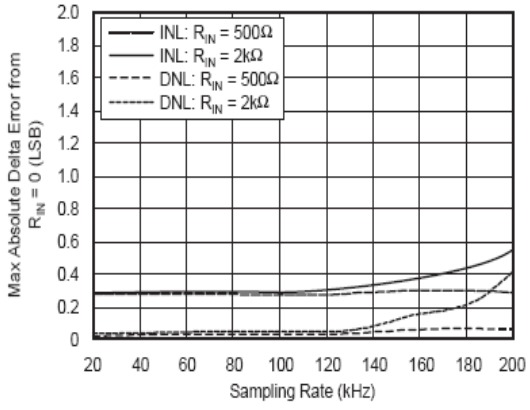
SWITCH ON-RESISTANCE VS VCC
(XP,YP:VCC to Pin;XN,YN:Pin to GND)



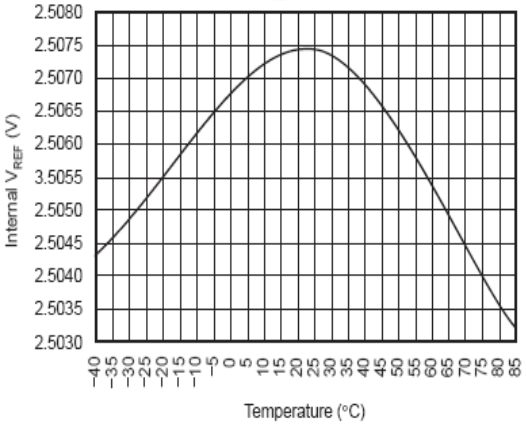
SWITCH ON-RESISTANCE VS TEMPERATURE
(XP,YP:VCC to Pin;XN,YN:Pin to GND)



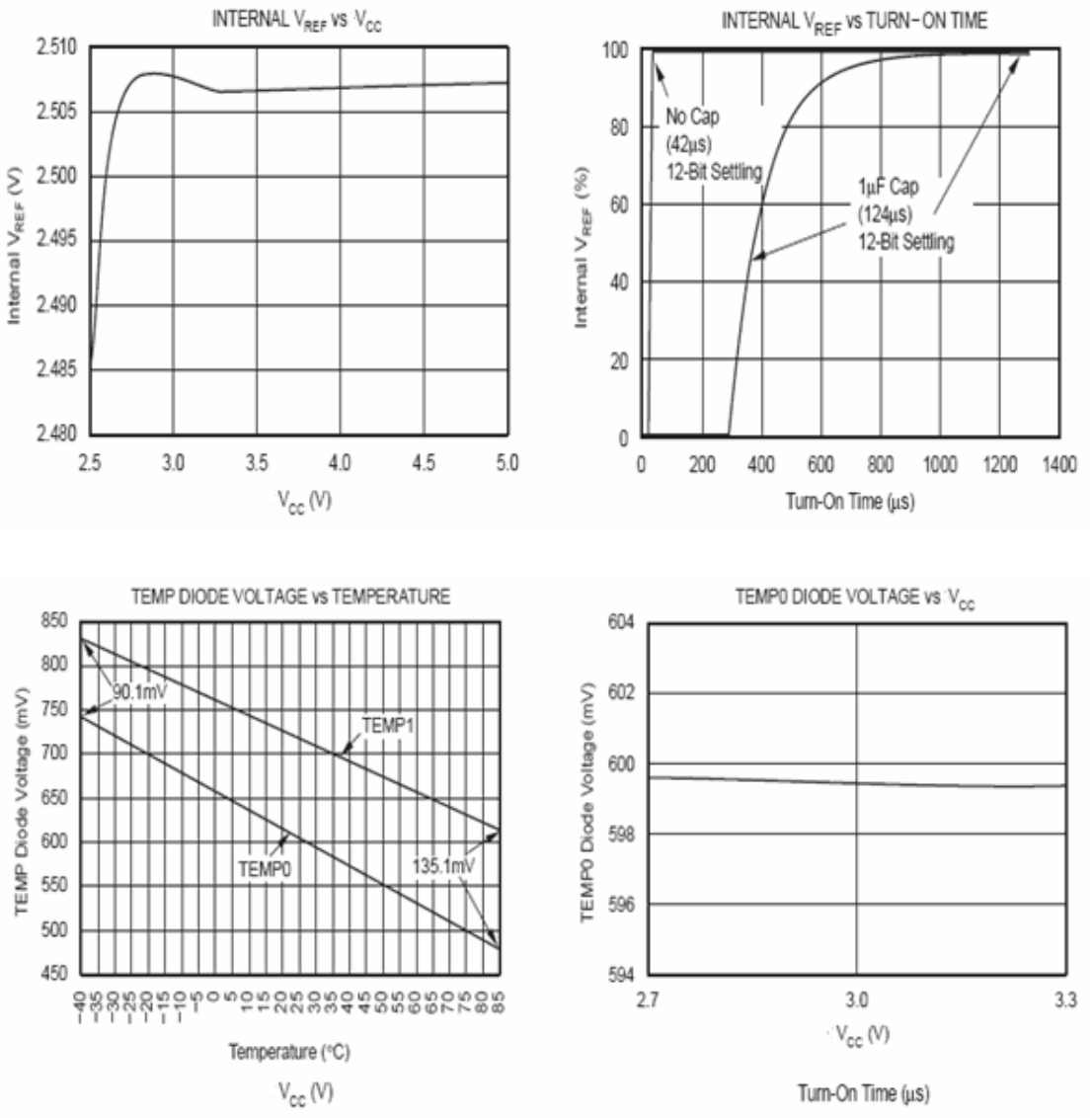
MAXIMUM SAMPLING RATE vs R_{IN}



INTERNAL V_{REF} vs TEMPERATURE



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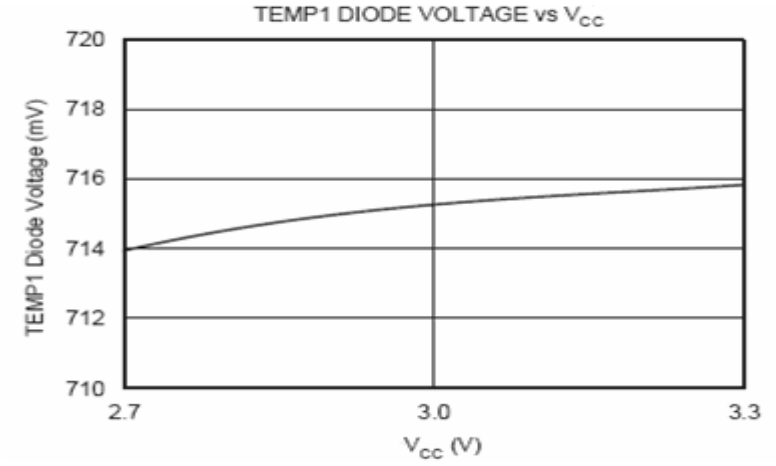


Figure 3. Typical Characteristics

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Theory Of Opration

The XPT2046 is a classic successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on capacitive redistribution, which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6μm CMOS process. The basic operation of the XPT2046 is shown in Figure 4 The device features an internal 2.5V reference and uses an external clock. Operation is maintained from a single supply of 2.7V to 5.25V. The internal reference can be overdriven with an external, low-impedance source between 1V and +VCC. The value of the reference voltage directly sets the input range of the converter. The analog input (X-, Y-, and Z-Position coordinates, auxiliary input, battery voltage, and chip temperature) to the converter is provided via a multiplexer. A unique configuration of low on-resistance touch panel driver switches allows an unselected ADC input channel to provide power and the accompanying pin to provide ground for an external device, such as a touch screen. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the error from each touch panel driver switch's on-resistance (if this is a source of error for theparticular measurement).

Basic Operation of the XPT2046

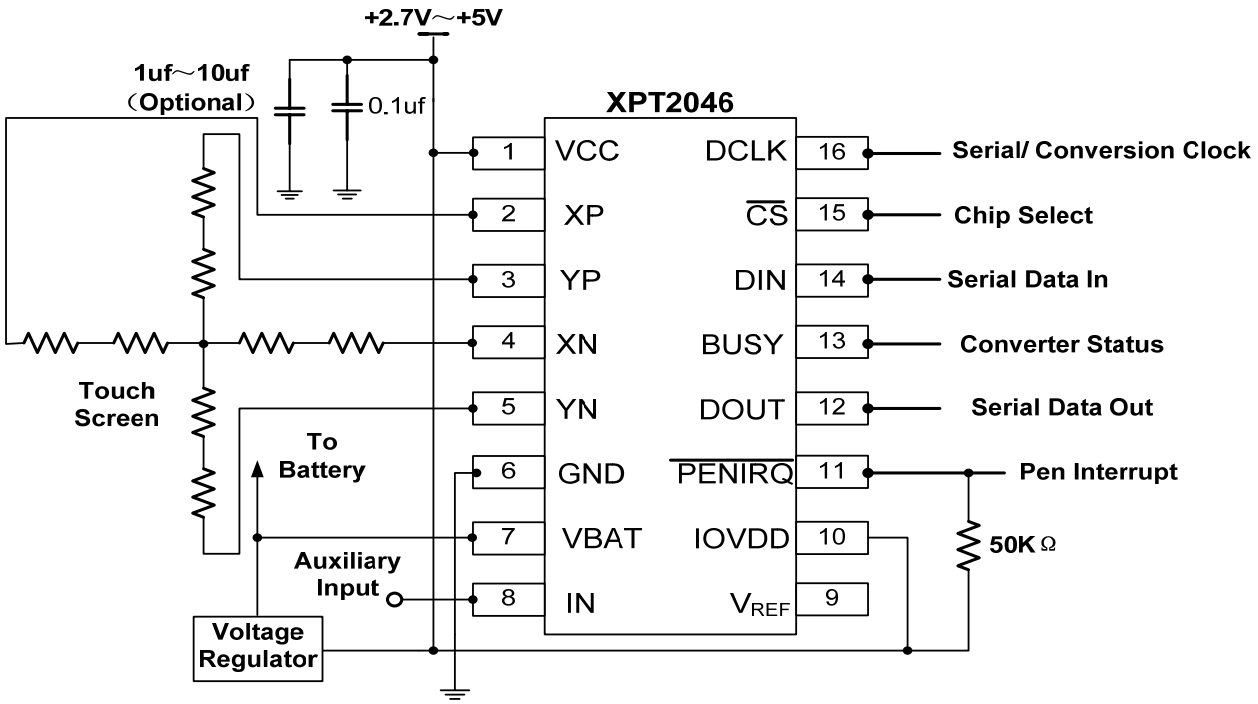


Figure 4. Basic Operation

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Analog Input

Figure 5 hows a block diagram of the input multiplexer on the XPT2046, the differential input of the ADC, and he differential reference of the converter. Table 4 and Table 5 show the relationship between the A2, A1, A0, and SER/DFR control bits and the configuration of the XPT2046.The control bits are provided serially via the DIN pin—see the*Digital Interface* section of this data sheet for more details.

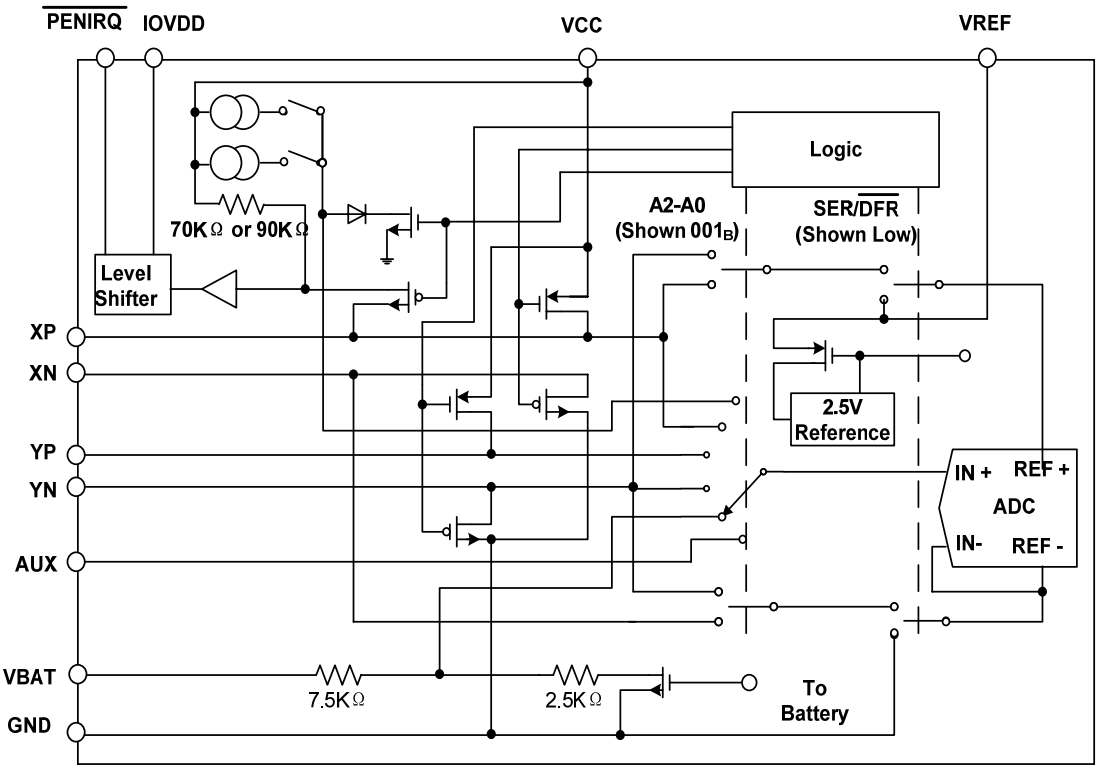


Figure 5. Simplified Diagram of Analog Input

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A2	A1	A0	VBAT	AUXIN	TEMP	YN	XP	YP	Y-POSITIO	X-POSITION	Z1-POSITION	Z2-POSITION	X-DRIVERS	Y-DRIVERS
0	0	0			+IN (TEMP0)								off	off
0	0	1					+IN		M				Off	On
0	1	0	+IN										Off	Off
0	1	1					+IN				M		XN, On	YP, On
1	0	0				+IN						M	XN, On	YP, On
1	0	1						+IN		M			On	Off
1	1	0		+IN									Off	Off
1	1	1			+IN								Off	Off

Table 4.Input Configuration (DIN), Differential Reference Mode (SER/DFR low)

A2	A1	A0	+REF	-REF	YN	XP	YP	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	DRIVERS
0	0	1	YP	YN		+IN		M				YP, YN
0	1	1	YP	XN		+IN				M		YP,
1	0	0	YP	XN	+IN						M	YP,
1	0	1	XP	XN			+IN		M			XP,

Table 5.Input Configuration (DIN), Differential Reference Mode (SER/DFR low)

Internal Reference

The XPT2046 has an internal 2.5V voltage reference that can be turned on or off with the control bit, PD1 (see Table 8 and Figure 6. Typically, the internal reference voltage is onlyused in the single-ended mode for battery monitoring, temperature measurement, and for using the auxiliary input.Optimal touch screen performance is achieved when using the differential mode. The internal reference voltage of the XPT2046 must be commanded to be off to maintain compatibility with the ADS7843. Therefore, after power-up,a write of PD1 = 0 is required to insure the reference is off (see the Typical Characteristics for power-up time of the reference from power-down).

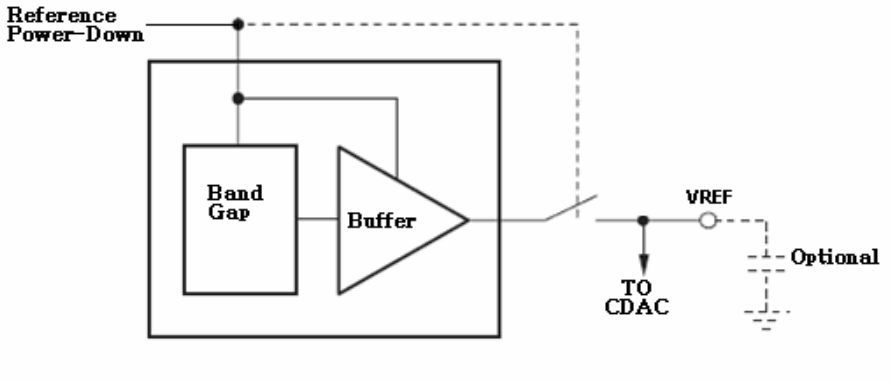


Figure 6. Simplified Diagram of the Internal Reference

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Reference Input

The voltage difference between +REF and –REF (see Figure 5 sets the analog input range. The XPT2046 perates with a reference in the range of 1V to +VCC. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced.

This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096 in 12-bit mode. Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. With a ower reference voltage, more care mustbe taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, alow-noise reference (if an external reference is used), and a low-noise input signal.The voltage into the VREF input directly drives the capacitor digital-to-analog converter (CDAC) portion of the XPT2046. Therefore, the input current is very low (typically< 13 A).

Simplified Diagram of Single-Ended Reference

There is also a critical item regarding the reference when making measurements while the switch drivers are ON. For this discussion, it is useful to consider the basic operation of the XPT2046 (see Figure 4. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y-Position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+ (Figure 7 hows a block diagram). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern). However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it is not possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition,the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

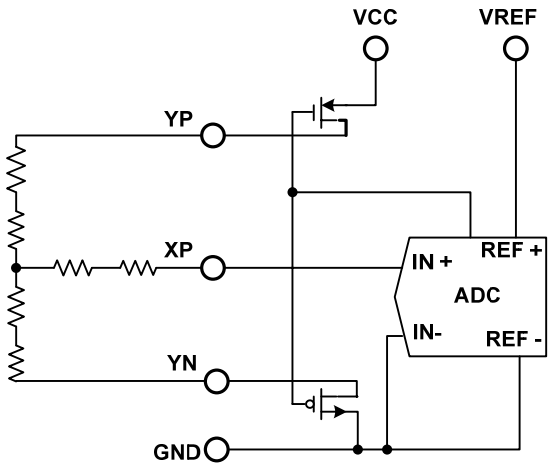


Figure 7. Simplified Diagram of Single-Ended Reference (SER/DFR high, Y switches enabled,X+ is analog input)

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Simplified Diagram of Differential Reference

This situation can be remedied as shown in Figure 8 By setting the SER/DFR bit low, the +REF and –REF inputs are connected directly to Y+ and Y–, respectively, which makes the analog-to-digital conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation (see the *Power Dissipation* section for more details). As a final note about the differential reference mode, it must be used with +VCC as the source of the +REF voltage and cannot be used with VREF. It is possible to use a high-precision reference on VREF and single-ended reference mode for measurements which do not need to be ratiometric. In some cases, it is possible to power the converter directly from a precision reference. Most references can provide enough power for the XPT2046,but might not be able to supply enough current for the external load (such as a resistive touch screen).

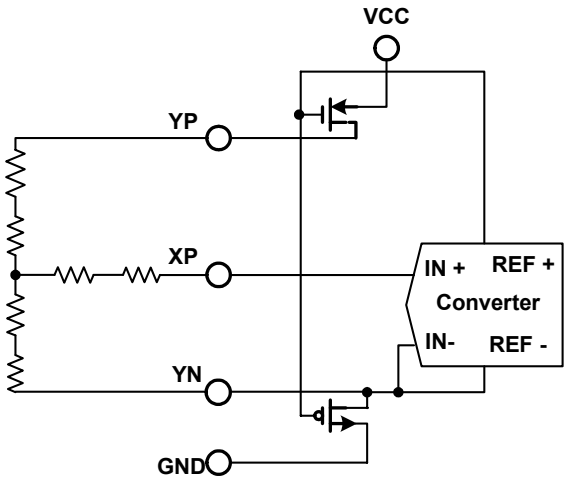


Figure 8. Simplified Diagram of Differential Reference (SER/DFR low, Y switches enabled,X+ is analog input)

Touch Screen Settling

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (e.g., noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but cause a settling time requirement when the panel is touched that typically shows up as a gain error. There are several methods for minimizing or eliminating this issue. The problem is that the input and/or reference has not settled to the final steady-state value prior to the ADC sampling the input(s)and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle. Option 1 is to stop or slow down the XPT2046 DCLK for the required touch screen settling time. This allows the input and reference to have stable values for the Acquire period (3 clock cycles of the XPT2046; see Figure 12). This works for both the single-ended and the differential modes.Option 2 is to operate the XPT2046 in

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the differential mode only for the touch screen measurements and command the XPT2046 to remain on (touch screen drivers ON) and not go into power-down (PD0 = 1). Several conversions are made depending on thes ettling time required and the XPT2046 data rate. Once the required number of conversions have been made, the processor commands the XPT2046 to go into its power-down state on the last measurement. This process isr equired for X-Position,Y-Position, and Z-Position measurements. Option 3 is to operate in the 15 Clock-per-Conversion mode, which overlaps the analog-to-digital conversions and maintains the touch screen drivers on until commanded to stop by the processor (see Figure 16).

Temperature Measurement

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the XPT2046 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (VBE) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25 C value of the VBE voltage and then monitoring the delta of that voltage as the temperature changes. The XPT2046 offers two modes of operation. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. A diode is used (turned on) during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the forward bias voltage by the ADC with an address of A2 = 0, A1 = 0, and A0 = 0 (see Table 1 and Figure 6 for details). This voltage is typically 600mV at +25 C with a 20 A current through the diode. The absolute value of this diode voltage can vary a few millivolts.However, the TC of this voltage is very consistent at –2.1mV/ C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3 C/LSB (in 12-bit mode).

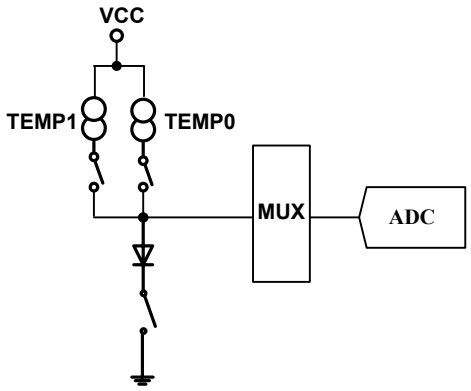


Figure 9. Functional Block Diagram of Temperature Measurement

The second mode does not require a test temperature calibration, but uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2 C accuracy. This mode requires a second conversion with an address of A2 = 1, A1 = 1, and A0 = 1, with a 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current is represented by Equation (1):

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$$\triangle V = \frac{kT}{q} \bullet \ln(N) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (1)$$

where:

N is the current ratio = 91.

k = Boltzmann's constant (1.38054 • 10−23 electron volts/ degrees Kelvin).

q = the electron charge (1.602189 • 10–19 C).

T = the temperature in degrees Kelvin.

This method can provide improved absolute temperature measurement over the first mode at the cost of less resolution (1.6°C/LSB). The equation for solving for °K is:

$$^{\circ}K = q \bullet \frac{\Delta V}{(k \bullet \ln(N))} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$$

where:

ΔV = V (I91) – V (I1) (in mV)

°K = 2.573 °K/mV • ΔV

°C = 2.573 • ΔV(mV) – 273°K

NOTE: The bias current for each diode temperature measurement is only on for 3 clock cycles (during the acquisition mode) and, therefore, does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

Battery Measurement

An added feature of the XPT2046 is the ability to monitor the battery voltage on the other side of the voltage regulator(DC/DC converter), as shown in Figure 10. The battery voltage can vary from 0V to 6V, while maintaining the voltage to the XPT2046 at 2.7V, 3.3V, etc. The input voltage (VBAT)is divided down by 4 so that a 5.5V battery voltage is represented as 1.375V to the ADC. This simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only on during the sampling period when A2 = 0, A1 = 1, and A0 = 0 (see Table 1 for the relationship between the control bits and configuration of the XPT2046).

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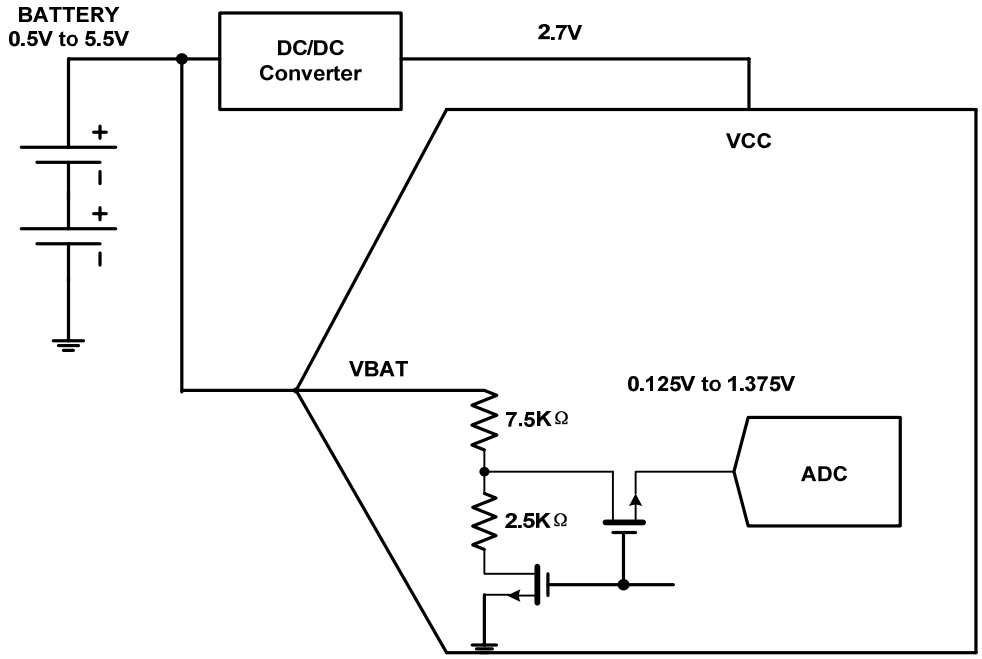


Figure 10. Battery Measurement Functional Block Diagram

Pressure Measurement

Measuring touch pressure can also be done with the XPT2046. To determine pen or finger touch, the pressure of the touch needs to be determined. Generally, it is not necessary to have very high performance for this test; therefore, the 8-bit resolution mode is recommended(however, calculations will be shown here in the 12-bit resolution mode). There are several different ways of performing this measurement. The XPT2046 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross panel measurements (Z1 and Z2) of the touch screen, as shown in Figure 11. Using Equation (3) calculates the touch resistance:

$$R_{触摸} = R_{X\,面板} \cdot \frac{X\text{Position}}{4096}\left(\frac{Z2}{Z1} - 1\right) \quad \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z1. Using Equation (4) also calculates the touch resistance:

$$Rtouch = \frac{R_{X\text{-Plate}} \bullet X\text{-Position}}{4096}\left(\frac{4096}{Z_1} - 1\right) - R_{Y\,-\,Plate}\left(1 - \frac{Y\text{-Position}}{4096}\right) \quad \cdots\cdots (4)$$

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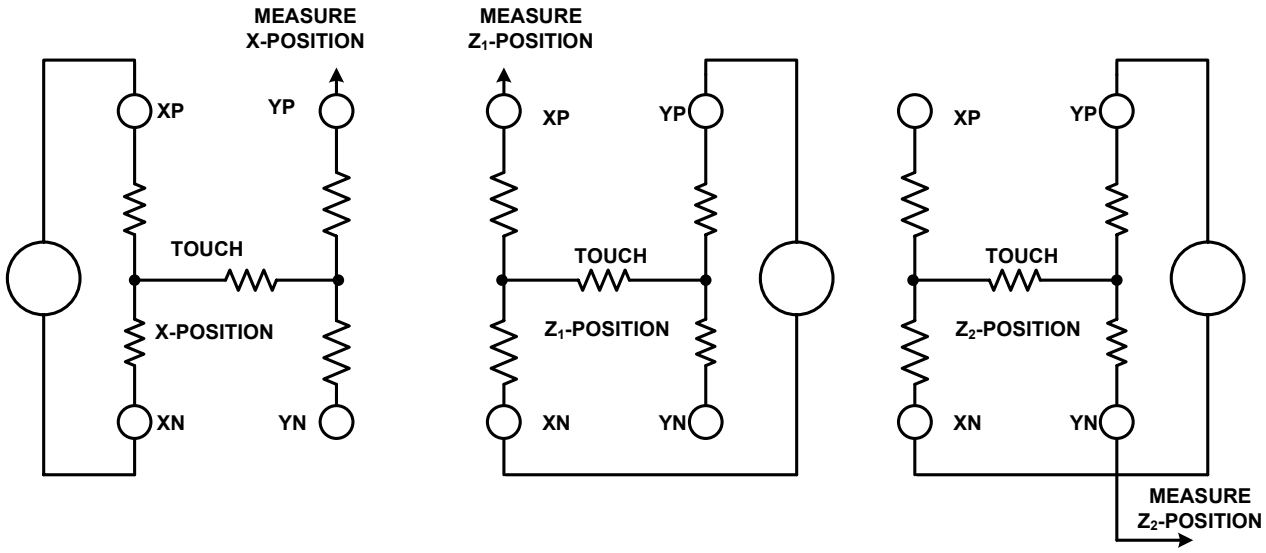


Figure 11. Pressure Measurement Block Diagrams

Digital Interface

See Figure 12 for the typical operation of the XPT2046 digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface.Each communication between the processor and the converter,such as SPI, SSI, or Microwire_ synchronous serial interface, consists of eight clock cycles. One complete conversion can be accomplished with three serial communications for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the touch panel drivers are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the touch panel drivers turn off (in single-ended mode). The next 12 clock cycles accomplish the actual analogto-digital conversion. If the conversion is ratiometric(SER/DFR = 0), the drivers are on during the conversion and a 13th clock cycle is needed for the last bit of the conversionr esult. Three more clock cycles are needed to complete the last byte (DOUT will be low), which are ignored by the converter.

Control Byte

The control byte (on DIN), as shown in Table 3, provides the start conversion, addressing, ADC resolution, configuration,and power-down of the XPT2046. Figure 12, Table 3 and Table 4 give detailed information regarding the order and description of these control bits within the control byte.

Initiate START—The first bit, the S bit, must always be high and initiates the start of the control byte. The XPT2046 ignores inputs on the DIN pin until the start bit is detected.

Addressing—The next three bits (A2, A1, and A0) select the active input channel(s) of the input multiplexer (see Table 1, Table 2, and Figure 5), touch screen drivers, and the reference inputs.

MODE—The mode bit sets the resolution of the ADC. With this bit low, the next conversion has 12 bits ofr esolution,whereas with this bit high, the next conversion has eight bits of resolution.

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SER/DFR—The SER/DFR bit controls the reference mode, either single-ended (high) or differential (low). The differential mode is also referred to as the ratiometric conversion mode and is preferred for X-Position,Y-Position, and Pressure-Touch measurements for optimum performance. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a reference voltage is not needed as the reference voltage to the ADC is the voltage across the touch screen. In the single-ended mode, the converter reference voltage is always the difference between the VREF and GND pins (see Table 1 and Table 2, and Figure 5 through Figure 8, for further information).

BIT7(MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0(LSB)
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0

Table 6. Order of the Control Bits in the Control Byte

BIT	NAME	DESCRIPTION
7	S	Start bit. Control byte starts with first high bit on DIN.A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode (see Figure 16).
6-4	A2-A0	Channel Select bits. Along with the SER/DFR bit,these bits control the setting of the multiplexer input,touch driver switches, and reference inputs (seeTable 1 and Figure 16).
3	MODE	12-Bit/8-Bit Conversion Select bit. This bit controls the number of bits for the next conversion: 12-bits(low) or 8-bits (high).
2	SER/$\overline{\text{DFR}}$	Single-Ended/Differential Reference Select bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, touch driver switches, and reference inputs (see Table 1 and Table 2).
1-0	PD1-PD0	Power-Down Mode Select bits. Refer to Table 5 fordetails.

Table 7. Descriptions of the Control Bits within the Control Byte

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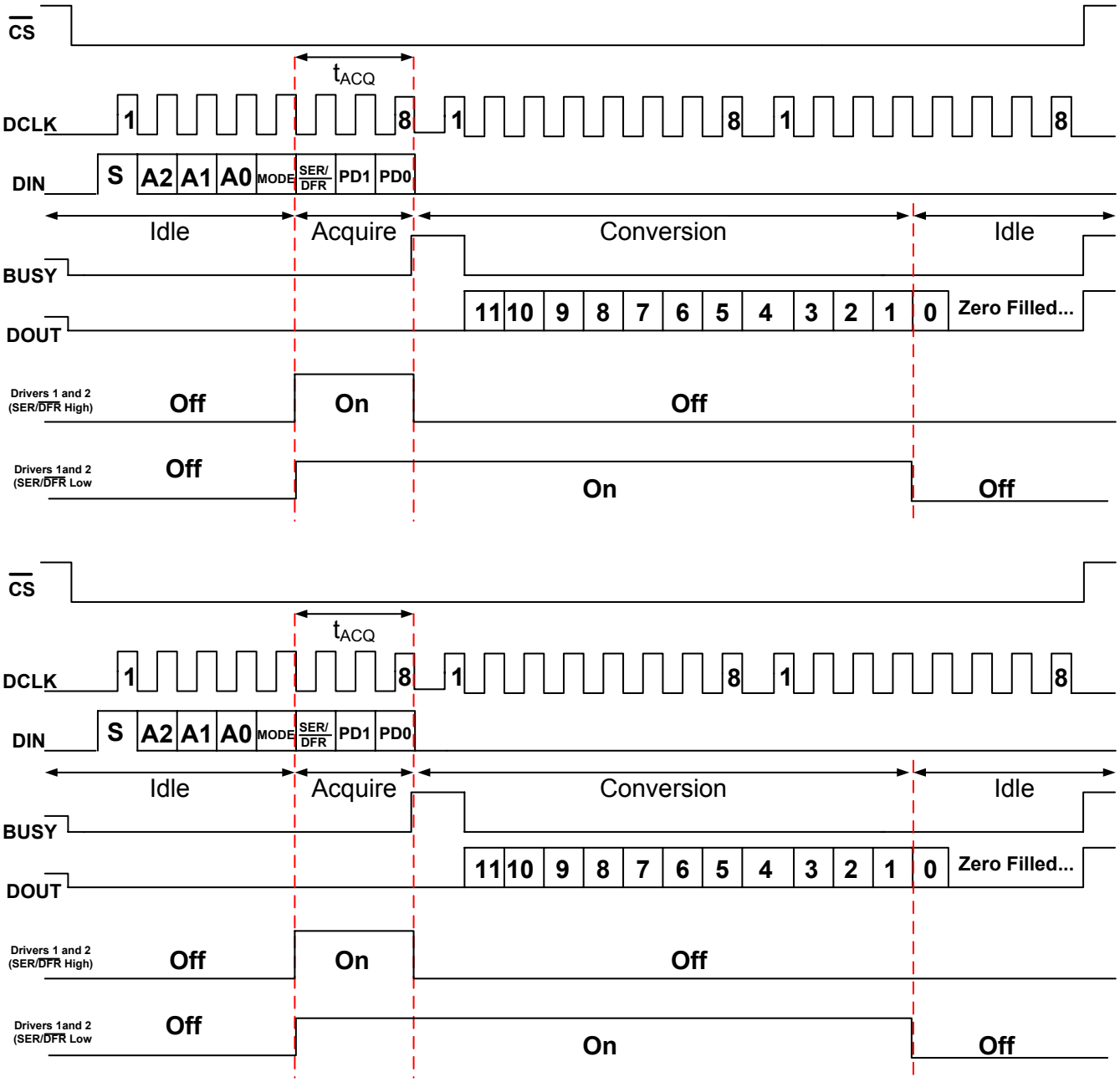


Figure 12. Conversion Timing, 24 Clocks-per-Conversion, 8-Bit Bus Interface.
No DCLK delay required with dedicated serial port

If X-Position, Y-Position, and Pressure-Touch are measured in the single-ended mode, an external reference voltage is needed. The XPT2046 must also be powered from the external reference. Caution should be observed when using the single-ended mode such that the input voltage to the ADC does not exceed the internal reference voltage, especially if the supply voltage is greater than 2.7V.

NOTE: The differential mode can only be used for X-Position, Y-Position, and Pressure-Touch measurements. All other measurements require the single-ended mode.

PD0 and PD1—Table 5 describes the power-down and the internal reference voltage configurations. The internal reference voltage can be turned on or off independently of the ADC. This can allow extra time for the internal reference voltage to settle to the final value prior to making a conversion. Make sure to also allow this extra

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wake-up time if the internal reference is powered down. The ADC requires no wake-up time and can be instantaneously used. Also note that the status of the internal reference power-down is latched into the part (internally) with BUSY going high. In order to turn the reference off, an additional write to the XPT2046 is required after the channel has been converted.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-Down Between Conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to ensure full operation, and the very first conversion is valid. The Y− switch is on when in power-down.
0	1	Disabled	Reference is off and ADC is on.
1	0	Enabled	Reference is on and ADC is off.
1	1	Disabled	Device is always powered. Reference is on and ADC is on.

Table 8. Power-Down and Internal Reference Selection

PENIRQ Output

The pen-interrupt output function is shown in Figure 13.While in power-down mode with PD0 = 0, the Y-driver is on and connects the Y-plane of the touch screen to GND. The PENIRQ output is connected to the X+ input through two transmission gates. When the screen is touched, the X+ input is pulled to ground through the touch screen.In most of the XPT2046 models, the internal pullup resistor value is nominally 50k , but this may vary between 36k and 67k . given process and temperature variations. In order to assure a logic low of 0.35 _ (+VCC) is presented to the PENIRQ circuitry, the total resistance between the X+ and Y− terminals must be less than 21k .

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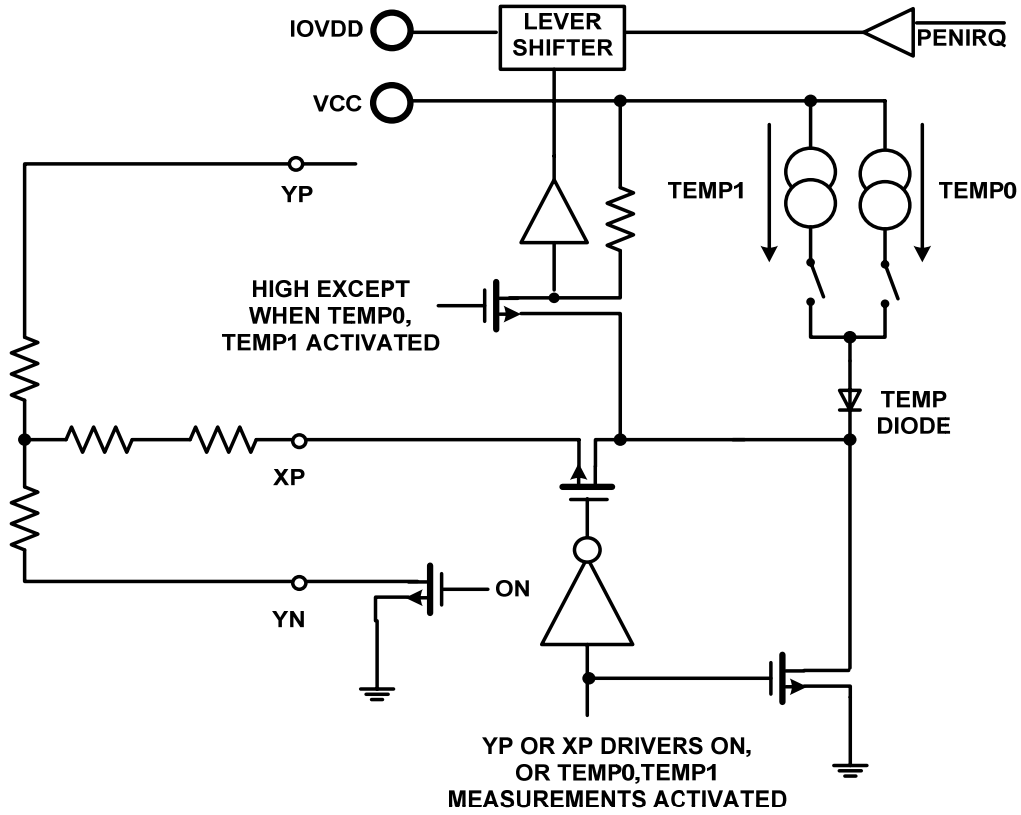


Figure 13. PENIRQ Functional Block Diagram

The −90 version of the XPT2046 uses a nominal 90k pullup resistor, which allows the total resistance between the X+ and Y− terminals to be as high as 30k ˜. Note that the higher pullup resistance will cause a slower response time of the PENIRQ to a screen touch, so user software should take this into account. The PENIRQ output goes low due to the current path through the touch screen to ground, which initiates an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input is disconnected from the PENIRQ internal pull-up resistor. This is done to eliminate any leakage current from the internal pull-up resistor through the touch screen, thus causing no errors.

Furthermore, the PENIRQ output is disabled and low during the measurement cycle for X-, Y-, and Z-Position. The PENIRQ output is disabled and high during the measurement cycle for battery monitor, auxiliary input, and chip temperature. If the last control byte written to the XPT2046 contains PD0 = 1, the pen-interrupt output function is disabled and is not able to detect when the screen is touched. In order to re-enable the pen-interrupt output function under these circumstances, a control byte needs to be written to the XPT2046 with PD0 = 0. If the last control byte written to the XPT2046 contains PD0 = 0, the pen-interrupt output function is enabled at the end of the conversion. The end of the conversion occurs on the falling edge of DCLK after bit 1 of the converted data is clocked out of the XPT2046.

It is recommended that the processor mask the interrupt PENIRQ is associated with whenever the processor sends a control byte to the XPT2046. This prevents false triggering of interrupts when the PENIRQ output is disabled in the cases discussed in this section.

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per-Conversion

16 Clocks-per-Conversion

The control bits for conversion *n* + 1 can be overlapped with conversion *n* to allow for a conversion every 16 clock cycles, as shown in Figure 14. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer from the processor to the converter. This is possible, provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that is captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the XPT2046 is fully powered while other serial communications are taking place during a conversion.

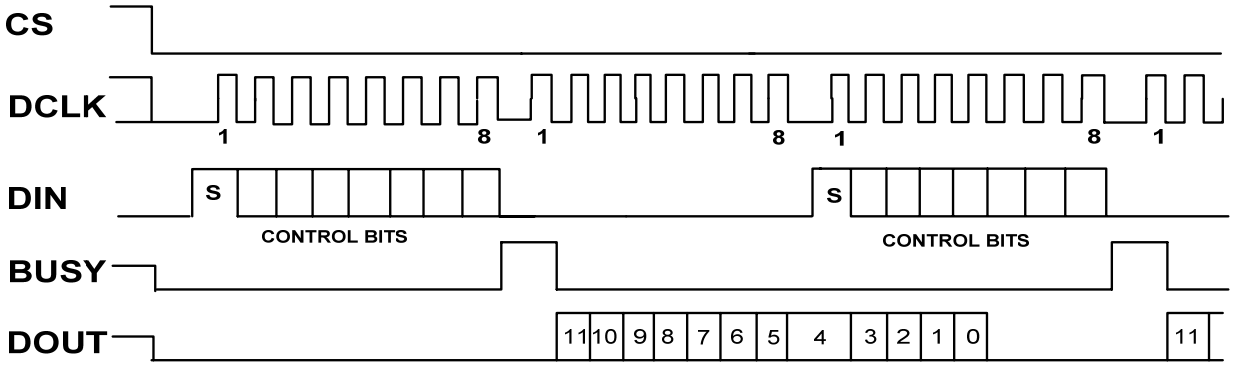


Figure 14. Conversion Timing, 16 Clocks-per-Conversion, 8-Bit Bus Interface.
No DCLK delay required with dedicated serial port

Digital Timing

Figure 12, Figure 15 and Table 6 provide detailed timing for the digital interface of the XPT2046.

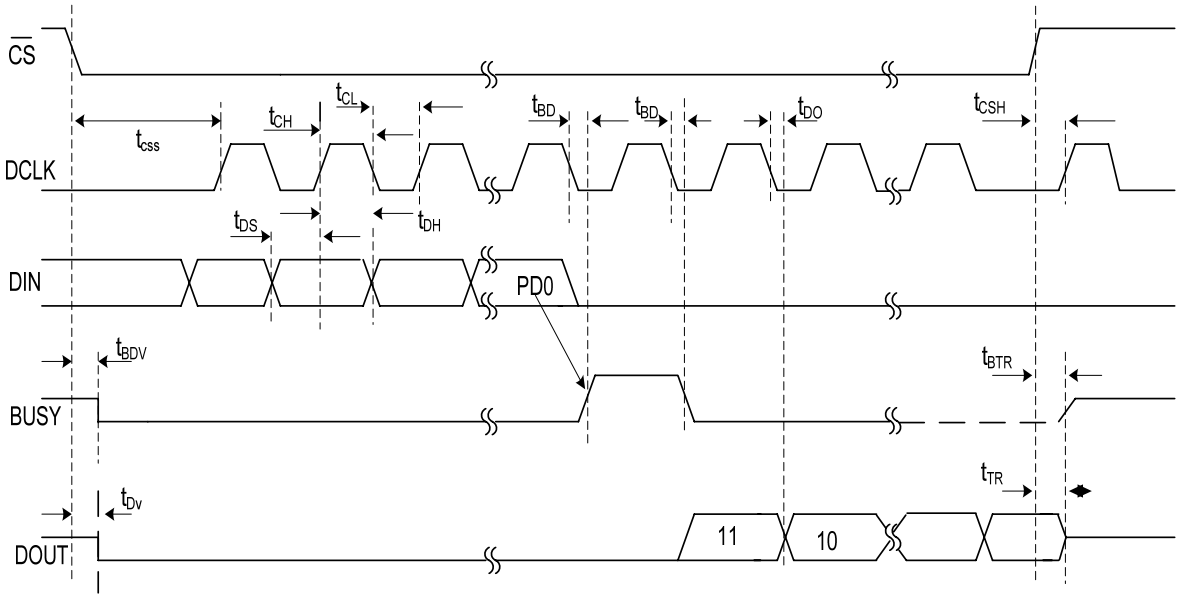


Figure 15. Detailed Timing Diagram

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SYMBOL	DESCRIPTION	+VCC· 2.7V, +VCC· IOVDD·1.5V, C_{LOAD} = 50pF			UNITS
		MIN	TYP	MAX	
tACQ	Acquisition Time	1.5			µs
tDS	DIN Valid Prior to DCLK Rising	100			ns
tDH	DIN Hold After DCLK High	50			ns
tDO	DCLK Falling to DOUT Valid			200	ns
tDV	$\overline{CS}$ Falling to DOUT Enabled			200	ns
tTR	$\overline{CS}$ Rising to DOUT Disabled			200	ns
tCSS	$\overline{CS}$ CS Falling to First DCLK Rising	100			ns
tCSH	$\overline{CS}$ Rising to DCLK Ignored	10			ns
tCH	DCLK High	200			ns
tCL	DCLK Low	200			ns
tBD	DCLK Falling to BUSY Rising/Falling			200	ns
tBDV	$\overline{CS}$ Falling to BUSY Enabled			200	ns
tBTR	$\overline{CS}$ Rising to BUSY Disabled			200	ns

Table 9. Timing Specifications,

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15 Clocks-per-Conversion

Figure 16 provides the fastest way to clock the XPT2046.This method does not work with the serial interface of most microcontrollers and digital signal processors, as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method can be used with field-programmable gate arrays (FPGAs) or applicationspecific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

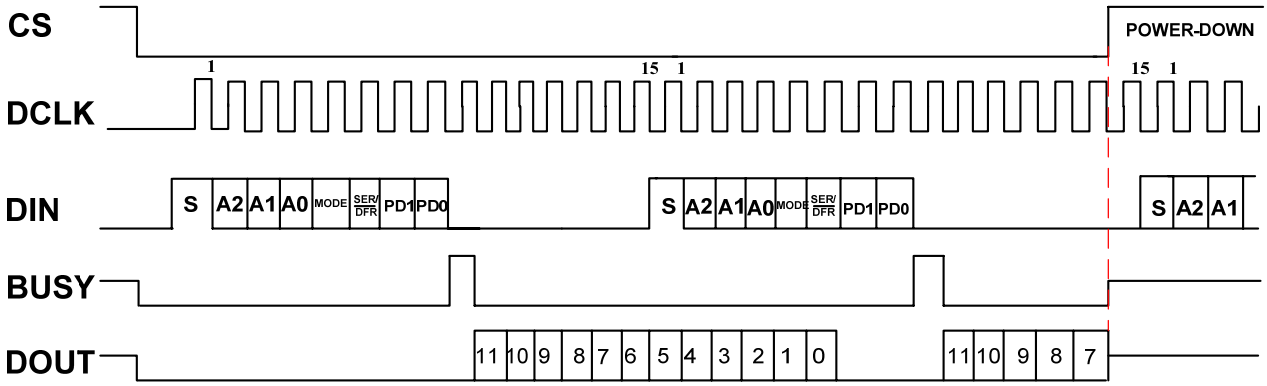


Figure 16. Maximum Conversion Rate, 15 Clocks-per-Conversion

Data Format

The XPT2046 output data is in Straight Binary format, as shown in Figure 17. This figure shows the ideal output code for the given input voltage and does not include the ffects of offset, gain, or noise.

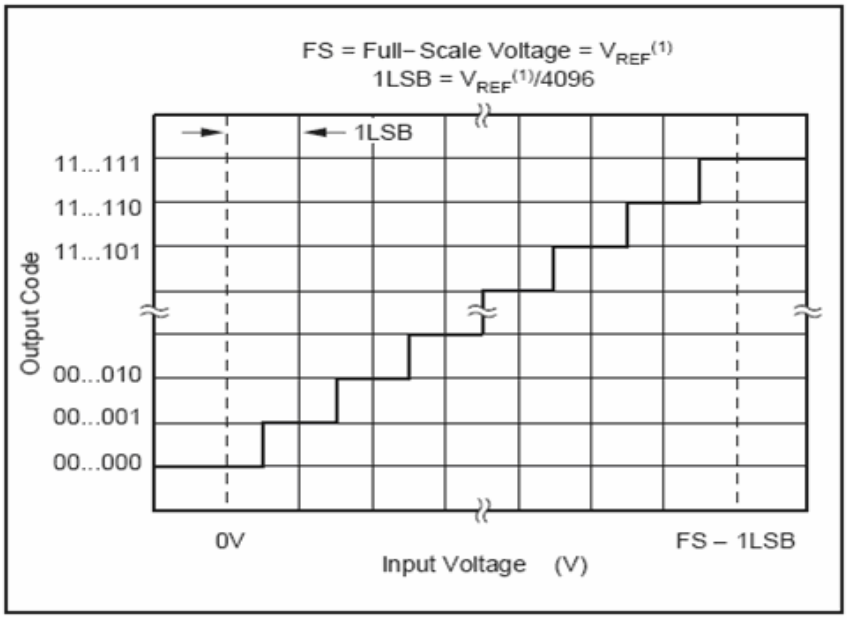


Figure 17. Ideal Input Voltages and Output Codes

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8-Bit Conversion

The XPT2046 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at afaster clock rate. This is because the internal settling time of the XPT2046 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

Power Dissipation

There are two major power modes for the XPT2046: full-power (PD0 = 1) and auto power-down (PD0 = 0). When operating at full speed and 16 clocks-per-conversion (see Figure 14), theXPT2046 spends most of the time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are done less often, the difference between the two modes is dramatic.

Figure 18 shows the difference between reducing the DCLK frequency (scaling DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the latter case, the converter spends an increasing percentage of time in power-down mode (assuming the auto power-down mode is active).

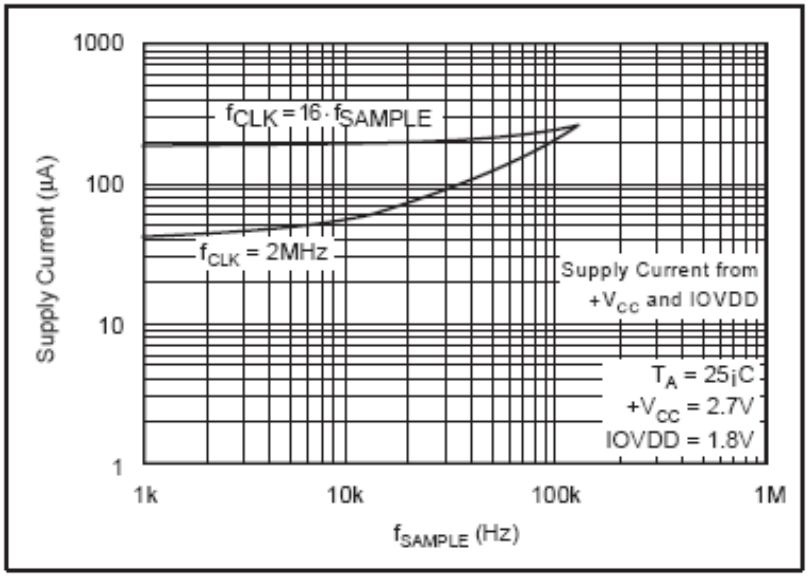


Figure 18. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Maintaining DCLK at the Maximum Possible Frequency

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Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the touch panel drivers are ON only when the analog input voltage is being acquired (see Figure 12 and Table 1). The external device (e.g., a resistive touch screen), therefore, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 12). If the conversion rate is high, this could substantially increase power dissipation.CS also puts the XPT2046 into power-down mode. When CS goes high, the XPT2046 immediately goes into power-down mode and does not complete the current conversion. The internal reference, however, does not turn off with CS going high. To turn the reference off, an additional write is required before CS goes high (PD1 = 0).When the XPT2046 first powers up, the device draws about 20μA of current until a control byte is written to it with PD0 = 0 to put it into power-down mode. This can be avoided if the XPT2046 is powered up with CS = 0 and DCLK = IOVDD.

Demo

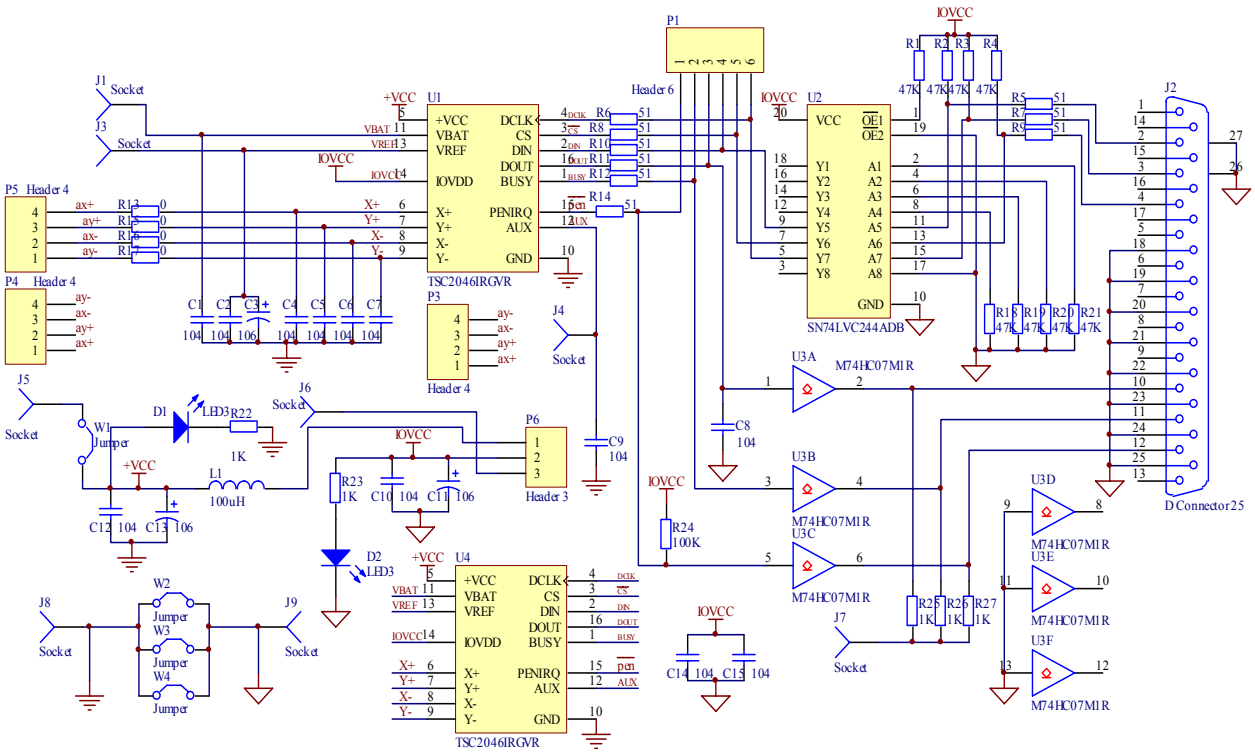


Figure 19. Demo

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