YM3812

FM OPERATOR TYPE-L II (OPL II)

■ OUTLINE:

The OPLII(FM OPERATOR type-LII) is an LSI IC which can be used as a sound generation system for computer apparatus, teletext instruments, etc. The OPLII employs frequency modulation for the melody sounds, and has rhythm sounds very close to those of natural musical instruments, making it possible to synthesize various tones by software control from a CPU. In addition, an LFO is built in to generate effects such as vibrato and tremolo, thus reducing the software load.
The OPLII can be easily interfaced with the DAC YM3014.

■ FEATURES

- FM sound generation system for realistic sound
- Mode selection of simultaneous voicing of 9 sounds or 6 melody sounds and 5 rhythm sounds is possible. Both modes can produce various sounds.
- Built-in vibrato oscillator/amplitude modulation oscillator (AM)
- Composite sine wave speech synthesis also possible
- Input/output TTL compatible
- Si-gate CMOS-LSI
- 5V single power supply

YAMAHA CORPORATION

YM3812 CATALOG
CATALOG No.: LSI-2138123
1992. 4

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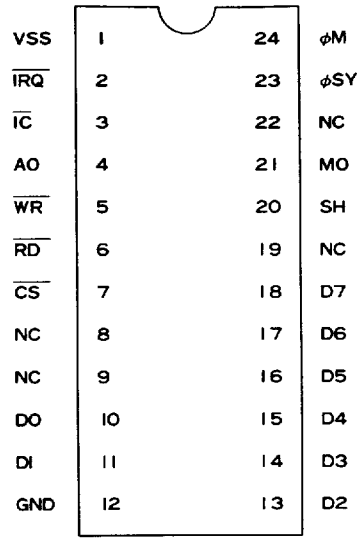
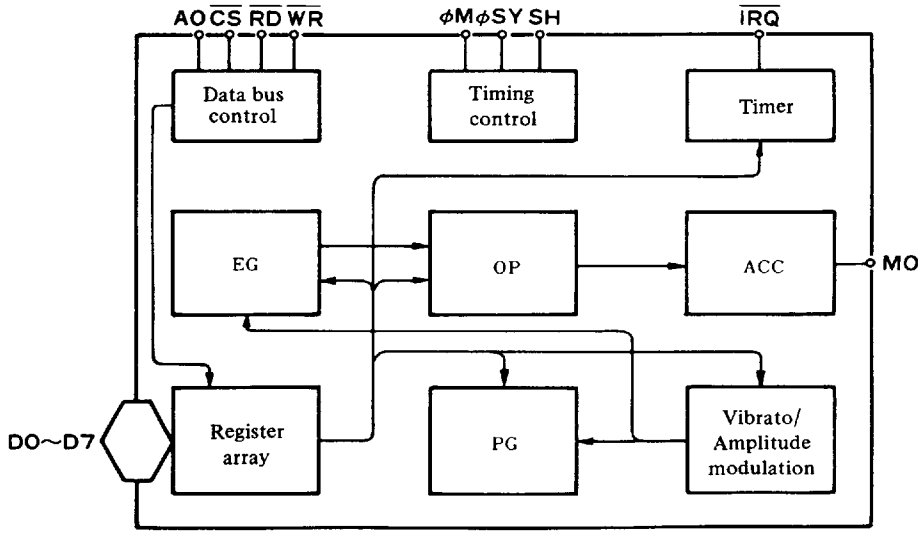
■ PIN LAYOUT



* NC : No Connection

TOP VIEW (24PIN DIP, 24 PIN SOP)

■ BLOCK DIAGRAM



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■ DESCRIPTION OF PIN FUNCTIONS

a) φM
Master clock of OPL; input frequency is 3.58MHz.

b) φSY·SH
Clock (φSY) and Syncronization Signal (SH) to convert digital output of FM sound generator to analog signal.

c) D0 ~ D7
8 bit bidirectional data communication between OPLII and processor.

d) $\overline{CS}$·$\overline{RD}$·$\overline{WR}$·A0
Control data bus comprised of D0 ~ D7.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A0	
0	1	0	0	Write address of register to OPL
0	1	0	1	Write contents of register to OPL
0	0	1	0	Status of OPL is read.
0	0	1	1	Data of data bus not assured
1	×	×	×	Set data bus D0 ~ D7 to high impedance

e) $\overline{IRQ}$
Interrupt signal sent from either of two timers. Interrupts can be masked by program.

f) $\overline{IC}$
Set the contents of registers to "0" and the system will be reset when driven to low level.

g) MO
Digital output of FM sound generator. The external D/A convertor unit is necessary.

h) Vcc
+5V power supply pin

i) GND
Ground pin

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GENERAL FUNCTIONS

OPLII has two voice modes: simultaneous voicing of 9 sounds, and 6 melody sounds and 5 rhythm sounds. Furthermore, these melody sounds can be produced with different voices at one time. Operation by software control makes the OPLII suitable as a sound generation system for computer-based apparatus such as game machines, teletext, etc.

The frequency modulation system in the OPLII synthesizes tones with 2 operators in 9 channels. The resultant algorithms are expressed by the following formula.

$$F_1 = I_1 \sin w_1 t + I_2 \sin w_2 t \quad -(1)$$

$$F_2 = I_2 (w_1 t + I_2 \sin w_2 t) \quad -(2)$$

where formula (1) shows the production of a tone by sine waves addition,and formula (2) shows a sine wave modulating another sine wave, i.e. frequency modulation.

The synthesizer, which mixes several waveforms, and the noise generator are used to produce each individual rhythm sound. Five voices are available: Bass drum (BD), Snare drum (SD), High hat (HH), Top cymbal (TC), and Tom (TOM).

The following 8 functional blocks detail the OPLII internal configuration.

1. Register array:
   Voice parameters and data for FM operation such as frequency data are set here. All the functions of the OPLII are controlled by the data set in this register array.
2. Phase generator:
   This circuit generates the frequency of the operators (phase) data, which corresponds to the frequency data set in the register array, to determine the frequency of the operators.
3. Envelope generator:
   This is a circuit which creates the envelope, that is the change in the sound over time that corresponding to the register data.
4. Operator:
   The operator receives the phase data (wt) from the phasegenerator and the envelope data (I(t)) from the envelope generator, and computes I sin wt.
5. Accumulator:
   This accumulates the output levels of the operators at each sampling period (sampling is carried out at 50kHz), and converts them into data available for the DAC and interface.
6. Vibrato/Amplitude modulation oscillator:
   This is a low frequency oscillator for vibrato and amplitude modulation.
7. Timer:
   General purpose timer applicable for variable length time settings.
8. Data bus controller.

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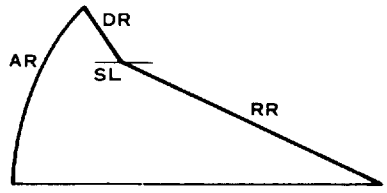
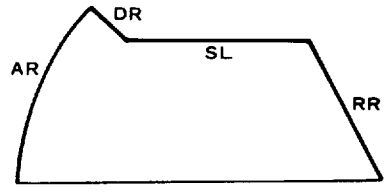
■ CONTENTS OF EACH REGISTER

	Address	
1	01	TEST information. Usually set to "0". On this stage the waveform is Sine wave and compatible with YM3526. If any waveform other than Sine wave will be selected, set D5 to "1".
2	02	Times setting on timer 1. 80μs~20.4ms
3	03	Times setting on timer 2. 320μs~82ms
4	04	Controls the operation of timers 1 and 2 and resets interrupt signals.
5	08	CSM is for the CSM speech synthesis modie. NOTE SEL is for switching the keyboard split by using the F-Number.
6	20~35	MULTI controls the relationship between fundamental waves and harmonics. KSR is key scale of RATE. EG-TYPE is for the switching of Non Percussive Tone and Percussive Tone. 0 is for Percussive Tone and 1 is for Non Percussive Tone. VIB indicates the ON/OFF of vibrato. AM indicates the ON/OFF of modulation.
7	40~55	TL provides a total level for adjustment of each sound level. KSL is the level key scale.
8	60~75	DR sets the decay rate at the decay time. AR sets the rate of increase at the attack time.
9	80~95	RR provides the decay rate at Release/Sustain time. SL provides the level for shifting from decay to sustain.
10	A0~B8	F-Number provides chords within one octave, Block represents octave information for each sound. KON indicates that the sound being generated when it is "1".
11	BD	Controls rhythmic sounds and the corresponding bits for setting ON/OFF of each rhythm. When the R bit is 1, the system is in the rhythm mode. VIB DEP indicates the depth of vibrato. 0 = 7ø, 1 = 14ø. AM DEP indicates the depth of amplitude modulation. 0 = 1dB, 1 = 4.8dB.
12	C0~C8	FB indicates FM feedback factor. C indicates Sin wave synthesis or FM modulation.
13	E0~F5	Wave Select signal. When D5 of address $01 is "1", four kinds of waveform can be selected.



Percussive Tone



Non Percussive Tone

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

	Rating	Units
Pin voltage	−0.3 ~ 7.0	V
Operating ambient temperature	0 ~ 70	°C
Storage temperature	−50 ~ 125	°C

2. Recommended Operating Conditions

Item	Symbol	Minimum	Typical	Maximum	Unit
Power voltage	Vcc	4.5	5	5.5	V
	GND	0	0	0	V

3. DC Characteristics

Item		Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input high level voltage	All input	V_{IH}		2.0			V
Input low level voltage	All input	V_{IL}				0.8	V
Input leak current	øM·$\overline{WR}$·$\overline{RD}$·Ao	I_L	Vin = 0 ~ 5V	−10		10	μA
Three-state (OFF state) input current	D0 ~ D7	I_{TSL}	Vin = 0 ~ 5V	−10		10	μA
Output high level voltage	Output expect $\overline{IRQ}$	V_{OH1}	I_{OH1} = 0.4mA	2.4			V
		V_{OH2}	I_{OH2} = 40μA	3.3			V
Output low level voltage	All output	V_{OL}	I_{OL} = 2.0mA			0.4	V
Output leak current (OFF state)	$\overline{IRQ}$	I_{LOFF}	V_{OH} = 0 ~ 5V	−10		10	V
Pullup resistance	$\overline{IC}$, $\overline{CS}$	R_U		80		400	KΩ
Input capacity	All input	C_I				10	pF
Output capacity	All output	C_O				10	pF
Power voltage		I_{CC}				30	mA

4. AC Characteristics

Item		Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input clock frequency	øM	fc	Fig. A-1	2.0	3.58	4.0	MHz
Input clock duty cycle	øM			40	50	60	%
Input clock rise time	øM	t_R	Fig. A-1				ns
Input clock fall time	øM	t_f	Fig. A-1				ns
Address setup time	Ao	t_{AS}	Fig. A-2, Fig. A-3	10			ns
Address hold time	Ao	t_{AH}	Fig. A-2, Fig. A-3	20			ns
Chip select write width	$\overline{CS}$	t_{CSW}	Fig. A-2	100			ns
Chip select read width	$\overline{CS}$	t_{CSR}	Fig. A-3	200			ns
Write pulse write width	$\overline{WR}$	t_{WW}	Fig. A-2	100			ns
Write data setup time	D0 ~ D7	t_{DS}	Fig. A-2	20			ns
Write data hold time	D0 ~ D7	t_{DH}	Fig. A-2	30			ns
Read pulse width	$\overline{RD}$	t_{RW}	Fig. A-3	200			ns
Read data access time	D0 ~ D7	t_{ACC}	Fig. A-3			200	ns
Read data hold time	D0 ~ D7	t_{RDH}	Fig. A-3	10			ns
Output rise time	øSY	t_{OR1}	Fig. A-4			100	ns
	MO·SH	t_{OR2}	Fig. A-5			150	ns
Output fall time	øSY	t_{OF1}	Fig. A-4			100	ns
	MO·SH	t_{OF2}	Fig. A-5			150	ns
Reset pulse width	$\overline{IC}$	N_{ICW}	Fig. A-6	80			Cycle

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■ REGISTER MAP

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
01				TEST					TEST DATA OF LSI D5 indicates WAVE SELECT ENABLE.
02	TIMER-1								DATA OF TIMER-1
03	TIMER-2								DATA OF TIMER-2
04	RST	MASK T1 T2					ST2	ST1	IRQ-RESET/CONTROL OF RIMER-1, 2
08	CSM	SEL							CSM SPEECH SYNTHESIS MODE/NOTE SELECT
20 35	AM	VIB	EG-TYP	KSR	MULTI				AM/VIB/EG-TYPE/KSR/MULTIPLE
40 55	KSL		TL						KSL/TOTAL LEVEL
60 75	AR				DR				ATTACK RATE/DECAY RATE
80 95	SL				RR				SUSTAIN RATE/RELEASE RATE
A0 A8	F-Number (L)								KON/BLOCK/F-Number
B0 B8			KON	BLOCK			F-Num (H)		
BD	DEP AM	VIB	R	BD	SD	TOM	TC	HH	DEPTH(AM/VIB)/RHYTHM(BD·SD·TOM·TC·HH)
C0 C8					FB			C	FEEDBACK/CONNECTION
E0 F5							WS		WAVE SELECT

■ STATUS REGISTERS

IRQ	FLAG T1 T2		IRQ/FLAG(T1, T2)

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■ TIMING DIAGRAMS (Timing is based upon settings of $V_{IH} = 2.0V$ and $V_{IL} = 0.8V$)

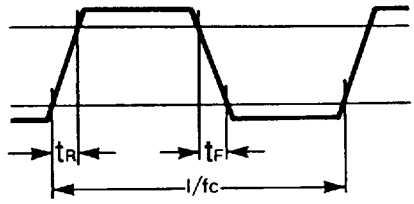
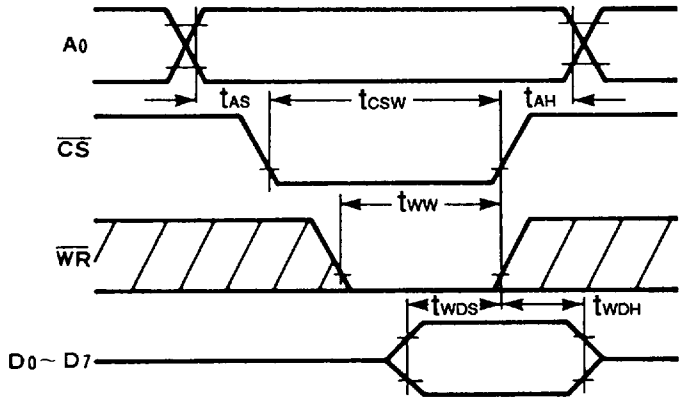
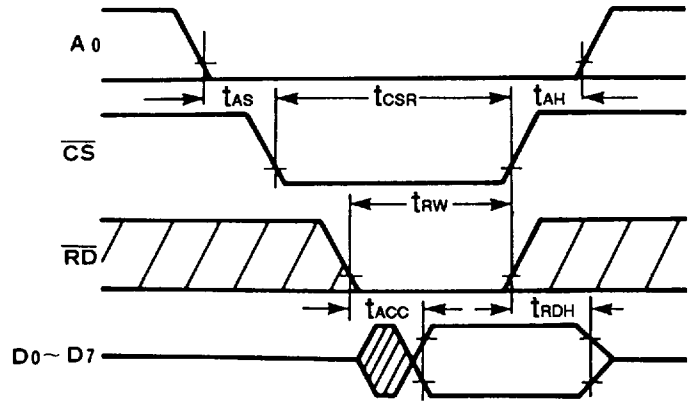


Fig. A-1 Clock Timing



Note: t_{CSW}, t_{WW}, and t_{WDH} are based on either $\overline{CS}$ or $\overline{WS}$ being driven to high level.

Fig. A-2 Write Timing



Note: t_{ACC} is based on whichever of $\overline{CS}$ or $\overline{RD}$ goes to the low level last.
t_{SCR}, t_{RW}, and t_{RDH} are based on either $\overline{CS}$ or $\overline{RD}$ being driven to high level.

Fig. A-3 Read Timing

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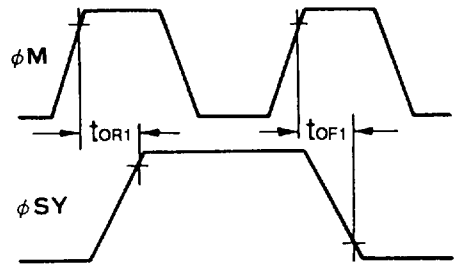

Fig. A-4 φM and φSY

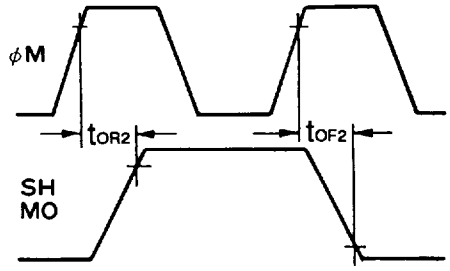

Fig. A-5 φM and SH·MO

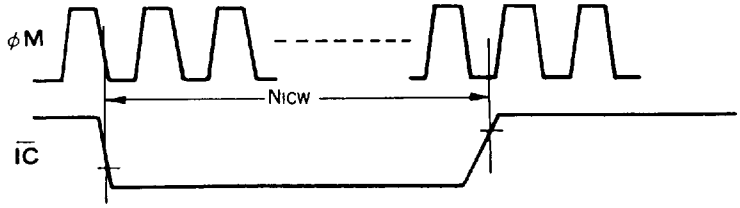

Fig. A-6 Reset Pulse

■ WAVE SELECT

When bit D_5 of address $\$\phi1$ is "0", the OPLII is fully compatible with YM3526 (OPL); there are no differences between the two devices. If a sine wave is input in this mode, the output will be a sine wave like the input. When bit D_5 of address $\$\phi1$ is "1", the input sine wave will be output as the distorted wave shown in Table 3-10.

$E0~$F5

D7	D6	D5	D4	D3	D2	D1	D0
						WAVE SELECT	

Table 3-10 Wave Select

D1	D0	Waveform
0	0	
0	1	
1	0	
1	1	

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■ DIMENSIONS

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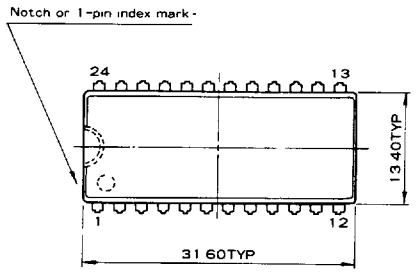



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